A1351

High Precision Linear Hall Effect Sensor IC with a Push/Pull, Pulse Width Modulated Output

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: October 31, 2011

Deadline for receipt of LAST TIME BUY orders: April 27, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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High Precision Linear Hall Effect Sensor IC with a Push/Pull, Pulse Width Modulated Output

Features and Benefits

- Pulse width modulated (PWM) output provides increased noise immunity compared to an analog output
- 1 mm case thickness provides greater coupling for current sensing applications
- Push/pull output
- Customer-programmable offset and sensitivity
- Factory-programmed 0%/°C Sensitivity Temperature Coefficient
- Programmability at end-of-line
- Selectable unipolar or bipolar quiescent duty cycles
- Selectable sensitivity range between 0.055% and 0.095% D/G
- Temperature-stable quiescent duty cycle output and sensitivity
- Precise recoverability after temperature cycling
- Output duty cycle clamps provide short circuit diagnostic capabilities
- Optional 50% D calibration test mode at device power-up
- Wide ambient temperature range: –40°C to 125°C
- Resistant to mechanical stress

Package: 4 pin SIP (suffix KT)

1 mm case thickness



Not to scale

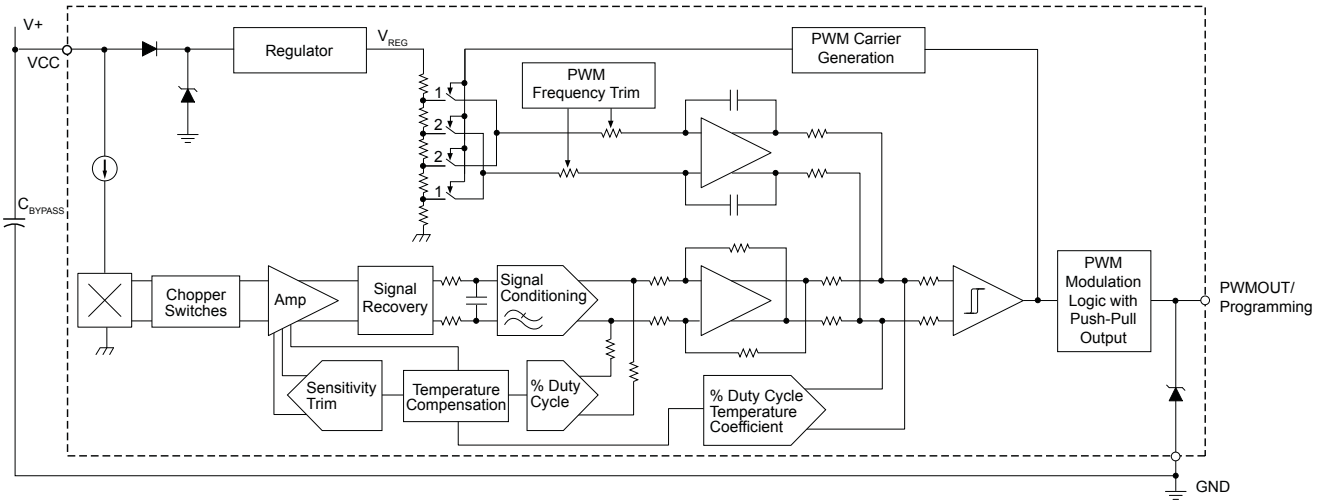
Description

The A1351 device is a high precision, programmable linear Hall effect sensor IC with a pulse width modulated (PWM) output. The duty cycle, D, of the PWM output signal is proportional to an applied magnetic field. The A1351 device converts an analog signal from its internal Hall element to a digitally encoded PWM output signal. The coupled noise immunity of the digitally encoded PWM output is far superior to the noise immunity of an analog output signal. A simple RC network can be used to convert the digital PWM signal back to analog signal.

The BiCMOS, monolithic circuit inside of the A1351 integrates a Hall element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and PWM conversion circuitry. The dynamic offset cancellation circuits reduce the residual offset voltage of the Hall element. Hall element offset is normally caused by device over molding, temperature dependencies, and thermal stress. The high frequency offset cancellation (chopping) clock allows for a greater sampling rate, which increases the accuracy of the output signal and results in faster signal processing capability.

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Functional Block Diagram



Description (continued)

An internal filter of approximately 150 Hz is used to achieve 11 bits of output resolution.

Key applications for the A1351 include battery current sensing, exhaust gas return (EGR), throttle position, ride height and seat belt tensioning systems.

The A1351 is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide[1]

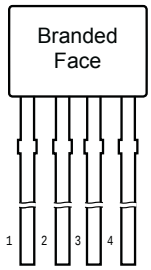
Part Number	Ambient Operating Temperature	Packing[2]
A1351KKTTN-T	–40°C to 125°C	4000 pieces per 13-in. reel

[1]All variants are programmable for unidirectional or bidirectional use.
[2]Contact Allegro for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		16	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward PWM Output Voltage	V_{PWMOUT}		28	V
Reverse PWM Output Voltage	$V_{RPWMOUT}$		–0.2	V
Ambient Operating Temperature	T_A	Range K	–40 to 125	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Junction Temperature	T_J(max)		165	°C

Pin-out Diagram



Terminal List Table

Number	Name	Description
1	VCC	Input power supply; use bypass capacitor to connect to ground
2	PWMOUT	Pulse width modulated output signal; also used for programming
3	NC	Not connected
4	GND	Ground

OPERATING CHARACTERISTICS valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on PWMOUT	–	6.7	10	mA
Parasitic Current	I_{PAR}	V_{CC} = 0 V, GND = 0 V	–	0	–	mA
Power On Time[1]	t_{PO}	T_A = 25°C, C_L (of test probe) = 10 pF, Sens = 0.095% D/G, C_{BYPASS} = open	–	25	–	ms
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal, C_L = 10 nF	–	150	–	Hz
Chopping Frequency[2]	f_C	T_A = 25°C	–	220	–	kHz
Output Characteristics						
Transient Current	$I_{OUT(SINK)}$	PWMOUT to VCC	–	7.8	–	mA
	$I_{OUT(SOURCE)}$	PWMOUT to GND	–	4.1	–	mA
Output Voltage Levels	$V_{OUT(HIGH)}$	$I_{OUT(SOURCE)}$ = 1 mA	4.8	–	–	V
	$V_{OUT(LOW)}$	$I_{OUT(SINK)}$ = 2.5 mA	–	–	0.2	V
Rise Time[3]	t_r	$R_{L(PULLUP)}$ = 2.35 kΩ, C_L = 14.7 nF	–	9.5	–	µs
Fall Time[3]	t_f	$R_{L(PULLUP)}$ = 2.35 kΩ, C_L = 14.7 nF	–	7	–	µs
Response Time[1]	$t_{RESPONSE}$	T_A = 25°C, C_L (of test probe) = 10 pF, Impulse magnetic field of 420 G, Sens = 0.095% D/G	–	25	–	ms
Settling Time After Removal of Overload Magnetic Field[1]	t_{SETTLE}	T_A = 25°C, Primary Overload > 5000 G	–	25	–	ms
Clamp Duty Cycles	$D_{CLP(HIGH)}$	T_A = 25°C, B = 530 G, Sens = 0.095% D/G, $R_{L(PULLDOWN)}$ = 10 kΩ	90	92	95	% D
	$D_{CLP(LOW)}$	T_A = 25°C, B = -530 G, Sens = 0.095% D/G, $R_{L(PULLUP)}$ = 10 kΩ	5	8	10	% D
Duty Cycle Jitter[1,4]	$Jitter_{PWM}$	T_A = –10°C to 65°C, Sens = 0.095% D/G, measured over 1000 output PWM clock periods	–	±0.05	–	% D
Duty Cycle Resolution	Res_{PWM}	T_A = –10°C to 65°C, Sens = 0.095% D/G, measured over 1000 output PWM clock periods	–	±1.5	–	G
Load Resistance	$R_{L(PULLUP)}$	PWMOUT to VCC	2	–	–	kΩ
	$R_{L(PULLDWN)}$	PWMOUT to GND	4.8	–	–	kΩ
Load Capacitance	C_L	PWMOUT to GND	–	–	14.7	nF
Pre-Programming Target[5]						
Pre-Programming Quiescent Duty Cycle Output	$D_{(Q)PRE}$	B = 0 G, T_A = 25°C	–	52	–	% D
Pre-Programming Sensitivity	$Sens_{PRE}$	T_A = 25°C	–	0.045	–	% D/G
Pre-Programming PWM Output Carrier Frequency	f_{PWMPRE}	T_A = 25°C	–	170	–	Hz

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OPERATING CHARACTERISTICS (continued) valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Quiescent Duty Cycle Programming						
Initial Quiescent Duty Cycle Output	$D_{(Q)UNIinit}$	B = 0 G, T_A = 25°C	–	19.5	–	% D
	$D_{(Q)BIinit}$	B = 0 G, T_A = 25°C	–	$D_{(Q)PRE}$	–	% D
Coarse Quiescent Duty Cycle Output Programming Bits[6]			–	1	–	bit
Guaranteed Quiescent Duty Cycle Output Range[7]	$D_{(Q)UNI}$	B = 0 G, T_A = 25°C	10	–	25	% D
	$D_{(Q)BI}$	B = 0 G, T_A = 25°C	36	–	66	% D
Quiescent Duty Cycle Output Programming Bits			–	9	–	bit
Average Quiescent Duty Cycle Output Step Size[8,9]	$Step_{D(Q)}$	T_A = 25°C	0.07	0.08	0.09	% D
Quiescent Duty Cycle Output Programming Resolution[10]	$Err_{PGD(Q)}$	T_A = 25°C	–	$Step_{D(Q)}$ × ±0. 5	–	% D
Sensitivity Programming						
Initial Sensitivity	$Sens_{init}$		–	$Sens_{PRE}$	–	% D/G
Guaranteed Sensitivity Range[11]	Sens	T_A = 25°C	0.055	–	0.095	% D/G
Sensitivity Programming Bits			–	8	–	bit
Average Sensitivity Step Size[8,9]	$Step_{SENS}$	T_A = 25°C	700	785	870	µ% D/G
Sensitivity Programming Resolution[10]	Err_{PGSENS}	T_A = 25°C	–	$Step_{SENS}$ × ±0.5	–	µ% D/G
Carrier Frequency Programming						
Guaranteed Carrier Frequency Programming Range[1,13]	f_{PWM}		105	125	160	Hz
Carrier Frequency Programming Bits			–	4	–	bit
Average Carrier Frequency Step Size[8,9]	$Step_{fPWM}$	T_A = 25°C	5	6.7	8	Hz
Carrier Frequency Programming Resolution[10]	Err_{PGfPWM}			$Step_{fPWM}$ × ±0.5		Hz
Calibration Test Mode Programming						
Calibration Test Mode Selection Bit	CAL		–	1	–	bit
Lock Bit Programming						
Overall Programming Lock Bit	LOCK		–	1	–	bit
Factory Programmed Temperature Coefficients						
Sensitivity Temperature Coefficient[12]	TC_{Sens}	T_A = 125 °C	–	0	–	%/°C
Sensitivity Temperature Coefficient Error	Err_{TCSENS}	T_A = 125 °C	–	< ±0.01	–	%/°C
Quiescent Duty Cycle Drift[12]	$\Delta D_{(Q)}$	T_A = 125 °C	–	0	–	% D
Quiescent Duty Cycle Drift Error	$Err\Delta D_{(Q)}$	T_A = 125 °C, Sens = $Sens_{PRE}$	–	< ±0.2	–	% D

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OPERATING CHARACTERISTICS (continued) valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Drift Characteristics						
Maximum Sensitivity Drift Through Temperature Range[14]	$\Delta Sens_{TC}$		–	< ±2	–	%
Sensitivity Drift Due to Package Hysteresis[1]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling	–	< ±1	–	%
Error Components						
Linearity Sensitivity Error[15]	Lin_{ERR}	B = 400 G and 200 G, and B = –400 G and –200 G	–	< ±0.5	–	%
Symmetry Sensitivity Error[16]	Sym_{ERR}	B = ±300 G	–	< ±1	–	%

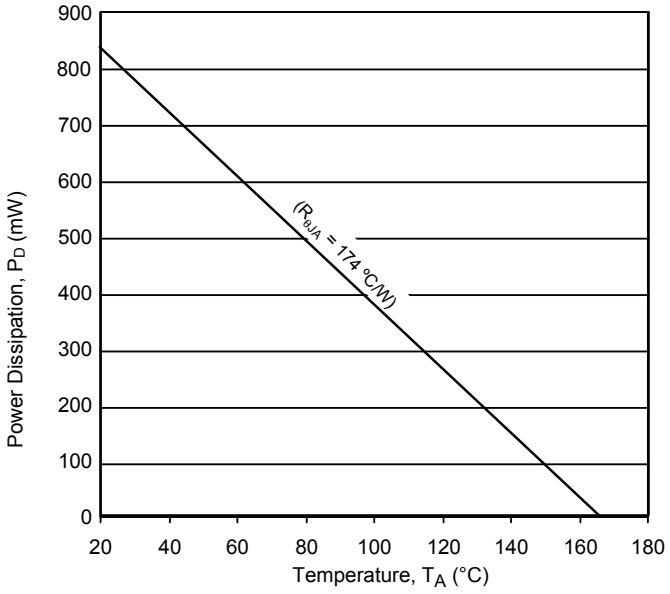
[1] See Characteristic Definitions section.
[2] f_C varies up to approximately ±20% over the full operating ambient temperature range, T_A, and process.
[3] Measured as 10% to 90% (or 90% to 10%) of the PWM signal.
[4] Jitter is dependent on the sensitivity of the device.
[5] Raw device characteristic values before any programming.
[6] Bit for selecting between $D_{(Q)UNI}$ and $D_{(Q)BI}$ programming ranges.
[7] $D_{(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $D_{(Q)}$ range is the total range from $D_{(Q)}$(init) up to and including $D_{(Q)}$(max). See Characteristic Definitions section. Quiescent Duty Cycle may drift by an additional –0.8% D to 0.3% D over the lifetime of this product.
[8] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[9] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{D(Q)}$, $Step_{SENS}$, or $Step_{fPWM}$.
[10] Overall programming value accuracy. See Characteristic Definitions section.
[11] Sens(max) is the value available with all programming fuses blown (maximum programming code set). Sens range is the total range from $Sens_{init}$ up to and including Sens(max). See Characteristic Definitions section. Sensitivity may drift by an additional ±2.5% over the lifetime of this product.
[12] Programmed at 125°C and calculated relative to 25°C.
[13] PWM Carrier Frequency may drift by an additional ±17 Hz over the lifetime of this product.
[14] Sensitivity drift from expected value at T_A after programming TC_{SENS}. See Characteristic Definitions section.
[15] Linearity is only guaranteed for output duty cycle ranges of ±40% D from the quiescent output for bidirectional devices and +40% D from the quiescent output for unidirectional devices. These linearity ranges are only valid within the operating output range of the device. The operating output range is confined to the region between the output clamps. Linearity may shift by up to ±0.25% over the lifetime of this product.
[16] Symmetry error is only valid for bipolar devices. Symmetry may shift by up to ±0.6% over the lifetime of this product.

Thermal Characteristics may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	174	°C/W

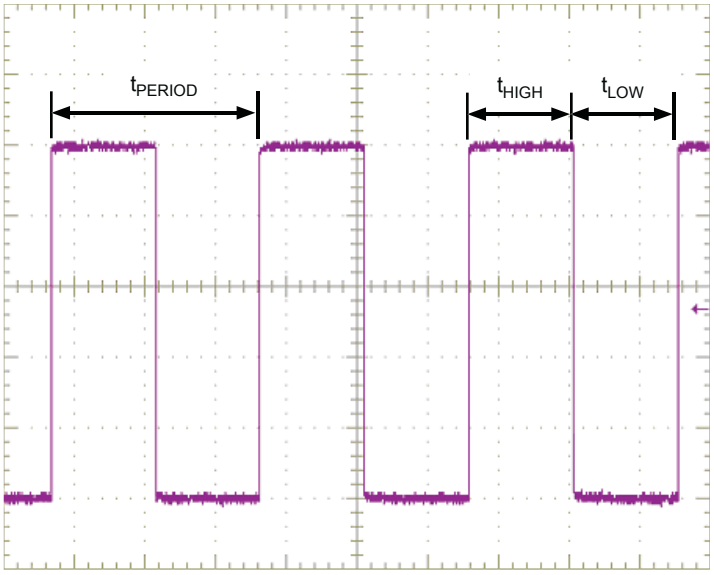
*Additional thermal information available on Allegro website.

Power Dissipation versus Ambient Temperature

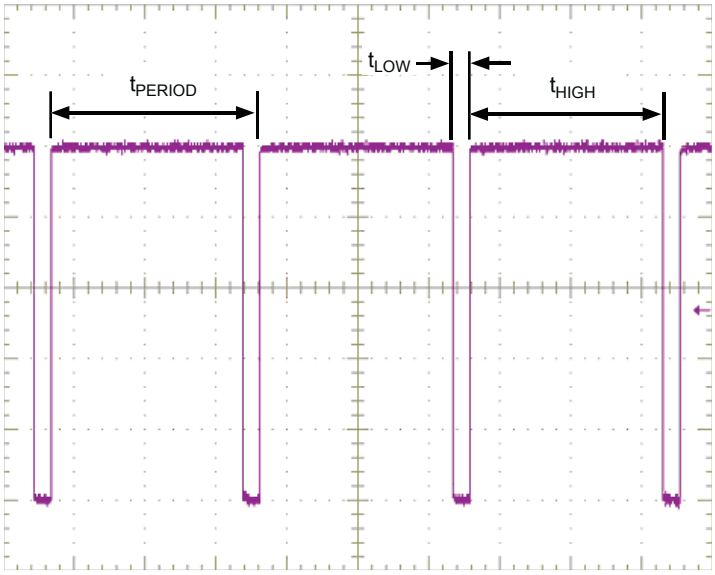


Characteristic Data

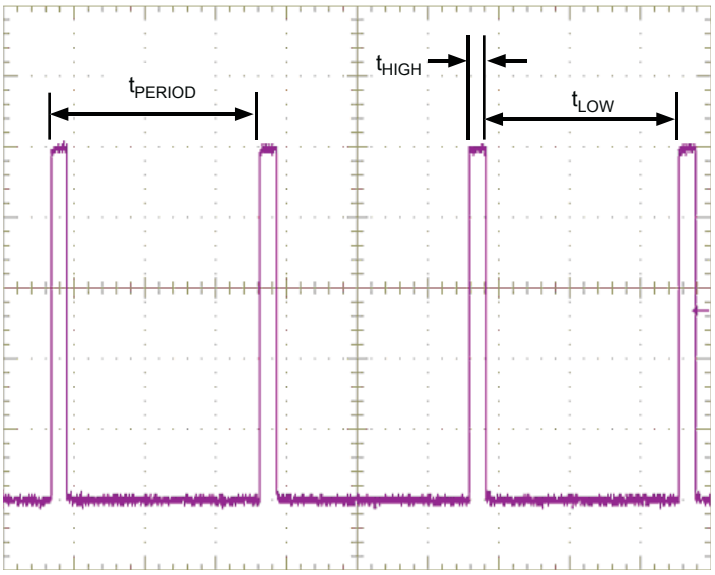
$D_{(Q)}$, D ≈ 50%



High Clamp, D ≈ 90%



Low Clamp, D ≈ 10%



t_{HIGH} – duration of a high voltage pulse
t_{LOW} – duration of the low voltage
t_{PERIOD} – one full frequency cycle
$D = (t_{HIGH} / t_{PERIOD}) \times 100\%$

Uni-Directional Field Detection

Duty Cycle, D	Field Detection
10%	0 Gauss
10%-90%	0 to +X Gauss

Bi-Directional Field Detection

Duty Cycle, D	Field Detection
50%	0 Gauss
50%-90%	0 to +X Gauss
50%-10%	0 to –X Gauss

Characteristic Definitions

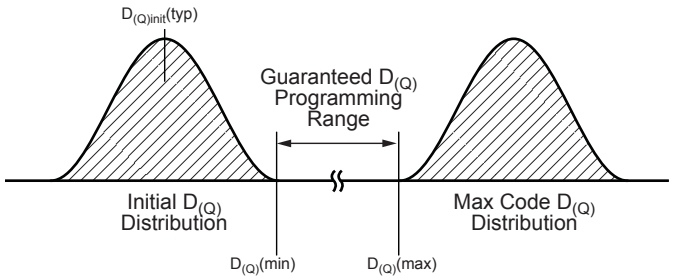
Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before supplying a valid PWM output duty cycle. Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±5% D of its steady state value with no applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min).

Response Time The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied magnetic field.

Settling Time After Removal of Overload Magnetic Field The pulse width modulated output, PWMOUT, of the Hall element requires a finite time to recover from an overload magnetic field. The amount of time, t_{SETTLE}, the device takes to recover from the overload is defined as: the time it takes for the quiescent Hall output duty cycle, $D_{OUT(Q)}$, to settle to within ±5% D of its steady state value after the overload field has fallen below 100 G. For this specification the overload field should step from 5000 G to 0 G in less than 1ms.

Quiescent Voltage Output In the quiescent state (no significant magnetic field: B = 0 G), the output duty cycle, $D_{(Q)}$, equals a specific programmed duty cycle throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Duty Cycle Output Range The quiescent duty cycle output, $D_{(Q)}$, can be programmed around its nominal value of 50% D or 10% D, within the guaranteed quiescent duty cycle range limits: $D_{(Q)}$(min) and $D_{(Q)}$(max). The available guaranteed programming range for $D_{(Q)}$ falls within the distributions of the initial, $D_{(Q)init}$, and the maximum programming code for setting $D_{(Q)}$, as shown in the following diagram.



Average Quiescent Voltage Output Step Size The average quiescent duty cycle output step size for a single device is determined using the following calculation:

$$Step_{D(Q)} = \frac{D_{(Q)maxcode} - D_{(Q)init}}{2^n - 1} . \quad (1)$$

where:

n is the number of available programming bits in the trim range,

$2^n - 1$ is the value of the maximum programming code in the range, and

$D_{(Q)maxcode}$ is the quiescent duty cycle output at code $2^n - 1$.

Quiescent Duty Cycle Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGD(Q)}(typ) = 0.5 \times Step_{D(Q)}(typ) . \quad (2)$$

Quiescent Duty Cycle Output Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent duty cycle output, $D_{(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Duty Cycle Output Drift Through Temperature Range, $\Delta D_{(Q)}$ (%D), is defined as:

$$\Delta D_{(Q)} = D_{(Q)(TA)} - D_{(Q)(25°C)} . \quad (3)$$

$\Delta D_{(Q)}$ should be calculated using the actual measured values of $\Delta D_{(Q)(TA)}$ and $\Delta D_{(Q)(25°C)}$ rather than programming target values.

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output duty cycle from its quiescent value toward the maximum duty cycle limit. The amount of the output duty cycle increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output duty cycle from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (%D/G), of the device, and it is defined for bipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(BNEG)}}{BPOS - BNEG} , \quad (4)$$

and for unipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(Q)}}{BPOS} \quad , \qquad (5)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range The magnetic sensitivity, Sens, can be programmed around its nominal value within the sensitivity range limits: Sens(min) and Sens(max). Refer to the Guaranteed Quiescent Duty Cycle Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Sensitivity Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Carrier Frequency Programming Range The PWM output signal carrier frequency, f_{PWM} ,can be programmed around its nominal value within the carrier frequency range limits, f_{PWM}(min) and f_{PWM}(max). Refer to the Guaranteed Quiescent Duty Cycle Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Carrier Frequency Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Carrier Frequency Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 125°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{Sens} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\% \right) \left(\frac{1}{T2 - T1} \right) \quad , \qquad (6)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 125°C. The ideal value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = Sens_{T1} \left[1 + TC_{SENS} \left(T_A - T1 \right) / 100\% \right] \qquad (7)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ and TC_{SENS} rather than programming target values.

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. For purposes of specification, the sensitivity drift through temperature range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (8)$$

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling.

For purposes of specification, the sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (9)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 125°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The 1351 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}} \right) \times 100\% \quad ,$$
$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}} \right) \times 100\% \quad , \qquad (10)$$

where:

$$Sens_{Bx} = \frac{|D_{(Bx)} - D_{(Q)}|}{B_x} \quad , \qquad (11)$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent voltage output such that $B_{POS2} = 2 \times B_{POS1}$ and $B_{NEG2} = 2 \times B_{NEG1}$. Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \qquad (12)$$

Note that unipolar devices only have positive linearity error, Lin_{ERRPOS}.

Symmetry Sensitivity Error The magnetic sensitivity of an A1351 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities.

Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (13)$$

where $Sens_{Bx}$ is as defined in equation 4, and B_{POS} and B_{NEG} are positive and negative magnetic fields such that $|B_{POS}| = |B_{NEG}|$. Note that the symmetry error specification is only valid for bipolar devices.

Duty Cycle Jitter The duty cycle of the PWM output may vary slightly over time despite:

- the presence of a constant applied magnetic field, and
- a constant carrier frequency for the PWM signal.

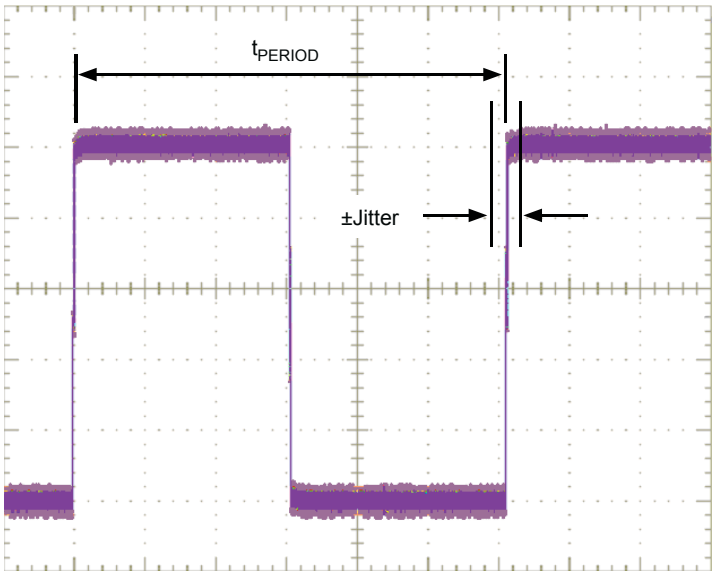
This phenomenon is known as jitter, and is defined as:

$$J_D = \pm \frac{\%D_B(max) - \%D_B(min)}{2} \quad , \qquad (14)$$

where $\%D_B(max)$ and $\%D_B(min)$ are the maximum and minimum duty cycles measured the over 1000 PWM clock periods with a constant applied magnetic field. J_D is given in %D (see figure below).

Duty Cycle Resolution The ability to know the value of the applied magnetic field from the device output is affected by jitter. The resolution of the magnetic field, in Gauss (G), is defined as:

$$RES = \frac{J_{DC}}{Sens} \quad . \qquad (15)$$



Jitter is instability or small rapid irregularity about a specific data position in a periodic electrical signal waveform from cycle to cycle. In this figure, the A1351 PWM Output jitter is ±0.025% D at 25°C, Sens = 0.095% D/G.

A1351 Calibration Test Mode

In customer applications the PWM interface circuitry (body control module; BCM in figure 12) and the A1351 may be powered via different power and ground circuits. As a result, the ground reference for the A1351 may differ from the ground reference of the BCM. In some customer applications this ground difference can be as large as ± 0.5 V. Differences in the ground reference for the A1351 and the BCM can result in variations in the threshold voltage used to measure the duty cycle of the A1351. If the PWM conversion threshold voltage varies, then the duty cycle will vary because there is a finite rise time (t_r) and fall time (t_f) in the PWM waveform. This problem is shown in figure 13.

The A1351 Output Calibration mode is used to compensate for this error in the duty cycle. While the A1351 is in Output Calibration mode, the device output waveform is a fixed 50% duty cycle (the programmed quiescent duty cycle value) regardless of the applied external magnetic field. After powering-up, the 1351 outputs its quiescent duty cycle waveform for 800 ms, regardless of the applied magnetic field (see figure 14). This allows the BCM to compare the measured quiescent duty cycle with an ideal 50% duty cycle.

This test period allows end users to compensate for any threshold errors that result from a difference in system ground potentials.

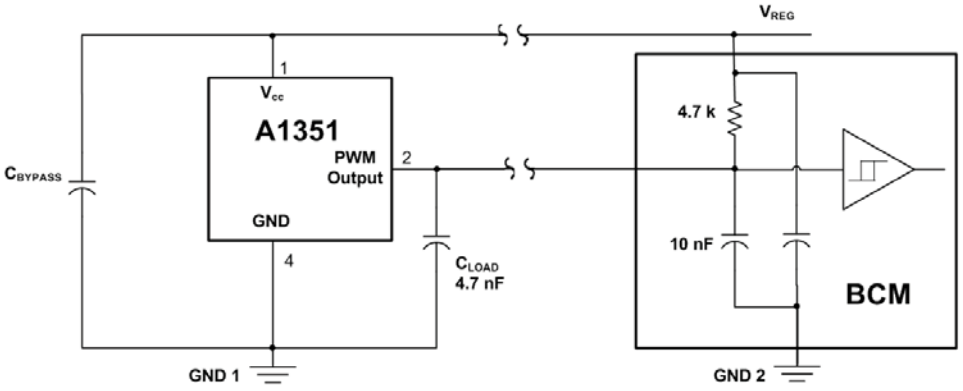


Figure 12. In many applications the A1351 may be powered using a different ground reference than the BCM. This may cause the ground reference for the A1351 (GND 1) to differ from the ground reference of the BCM (GND 2) by as much as to ± 0.5 V.

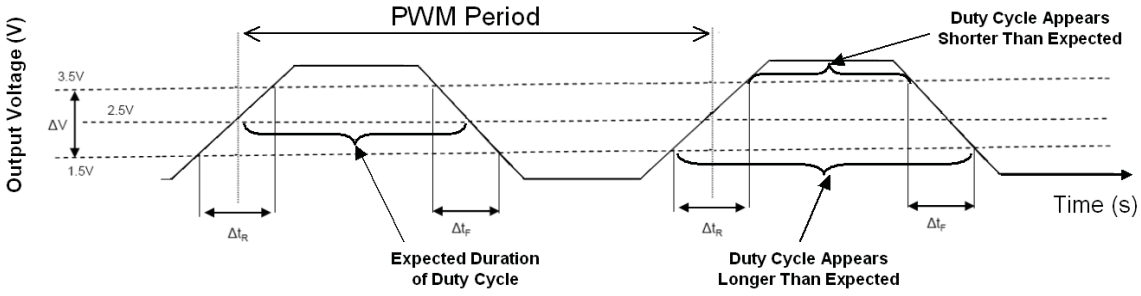


Figure 13. When the threshold voltage is correctly centered between V_{OH} and V_{OL}, the duty cycle accurately coincides with the applied magnetic field. If the threshold voltage is raised, the output duty cycle appears shorter than expected. Conversely, if the threshold voltage is lowered the output duty cycle is longer than expected.

After the initial 800 ms has elapsed, the duty cycle will correspond to an applied magnetic field as expected. The 800 ms calibration test time corresponds with a target PWM frequency of 125 Hz. If the PWM frequency is programmed away from its target of 125 Hz, the duration of the calibration test time will scale inversely with the change in PWM frequency.

This test mode is optional and must be enabled by blowing its programming bit. After the test mode bit has been blown, the device enters Output Calibration mode every time the device is powered-on. This test mode is provided so that the user can compensate for differences in the ground potential between the A1351 and any interface circuitry used to measure the pulse width of the A1351 output.

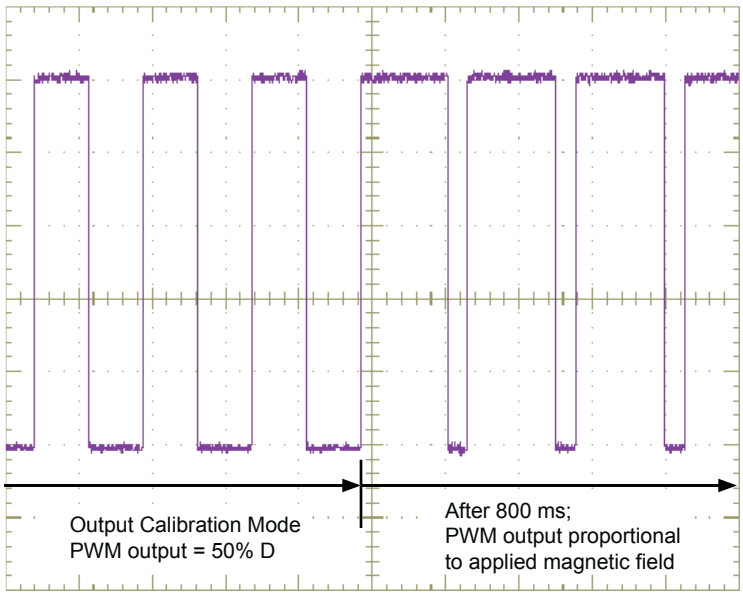
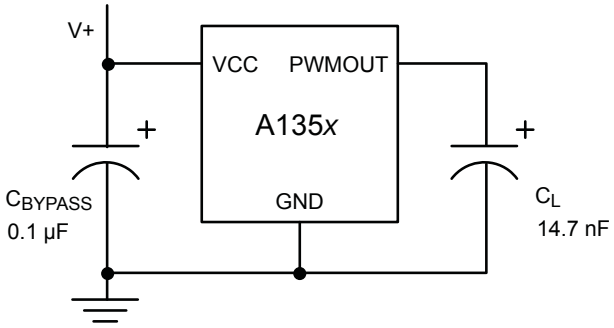


Figure 14. After powering-on, the A1351 outputs a 50% D for the first 800 ms, regardless of the applied magnetic field (Output Calibration mode in effect). After the initial 800 ms has elapsed, the output responds to a magnetic field as expected. The example in this figure assumes that a large +B field is applied to the device after the initial 800 ms.

Typical Application Drawing



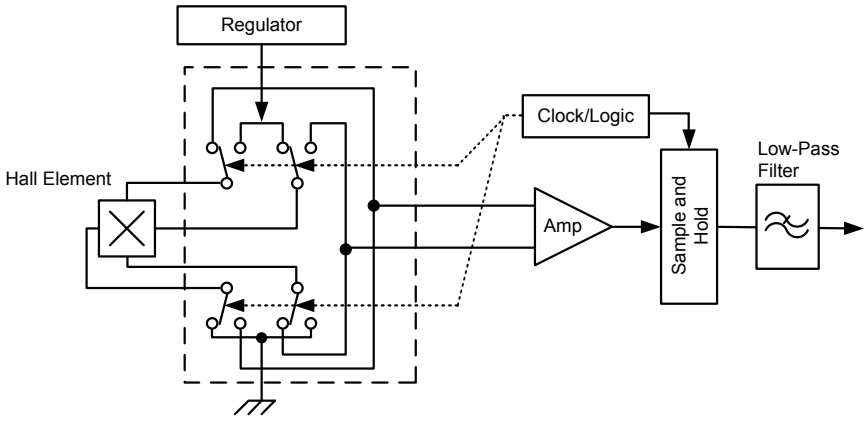
Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process.

The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 220 kHz high frequency clock.

For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (440 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

Programming Guidelines

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the PWMOUT pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value.

There are three voltage levels that must be taken into account when programming. These levels are referred to as *high*, $V_{P(HIGH)}$, *mid*, $V_{P(MID)}$, and *low*, $V_{P(LOW)}$. There are two programming pulse levels. A *high* voltage pulse, V_{PH}, refers to a $V_{P(LOW)}$ $-V_{P(HIGH)}$ $-V_{P(LOW)}$ sequence. A *mid* voltage pulse, V_{PM}, refers to a $V_{P(LOW)}$ $-V_{P(MID)}$ $-V_{P(LOW)}$ sequence.

The 1351 features three modes used during programming: Try mode, Blow mode, and Lock mode:

- In Try mode, the value of a single programmable parameter may be set and measured. The parameter value is stored temporarily, and resets after cycling the supply voltage. (Note that other parameters cannot be accessed simultaneously in this mode.)
- In Blow mode, the value of a single programmable parameter may be set permanently by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially.
- In Lock mode, a device-level fuse is blown, blocking the further programming of all parameters.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Any programmable variable power supply can be used to generate the pulse waveforms, although Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro Web site On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

Definition of Terms

Register One of several sections of the programming logic that control the bit fields storing the code choices for setting programming modes and programmable parameters.

Bit Field The set of internal fuses controlled by a single register. Each fuse in a bit field represents a binary digit in the code setting for that register. The internal logic of the device interprets that code and applies the result to a programmable parameter of the device. Individual fuses can be temporarily activated for testing of the result, or permanently blown.

Key A series of one or more consecutive mid voltage pulses that indicate by their quantity the register being addressed. The quantity of mid voltage pulses corresponds to the decimal equivalent of the binary value of the register being addressed. For example, the LSB of a key is bit 0 (binary 0), corresponding to register 1, and indicated by key 1 (decimal 1), a single mid voltage pulse.

Code A series of one or more consecutive mid voltage pulses that indicate by their quantity the combination of fuses to be activated or blown in the currently-selected register. The quantity of pulses in the code corresponds to the decimal equivalent of the binary value of the bits (links) to be activated or blown. The LSB of a bit field is bit 0, activated by code 1 (decimal 1), a single mid voltage pulse.

Addressing Indicating the target register or bit field setting by incrementing the key or code by means of pulse trains of consecutive mid voltage pulses transmitted through the PWMOUT pin of the device. During the addressing process, each parameter can be measured, before either blowing the fuses to permanently set the programming code (and parameter value), or cycling the power to reset the unblown bits.

Fuse Blowing Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. After a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, protocol at T_A = 25°C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Units
Programming Voltage	$V_{P(LOW)}$	Measured at the PWMOUT pin.	–	–	5.5	V
	$V_{P(MID)}$		13	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the PWMOUT and GND pins during programming, to provide the current necessary for fuse blowing. The blowing capacitor should be removed and the load capacitance used for proper programming duty cycle measurements.	300	–	–	mA
Pulse Width	t_{LOW}	Duration of $V_{P(LOW)}$ voltage level for separating $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses, and delay time after the final V_{BLOW} pulse.	40	–	–	µs
	t_{ACTIVE}	Duration of $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses for register selection or bit field addressing.	40	–	–	µs
	t_{BLOW}	Duration of $V_{P(HIGH)}$ pulses for fuse blowing.	40	–	–	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	5	–	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ or $V_{P(MID)}$ to $V_{P(LOW)}$.	5	–	100	µs

Programming Procedures

Parameter Selection

Each of the five programmable parameters can be accessed through its corresponding parameter register. There is also a LOCK register. These registers and their parameters are:

Register 1:
- Sensitivity, Sens
- Coarse quiescent duty cycle, $D_{(Q)}$

Register 2:
- Quiescent duty cycle output, $D_{(Q)}$

Register 3:
- PWM carrier frequency, f_{PWM}
- Calibration test mode

Register 5:
- Overall device locking, LOCK

To select a register, a sequence of one V_{PH} pulse, the key for the register, and a second V_{PH} pulse (with no VCC supply interruptions) must be applied serially to the PWMOUT pin. The pulse train used for selection of the first register, key 1, is shown in figure 1.

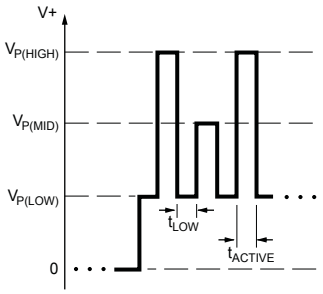


Figure 1. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single V_{PM} pulse.

After the falling edge of the second V_{PH} pulse, the selected register bit field may be addressed with the appropriate code (see Bit Field Addressing section, below).

Bit Field Addressing

After the register of a programmable parameter has been selected as described above, the code pulses must be applied serially to the PWMOUT pin with no VCC supply interruptions. As each additional pulse in the code is transmitted, the overall setting of the bit field increments by 1, up to the maximum possible code for that register (see the Programming Logic table). The A1351 logic interprets the overall setting (the binary sum of all of the activated or blown fuses) and applies it to the value of the parameter, according to the step size for the parameter (shown in the Electrical Characteristics table).

Addressing activates the corresponding fuse locations in the given bit field by incrementing the binary value of an internal DAC. Measurements can be taken after each pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

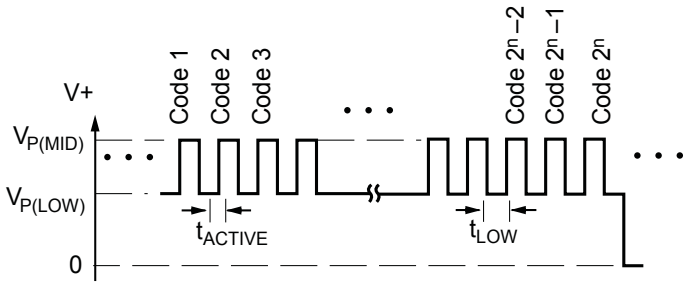


Figure 2. Bit field addressing pulse train. Addressing the bit field by incrementing the code causes the programmable parameter value to change. The number of bits available for a given programming code, *n*, varies among parameters; for example, the bit field for Sensitivity has 8 bits available, which allows 255 separate codes to be used.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a high voltage pulse, called a blow pulse, of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the desired parameter value must be translated to a binary number. For example, as shown in figure 3, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed and blown. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2, is acceptable.

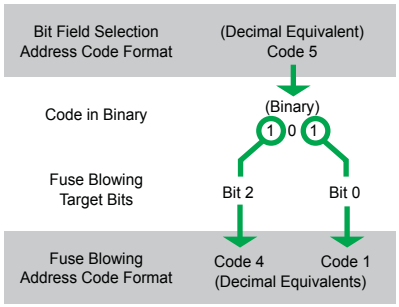


Figure 3. Example of code 5 broken into its binary components, equaling code 4 and code 1.

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters. See the Lock Mode section for lock pulse sequence.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the PWMOUT pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The final application capacitance, C_L, should be used when measuring the output duty cycle during programming. (The maximum load capacitance is 14.7 nF for proper operation.)
- The blowing capacitor, C_{BLOW}, should be removed during measurements; it should only be applied when addressing bit fields and when blowing fuses.
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:

  1. PWM carrier frequency
  2. Coarse $D_{(Q)}$
  3. Sens
  4. $D_{(Q)}$
  5. LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

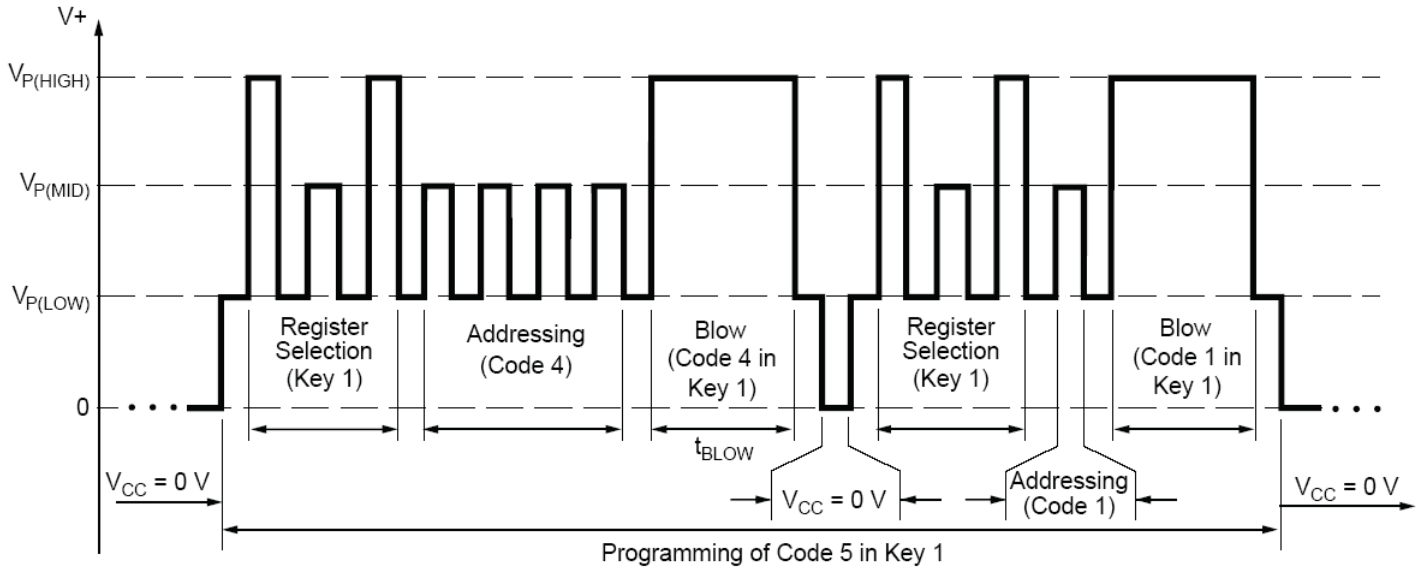


Figure 4. Example of programming pulses applied to the PWMOUT pin that result in permanent parameter settings. In this example, the register corresponding to key 1 is selected (twice) and code 5 is addressed and blown (in two stages).

Programming Modes

Try Mode

Try mode allows a single programmable parameter to be tested without permanently setting its value. (Note that multiple parameters cannot be tested simultaneously with the A1351 device.) Try mode is a required step of parameter blowing. (See the Blow Mode section for additional information.) After powering the VCC supply, select the desired parameter register and address its bit field. When addressing the bit field, each V_{PM} pulse increments the value of the parameter register, up to the maximum possible code (see the Programming Logic table). The addressed parameter value remains stored in the device even after the programming drive voltage is removed from the PWMOUT pin, allowing the value to be measured. Note that for accurate programming, the blow capacitor, C_{BLOW}, should be replaced with the application load capacitance, C_L, during output voltage measurement. It is not possible to decrement the value of the register without resetting the parameter bit field. To reset the bit field, and thus the value of the programmable parameter, cycle the supply (VCC) voltage.

Blow Mode

After the required value of the programmable parameter is found using Try mode, its corresponding code should be blown to make its value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Lock Mode

To lock the device, address the LOCK bit and apply a blow pulse with C_{BLOW} in place. The LOCK bit is located in register 5, code 512. After locking the device, no future programming of any parameter is possible.

Programming State Machine

Initial State

After system power-up, the programming logic is reset to a known state. This is referred to as the *Initial* state. All the bit field locations that have intact fuses are set to logic 0. While in the Initial state, any V_{PM} pulses on the PWMOUT pin are ignored. To enter the Parameter Selection state, apply a single V_{PH} pulse on the PWMOUT pin.

Parameter Selection State

This state allows the selection of the parameter register containing the bit fields to be programmed. To select a parameter register, increment through the keys by sending V_{PM} pulses on the PWMOUT pin. Register keys select among the following programming parameters:

1 pulse – Sens / Coarse $D_{(Q)}$
2 pulses – $D_{(Q)}$
3 pulses – PWM Frequency / Calibration Test Mode
5 pulses – LOCK

Bit Field Addressing State

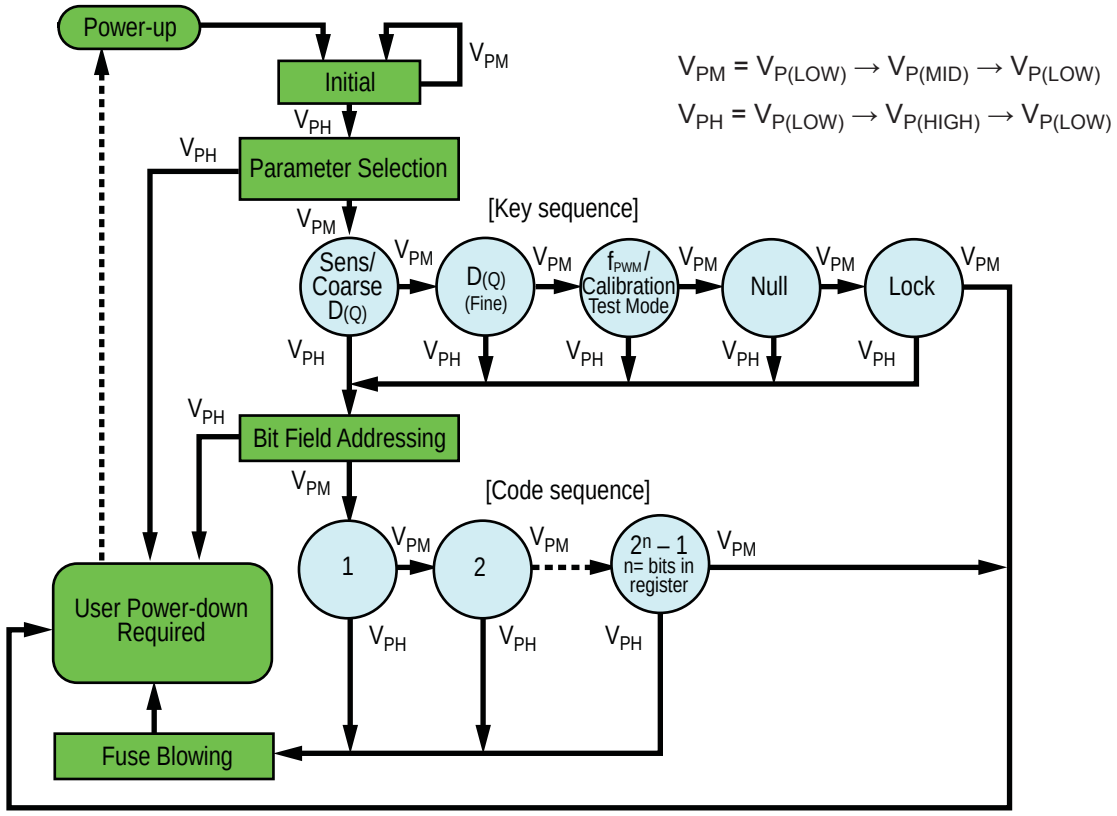
To enter the Bit Field Addressing state, apply one V_{PH} pulse on the PWMOUT pin. This state allows the selection of the individual bit fields to be programmed in the selected parameter register (see the Programming Logic table). To leave this state, either cycle device power or blow the fuses for the selected code.

Note: Merely addressing the bit field does not permanently set the value of the selected programming parameter; fuses must be blown to do so.

Fuse Blowing State

To blow an addressed bit field, apply a V_{PH} pulse on the PWMOUT pin. Power to the device should then be cycled before additional programming is attempted.

Note: Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).



Programming Logic Table

Register Selection (Key)	Binary Bit Field Address (MSB→LSB)	Decimal Equivalent Code	Description
Sensitivity (1)	000000000	0	Initial value; Sens = $Sens_{init}$
	011111111	255	Maximum gain value in range
Coarse $D_{(Q)}$ (1)	000000000	0	Initial value; $D_{(Q)} = D_{(Q)BIinit}$
	100000000	256	Enable coarse $D_{(Q)}$ bit; switch from bidirectional programming to unidirectional programming; $D_{(Q)} = D_{(Q)UNIinit}$
Fine $D_{(Q)}$ (B = 0 Gauss) (2)	000000000	0	Initial value
	011111111	255	Maximum quiescent duty cycle in range
	100000000	256	Switch from programming increasing $D_{(Q)}$ to programming decreasing $D_{(Q)}$; $D_{(Q)} = D_{(Q)init}$
	111111111	511	Minimum quiescent duty cycle in range
PWM Frequency / Calibration Test Mode (3)	00000	0	Initial value; $f_{PWM} = f_{PWMPRE}$
	01111	15	Minimum PWM frequency in range
	10000	16	Enable 50% D Calibration Test Mode
Lock All (5)	0000000000	0	Initial value
	1000000000	512	Lock all registers

Constructing a Current Sensor Using the A1351

To construct a current sensor using the A1351, first consider a current carrying wire that we want to observe. As dictated by Ampere's Law, a magnetic field is produced around the wire that is proportional to the amount of current flowing through the wire. By passing this wire through a soft magnetic core, the magnetic flux produced by the wire can be concentrated and directed through a gap in the core. The magnetic flux density can be measured by inserting the A1351 SIP into the gap in the core. As a result, the output of the A1351 device will be proportional to the amount of current flowing through the wire.

The example feedthrough current sensing setup shown below (figure 7) has a core made of "mu metal" that is 2 mm thick and 4 mm wide. The inner radius of the core is 14.5 mm and the outer radius is 18.5 mm. The wire going through the center of the core has a radius of 9 mm. Using this setup with a gap of 1.7 mm, a field strength results that is on the order of 7 G/A at the Hall element in the A1351.

The recommended core material for construction of the concentrator depends on the specific application. If high flux saturation is desired, then an alloy such as HyPerm49 is recommended. For lower-current level sensing applications, a material such as HyMu80 may be desired. (HyMu80 has lower magnetic flux saturation than HyPerm49, therefore more HyMu80 material is required to carry the same amount of flux compared to Hyperm49.) If frequency response is a concern, then eddy currents can be reduced by either laminating the HyPerm49 or HyMu80 alloys, or by using a ferrite core.

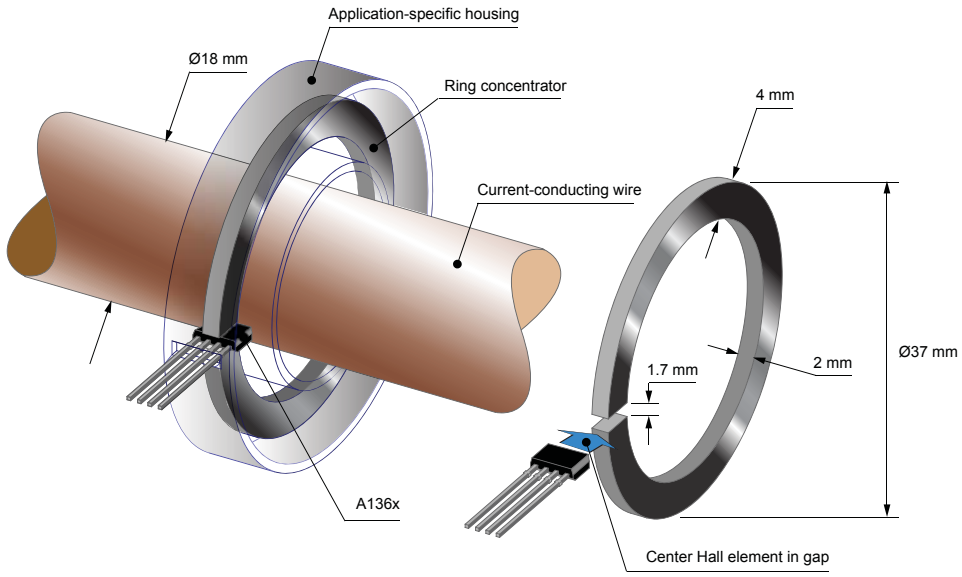


Figure 7. The example current sensor setup used to generate the data in this section was constructed with a split-ring concentrator and an A1351 device. A copper wire was fed through the concentrator, and the A1351 placed in its gap. This approximates a typical ammeter application on a thick wire, such as shown in the left view. Note that such applications usually have a protective housing, which should be taken into consideration when designing the final application. The housing is beyond the scope of this example.

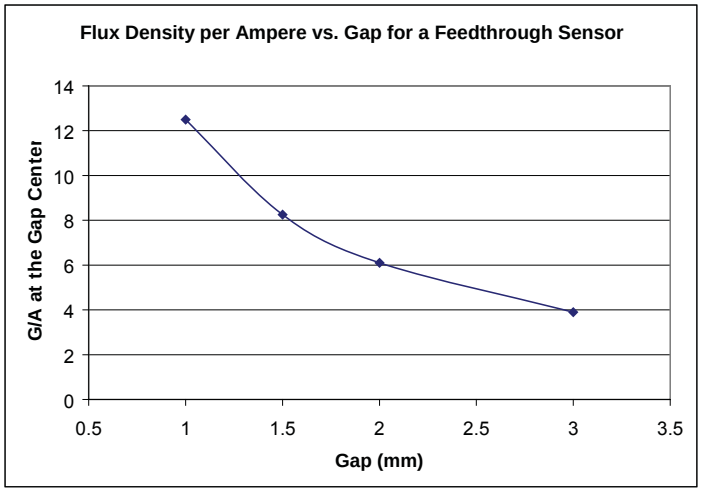


Figure 8. The flux density per ampere measured by the A1351 Hall device is related to the core gap, as shown. This figure assumes that the current sensing application is constructed using the example setup.

The flux density measured by the A1351 SIP is related to the size of the gap cut into the core. The larger the gap in the core, the smaller the flux density per ampere of applied current (see figure 8).

Figure 9 depicts the magnetic flux density through the center of the SIP as a function of SIP to core alignment. Note that a core with a larger cross-sectional area would reduce the attenuation in flux density that results from any SIP misalignment. The flat portion of the curve in figure 9 would span a larger distance in millimeters if the cross-sectional area of the core were increased.

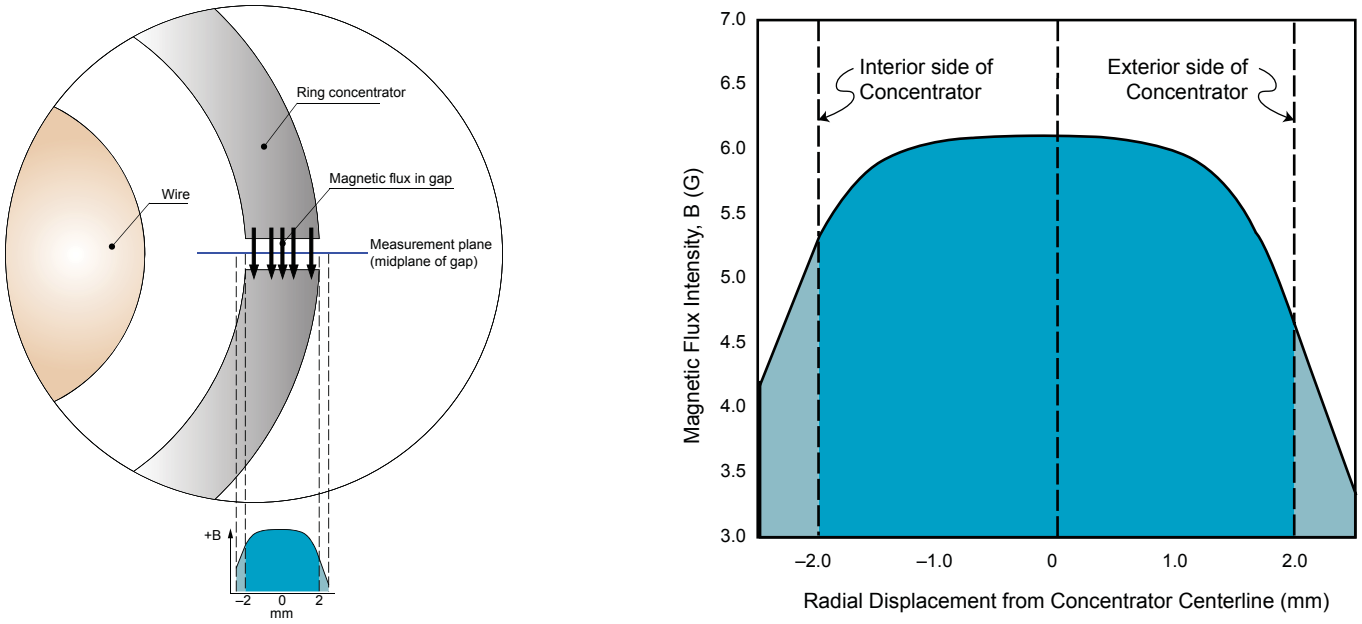
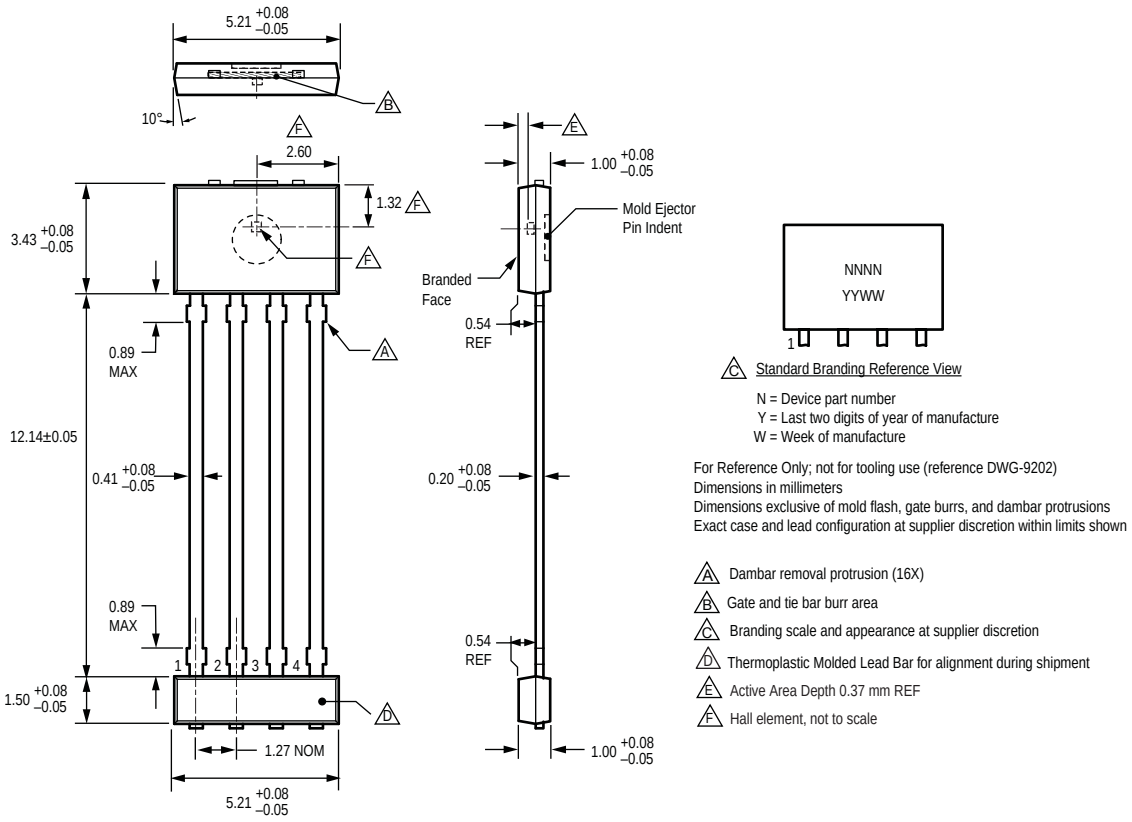


Figure 9. Side view of example current-conducting wire and split ring concentrator (left), and magnetic profile (right) through the midplane of the gap in the split ring concentrator. The flux denisty through the center of the gap varies between the inside and the outside of the gap.

Package KT, 4-Pin SIP



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