Source Control Drawing

Part Description:	3 x 3 x 0.9 mm Ultra Low Power RTC IC User's Guide
Customer Part Number:	
Abracon Part Number:	

Customer Approval (Please return this copy as a certification of your approval.)	
Approved By:	
Approval Date:	

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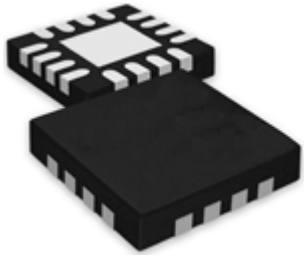
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Revision History

Rev.	ECO	Description	Date	Prep'd By	Ck'd By	Ck'd By	Appr'd By
A		- Added limits and/or temperature range specifications for the following parameters: $V_{CC,ABSMAX}$, $V_{BAT,ABSMAX}$, V_{CCIO}, V_{CCRST}, V_{CCSWR}, V_{CCSWF}, V_{CCRS}, V_{CCFS}, V_{BATRST}, V_{T+}, V_{T-}, I_{LEAK}, I_{OH}, I_{OL}, R_{DSON}, I_{OLEAK}, C_{EX}, OA_{XT}, F_{RCC}, F_{RCU}, T_{AC}, $I_{VCC:I2C}$, $I_{VCC:SPIW}$, $I_{VCC:SPIR}$, $I_{VCC:XT}$, $I_{VCC:RC}$, $I_{VCC:ACAL}$, $I_{VCC:CK32}$, $I_{VCC:CLK128}$, $I_{VBAT:XT}$, $I_{VBAT:RC}$, $I_{VBAT:ACAL}$, $I_{VBAT:VCC}$, V_{BRF}, V_{BRR}, V_{BRH}, T_{BR}, $t_{LOW:VCC}$, $t_{VL:FOUT}$, $t_{VH:FOUT}$, t_{XTST}, $t_{VL:NRST}$, $t_{VH:NRST}$, $t_{RL:NRST}$, $t_{RH:NRST}$ - Removed t_{BREF} parameter - Additional note on autocalibration operating temperature range in the electrical specification section - Added additional text to the Autocalibration Fail section - Updated XT digital calibration adjustment value equation - Removed V_{CCRS} parameter as there is no requirement for the V_{CC} rising slew rate - Added curves to the electrical specification section: VCC Current vs. Voltage in different operating modes, VCC Current vs. Voltage During I^2C/SPI burst read/write, VCC Current vs. Voltage with 32.768kHz Clock Output, VBAT Current vs. Voltage in different operating modes, VBAT current vs. Voltage in VCC power state - Removed typ. values at 1.5V and 3.6V in VCC supply current table and replaced with VCC supply current vs. voltage curves - Removed typical values at 1.5V and 3.6V in VBAT supply current table and replaced with VBAT current vs. voltage curve	10/31/2013	SR	YH	CB	JE
B		- Reduced part selection to AB1805 and AB1815 - Updated RCPLS value to be consistent across the datasheet - Renamed datasheet to AB18X5	05/08/2014	SR	YH	CB	JE
C		- Corrected a few typographical errors - Added additional text to PWGT bit description - Specified VCC voltage range for I_{OLEAK} parameter - Updated the AB0805 and AB0815 number of output pins in the Family Summary Table - Clarified pin descriptions in Table 3	09/16/2014	SR	YH	CB	JE

Features

- Ultra-low supply current (all at 3V):
  - 14 nA with RC oscillator
  - 22 nA with RC oscillator and Autocalibration
  - 55 nA with crystal oscillator
- Baseline timekeeping features:
  - 32.768 kHz crystal oscillator with integrated load capacitor/resistor
  - Counters for hundredths, seconds, minutes, hours, date, month, year, century, and week-day
  - Alarm capability on all counters
  - Programmable output clock generation (32.768 kHz to 1 year)
  - Countdown timer with repeat function
  - Automatic leap year calculation
- Advanced timekeeping features:
  - Integrated power optimized RC oscillator
  - Advanced crystal calibration to ± 2 ppm
  - Advanced RC calibration to ± 16 ppm
  - Automatic calibration of RC oscillator to crystal oscillator
  - Watchdog timer with hardware reset
  - 256 bytes of general purpose RAM
- Power management features:
  - Integrated ~1Ω power switch for off-chip components such as a host MCU
  - System sleep manager for managing host processor wake/sleep states
  - External reset signal monitor
  - Reset output generator
  - Supercapacitor trickle charger with programmable charging current
  - Automatic switchover to VBAT
  - External interrupt monitor
  - Programmable low battery detection threshold
  - Programmable analog voltage comparator
- I^2C (up to 400 kHz) and 3-wire or 4-wire SPI (up to 2 MHz) serial interfaces available
- Operating voltage 1.5-3.6 V
- Clock and RAM retention voltage 1.5-3.6 V
- Operating temperature –40 to 85 °C
- All inputs include Schmitt Triggers
- 3x3 mm QFN-16 package



Applications

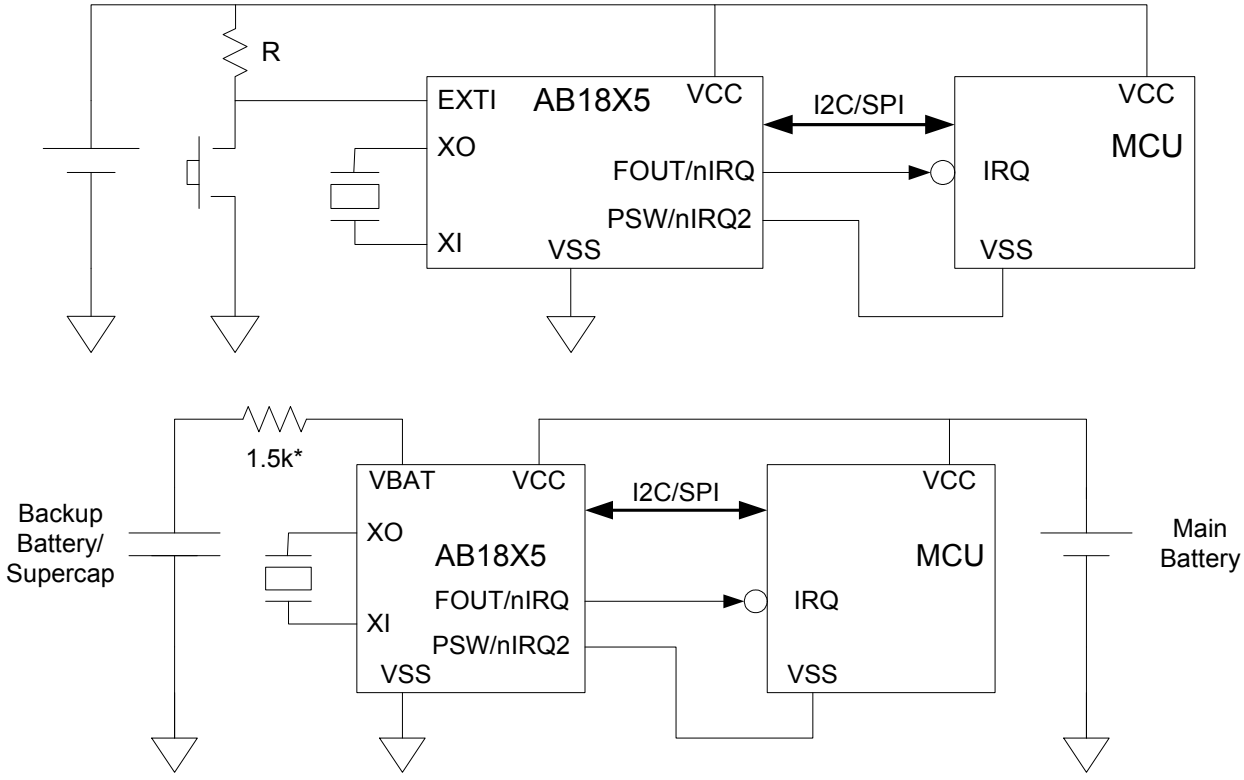
- Smart cards
- Wireless sensors and tags
- Medical electronics
- Utility meters
- Data loggers
- Appliances
- Handsets
- Consumer electronics
- Communications equipment

Description

The ABRACON AB18X5 Real-Time Clock with Power Management family provides a groundbreaking combination of ultra-low power coupled with a highly sophisticated feature set. With power requirements significantly lower than any other industry RTC (as low as 14 nA), these are the first semiconductors based on innovative SPOT™ (Subthreshold Power Optimized Technology) CMOS platform. The AB18X5 includes on-chip oscillators to provide minimum power consumption, full RTC functions including battery backup and programmable counters and alarms for timer and watchdog functions, and either an I^2C or SPI serial interface for communication with a host controller. An integrated power switch and a sophisticated system sleep manager with counter, timer, alarm, and interrupt capabilities allows the AB18X5 to be used as a supervisory component in a host microcontroller based system.

Disclaimer: AB18X5 series of devices are based on innovative SPOT technology, proprietary to Ambiq Micro.

Typical Application Circuit



* Total battery series impedance = 1.5k ohms, which may require an external resistor

Note: Recommended tuning fork crystal is ABS07-120-32.768kHz-T.

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1. Family Summary

The AB18X5 family consists of several members (see Table 1). All devices are supplied in a standard 3x3 mm QFN-16 package. Members of the software and pin compatible AB08X5 RTC family are also listed.

Table 1: Family Summary

Part #	Baseline Timekeeping		Advanced Timekeeping				Power Management				Interface
	XT Osc	Number of GP Outputs	RC Osc	Calib/ Auto-calib	Watch-dog	RAM (B)	VBAT Switch	Reset Mgmt	Ext Int	Power Switch and Sleep FSM	
AB1805	■	4	■	■	■	256	■	■	■	■	I^2C
AB1815	■	3	■	■	■	256	■	■	■	■	SPI
Software and Pin Compatible AB08X5 Family Components											
AB0805	■	3	■	■	■	256	■		■		I^2C
AB0815	■	2	■	■	■	256	■		■		SPI

2. Package Pins

2.1 Pin Configuration and Connections

Figure 1 and Table 2 show the QFN-16 pin configurations for the AB18X5 parts. Pins labeled NC must be left unconnected. The thermal pad, pin 17, on the QFN-16 packages must be connected to VSS.

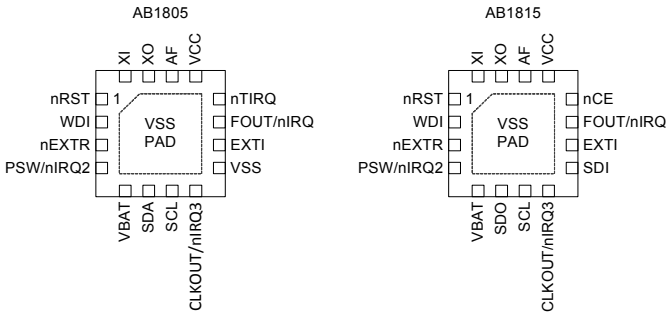


Figure 1. Pin Configuration Diagram

Table 2: Pin Connections

Pin Name	Pin Type	Function	Pin Number	
			AB1805	AB1815
VSS	Power	Ground	9,17	17
VCC	Power	System power supply	13	13
XI	XT	Crystal input	16	16
XO	XT	Crystal output	15	15
AF	Output	Autocalibration filter	14	14
VBAT	Power	Battery power supply	5	5
SCL	Input	I^2C or SPI interface clock	7	7
SDO	Output	SPI data output		6
SDI	Input	SPI data input		9
nCE	Input	SPI chip select		12
SDA	Input	I^2C data input/output	6	
EXTI	Input	External interrupt input	10	10
WDI	Input	Watchdog reset input	2	2
nEXTR	Input	External reset input	3	3
FOUT/nIRQ	Output	Int 1/function output	11	11
nIRQ2	Output	Int 2 output	4	4
CLKOUT/nIRQ3	Output	Int 3/clock output	8	8
nTIRQ	Output	Timer interrupt output	12	
nRST	Output	Reset output	1	1

2.2 Pin Descriptions

Table 3 provides a description of the pin connections.

Table 3: Pin Descriptions

Pin Name	Description
VSS	Ground connection. In the QFN-16 packages the ground slug on the bottom of the package must be connected to VSS.
VCC	Primary power connection. If a single power supply is used, it must be connected to VCC.
VBAT	Battery backup power connection. If a backup battery is not present, VBAT must be connected directly to VSS, but it may also be used to provide the analog input to the internal comparator (see Analog-Comparator).
XI	Crystal oscillator input connection.
XO	Crystal oscillator output connection.
AF	Autocalibration filter connection. A 47pF ceramic capacitor must be placed between this pin and VSS for improved Autocalibration mode timing accuracy.
SCL	I/O interface clock connection. It provides the SCL input in both I^2C and SPI interface parts. A pull-up resistor is required on this pin.
SDA (only available in I^2C environments)	I/O interface I^2C data connection. A pull-up resistor is required on this pin.
SDO (only available in SPI environments)	I/O interface SPI data output connection.
SDI	I/O interface SPI data input connection.
nCE (only available in SPI environments)	I/O interface SPI chip select input connection. It is an active low signal. A pull-up resistor is recommended to be connected to this pin to ensure it is not floating. A pull-up resistor also prevents inadvertent writes to the RTC during power transitions.
EXTI	External interrupt input connection. It may be used to generate an External 1 interrupt with polarity selected by the EX1P bit if enabled by the EX1E bit. The value of the EXTI pin may be read in the EXIN register bit. This pin does not have an internal pull-up or pull-down resistor and so one must be added externally. It must not be left floating or the RTC may consume higher current. Instead, it must be connected directly to either VCC or VSS if not used.
WDI	Watchdog Timer reset input connection. It may also be used to generate an External 2 interrupt with polarity selected by the EX2P bit if enabled by the EX2E bit. The value of the WDI pin may be read in the WDIN register bit. This pin does not have an internal pull-up or pull-down resistor and so one must be added externally. It must not be left floating or the RTC may consume higher current. Instead, it must be connected directly to either VCC or VSS if not used.
nEXTR	External reset input connection. If nEXTR is low and the RS1E bit is set, the nRST output will be driven to its asserted value as determined by the RSP bit. This pin does not have an internal pull-up or pull-down resistor and so one must be added externally. It must not be left floating or the RTC may consume higher current. Instead, it must be connected directly to either VCC or VSS if not used.
FOUT/nIRQ	Primary interrupt output connection. This pin is an open drain output. An external pull-up resistor must be added to this pin. It should be connected to the host device and is used to indicate when the RTC can be accessed via the serial interface. FOUT/nIRQ may be configured to generate several signals as a function of the OUT1S field(see 0x11 - Control2). FOUT/nIRQ is also asserted low on a power up until the AB18X5 has exited the reset state and is accessible via the I/O interface. 1. FOUT/nIRQ can drive the value of the OUT bit. 2. FOUT/nIRQ can drive the inverse of the combined interrupt signal IRQ (see Interrupts). 3. FOUT/nIRQ can drive the square wave output (see 0x13 - SQW) if enabled by SQWE. 4. FOUT/nIRQ can drive the inverse of the alarm interrupt signal AIRQ (see Interrupts).

Table 3: Pin Descriptions

Pin Name	Description
PSW/nIRQ2	Secondary interrupt output connection. It is an open drain output. This pin can be left floating if not used. PSW/nIRQ2 may be configured to generate several signals as a function of the OUT2S field (see 0x11 - Control2). This pin will be configured as an ~1 Ω switch if the PWR2 bit is set. 1. PSW/nIRQ2 can drive the value of the OUTB bit. 2. PSW/nIRQ2 can drive the square wave output (see 0x13 - SQW) if enabled by SQWE. 3. PSW/nIRQ2 can drive the inverse of the combined interrupt signal IRQ(see Interrupts). 4. PSW/nIRQ2 can drive the inverse of the alarm interrupt signal AIRQ(see Interrupts). 5. PSW/nIRQ2 can drive either sense of the timer interrupt signal TIRQ. 6. PSW/nIRQ2 can function as the power switch output for controlling the power of external devices (see Sleep Control).
nTIRQ (only available in I^2C environments)	Timer interrupt output connection. It is an open drain output. nTIRQ always drives the active low nTIRQ signal. If this pin is used, an external pull-up resistor must be added to this pin. If the pin is not used, it can be left floating.
CLKOUT/nIRQ3	Square Wave output connection. It is a push-pull output, and may be configured to generate one of two signals. 1. CLKOUT/nIRQ3 can drive the value of the OUT bit. 2. CLKOUT/nIRQ3 can drive the square wave output (see 0x13 - SQW) if enabled by SQWE.
nRST	External reset output connection. It is an open drain output. If this pin is used, an external pull-up resistor must be added to this pin. If the pin is not used, it can be left floating.The polarity is selected by the RSP bit, which will initialize to 0 on power up to produce an active low output. See Autocalibration Fail Interrupt ACIRQ for details of the generation of nRST.

3. Digital Architecture Summary

Figure 2 illustrates the overall architecture of the pin inputs and outputs of the AB18X5.

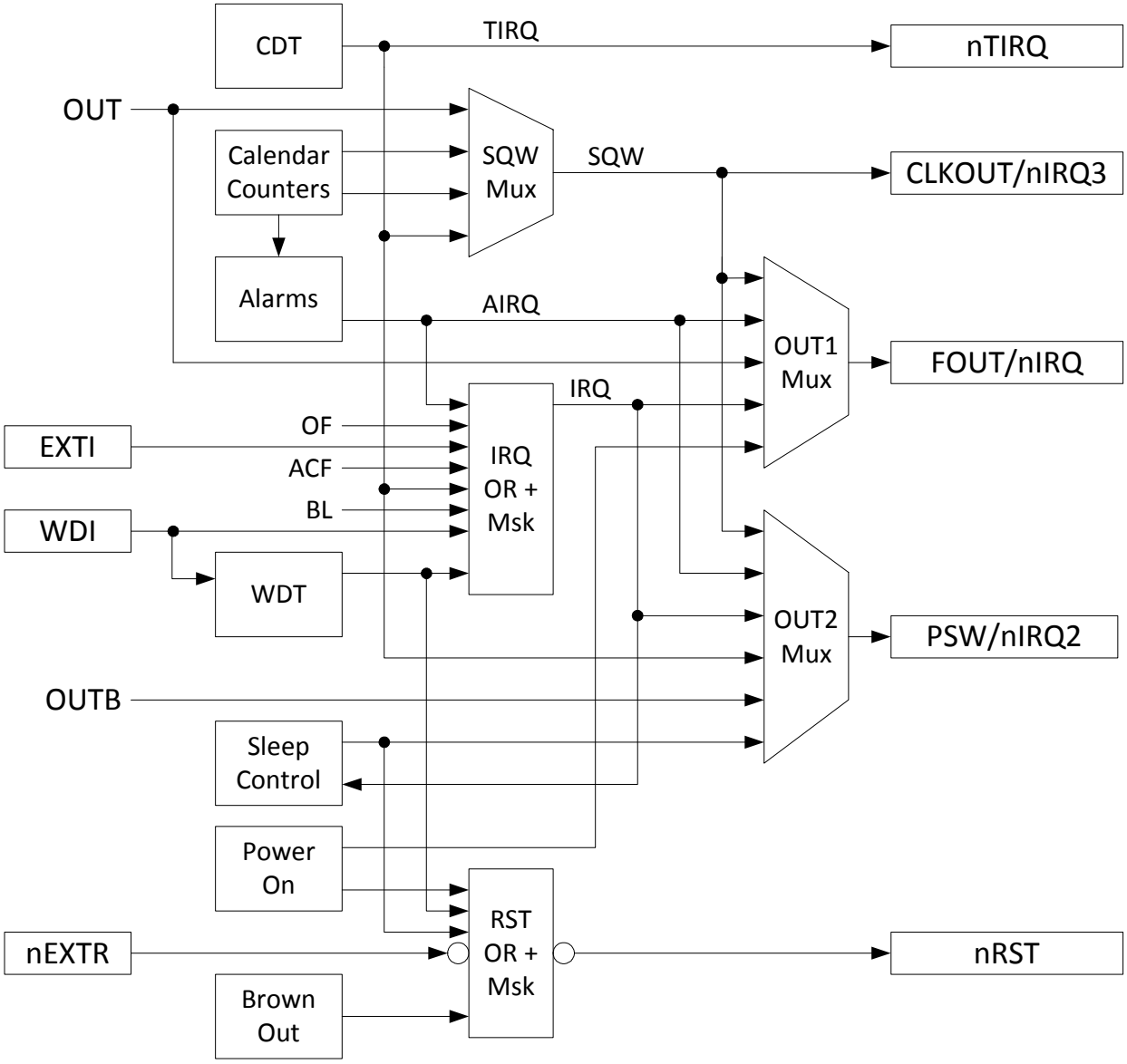


Figure 2. Digital Architecture Summary

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings.

Table 4: Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	System Power Voltage		-0.3		3.8	V
V_{BAT}	Battery Voltage		-0.3		3.8	V
V_I	Input voltage	VCC Power state	-0.3		V_{CC}+ 0.3	V
V_I	Input voltage	VBAT Power state	-0.3		V_{BAT}+ 0.3	V
V_O	Output voltage	VCC Power state	-0.3		V_{CC}+ 0.3	V
V_O	Output voltage	VBAT Power state	-0.3		V_{BAT}+ 0.3	V
I_I	Input current		-10		10	mA
I_O	Output current		-20		20	mA
I_{OPC}	PSW Output continuous current				50	mA
I_{OPP}	PSW Output pulsed current	1 second pulse			150	mA
V_{ESD}	ESD Voltage	CDM			±500	V
		HBM			±4000	V
I_{LU}	Latch-up Current				100	mA
T_{STG}	Storage Temperature		-55		125	°C
T_{OP}	Operating Temperature		-40		85	°C
T_{SLD}	Lead temperature	Hand soldering for 10 seconds			300	°C
T_{REF}	Reflow soldering temperature	Reflow profile per JEDEC J-STD-020D.1			260	°C

4.2 Power Supply Parameters

Figure 3 and Table 5 describe the power supply and switchover parameters. See Power Control and Switching for a detailed description of the operations.

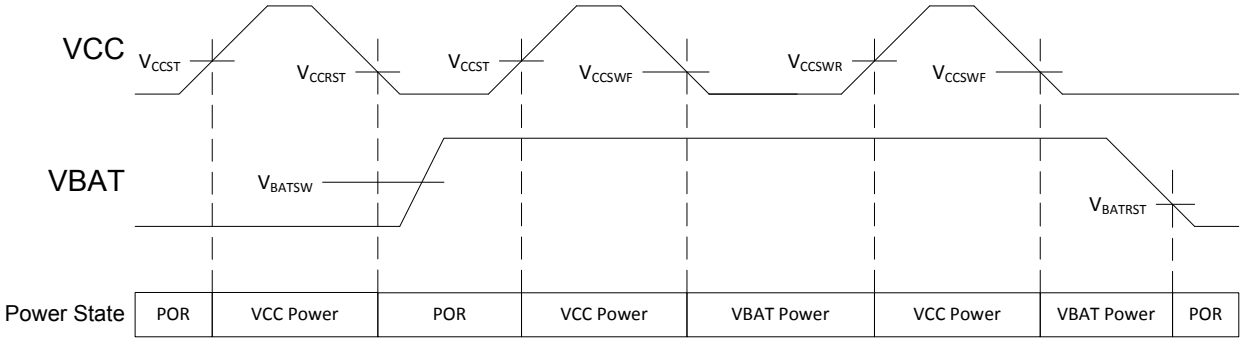


Figure 3. Power Supply Switchover

For Table 5, T_A = -40 °C to 85 °C, TYP values at 25 °C.

Table 5: Power Supply and Switchover Parameters

SYMBOL	PARAMETER	PWR	TYPE	POWER STATE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	System Power Voltage	VCC	Static	VCC Power	Clocks operating and RAM and registers retained	1.5		3.6	V
V_{CCIO}	VCC I/O Interface Voltage	VCC	Static	VCC Power	I^2C or SPI operation	1.5		3.6	V
V_{CCST}	VCC Start-up Voltage(1)	VCC	Rising	POR -> V_{CC} Power		1.6			V
V_{CCRST}	VCC Reset Voltage	VCC	Falling	VCC Power -> POR	$V_{BAT} < V_{BAT,MIN}$ or no V_{BAT}		1.3	1.5	V
V_{CCSWR}	VCC Rising Switch-over Threshold Voltage	VCC	Rising	VBAT Power -> VCC Power	$V_{BAT} \geq V_{BATRST}$		1.6	1.7	V
V_{CCSWF}	VCC Falling Switch-over Threshold Voltage	VCC	Falling	VCC Power -> VBAT Power	$V_{BAT} \geq V_{BATSW,MIN}$	1.2	1.5		V
V_{CCSWH}	VCC Switchover Threshold Hysteresis(2)	VCC	Hyst.	VCC Power <-> VBAT Power			70		mV
V_{CCFS}	VCC Falling Slew Rate to switch to VBAT state(4)	VCC	Falling	VCC Power -> VBAT Power	$V_{CC} < V_{CCSW,MAX}$	0.7	1.4		V/ms
V_{BAT}	Battery Voltage	VBAT	Static	VBAT Power	Clocks operating and RAM and registers retained	1.4		3.6	V
V_{BATSW}	Battery Switchover Voltage Range(5)	VBAT	Static	VCC Power -> VBAT Power		1.6		3.6	V

Table 5: Power Supply and Switchover Parameters

SYMBOL	PARAMETER	PWR	TYPE	POWER STATE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATRST}	Falling Battery POR Voltage(7)	VBAT	Falling	VBAT Power -> POR	$V_{CC} < V_{CCSWF}$		1.1	1.4	V
V_{BMRG}	V_{BAT} Margin above V_{CC}(3)	VBAT	Static	V_{BAT} Power		200			mV
V_{BATESR}	V_{BAT} supply series resistance(6)	VBAT	Static	V_{BAT} Power		1.0	1.5		kΩ

(1) V_{CC} must be above V_{CCST} to exit the POR state, independent of the V_{BAT} voltage.

(2) Difference between V_{CCSWR} and V_{CCSWF}.

(3) V_{BAT} must be higher than V_{CC} by at least this voltage to ensure the AB18X5 remains in the VBAT Power state.

(4) Maximum VCC falling slew rate to guarantee correct switchover to VBAT Power state. There is no V_{CC} falling slew rate requirement if switching to the VBAT power source is not required.

(5) V_{BAT} voltage to guarantee correct transition to VBAT Power state when V_{CC} falls.

(6) Total series resistance of the power source attached to the VBAT pin. The optimal value is 1.5kΩ, which may require an external resistor. VBAT power source ESR + external resistor value = 1.5kΩ.

(7) V_{BATRST} is also the static voltage required on V_{BAT} for register data retention.

4.3 Operating Parameters

Table 6 lists the operating parameters.

For Table 6, T_A = -40 °C to 85 °C, TYP values at 25 °C.

Table 6: Operating Parameters

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going Input Threshold Voltage		3.0V		1.5	2.0	V
			1.8V		1.1	1.25	
V_{T-}	Negative-going Input Threshold Voltage		3.0V	0.8	0.9		V
			1.8V	0.5	0.6		
I_{ILEAK}	Input leakage current		3.0V		0.02	80	nA
C_I	Input capacitance				3		pF
V_{OH}	High level output voltage on push-pull outputs		1.7V – 3.6V	0.8•V_{CC}			V
V_{OL}	Low level output voltage		1.7V – 3.6V			0.2•V_{CC}	V
I_{OH}	High level output current on push-pull outputs	V_{OH} = 0.8•V_{CC}	1.7V	-2	-3.8		mA
			1.8V	-3	-4.3		
			3.0V	-7	-11		
			3.6V	-8.8	-15		
I_{OL}	Low level output current	V_{OL} = 0.2•V_{CC}	1.7V	3.3	5.9		mA
			1.8V	6.1	6.9		
			3.0V	17	19		
			3.6V	18	20		
R_{DSON}	PSW output resistance to VSS	PSW Enabled	1.7V		1.7	5.8	Ω
			1.8V		1.6	5.4	
			3.0V		1.1	3.8	
			3.6V		1.05	3.7	
I_{OLEAK}	Output leakage current		1.7V – 3.6V		0.02	80	nA

4.4 Oscillator Parameters

Table 7 lists the oscillator parameters.

For Table 7, T_A = -40 °C to 85 °C unless otherwise indicated.
V_{CC} = 1.7 to 3.6V, TYP values at 25 °C and 3.0V.

Table 7: Oscillator Parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{XT}	XI and XO pin Crystal Frequency			32.768		kHz
F_{OF}	XT Oscillator failure detection frequency			8		kHz
C_{INX}	Internal XI and XO pin capacitance			1		pF
C_{EX}	External XI and XO pin PCB capacitance			1		pF
OA_{XT}	XT Oscillation Allowance	At 25°C using a 32.768 kHz crystal	270	320		kΩ
F_{RCC}	Calibrated RC Oscillator Frequency(1)	Factory Calibrated at 25°C, VCC = 2.8V		128		Hz
F_{RCU}	Uncalibrated RC Oscillator Frequency	Calibration Disabled (OFFSETR = 0)	89	122	220	Hz
J_{RCCC}	RC Oscillator cycle-to-cycle jitter	Calibration Disabled (OFFSETR = 0) – 128 Hz		2000		ppm
		Calibration Disabled (OFFSETR = 0) – 1 Hz		500		
A_{XT}	XT mode digital calibration accuracy(1)	Calibrated at an initial temperature and voltage	-2		2	ppm
A_{AC}	Autocalibration mode timing accuracy, 512 second period, T_A = -10°C to 60°C(1)	24 hour run time		35		ppm
		1 week run time		20		
		1 month run time		10		
		1 year run time		3		
T_{AC}	Autocalibration mode operating temperature(2)		-10		60	°C

(1) Timing accuracy is specified at 25°C after digital calibration of the internal RC oscillator and 32.768 kHz crystal. A typical 32.768 kHz tuning fork crystal has a negative temperature coefficient with a parabolic frequency deviation, which due to the crystal alone can result in a change of up to 150 ppm across the entire operating temperature range of -40°C to 85°C in XT mode. Autocalibration mode timing accuracy is specified relative to XT mode timing accuracy from -10°C to 60°C.

(2) Outside of this temperature range, the RC oscillator frequency change due to temperature may be outside of the allowable RC digital calibration range (+/-12%) for autocalibration mode.If this happens, an autocalibration failure will occur and the ACF interrupt flag is set. The AB18X5 should be switched to use the XT oscillator as its clock source. Please see the Autocalibration Fail section for more details.

Figure 4 shows the typical calibrated RC oscillator frequency variation vs. temperature. RC oscillator calibrated at 2.8V, 25°C.

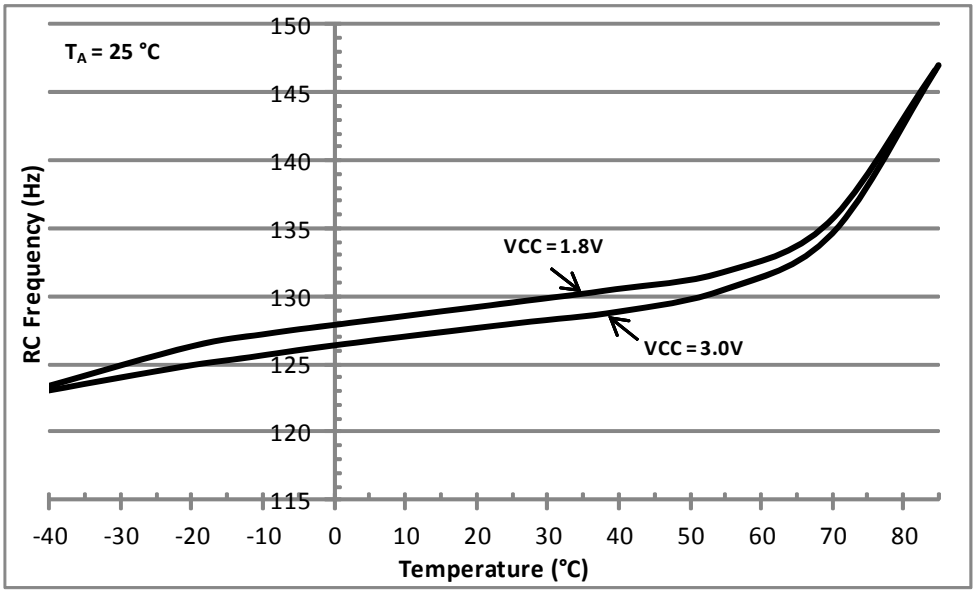


Figure 4. Calibrated RC Oscillator Typical Frequency Variation vs. Temperature

Figure 5 shows the typical uncalibrated RC oscillator frequency variation vs. temperature.

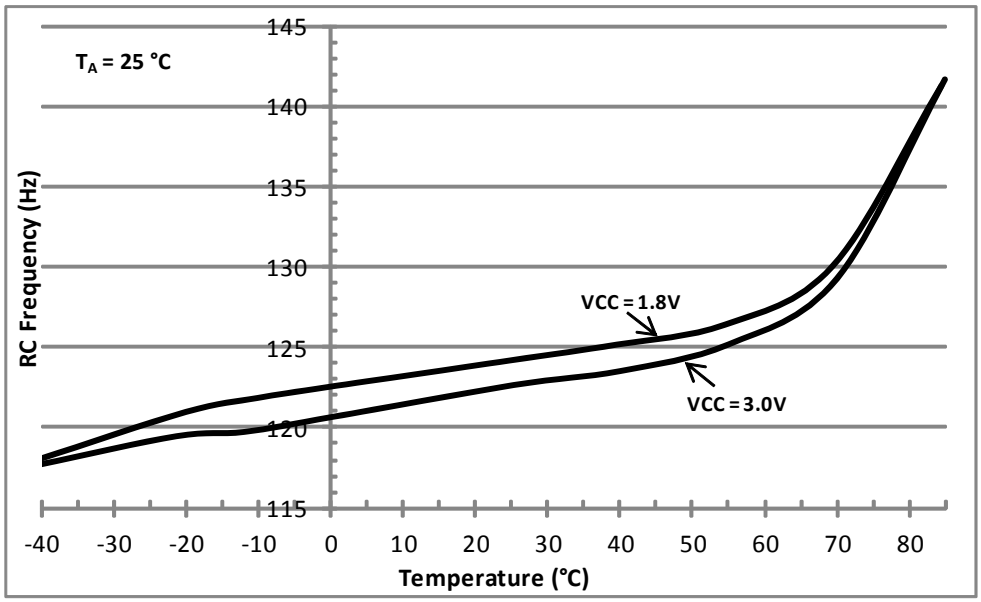


Figure 5. Uncalibrated RC Oscillator Typical Frequency Variation vs. Temperature

4.5 V_{CC} Supply Current

Table 8 lists the current supplied into the VCC power input under various conditions.

For Table 8, T_A = -40 °C to 85 °C, VBAT = 0 V to 3.6 V
TYP values at 25 °C, MAX values at 85 °C, VCC Power state

Table 8: V_{CC} Supply Current

SYMBOL	PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{VCC:I2C}$	V_{CC} supply current during I^2C burst read/write	400kHz bus speed, 2.2k pull-up resistors on SCL/SDA(1)	3.0V		6	10	µA
			1.8V		1.5	3	
$I_{VCC:SPIW}$	V_{CC} supply current during SPI burst write	2 MHz bus speed (2)	3.0V		8	12	µA
			1.8V		4	6	
$I_{VCC:SPIR}$	V_{CC} supply current during SPI burst read	2 MHz bus speed (2)	3.0V		23	37	µA
			1.8V		13	21	
$I_{VCC:XT}$	V_{CC} supply current in XT oscillator mode	Time keeping mode with XT oscillator running(3)	3.0V		55	330	nA
			1.8V		51	290	
$I_{VCC:RC}$	V_{CC} supply current in RC oscillator mode	Time keeping mode with only the RC oscillator running (XT oscillator is off)(3)	3.0V		14	220	nA
			1.8V		11	170	
$I_{VCC:ACAL}$	Average V_{CC} supply current in Autocalibrated RC oscillator mode	Time keeping mode with only RC oscillator running and Autocalibration enabled. ACP = 512 seconds(3)	3.0V		22	235	nA
			1.8V		18	190	
$I_{VCC:CK32}$	Additional V_{CC} supply current with CLKOUT at 32.786 kHz	Time keeping mode with XT oscillator running, 32.786 kHz square wave on CLKOUT(4)	3.0V		3.6	8	µA
			1.8V		2.2	5	
$I_{VCC:CK128}$	Additional V_{CC} supply current with CLKOUT at 128 Hz	All time keeping modes, 128 Hz square wave on CLKOUT(4)	3.0V		7	35	nA
			1.8V		2.5	20	

(1) Excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0V or V_{CC}. AB1805 only. Test conditions: Continuous burst read/write, 0x55 data pattern, 25 µs between each data byte, 20 pF load on each bus pin.

(2) Excluding external peripheral current. All other inputs (besides SDI, nCE and SCL) are at 0V or V_{CC}. AB1815 only. Test conditions: Continuous burst write, 0x55 data pattern, 25 µs between each data byte, 20 pF load on each bus pin.

(3) All inputs and outputs are at 0 V or V_{CC}.

(4) All inputs and outputs except CLKOUT are at 0 V or V_{CC}. 15 pF capacitive load on CLKOUT.

Figure 6 shows the typical VCC power state operating current vs. temperature in XT mode.

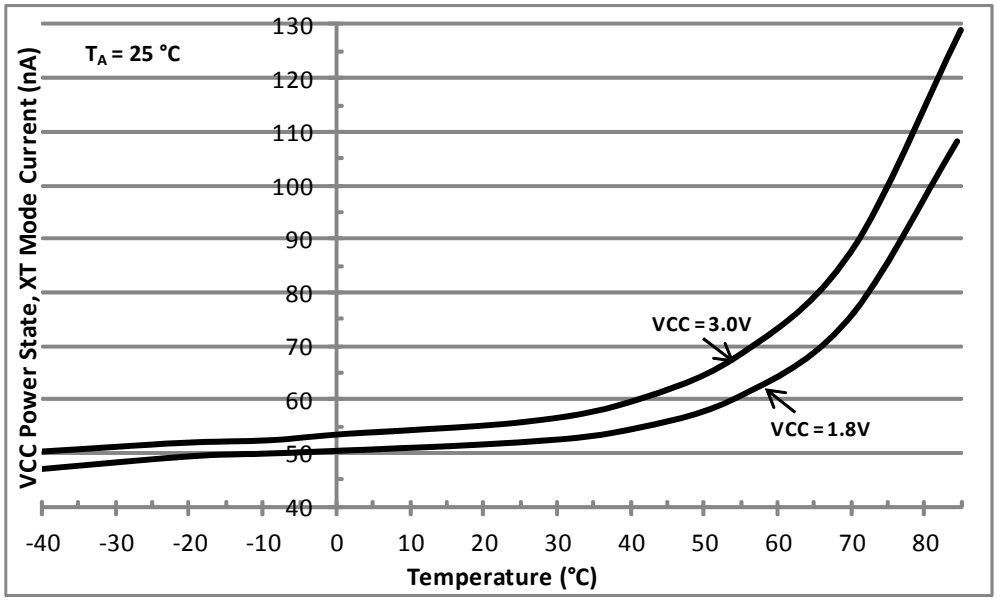


Figure 6. Typical VCC Current vs. Temperature in XT Mode

Figure 7 shows the typical VCC power state operating current vs. temperature in RC mode.

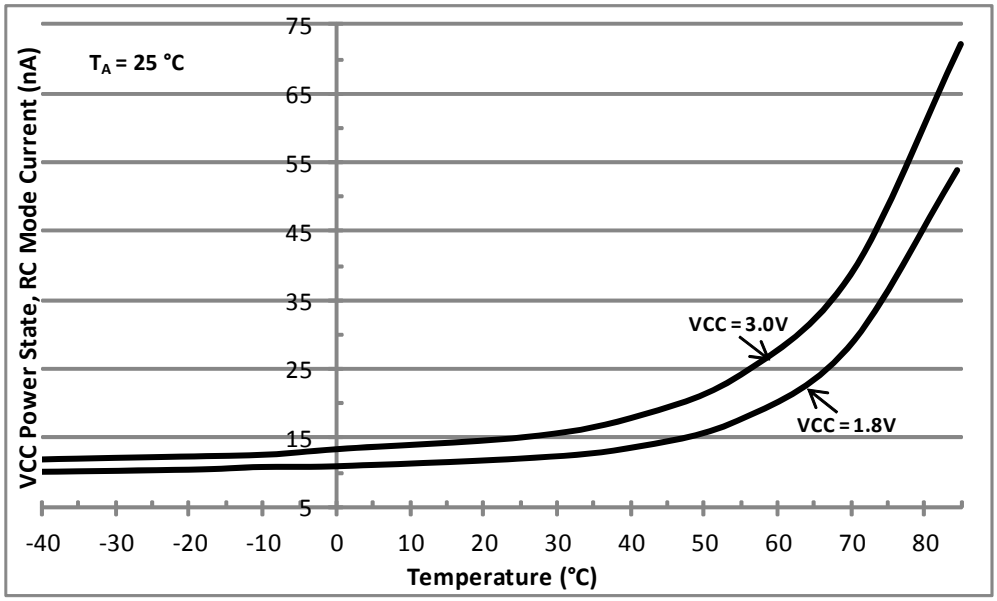


Figure 7. Typical VCC Current vs. Temperature in RC Mode

Figure 8 shows the typical VCC power state operating current vs. temperature in RC Autocalibration mode.

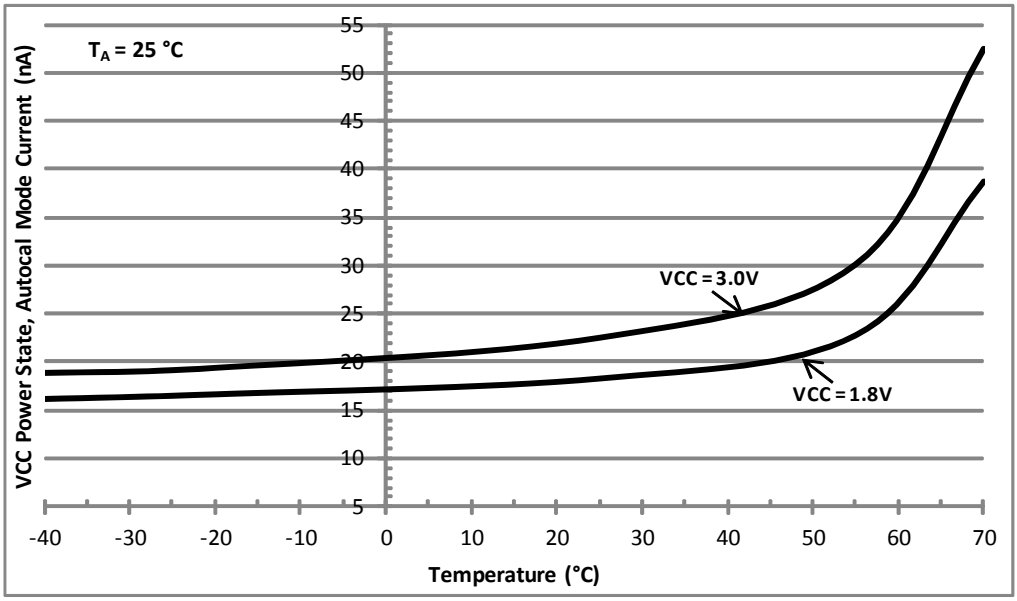


Figure 8. Typical VCC Current vs. Temperature in RC Autocalibration Mode

Figure 9 shows the typical VCC power state operating current vs. voltage for XT Oscillator and RC Oscillator modes and the average current in RC Autocalibrated mode.

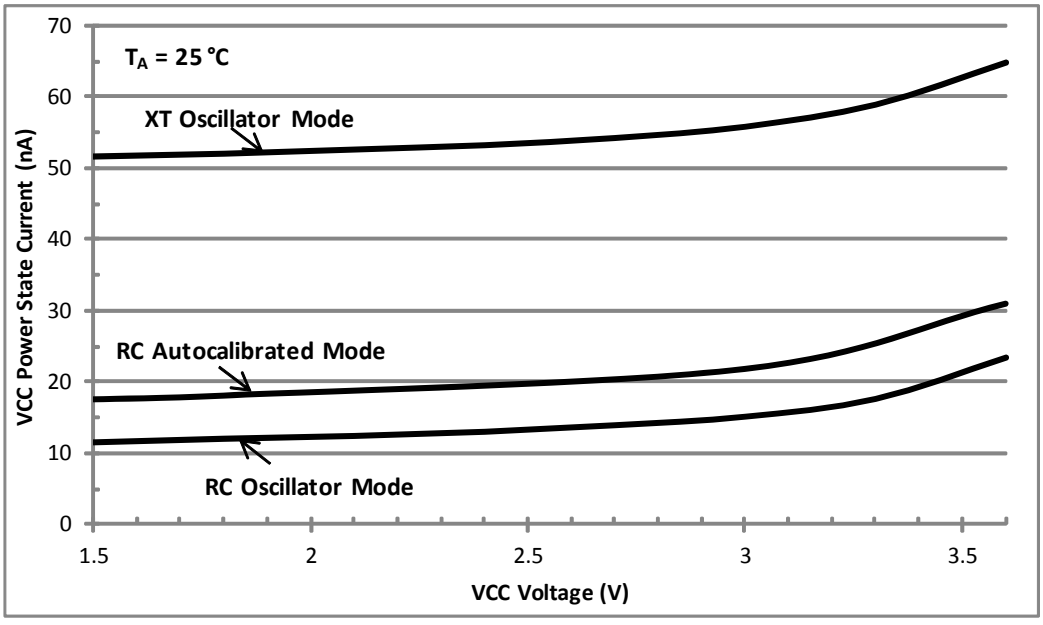


Figure 9. Typical VCC Current vs. Voltage, Different Modes of Operation

Figure 10 shows the typical VCC power state operating current during continuous I^2C and SPI burst read and write activity. Test conditions: T_A = 25 °C, 0x55 data pattern, 25 µs between each data byte, 20 pF load on each bus pin, pull-up resistor current not included.

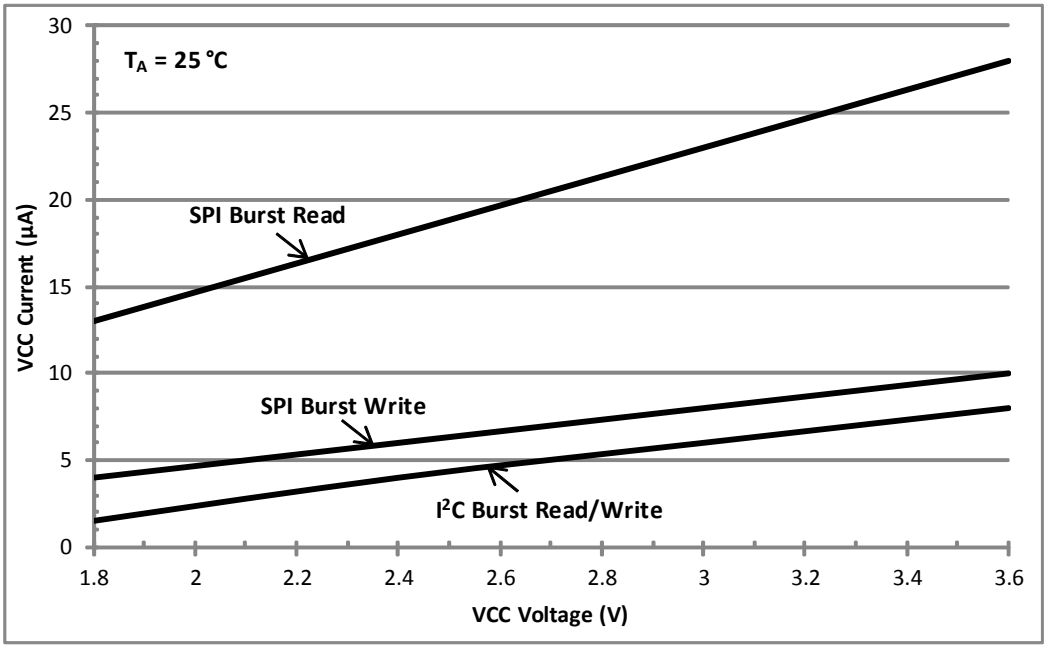


Figure 10. Typical VCC Current vs. Voltage, I^2C and SPI Burst Read/Write

Figure 11 shows the typical VCC power state operating current with a 32.768 kHz clock output on the CLKOUT pin. Test conditions: T_A = 25 °C, All inputs and outputs except CLKOUT are at 0 V or VCC. 15 pF capacitive load on the CLKOUT pin.

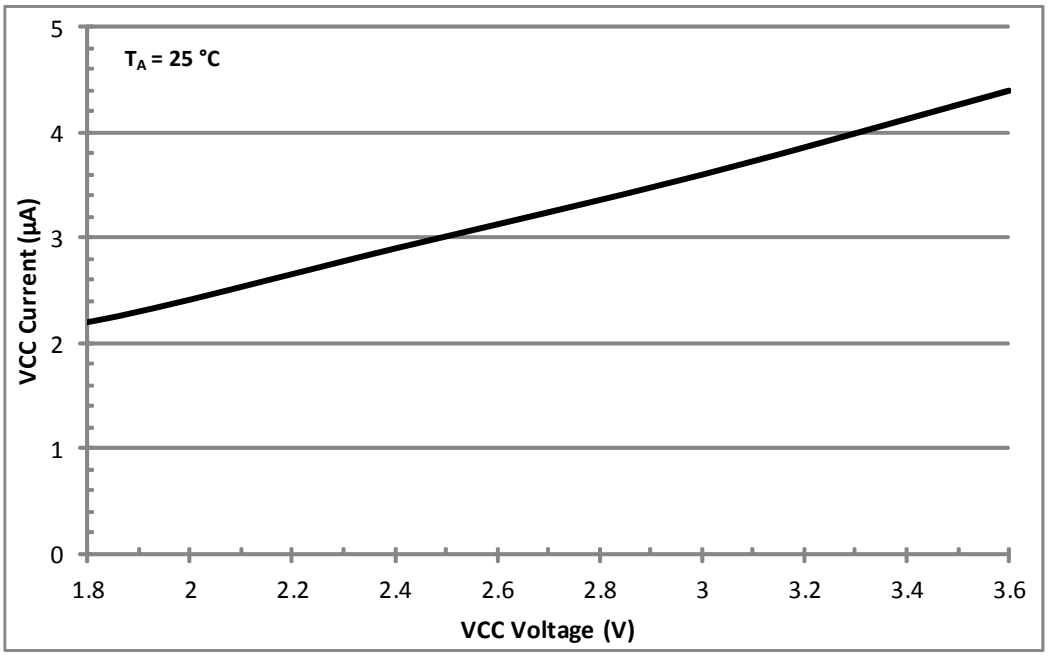


Figure 11. Typical VCC Current vs. Voltage, 32.768 kHz Clock Output

4.6 VBAT Supply Current

Table 9 lists the current supplied into the VBAT power input under various conditions.

For Table 9, T_A = -40 °C to 85 °C, TYP values at 25 °C, MAX values at 85 °C, V_{BAT} Power state.

Table 9: V_{BAT} Supply Current

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	V_{BAT}	MIN	TYP	MAX	UNIT
$I_{VBAT:XT}$	VBAT supply current in XT oscillator mode	Time keeping mode with XT oscillator running(1)	< V_{CCSWF}	3.0V		56	330	nA
				1.8V		52	290	
$I_{VBAT:RC}$	VBAT supply current in RC oscillator mode	Time keeping mode with only the RC oscillator running (XT oscillator is off)(1)	< V_{CCSWF}	3.0V		16	220	nA
				1.8V		12	170	
$I_{VBAT:ACAL}$	Average VBAT supply current in Autocalibrated RC oscillator mode	Time keeping mode with the RC oscillator running. Autocalibration enabled. ACP = 512 seconds(1)	< V_{CCSWF}	3.0V		24	235	nA
				1.8V		20	190	
$I_{VBAT:VCC}$	VBAT supply current in VCC powered mode	V_{CC} powered mode(1)	1.7 - 3.6 V	3.0V	-5	0.6	20	nA
				1.8V	-10	0.5	16	

(1) Test conditions: All inputs and outputs are at 0 V or V_{CC}.

Figure 12 shows the typical VBAT power state operating current vs. temperature in XT mode.

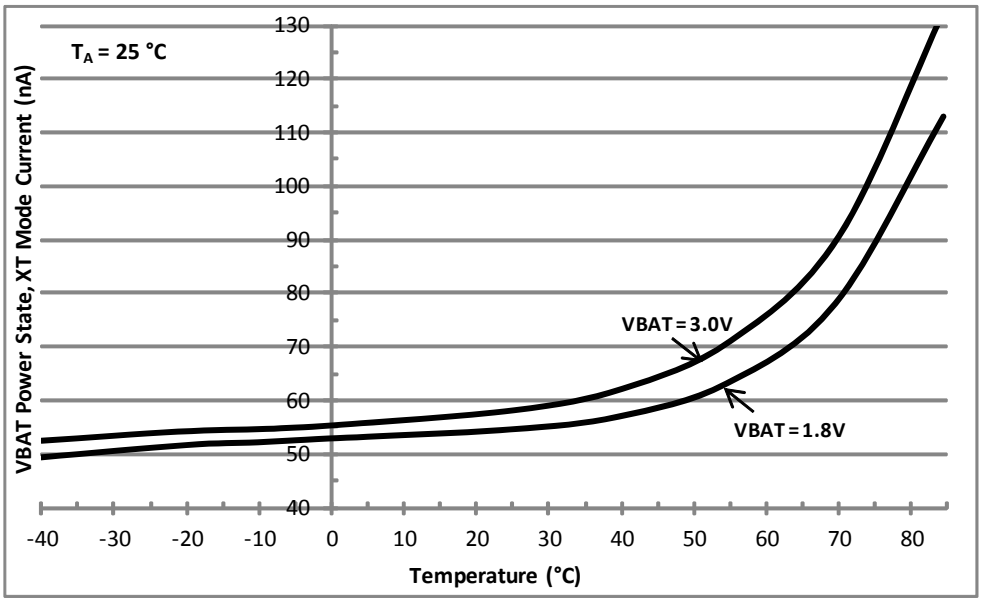


Figure 12. Typical VBAT Current vs. Temperature in XT Mode

Figure 13 shows the typical VBAT power state operating current vs. temperature in RC mode.

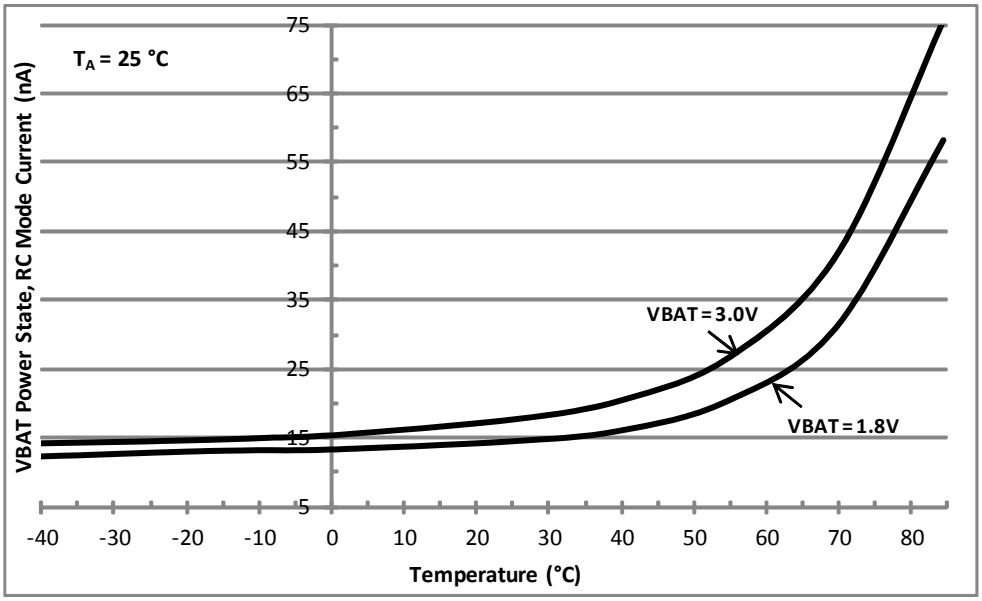


Figure 13. Typical VBAT Current vs. Temperature in RC Mode

Figure 14 shows the typical VBAT power state operating current vs. temperature in RC Autocalibration mode.

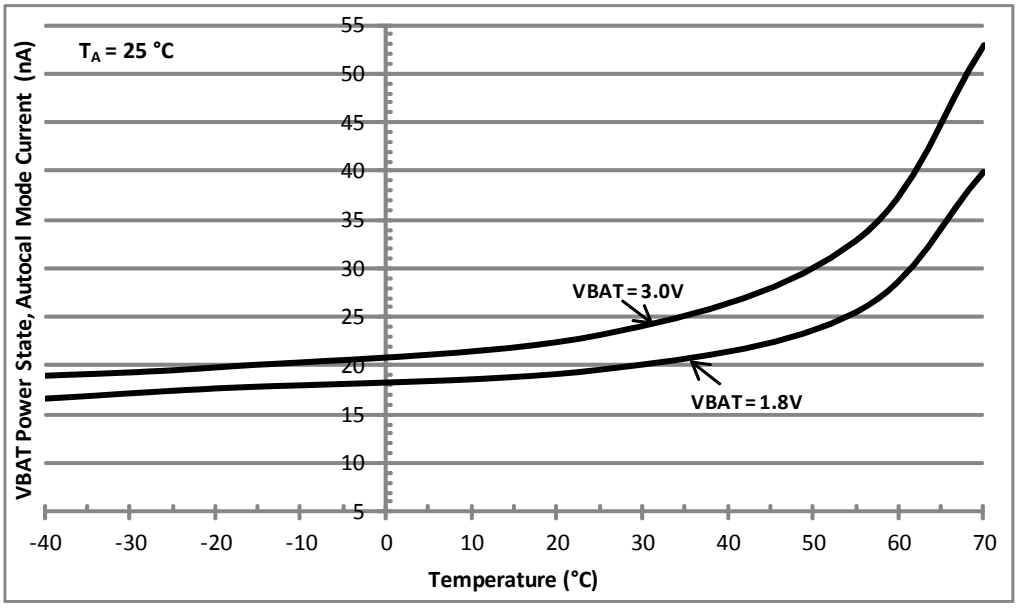


Figure 14. Typical VBAT Current vs. Temperature in RC Autocalibration Mode

Figure 15 shows the typical VBAT power state operating current vs. voltage for XT Oscillator and RC Oscillator modes and the average current in RC Autocalibrated mode, VCC = 0 V.

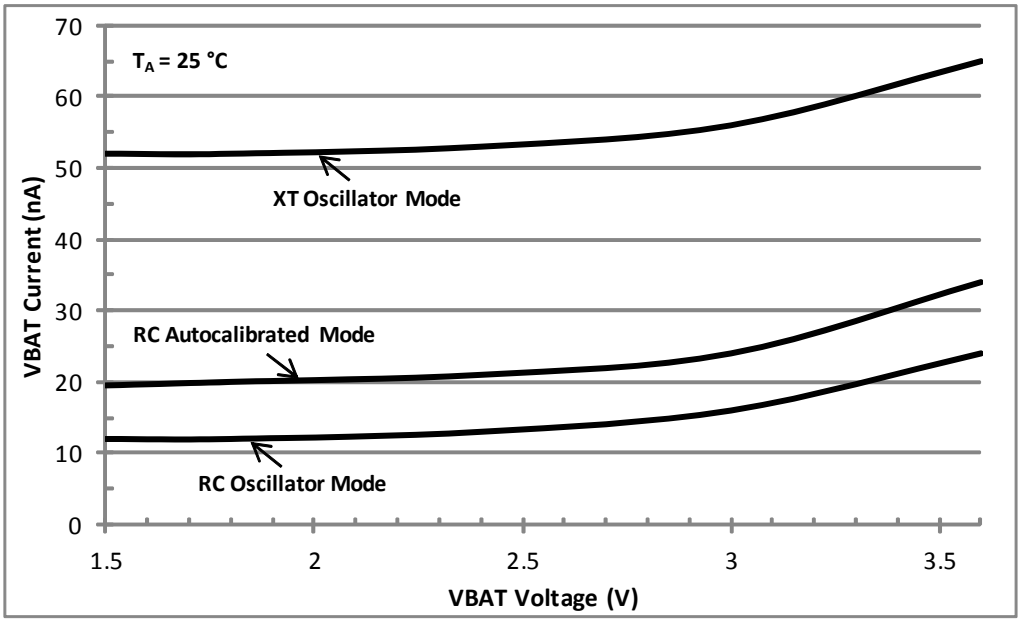


Figure 15. Typical VBAT Current vs. Voltage, Different Modes of Operation

Figure 16 shows the typical VBAT current when operating in the VCC power state, VCC = 1.7 V.

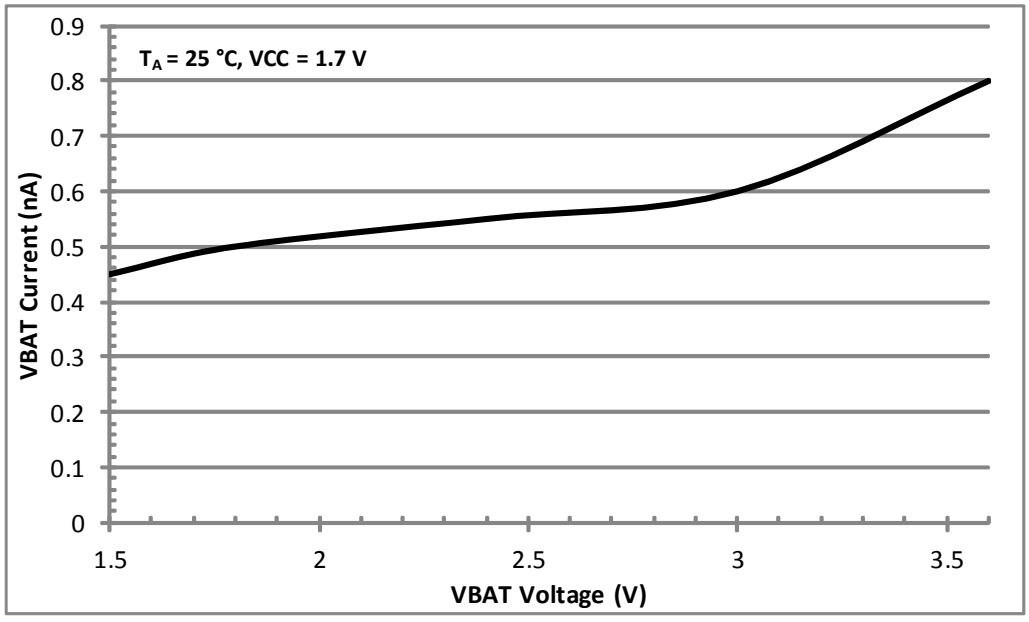


Figure 16. Typical VBAT Current vs. Voltage in VCC Power State

4.7 BREF Electrical Characteristics

Table 10 lists the parameters of the VBAT voltage thresholds. BREF values other than those listed in the table are not supported.

For Table 10, T_A = -20 °C to 70 °C, TYP values at 25 °C, VCC = 1.7 to 3.6V.

Table 10: BREF Parameters

SYMBOL	PARAMETER	BREF	MIN	TYP	MAX	UNIT
V_{BRF}	VBAT falling threshold	0111	2.3	2.5	3.3	V
		1011	1.9	2.1	2.8	
		1101	1.6	1.8	2.5	
		1111		1.4		
V_{BRR}	VBAT rising threshold	0111	2.6	3.0	3.4	V
		1011	2.1	2.5	2.9	
		1101	1.9	2.2	2.7	
		1111		1.6		
V_{BRH}	VBAT threshold hysteresis	0111		0.5		V
		1011		0.4		
		1101		0.4		
		1111		0.2		
T_{BR}	VBAT analog comparator recommended operating temperature range	All values	-20		70	°C

4.8 I²C AC Electrical Characteristics

Figure 17 and Table 11 describe the I²C AC electrical parameters.

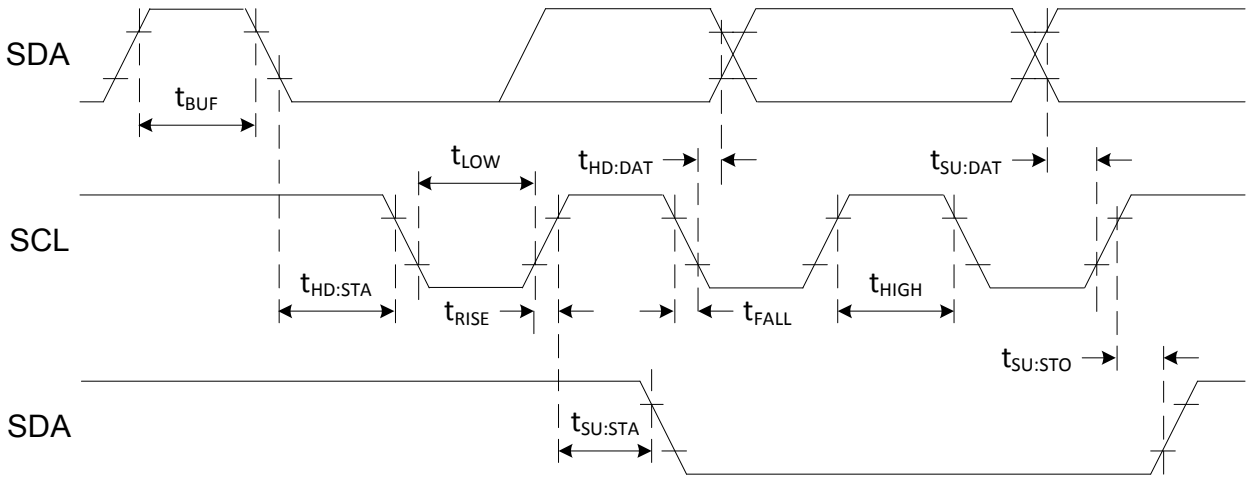


Figure 17. I²C AC Parameter Definitions

For Table 11, T_A = -40 °C to 85 °C, TYP values at 25 °C.

Table 11: I²C AC Electrical Parameters

SYMBOL	PARAMETER	VCC	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	1.7V-3.6V	10		400	kHz
t_{LOW}	Low period of SCL clock	1.7V-3.6V	1.3			µs
t_{HIGH}	High period of SCL clock	1.7V-3.6V	600			ns
t_{RISE}	Rise time of SDA and SCL	1.7V-3.6V			300	ns
t_{FALL}	Fall time of SDA and SCL	1.7V-3.6V			300	ns
$t_{HD:STA}$	START condition hold time	1.7V-3.6V	600			ns
$t_{SU:STA}$	START condition setup time	1.7V-3.6V	600			ns
$t_{SU:DAT}$	SDA setup time	1.7V-3.6V	100			ns
$t_{HD:DAT}$	SDA hold time	1.7V-3.6V	0			ns
$t_{SU:STO}$	STOP condition setup time	1.7V-3.6V	600			ns
t_{BUF}	Bus free time before a new transmission	1.7V-3.6V	1.3			µs

4.9 SPI AC Electrical Characteristics

Figure 18, Figure 19, and Table 12 describe the SPI AC electrical parameters.

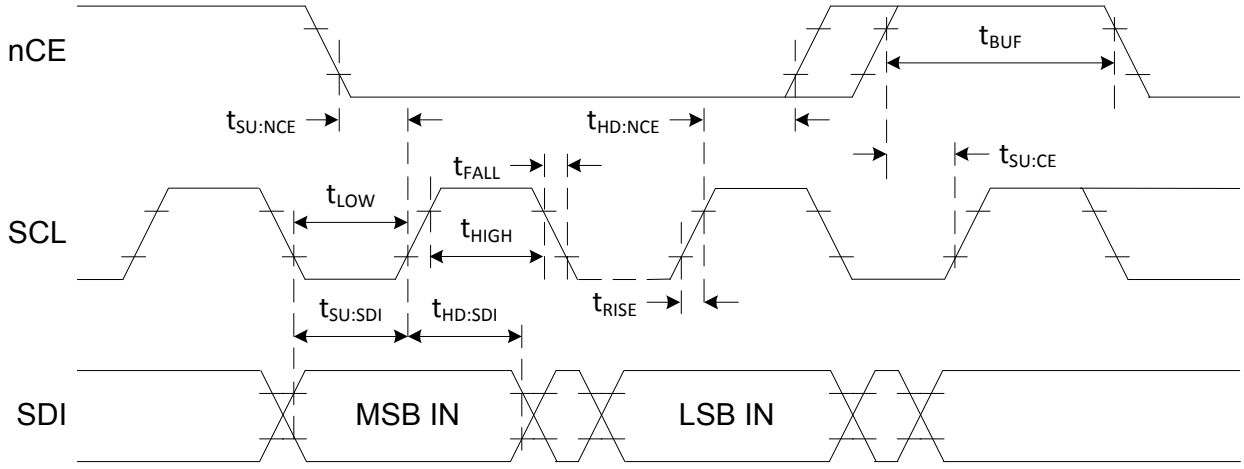


Figure 18. SPI AC Parameter Definitions – Input

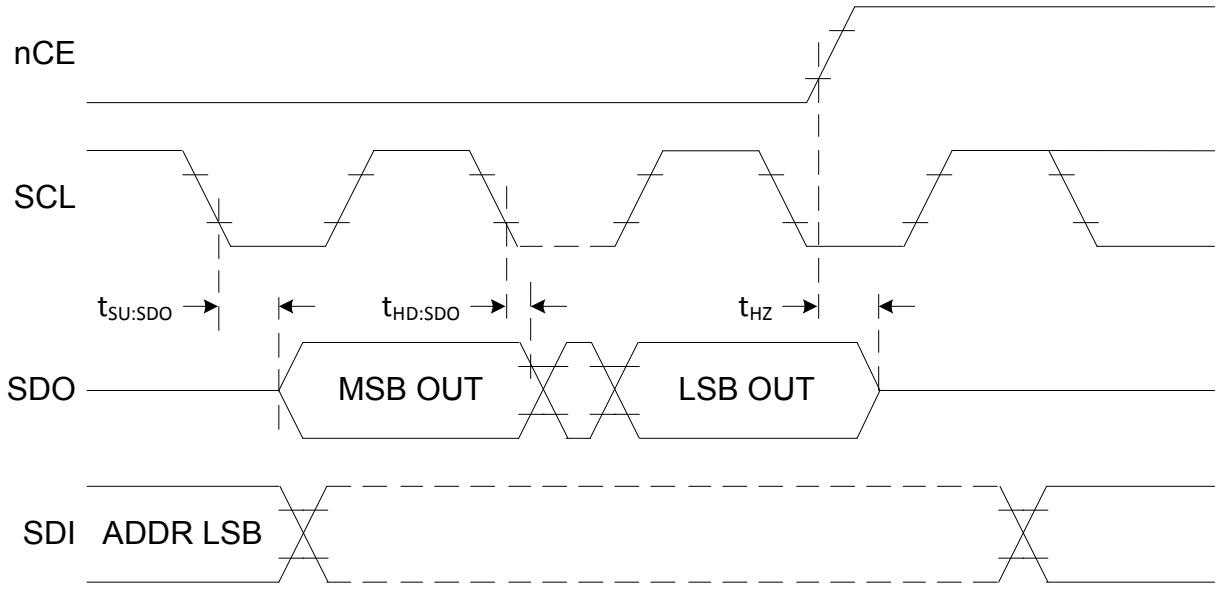


Figure 19. SPI AC Parameter Definitions – Output

For Table 12, T_A = -40 °C to 85 °C, TYP values at 25 °C.

Table 12: SPI AC Electrical Parameters

SYMBOL	PARAMETER	VCC	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	1.7V–3.6V	0.01		2	MHz
t_{LOW}	Low period of SCL clock	1.7V–3.6V	200			ns
t_{HIGH}	High period of SCL clock	1.7V–3.6V	200			ns
t_{RISE}	Rise time of all signals	1.7V–3.6V			1	µs
t_{FALL}	Fall time of all signals	1.7V–3.6V			1	µs
$t_{SU:NCE}$	nCE low setup time to SCL	1.7V–3.6V	200			ns
$t_{HD:NCE}$	nCE hold time to SCL	1.7V–3.6V	200			ns
$t_{SU:CE}$	nCE high setup time to SCL	1.7V–3.6V	200			ns
$t_{SU:SDI}$	SDI setup time	1.7V–3.6V	40			ns
$t_{HD:SDI}$	SDI hold time	1.7V–3.6V	50			ns
$t_{SU:SDO}$	SDO output delay from SCL	1.7V–3.6V			150	ns
$t_{HD:SDO}$	SDO output hold from SCL	1.7V–3.6V	0			ns
t_{HZ}	SDO output Hi-Z from nCE	1.7V–3.6V			250	ns
t_{BUF}	nCE high time before a new transmission	1.7V–3.6V	200			ns

4.10 Power On AC Electrical Characteristics

Figure 20 and Table 13 describe the power on AC electrical characteristics for the FOUT pin and XT oscillator.

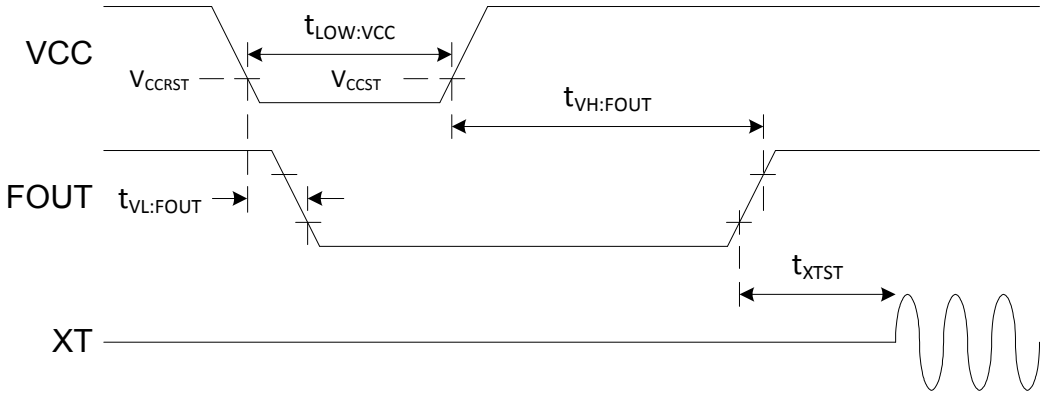


Figure 20. Power On AC Electrical Characteristics

For Table 13, T_A = -40 °C to 85 °C, VBAT < 1.2 V

Table 13: Power On AC Electrical Parameters

SYMBOL	PARAMETER	VCC	T_A	MIN	TYP	MAX	UNIT
$t_{LOW:VCC}$	Low period of VCC to ensure a valid POR	1.7V–3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VL:FOUT}$	VCC low to FOUT low	1.7V–3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VH:FOUT}$	VCC high to FOUT high	1.7V–3.6V	85 °C		0.4		s
			25 °C		0.5		
			-20 °C		3		
			-40 °C		20		
t_{XTST}	FOUT high to XT oscillator start	1.7V–3.6V	85 °C		0.4		s
			25 °C		0.4		
			-20 °C		0.5		
			-40 °C		1.5		

4.11 nRST AC Electrical Characteristics

Figure 21 and Table 14 describe the nRST and nEXTR AC electrical characteristics.

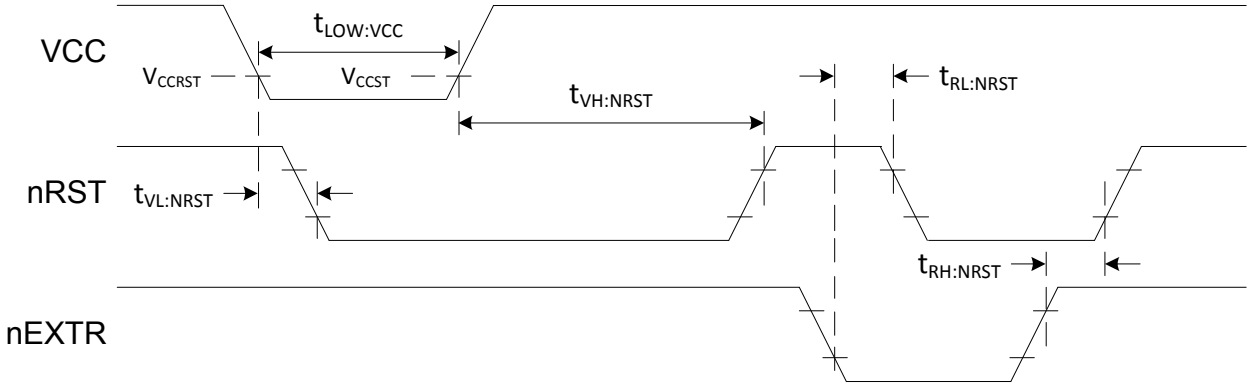


Figure 21. nRST AC Parameter Characteristics

For Table 14, T_A = -40 °C to 85 °C, TYP at 25 °C unless specified otherwise, VBAT < 1.2 V.

Table 14: nRST AC Electrical Parameters

SYMBOL	PARAMETER	VCC	T_A	MIN	TYP	MAX	UNIT
$t_{LOW:VCC}$	Low period of VCC to ensure a valid POR	1.7V-3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VL:NRST}$	VCC low to nRST low	1.7V-3.6V	85 °C		0.1		s
			25 °C		0.1		
			-20 °C		1.5		
			-40 °C		10		
$t_{VH:NRST}$	VCC high to nRST high	1.7V-3.6V	85 °C		0.5		s
			25 °C		0.5		
			-20 °C		3.5		
			-40 °C		25		
$t_{RL:NRST}$	nEXTR low to nRST low	1.7V-3.6V	-40 °C to 85 °C		30	50	ns
$t_{RH:NRST}$	nEXTR high to nRST high	1.7V-3.6V	-40 °C to 85 °C		50	80	ns

5. Functional Description

Figure 22 illustrates the AB18X5 functional design.

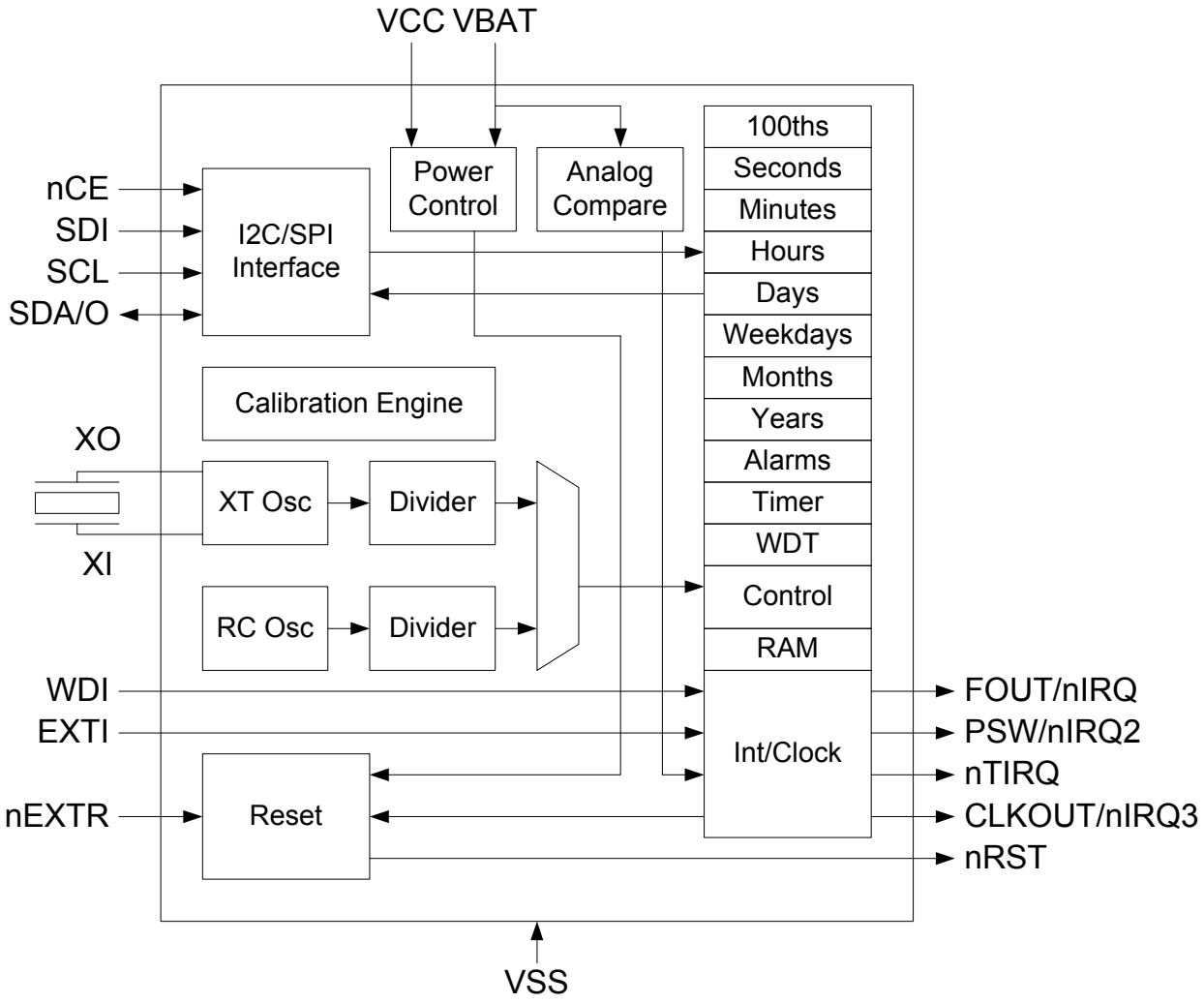


Figure 22. Detailed Block Diagram

AB18X5 serves as a companion part for host processors including microcontrollers, radios, and digital signal processors. It tracks time as in a typical RTC product and additionally provides unique power management functionality that makes it ideal for highly energy-constrained applications. To support such operation, the AB18X5 includes 3 distinct feature groups: 1) baseline timekeeping features, 2) advanced timekeeping features, and 3) power management features. Functions from each feature group may be controlled via I/O offset mapped registers. These registers are accessed using either an I^2C serial interface (e.g., in the AB1805) or a SPI serial interface (e.g., in the AB1815). Each feature group is described briefly below and in greater detail in subsequent sections.

The baseline timekeeping feature group supports the standard 32.786 kHz crystal (XT) oscillation mode for maximum frequency accuracy with an ultra-low current draw of 55 nA. The baseline timekeeping feature group also includes a standard set of counters monitoring hundredths of a second up through centuries. A

complement of countdown timers and alarms may additionally be set to initiate interrupts or resets on several of the outputs.

The advanced timekeeping feature group supports two additional oscillation modes: 1) RC oscillator mode, and 2) Autocalibration mode. At only 14 nA, the temperature-compensated RC oscillator mode provides an even lower current draw than the XT oscillator for applications with reduced frequency accuracy requirements. A proprietary calibration algorithm allows the AB18X5 to digitally tune the RC oscillator frequency and the XT oscillator frequency with accuracy as low as 2 ppm at a given temperature. In Autocalibration mode, the RC oscillator is used as the primary oscillation source and is periodically calibrated against the XT oscillator. Autocalibration may be done automatically every 8.5 minutes or 17 minutes and may also be initiated via software. This mode enables average current draw of only 22 nA with frequency accuracy similar to the XT oscillator. The advanced timekeeping feature group also includes a rich set of input and output configuration options that enables the monitoring of external interrupts (e.g., pushbutton signals), the generation of clock outputs, and watchdog timer functionality.

Power management features built into the AB18X5 enable it to operate as a backup device in both line-powered and battery-powered systems. An integrated power control module automatically detects when main power (VCC) falls below a threshold and switches to backup power (VBAT). 256B of ultra-low leakage RAM enable the storage of key parameters when operating on backup power.

The AB18X5 is the first RTC to incorporate a number of more advanced power management features. In particular, the AB18X5 includes a finite state machine (integrated with the Power Control block in Figure 22) that can control a host processor as it transitions between sleep/reset states and active states. Digital outputs can be configured to control the reset signal or interrupt input of the host controller. The AB18X5 additionally integrates a power switch with ~1 Ω impedance that can be used to cut off ground current on the host microcontroller and reduce sleep current to <1 nA. The AB18X5 parts can wake up a sleeping system using internally generated timing interrupts or externally generated interrupts generated by digital inputs (e.g., using a pushbutton) or an analog comparator. The aforementioned functionality enables users to seamlessly power down host processors, leaving only the energy-efficient AB18X5 chip awake. The AB18X5 also includes voltage detection on the backup power supply.

Each functional block is explained in detail in the remainder of this section. The functional descriptions refer to the registers shown in the Register Definitions (0x00 to 0x0F) and Register Definitions (0x10 to 0xFF) tables. A detailed description of all registers can be found in the Registers section of this document.

5.1 I^2C Interface

The AB18X5 includes a standard I^2C interface. The device is accessed at addresses 0xD2/D3, and supports Fast Mode (up to 400 kHz). The I^2C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver”. The device that controls the message transfer by driving SCL is called “master”. The devices that are controlled by the master are called “slaves”. The AB18X5 is always a slave device.

I^2C termination resistors should be above 2.2 kΩ, and for systems with short I^2C bus wires/traces and few connections these terminators can typically be as large as 22 kΩ (for 400 kHz operation) or 56 kΩ (for 100 kHz operation). Larger resistors will produce lower system current consumption.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

A number of bus conditions have been defined (see Figure 23) and are described in the following sections.

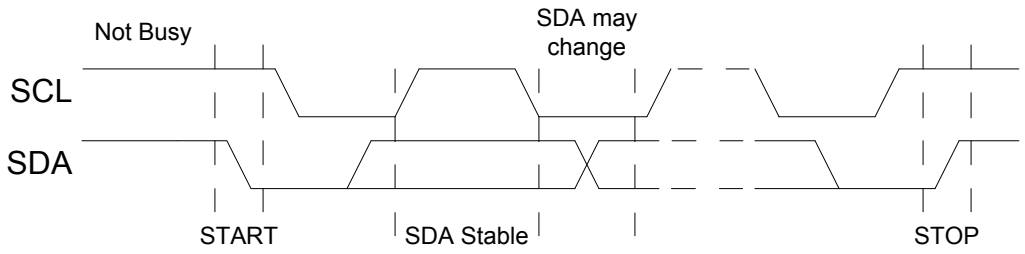


Figure 23. Basic I^2C Conditions

5.1.1 Bus Not Busy

Both SDA and SCL remain high.

5.1.2 Start Data Transfer

A change in the state of SDA from high to low, while SCL is high, defines the START condition. A START condition which occurs after a previous START but before a STOP is called a RESTART condition, and functions exactly like a normal STOP followed by a normal START.

5.1.3 Stop Data Transfer

A change in the state of SDA from low to high, while SCL is high, defines the STOP condition.

5.1.4 Data Valid

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

5.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge (ACK) bit as shown in Figure 24. This acknowledge bit is a low level driven onto SDA by the receiver, whereas the master generates an extra acknowledge related SCL pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, on a read transfer a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related SCL pulse. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge (a NAK) on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

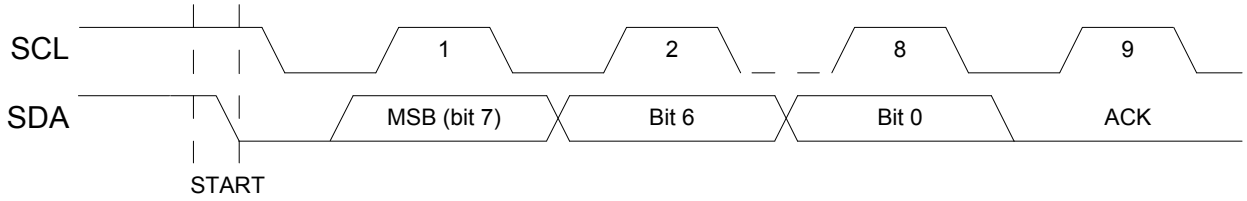


Figure 24. I²C Acknowledge Address Operation

Figure 25 illustrates the operation with which the master addresses the AB18X5. After the START condition, a 7-bit address is transmitted MSB first. If this address is 0b1101001 (0xD2/3), the AB18X5 is selected, the eighth bit indicate a write (RW = 0) or a read (RW = 1) operation and the AB18X5 supplies the ACK. The AB18X5 ignores all other address values and does not respond with an ACK.

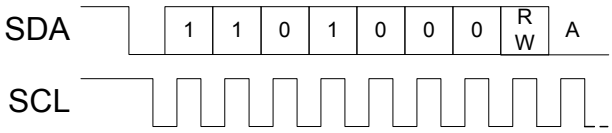


Figure 25. I²C Address Operation

5.1.6 Offset Address Transmission

If the RW bit of the Address Operation indicates a write, the next byte transmitted from the master is the Offset Address as shown in Figure 26. This value is loaded into the Address Pointer of the AB18X5.

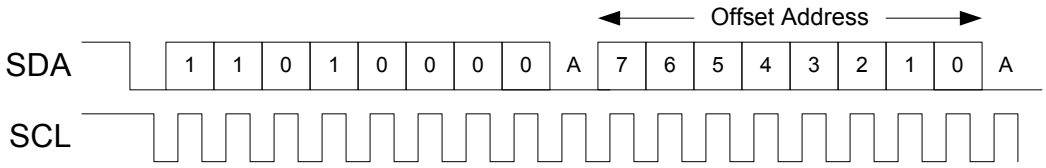


Figure 26. I²C Offset Address Transmission

5.1.7 Write Operation

In a write operation the master transmitter transmits to the AB18X5 slave receiver. The Address Operation has a RW value of 0, and the second byte contains the Offset Address as in Figure 26. The next byte is written to the register selected by the Address Pointer (which was loaded with the Offset Address) and the

Address Pointer is incremented. Subsequent transfers write bytes into successive registers until a STOP condition is received, as shown in Figure 27.

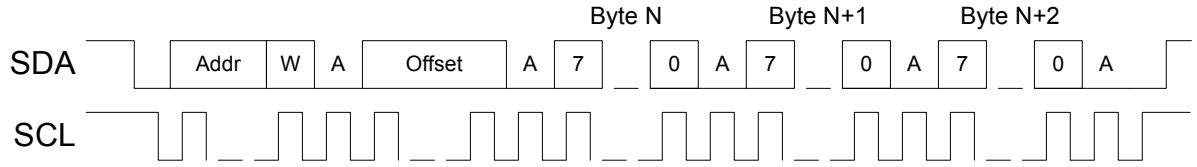


Figure 27. I²C Write Operation

5.1.8 Read Operation

In a read operation, the master first executes an Offset Address Transmission to load the Address Pointer with the desired Offset Address. A subsequent operation will again issue the address of the AB18X5 but with the RW bit as a 1 indicating a read operation. Figure 28 illustrates this transaction beginning with a RESTART condition, although a STOP followed by a START may also be used. After the address operation, the slave becomes the transmitter and sends the register value from the location pointed to by the Address Pointer, and the Address Pointer is incremented. Subsequent transactions produce successive register values, until the master receiver responds with a NAK and/or STOP or RESTART to complete the operation. Because the Address Pointer holds a valid register address, the master may initiate another read sequence at this point without performing another Offset Address operation.

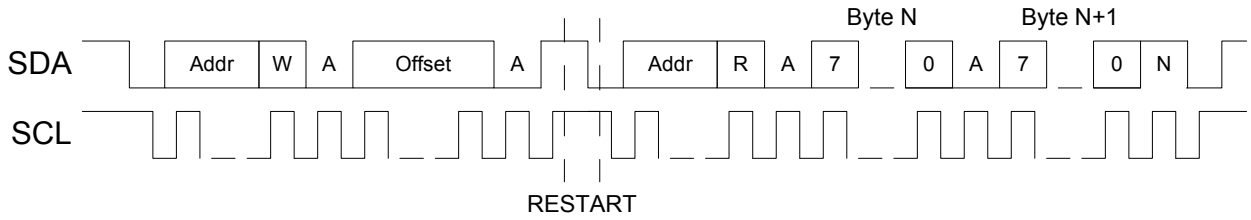


Figure 28. I²C Read Operation

5.2 SPI Interface

The AB18X5 includes a standard 4-wire SPI interface. The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It typically consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and an active low chip enable (nCE).

The AB18X5 may be connected to a master with a 3-wire SPI interface by tying SDI and SDO together. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver.” The device that controls the message transfer by driving SCL is called “master.” The devices that are controlled by the master are called “slaves”. The AB18X5 is always a slave device.

The nCE input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master and the slave devices via the SDI (master to slave) and SDO (slave to master) lines. The SCL input, which is generated by the master, is active only during address and data transfer to any device on the SPI bus.

The AB18X5 supports clock frequencies up to 2 MHz, and responds to either (CPOL = 0, CPAH = 0 or CPOL = 1, CPAH = 1). For these two modes, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL. There is one clock for

each bit transferred. Address and data bits are transferred in groups of eight bits. Some MCUs specify CPOL and CPAH in different ways, so care should be taken when configuring the SPI Master.

5.2.1 Write Operation

Figure 29 illustrates a SPI write operation. The operation is initiated when the nCE signal to the AB18X5 goes low. At that point an 8-bit Address byte is transmitted from the master on the SDI line, with the upper RW bit indicating read (if 0) or write (if 1). In this example the RW bit is a one selecting a write operation, and the lower 7 bits of the Address byte contain the Offset Address, which is loaded into the Address Pointer of the AB18X5.

Each subsequent byte is loaded into the register selected by the Address Pointer, and the Address Pointer is incremented. Because the address is only 7 bits long, only the lower 128 registers of the AB18X5 may be accessed via the SPI interface. The operation is terminated by the master by bringing the nCE signal high. Note that the SDO line is not used in a write operation and is held in the high impedance state by the AB18X5.

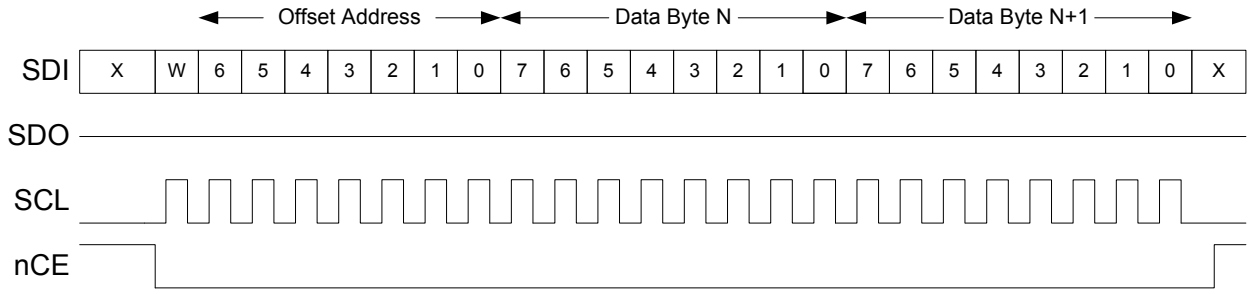


Figure 29. SPI Write Operation

5.2.2 Read Operation

Figure 30 illustrates a read operation. The address is transferred from the master to the slave just as it is in a write operation, but in this case the RW bit is a 0 indicating a read. After the transfer of the last address bit, bit 0, the AB18X5 begins driving data from the register selected by the Address Pointer onto the SDO line, bit 7 first, and the Address Pointer is incremented. The transfer continues until the master brings the nCE line high.

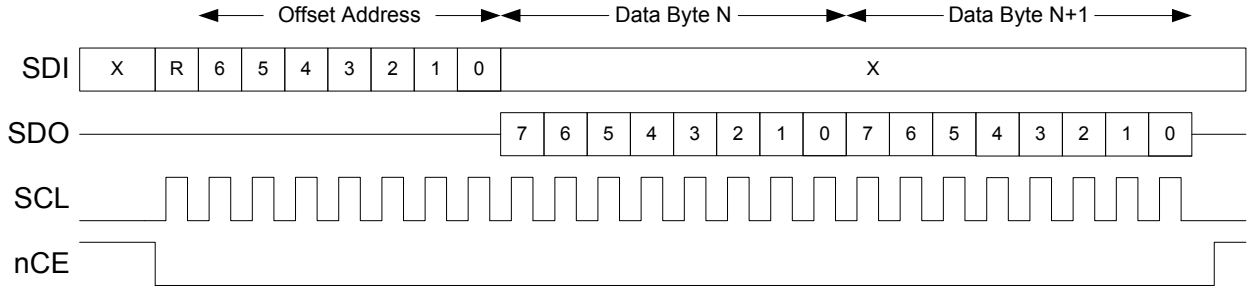


Figure 30. SPI Read Operation

5.3 XT Oscillator

The AB18X5 includes a very power efficient crystal (XT) oscillator which runs at 32.786 kHz. This oscillator is selected by setting the OSEL bit to 0 and includes a low jitter calibration function.

5.4 RC Oscillator

The AB18X5 includes an extremely low power RC oscillator which runs at 128 Hz. This oscillator is selected by setting the OSEL bit to 1. Switching between the XT and RC Oscillators is guaranteed to produce less than one second of error in the Calendar Counters. The AB18X5 may be configured to automatically switch to the RC Oscillator when VCC drops below its threshold by setting the AOS bit, and/or be configured to automatically switch if an XT Oscillator failure is detected by setting the FOS bit.

5.5 RTC Counter Access

When reading any of the counters in the RTC using a burst operation, the 1 Hz and 100 Hz clocks are held off during the access. This guarantees that a single burst will either read or write a consistent timer value (other than the Hundredths Counter – see Hundredths Synchronization). There is a watchdog function to ensure that a very long pause on the interface does not cause the RTC to lose a clock.

On a write to any of the Calendar Counters, the entire timing chain up to 100 Hz (if the XT Oscillator is selected) or up to 1Hz (if the RC Oscillator is selected) is reset to 0. This guarantees that the Counters will begin counting immediately after the write is complete, and that in the XT oscillator case the next 100 Hz clock will occur exactly 10 ms later. In the RC Oscillator case, the next 1 Hz clock will occur exactly 1 second later. This allows a burst write to configure all of the Counters and initiate a precise time start. Note that a Counter write may cause one cycle of a Square Wave output to be of an incorrect period.

The WRTC bit must be set in order to write to any of the Counter registers. This bit can be cleared to prevent inadvertent software access to the Counters.

5.6 Hundredths Synchronization

If the Hundredths Counter is read as part of the burst read from the counter registers, the following algorithm must be used to guarantee correct read information.

1. Read the Counters, using a burst read. If the Hundredths Counter is neither 00 nor 99, the read is correct.
2. If the Hundredths Counter was 00, perform the read again. The resulting value from this second read is guaranteed to be correct.
3. If the Hundredths Counter was 99, perform the read again.
   A. If the Hundredths Counter is still 99, the results of the first read are guaranteed to be correct. Note that it is possible that the second read is not correct.
   B. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read plus 1, both reads produced correct values. Alternatively, perform the read again. The resulting value from this third read is guaranteed to be correct.
   C. If the Hundredths Counter has rolled over to 00, and the Seconds Counter value from the second read is equal to the Seconds Counter value from the first read, perform the read again. The resulting value from this third read is guaranteed to be correct.

5.7 Generating Hundredths of a Second

The generation of an exact 100 Hz signal for the Hundredths Counter requires a special logic circuit. The 2.048 kHz clock signal is divided by 21 for 12 iterations, and is alternately divided by 20 for 13 iterations. This produces an effective division of:

$$(21 * 12 + 20 * 13)/25 = 20.48$$

producing an exact long-term average 100 Hz output, with a maximum jitter of less than 1 ms. The Hundredths Counter is not available when the 128 Hz RC Oscillator is selected.

5.8 Watchdog Timer

The AB18X5 includes a Watchdog Timer (WDT), which can be configured to generate an interrupt or a reset if it times out. The WDT is controlled by the Watchdog Timer Register (see 0x1B - Watchdog Timer). The RB field selects the frequency at which the timer is decremented, and the BMB field determines the value loaded into the timer when it is restarted. If the timer reaches a value of zero, the WDS bit determines whether an interrupt is generated in nIRQ. The timer reaching zero sets the WDT flag in the Status Register, which may be cleared by setting the WDT flag to zero.

Two actions will restart the WDT timer:

1. Writing the Watchdog Timer Register with a new watchdog value.
2. A change in the level of the WDI pin.

If the Watchdog Timer generates an interrupt or reset, the Watchdog Timer Register must be written in order to restart the Watchdog Timer function. If the BMB field is 0, the Watchdog Timer function is disabled.

The BMB field describes the maximum timeout delay. For example, if RB = 01 so that the clock period is 250 ms, a BMB value of 9 implies that the timeout will occur between 2000 ms and 2250 ms after writing the Watchdog Timer Register.

5.9 Digital Calibration

5.9.1 XT Oscillator Digital Calibration

In order to improve the accuracy of the XT oscillator, a Distributed Digital Calibration function is included (see 0x14 - Calibration XT). This function uses a calibration value, OFFSETX, to adjust the clock period over a 16 second or 32 second calibration period. When the 32.786 kHz XT oscillator is selected, the clock at the 16.384 kHz level of the divider chain is modified on a selectable interval. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDX bit is a 0 (normal calibration), OFFSETX cycles of the 16.384 kHz clock are gated (negative calibration) or replaced by 32.786 kHz pulses (positive calibration) within every 32 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 1.907 ppm, with a maximum adjustment of ~+120/-122 ppm. If the CMDX bit is 1 (coarse calibration), OFFSETX cycles of the 16.384 kHz clock are gated or replaced by the 32.786 kHz clock within every 16 second calibration period. In this mode, each step in OFFSETX modifies the clock frequency by 3.814 ppm, with a maximum adjustment of ~+240/-244 ppm. OFFSETX contains a two's complement value, so the possible steps are from -64 to +63. Note that unlike other implementations, Distributed Digital Calibration guarantees that the clock is precisely calibrated every 32 seconds with normal calibration and every 16 seconds when coarse calibration is selected.

In addition to the normal calibration, the AB18X5 also includes an Extended Calibration field to compensate for low capacitance environments. The frequency generated by the Crystal Oscillator may be slowed by 122 ppm times the value in the XTCAL (see 0x1D – Oscillator Status Register) field (0, -122,-244 or -366 ppm). The clock is still precisely calibrated in 16 or 32 seconds. The pulses which are added to or subtracted from the 16.384 kHz clock are spread evenly over each 16 or 32 second period using the Ambiq Micro patented Distributed Calibration algorithm. This ensures that in XT mode the maximum cycle-to-cycle jitter in any clock of a frequency 16.384 kHz or lower caused by calibration will be no more than one 16.384 kHz period. This maximum jitter applies to all clocks in the AB18X5, including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto a clock output pin.

The XT oscillator calibration value is determined by the following process:

1. Set the OFFSETX, CMDX and XTCAL register fields to 0 to ensure calibration is not occurring.
2. Select the XT oscillator by setting the OSEL bit to 0.
3. Configure a 32768 Hz frequency square wave output on one of the output pins.

4. Precisely measure the exact frequency, Fmeas, at the output pin in Hz.
5. Compute the adjustment value required in ppm as ((32768 – Fmeas)*1000000)/32768 = PAdj
6. Compute the adjustment value in steps as PAdj/(1000000/2^19) = PAdj/(1.90735) = Adj
7. If Adj < -320, the XT frequency is too high to be calibrated
8. Else if Adj < -256, set XTCAL = 3, CMDX = 1, OFFSETX = (Adj +192)/2
9. Else if Adj < -192, set XTCAL = 3, CMDX = 0, OFFSETX = Adj +192
10. Else if Adj < -128, set XTCAL = 2, CMDX = 0, OFFSETX = Adj +128
11. Else if Adj < -64, set XTCAL = 1, CMDX = 0, OFFSETX = Adj + 64
12. Else if Adj < 64, set XTCAL = 0, CMDX = 0, OFFSETX = Adj
13. Else if Adj < 128, set XTCAL = 0, CMDX = 1, OFFSETX = Adj/2
14. Else the XT frequency is too low to be calibrated

5.9.2 RC Oscillator Digital Calibration

The RC Oscillator has a patented Distributed Digital Calibration function similar to that of the XT Oscillator (see 0x14 - Calibration XT). However, because the RC Oscillator has a greater fundamental variability, the range of calibration is much larger, with four calibration ranges selected by the CMDR field. When the 128 Hz RC oscillator is selected, the clock at the 64 Hz level of the divider chain is modified on a selectable interval using the calibration value OFFSETR. Clock pulses are either added or subtracted to ensure accuracy of the counters. If the CMDR field is 00, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 8,192 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 1.907 ppm, with a maximum adjustment of +15,623/-15,625 ppm (+/- 1.56%). If the CMDR field is 01, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 4,096 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 3.82 ppm, with a maximum adjustment of +31,246/ -31,250 ppm (+/-3.12%). If the CMDR field is 10, OFFSETR cycles of the 64 Hz clock are gated (negative calibration) or replaced by 128 Hz pulses (positive calibration) within every 2,048 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 7.64 ppm, with a maximum adjustment of +62,492/-62,500 ppm (+/- 6.25%). If the CMDR field is 11, OFFSETR cycles of the 64 Hz clock are gated or replaced by the 128 Hz clock within every 1,024 second calibration period. In this mode, each step in OFFSETR modifies the clock frequency by 15.28 ppm, with a maximum adjustment of +124,984/-125,000 ppm (+/-12.5%). OFFSETR contains a two's complement value, so the possible steps are from -8,192 to +8,191.

The pulses which are added to or subtracted from the 64 Hz clock are spread evenly over each 8,192 second period using the Ambiq Micro patented Distributed Calibration algorithm. This ensures that in RC mode the maximum cycle-to-cycle jitter in any clock of a frequency 64 Hz or lower caused by calibration will be no more than one 64 Hz period. This maximum jitter applies to all clocks in the AB18X5 including the Calendar Counter, Countdown Timer and Watchdog Timer clocks and any clock driven onto a clock output pin.

The RC oscillator calibration value is determined by the following process:

1. Set the OFFSETR and CMDR register fields to 0 to ensure calibration is not occurring.
2. Select the RC oscillator by setting the OSEL bit to 1.
3. Configure a 128 Hz frequency square wave output on one of the output pins.
4. Precisely measure the exact frequency, Fmeas, at the output pin in Hz.
5. Compute the adjustment value required in ppm as ((128 – Fmeas)*1000000)/Fmeas = PAdj
6. Compute the adjustment value in steps as PAdj/(1000000/2^19) = PAdj/(1.90735) = Adj
7. If Adj < -65,536, the RC frequency is too high to be calibrated
8. Else if Adj < -32,768, set CMDR = 3, OFFSETR = Adj/8

9. Else if Adj < -16,384, set CMDR = 2, OFFSETR = Adj/4
10. Else if Adj < -8,192, set CMDR = 1, OFFSETR = Adj/2
11. Else if Adj < 8192, set CMDR = 0, OFFSETR = Adj
12. Else if Adj < 16,384, set CMDR = 1, OFFSETR = Adj/2
13. Else if Adj < 32,768, set CMDR = 2, OFFSETR = Adj/4
14. Else if Adj < 65,536, set CMDR = 3, OFFSETR = Adj/8
15. Else the RC frequency is too low to be calibrated

5.10 Autocalibration

The AB18X5 includes a very powerful, patented automatic calibration feature, referred to as Autocalibration, which allows the RC Oscillator to be automatically calibrated to the XT Oscillator. The XT Oscillator typically has much better stability than the RC Oscillator but the RC Oscillator requires significantly less power. Autocalibration enables many system configurations to achieve accuracy and stability similar to that of the XT Oscillator while drawing current similar to that of the RC Oscillator. Autocalibration functions in two primary modes: XT Autocalibration Mode and RC Autocalibration Mode. See *Abracon Application Note* – AB08X5/AB18X5 *Family Autocalibration* for more details.

5.10.1 Autocalibration Operation

The Autocalibration operation counts the number of calibrated XT clock cycles within a specific period as defined by the RC Oscillator and then loads new values into the Calibration RC Upper and RC Lower registers which will then adjust the RC Oscillator output to match the XT frequency.

5.10.2 XT Autocalibration Mode

In XT Autocalibration Mode, the OSEL register bit is 0 and the AB18X5 uses the XT Oscillator whenever the system power VCC is above the V_{CCSWF} voltage. The RC Oscillator is periodically automatically calibrated to the XT Oscillator. If the AOS bit is set, when VCC drops below the V_{CCSWF} threshold the system will switch to using VBAT, the clocks will begin using the RC Oscillator, Autocalibration will be disabled and the XT Oscillator will be disabled to reduce power requirements. Because the RC Oscillator has been continuously calibrated to the XT Oscillator, it will be very accurate when the switch occurs. When VCC is again above the threshold, the system will switch back to use the XT Oscillator and restart Autocalibration.

5.10.3 RC Autocalibration Mode

In RC Autocalibration Mode, the OSEL register bit is 1 and the AB18X5 uses the RC Oscillator at all times. However, periodically the XT Oscillator is turned on and the RC Oscillator is calibrated to the XT Oscillator. This allows the system to operate most of the time with the XT Oscillator off but allow continuous calibration of the RC Oscillator.

5.10.4 Autocalibration Frequency and Control

The Autocalibration function is controlled by the ACAL field in the Oscillator Control register as shown in Table 15. If ACAL is 00, no Autocalibration occurs. If ACAL is 10 or 11, Autocalibration occurs every 1024 or 512 seconds, which is referred to as the Autocalibration Period (ACXP). In RC Autocalibration Mode, an Autocalibration operation results in the XT Oscillator being enabled for roughly 50 seconds. The 512

second Autocalibration cycles have the XT Oscillator enabled approximately 10% of the time, while 1024 second Autocalibration cycles have the XT Oscillator enabled approximately 4% of the time.

Table 15: Autocalibration Modes

ACAL Value	Calibration Mode
00	No Autocalibration
01	RESERVED
10	Autocalibrate every 1024seconds (~17minutes)
11	Autocalibrate every 512seconds (~9 minutes)

If ACAL is 00 and is then written with a different value, an Autocalibration cycle is immediately executed. This allows Autocalibration to be completely controlled by software. As an example, software could choose to execute an Autocalibration cycle every 2 hours by keeping ACAL at 00, getting a two hour interrupt using the alarm function, generating an Autocalibration cycle by writing ACAL to 10 or 11, and then returning ACAL to 00.

5.10.5 Autocalibration Filter (AF) Pin

In order to produce the optimal accuracy for the Autocalibrated RC Oscillator, a filter pin AF is provided. A 47 pF capacitor should be connected between the AF pin and VSS. In order to enable the filter, the value 0xA0 must be written to the AFCTRL Register at address 0x26(see 0x26 – AFCTRL). The AF filter is disabled by writing 0x00 to the AFCTRL Register. No other values should be written to this register. The Configuration Key Register must be written with the value 0x9D immediately prior to writing the AFCTRL Register.

If the filter capacitor is not connected to the AF pin or is not enabled, the RC Oscillator frequency will typically be between 10 and 50 ppm slower than the XT Oscillator. If the capacitor is connected to the AF pin and enabled, the RC Oscillator frequency will be within the accuracy range specified in the Oscillator Parameters table of the XT Oscillator.

5.10.6 Autocalibration Fail

If the operating temperature of the AB18X5 exceeds the Autocalibration range specified in the Oscillator Parameters table or internal adjustment parameters are altered incorrectly, it is possible that the basic frequency of the RC Oscillator is so far away from the nominal 128 Hz value (off by more than 12%) that the RC Calibration circuitry does not have enough range to correctly calibrate the RC Oscillator. If this situation is detected during an Autocalibration operation, the ACF interrupt flag is set, an external interrupt is generated if the ACIE register bit is set and the Calibration RC registers are not updated.

If an Autocalibration failure is detected while running in RC Autocalibration mode, it is advisable to switch into XT Autocalibration mode to maintain the timing accuracy. This is done by first ensuring a crystal oscillator failure has not occurred (OF flag = 0) and then clearing the OSEL bit. The ACAL field should remain set to either 11 (512 second period) or 10 (1024 second period). After the switch occurs, the OMODE bit is cleared.

While continuing to operate in XT Autocalibration mode, the following steps can be used to determine when it is safe to return to RC Autocalibration mode.

1. Clear the ACF flag and ACIE register bit.
2. Setup the Countdown Timer or Alarm to interrupt after the next Autocalibration cycle completes or longer time period.
3. After the interrupt occurs, check the status of the ACF flag.

4. If the ACF flag is set, it is not safe to return to RC Autocalibration mode. Clear the ACF flag and repeat steps 2-4.
5. If the ACF flag is still cleared, it is safe to return to RC Autocalibration mode by setting the OSEL bit.

As mentioned in the RC oscillator section, switching between XT and RC oscillators is guaranteed to produce less than one second of error. However, this error needs to be considered and can be safely managed when implementing the steps above. For example, switching between oscillator modes every 48 hours will produce less than 6 ppm of error.

5.11 Oscillator Failure Detection

If the 32.786 kHz XT Oscillator generates clocks at less than 8 kHz for a period of more than 32 ms, the AB18X5 detects an Oscillator Failure. The Oscillator Failure function is controlled by several bits in the Oscillator Control Register (see 0x1C Oscillator Control) and the Oscillator Status Register (see 0x1D - Oscillator Status Register). The OF flag is set when an Oscillator Failure occurs, and is also set when the initially powers up. If the OFIE bit is set, the OF flag will generate an interrupt on IRQ.

If the FOS bit is set and the AB18X5 is currently using the XT Oscillator, it will automatically switch to the RC Oscillator on an Oscillator Failure. This guarantees that the system clock will not stop in any case. The OMODE bit indicates the currently selected oscillator, which will not match the oscillator requested by the OSEL bit if the XT Oscillator is not running.

The OF flag will be set when the AB18X5 powers up, and will also be set whenever the XT Oscillator is stopped. This can happen when the STOP bit is set or the OSEL bit is set to 1 to select the RC Oscillator. Since the XT Oscillator is stopped in RC Autocalibration mode (see RC Autocalibration Mode), OF will always be set in this mode. The OF flag should be cleared whenever the XT Oscillator is enabled prior to enabling the OF interrupt with OFIE.

5.12 Interrupts

The AB18X5 may generate a variety of interrupts which are ORed into the IRQ signal. This may be driven onto either the FOUT/nIRQ pin or the nIRQ2 pin depending on the configuration of the OUT1S and OUT2S fields (see 0x11 - Control2).

5.12.1 Interrupt Summary

The possible interrupts are summarized in Table 16. All enabled interrupts are ORed into the IRQ signal when their respective flags are set. Note that most interrupt outputs use the inverse of the interrupt (i.e. nIRQ). The fields are:

- Interrupt - the name of the specific interrupt.
- Function - the functional area which generates the interrupt.
- Enable - the register bit which enables the interrupt. Note that for the Watchdog interrupt, WDS is the steering bit, so that the flag generates an interrupt if WDS is 0 and a reset if WDS is 1. In either case, the BMB field must be non-zero to generate the interrupt or reset.
- Pulse/Level - some interrupts may be configured to generate a pulse based on the register bits in this column. "Level Only" implies that only a level may be generated, and the interrupt will only go away when the flag is reset by software.

- Flag - the register bit which indicates that the function has occurred. Note that the flag being set will only generate an interrupt signal on an external pin if the corresponding interrupt enable bit is also set.

Table 16: Interrupt Summary

Interrupt	Function	Enable	Pulse/Level	Flag
AIRQ	Alarm Match	AIE	IM	ALM
TIRQ	Countdown Timer	TIM	TM	TIM
WIRQ	Watchdog	!WDS	Level Only	WDT
BLIRQ	Battery Low	BLIE	Level Only	BL
X1IRQ	External 1	EX1E	Level Only	EX1
X2IRQ	External 2	EX2E	Level Only	EX2
OFIRQ	Oscillator Fail	OFIE	Level Only	OF
ACIRQ	Autocal Fail	ACIE	Level Only	ACF

5.12.2 Alarm Interrupt AIRQ

The AB18X5 may be configured to generate the AIRQ interrupt when the values in the Time and Date Registers match the values in the Alarm Registers. Which register comparisons are required to generate AIRQ is controlled by the RPT field as described in the Repeat Function table, allowing software to specify the interrupt interval. When an Alarm Interrupt is generated, the ALM flag is set and an external interrupt is generated based on the AIE bit and the pin configuration settings. The IM field controls the period of the external interrupt, including both level and pulse configurations.

5.12.3 Countdown Timer Interrupt TIRQ

The AB18X5 may be configured to generate the TIRQ interrupt when the Countdown Timer is enabled by the TE bit and reaches the value of zero, which will set the TIM flag. The TM, TRPT and TFS fields control the interrupt timing (see 0x18 - Countdown Timer Control), and the TIE bit and the pin configuration settings control external interrupt generation. The Timer interrupt is always driven onto the nTIRQ pin if it is available, and may also be driven onto a clock output pin by a configuration of the SQFS field (see 0x13 - SQW).

5.12.4 Watchdog Timer Interrupt WIRQ

The AB18X5 may be configured to generate the WIRQ interrupt when the Watchdog Timer reaches its timeout value. This sets the WDT flag and is described in Watchdog Timer.

5.12.5 Battery Low Interrupt BLIRQ

The AB18X5 may be configured to generate the BLIRQ when the voltage on the VBAT pin crosses one of the thresholds set by the BREF field. The polarity of the detected crossing is set by the BPOL bit.

5.12.6 External Interrupts X1IRQ and X2IRQ

The AB18X5 may be configured to generate the X1IRQ and X2IRQ interrupts when the EXTI (X1IRQ) or WDI (X2IRQ) inputs toggle. The register bits EX1P and EX2P control whether the rising or falling transitions generate the respective interrupt. Changing EX1P or EX2P may cause an immediate interrupt, so the corresponding interrupt flag should be cleared after changing these bits.

The values of the EXTI and WDI pins may be directly read in the EXIN and WDIN register bits (see 0x3F - Extension RAM Address). By connecting an input such as a pushbutton to both EXTI and WDI, software can debounce the switch input using software configurable delays.

5.12.7 Oscillator Fail Interrupt OFIRQ

The AB18X5 may be configured to generate the OFIRQ interrupt if the XT oscillator fails (see Oscillator Failure Detection).

5.12.8 Autocalibration Fail Interrupt ACIRQ

The AB18X5 may be configured to generate the ACIRQ interrupt if an Autocalibration operation fails (see Autocalibration Fail).

5.12.9 Servicing Interrupts

When an interrupt is detected, software must clear the interrupt flag in order to prepare for a subsequent interrupt. If only a single interrupt is enabled, software may simply write a zero to the corresponding interrupt flag to clear the interrupt. However, because all of the flags in the Status register are written at once, it is possible to clear an interrupt which has not been detected yet if multiple interrupts are enabled. The ARST register bit is provided to ensure that interrupts are not lost in this case. If ARST is a 1, a read of the Status register will produce the current state of all the interrupt flags and then clear them. An interrupt occurring at any time relative to this read is guaranteed to either produce a 1 on the Status read, or to set the corresponding flag after the clear caused by the Status read. After servicing all interrupts which produced 1s in the read, software should read the Status register again until it returns all zeros in the flags, and service any interrupts with flags of 1.

Note that the OF and ACF interrupts are not handled with this process because they are in the Oscillator Status register, but error interrupts are very rare and typically do not create any problems if the interrupts are cleared by writing the flag directly.

5.13 Power Control and Switching

The main power supply to the AB18X5 is the VCC pin, which operates over the range specified by the V_{CCIO} parameter if there are I/O interface operations required, and the range specified by the V_{CC} parameter if only timekeeping operations are required. Some versions also include a backup supply which is provided on the VBAT pin and must be in the range specified by the V_{BAT} parameter in order to supply battery power if V_{CC} is below V_{CCSWF}. Refer to the Power Supply and Switchover Parameters table for the specifications related to the power supplies and switchover. There are several functions which are directly related to the VBAT input. If a single power supply is used it must be connected to the VCC pin.

Figure 31 illustrates the various power states and the transitions between them. There are three power states:

1. POR – the power on reset state. If the AB18X5 is in this state, all registers including the Counter Registers are initialized to their reset values.
2. VCC Power – the AB18X5 is powered from the VCC supply.
3. VBAT Power – the AB18X5 is powered from the VBAT supply.

Initially, VCC is below the V_{CCST} voltage, VBAT is below the V_{BATSW} voltage and the AB18X5 is in the POR state. VCC rising above the V_{CCST} voltage causes the AB18X5 to enter the VCC Power state. If VBAT remains below V_{BATSW}, VCC falling below the V_{CCRST} voltage returns the AB18X5 to the POR state.

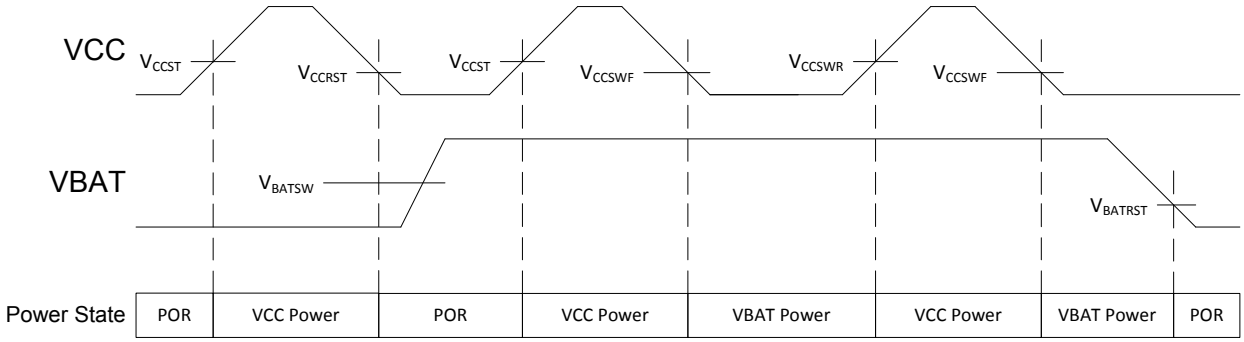


Figure 31. Power States

If VBAT rises above V_{BATSW} in the POR state, the AB18X5 remains in the POR state. This allows the AB18X5 to be built into a module with a battery included, and minimal current will be drawn from the battery until VCC is applied to the module the first time.

If the AB18X5 is in the VCC Power state and VBAT rises above V_{BATSW}, the AB18X5 remains in the VCC Power state but automatic switchover becomes available. VBAT falling below V_{BATSW} has no effect on the power state as long as VCC remains above V_{CCSWF}. If VCC falls below the V_{CCSWF} voltage while VBAT is above V_{BATSW} the AB18X5 switches to the VBAT Power state. VCC rising above V_{CCSWR} returns the AB18X5 to the VCC Power state. There is hysteresis in the rising and falling VCC thresholds to ensure that the AB18X5 does not switch back and forth between the supplies if VCC is near the thresholds. V_{CCSWF} and V_{CCSWR} are independent of the VBAT voltage and allow the AB18X5 to minimize the current drawn from the VBAT supply by switching to VBAT only at the point where VCC is no longer able to power the device.

If the AB18X5 is in the VBAT Power state and VBAT falls below V_{BATRST}, the AB18X5 will return to the POR state.

Whenever the AB18X5 enters the VBAT Power state, the BAT flag in the Status Register (see 0x0F - Status (Read Only)) is set and may be polled by software. If the XT oscillator is selected and the AOS bit (see 0x1C - Oscillator Control) is set, the AB18X5 will automatically switch to the RC oscillator in the VBAT Power state in order to conserve battery power. If the IOBM bit (see 0x27 – Batmode IO Register) is clear, the I^2C or SPI interface is disabled in the VBAT Power state in order to prevent erroneous accesses to the AB18X5 if the bus master loses power.

5.13.1 Battery Low Flag and Interrupt

If the VBAT voltage drops below the Falling Threshold selected by the BREF field (see 0x21 - BREF Control), the BL flag in the Status Register (see 0x0F - Status (Read Only)) is set. If the BLIE interrupt enable bit (see 0x12 - Interrupt Mask) is set, the IRQ interrupt is generated. This allows software to determine if a backup battery has been drained. Note that the BPOL bit must be set to 0. The algorithm in the Analog Comparator section should be used when configuring the BREF value.

If the VBAT voltage is above the rising voltage which corresponds to the current BREF setting, BBOD will be set. At that point the VBAT voltage must fall below the falling voltage in order to clear the BBOD bit, set

the BAT flag and generate a falling edge BL interrupt. If BBOD is clear, the VBAT voltage must rise above the rising voltage in order to clear the BBOD bit and generate a rising edge BL interrupt.

5.13.2 Analog Comparator

If a backup battery is not required, the VBAT pin may be used as an analog comparator input. The voltage comparison level is set by the BREF field. If the BPOL bit is 0, the BL flag will be set when the VBAT voltage crosses from above the BREF Falling Threshold to below it. If the BPOL bit is 1, the BL flag will be set when the VBAT voltage crosses from below the BREF Rising Threshold to above it. The BBOD bit in the Analog Status Register (see 0x2F – Analog Status Register (Read Only)) may be read to determine if the VBAT voltage is currently above the BREF threshold (BBOD = 1) or below the threshold (BBOD = 0).

There is a reasonably large delay (on the order of seconds) between changing the BREF field and a valid value of the BBOD bit. Therefore, the algorithm for using the Analog Comparator should comprise the following steps:

1. Set the BREF and BPOL fields to the desired values.
2. Wait longer than the maximum t_{BREF} time.
3. Clear the BL flag, which may have been erroneously set as BBOD settles.
4. Check the BBOD bit to ensure that the VBAT pin is at a level for which an interrupt can occur. If a falling interrupt is desired (BPOL = 0), BBOD should be 1. If a rising interrupt is desired (BPOL = 1), BBOD should be 0.

If the comparison voltage on the VBAT pin can remain when VCC goes to 0, it is recommended that a Software Reset be generated to the AB18X5 after power up.

5.13.3 Pin Control and Leakage Management

Like most ICs, the AB18X5 may draw unnecessary leakage current if an input pin floats to a value near the threshold or an output pin is pulled to a power supply. Because external devices may be powered from VCC, extra care must be taken to ensure that any input or output pins are handled correctly to avoid extraneous leakage when VCC goes away and the AB18X5 is powered from VBAT. The Output Control register (see 0x30 – Output Control Register), the Batmode IO register (see 0x27 – Batmode IO Register) and the Extension RAM Address register (see 0x3F - Extension RAM Address) include bits to manage this leakage, which should be used as follows:

1. EXBM should be cleared if the EXTI pin is connected to a device which is powered down when the AB18X5 is in the VBAT Power state.
2. WDBM should be cleared if the WDI pin is connected to a device which is powered down when the AB18X5 is in the VBAT Power state.
3. O4BM should be cleared if the CLKOUT/nIRQ3 pin is connected to a device which is powered down when the AB18X5 is in the VBAT Power state.
4. IOBM should be cleared if the I^2C or SPI bus master is powered down when the AB18X5 is in the VBAT Power state.

5.13.4 Power Up Timing

When the voltage levels on both the VCC and VBAT signals drop below V_{CCRST}, the AB18X5 will enter the POR state. Once VCC rises above V_{CCST}, the AB18X5 will enter the VCC Power state. I/O accesses via the I^2C or SPI interface will be disabled for a period of $t_{VH:FOUT}$. The FOUT/nIRQ pin will be low at power

up, and will go high when $t_{VH:FOUT}$ expires. Software should poll the FOUT/nIRQ value to determine when the AB18X5 may be accessed. Figure 32 illustrates the timing of a power down/up operation.

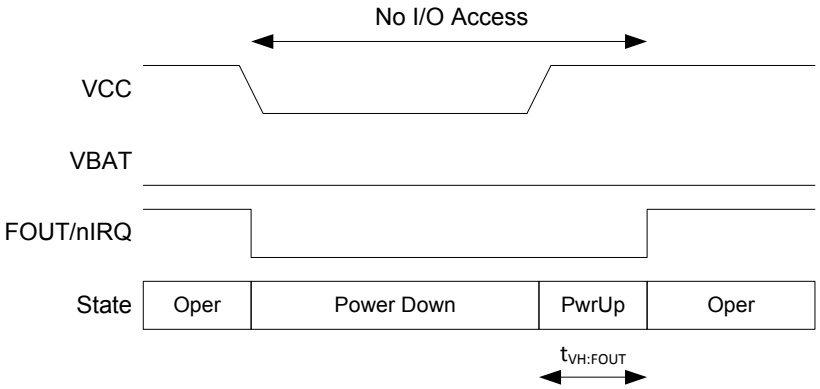


Figure 32. Power Up Timing

5.14 Reset Summary

The AB18X5 controls the nRST output in a variety of ways, as shown in Table 17. The assertion of nRST is a low signal if the RSP bit is 0, and the assertion is high if RSP is 1. RSP always powers up as a zero so that on power nRST is always asserted low.

Table 17: Reset Summary

Function	Enable
Power Up	Always Enabled
nEXTR Pin	RS1E
Watchdog	WDS
Sleep	SLRES

5.14.1 Power Up Reset

When the AB18X5 powers up (see Power Up Timing) FOUT/nIRQ and nRST will be asserted low until I/O accesses are enabled. At that point FOUT/nIRQ will go high, and nRST will continue to be asserted for the

delay $t_{VH:NRST}$, and will then be deasserted. Figure 33 illustrates the reset timing on Power Up. Software should sample the FOUT/nIRQ signal prior to accessing the AB18X5.

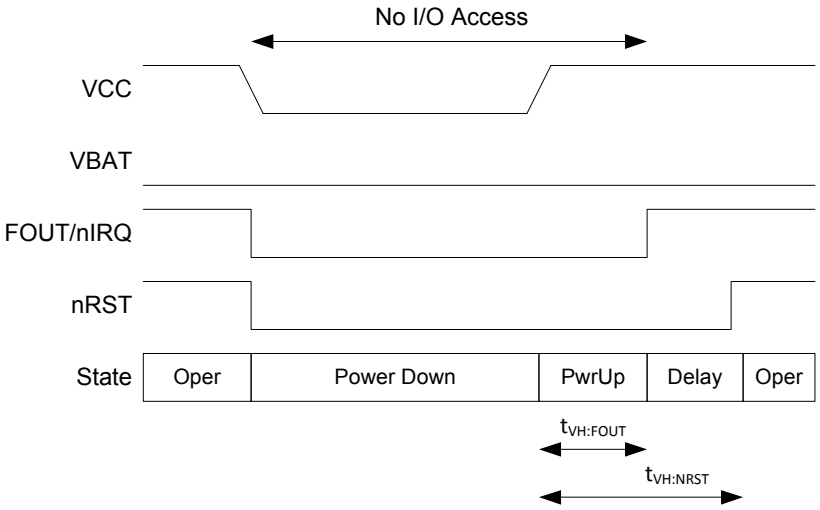


Figure 33. Power Up Reset Timing

5.14.2 nEXTR

If the RS1E bit is set, nRST will be asserted whenever the nEXTR input pin is low. If no other sources are asserting nRST, the nRST pin will be deasserted immediately upon nEXTR going high with no delay. The RS1E bit is initialized to 1 so nEXTR is enabled. For reset purposes, nEXTR can be connected to the reset output of other devices to provide a reset ORing function.

5.14.3 Watchdog Timer

If the WDS bit is 1, expiration of the Watchdog Timer (see Watchdog Timer) will cause nRST to be asserted for approximately 60 ms.

5.14.4 Sleep

If the SLRES bit is set, nRST will be asserted whenever the AB18X5 is in Sleep Mode. Once a trigger is received and the AB18X5 exits Sleep Mode, nRST will continue to be asserted for the $t_{VH:NRST}$ delay. Figure 34 illustrates the timing of this operation.

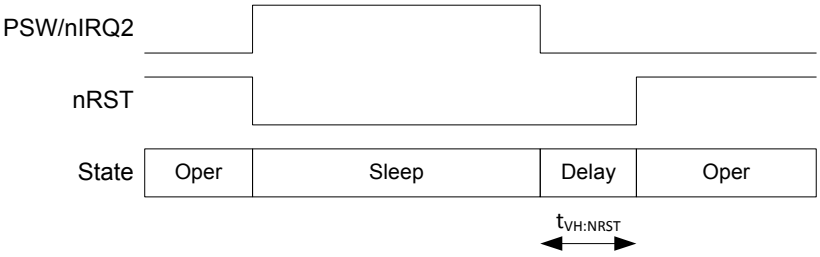


Figure 34. Sleep Reset Timing

5.15 Software Reset

Software may reset the AB18X5 by writing the special value of 0x3C to the Configuration Key register at offset 0x1F. This will provide the equivalent of a power on reset by initializing all of the AB18X5 registers. A software reset will not cause the nRST signal the be asserted.

5.16 Sleep Control

The AB18X5 includes a sophisticated Sleep Control system that allows the AB18X5 to manage power for other chips in a system. The Sleep Control system provides two outputs which may be used for system power control:

1. A reset (nRST) may be generated to put any host controller into a minimum power mode and to control sequencing during power up and power down operations.
2. A power switch signal may be generated (PWR), which allows theAB18X5 to completely power down other chips in a system by allowing the PSW/nIRQ2 pin to float. The OUT2S field must be set to a value of 6 to select the SLEEP output. When using the PWR output, PSW/nIRQ2 is configured as an open drain pin with approximately 1 Ω resistance. This allows the AB18X5 to directly switch power with no external components for small systems, or to control a single external transistor for higher current switching. The low resistance power switch is enabled by setting the PWR2 bit. If the I^2C or SPI master (i.e., the host controller) is powered down by the power switch, the PWGT bit should be set to ensure that a floating bus does not corrupt the AB18X5.
3. If OUT2S is 6 but the PWR2 bit is not set, PSW/nIRQ2 will be configured as a high true Sleep output which may be used as an interrupt.

The Sleep state machine in Figure 35 receives several inputs which it uses to determine the current Sleep State:

1. POR – the indicator that power is valid, i.e. the AB18X5 is in either the VCC Power state or the VBAT Power state.
2. SLP - the Sleep Request signal which is generated by a software access to the Sleep Register
3. TRIG - the OR of the enabled interrupt request from the Alarm comparison in the RTC, the interrupt signal from the Countdown Timer in the RTC, the interrupt signal from the Watchdog Timer in the RTC, the External Interrupt 1 or 2 pins, the Battery Low detection interrupt, the Autocalibration Fail interrupt or the Oscillator Fail interrupt.
4. TIM - the timeout signal from the SL Timeout counter, indicating that it has decremented to 0.

RUN is the normal operating state of the AB18X5. PWR and nRST are not asserted, SLP is 0, and SLST holds the state of the previous Sleep. SLST should be cleared by software before entering the SWAIT state.

5.16.1 SWAIT

Software can put the chip to sleep by setting the SLP bit, as long as a valid interrupt is enabled (see SLP Protection) indicated by VAL being asserted. If SLTO is between 1 and 7, the SM moves to the SWAIT state and waits for between SLTO and (SLTO+1) ~8 ms periods. This allows software to perform additional cleanup after setting SLP before the MCU is shut down. Operation is the same in SWAIT as it is in RUN, and if an enabled operational interrupt occurs (TRIG) the SM returns to the RUN state and clears the SLP bit. PWR and nRST are not asserted, SLP is 1, and SLST is 0.

If SLTO is set to 0, the SM moves immediately to the SLEEP state. If the MCU is configured to be powered down in Sleep Mode, the I/O operation to write the Sleep Register must be the last instruction executed by the MCU.

5.16.2 SLEEP

Once the programmed number of periods has elapsed in the SWAIT state, the TIM signal is asserted and the machine moves to the SLEEP state, putting the AB18X5 into Sleep Mode. In this case the PWR signal is removed, and nRST is asserted if SLRES is set. Once an enabled operational interrupt occurs (TRIG), the SM returns to the RUN state, reenables power and removes reset as appropriate. The SLST register bit is set when the SLEEP state is entered, allowing software to determine if a SLEEP has occurred.

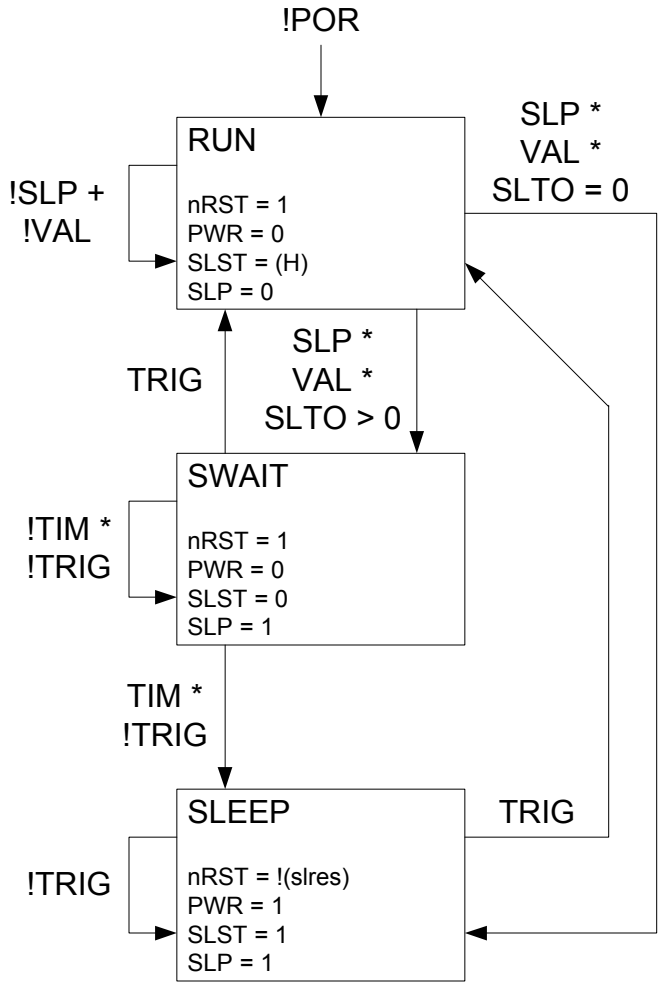


Figure 35. Sleep State Machine

5.16.3 SLP Protection

1. Since going into Sleep Mode may prevent an MCU from accessing the AB18X5, it is critical to ensure that the AB18X5 can receive a TRIG signal. To guarantee this, the SLP signal cannot be set unless the STOP bit is 0 and at least one of the following conditions exists:The AIE bit is 1, enabling an Alarm interrupt.
2. The TIE and the TE bits are 1, enabling a Countdown Timer interrupt.
3. The EX1E or EX2E bits are a 1, enabling an External interrupt.
4. The BMB field is not zero and the WDS bit is zero, enabling a Watchdog Interrupt.

In addition, SLP cannot be set if there is an interrupt pending. Software should read the SLP bit after attempting to set it. If SLP is not asserted, the attempt to set SLP was unsuccessful either because a

correct trigger was not enabled or because an interrupt was already pending. Once SLP is set, software should continue to poll it until the Sleep actually occurs, in order to handle the case where a trigger occurs before the AB18X5AB18X5 enters Sleep Mode.

5.16.4 OUT2S, OUTB and LKO2

If the OUT2S field is set to the initial value of 7, the PSW/nIRQ2 pin will be driven with the value of the OUTB bit which is initially zero. If this pin is used as the power switch, setting OUTB will remove power from the system and may prevent further access to the AB18X5. In order to ensure that this does not happen inadvertently, the LKO2 bit must be cleared in order to change the OUTB bit to a 1. Note that in this power switch environment the OUT2S register field must not be written to any value other than 6 or 7, even if the PSW/nIRQ2 pin would remain at zero, because it is possible that a short high pulse could be generated on the PSW/nIRQ2 pin which could create a power down.

5.16.5 Pin Control and Leakage Management

Like most ICs, the AB18X5 may draw unnecessary leakage current if an input pin floats to a value near the threshold or an output pin is pulled to a power supply. Because Sleep Mode can power down external devices connected to the AB18X5, extra care must be taken to ensure that any input or output pins are handled correctly to avoid extraneous leakage. The Output Control register includes bits to manage this leakage, which should be used as follows:

1. EXDS should be set if the EXTI pin is connected to a device which is powered down in Sleep Mode.
2. WDDS should be set if the WDI pin is connected to a device which is powered down in Sleep Mode.
3. O1EN should be cleared if the FOUT/nIRQ pin is connected to a device which is powered down in Sleep Mode.
4. O3EN should be cleared if the nTIRQ pin is connected to a device which is powered down in Sleep Mode (I^2C devices only).
5. O4EN should be cleared if the CLKOUT/nIRQ3 pin is connected to a device which is powered down in Sleep Mode.
6. RSEN should be cleared if the nRST pin is connected to a device which is powered down in Sleep Mode.

5.17 System Power Control Applications

The AB18X5 enables a variety of system implementations in which the AB18X5 can control power usage by other elements in the system. This is typically used when the entire system is powered from a battery and minimizing total power usage is critical. See *Abracon Application Note AN0001* – AB18X5 *Family System Power Management* for more details.

5.17.1 VSS Power Switched

Figure 36 illustrates the recommended implementation, in which the internal power switch of the AB18X5 is used to completely turn off the MCU and/or other system elements. In this case the PSW/nIRQ2 output is configured to generate the SLEEP function, and the SLRES bit is set to 0. Under normal circumstances, the PSW/nIRQ2 pin is pulled to VSS with approximately 1 Ω of resistance, so that the MCU receives full power. The MCU initiates a SLP operation, and when the AB18X5 enters the SLEEP state the PSW/nIRQ2 pin is opened and power is completely removed from the MCU. This results in significant additional power savings relative to the other alternatives.

The AB18X5 normally powers up selecting the OUTB register bit to drive the PSW/nIRQ2 pin, and the OUTB bit is zero. This ensures that the power switch is enabled at power up. If the power switch function is

used, software should only change the PSW/nIRQ2 selection between OUTB (0b111) and SLEEP (0b110) to ensure no glitches occur in the power switching function.

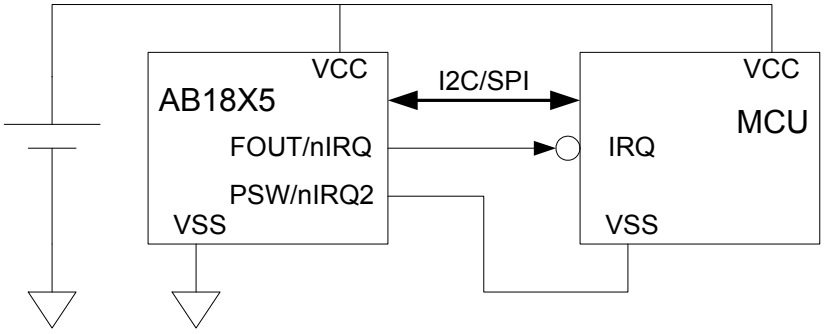


Figure 36. Switched VSS Power Control

5.17.2 VCC Power Switched

Figure 37 illustrates the application in which an external transistor switch T is used to turn off power to the MCU. The SLP function operates identically to the VSS switched case above, but this implementation allows switching higher current and maintains a common ground. R can be on the order of megohms, so that negligible current is drawn when the circuit is active and PSW/nIRQ2 is low.

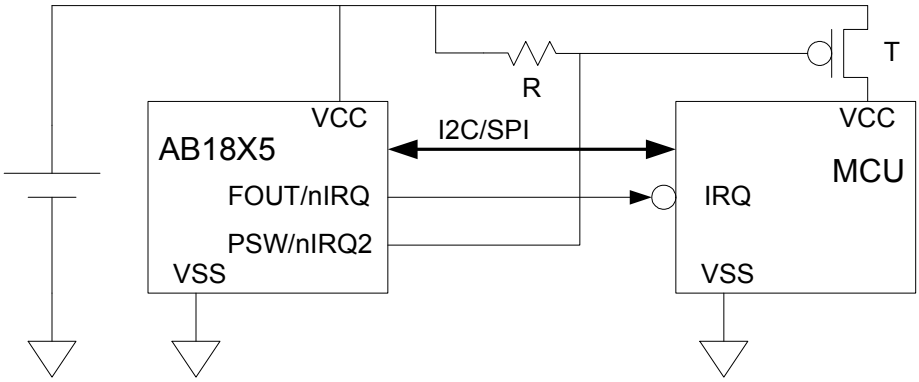


Figure 37. Switched VCC Power Control

5.17.3 Reset Driven

Figure 38 illustrates the application in which the AB18X5 communicates with the system MCU using the reset function. In this case the MCU sets the SLRES bit so that when the AB18X5 enters the SLEEP state, it brings nRST low to reset the MCU, and initiates a SLP operation. When the trigger occurs, the AB18X5 releases the MCU from reset, and may also generate an interrupt which the MCU can query to determine

how reset was exited. Since some MCUs use much less power when reset, this implementation can save system power.

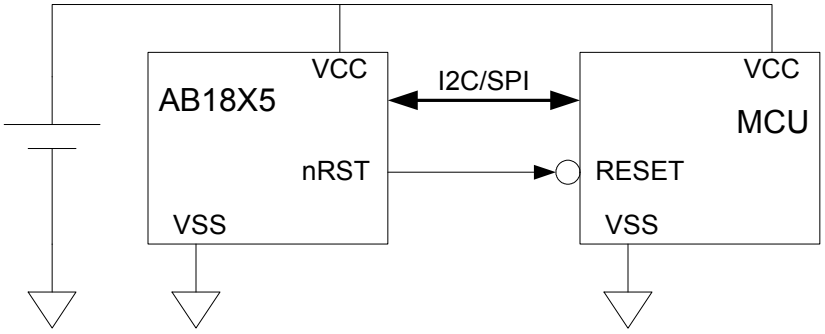


Figure 38. Reset Driven Power Control

One potential issue with this approach is that many MCUs include internal pull-up resistors on their reset inputs, and the current drawn through that resistor when the reset input is held low is generally much higher than the MCU would draw in its inactive state. Any pull-up resistor should be disabled and the nRST output of the AB18X5 should be configured as a push-pull output.

5.17.4 Interrupt Driven

Figure 39 illustrates the simplest application, in which the AB18X5 communicates with the system MCU using an interrupt. The MCU can go into standby mode, reducing power somewhat, until the AB18X5 generates an interrupt based on an alarm or a timer function.

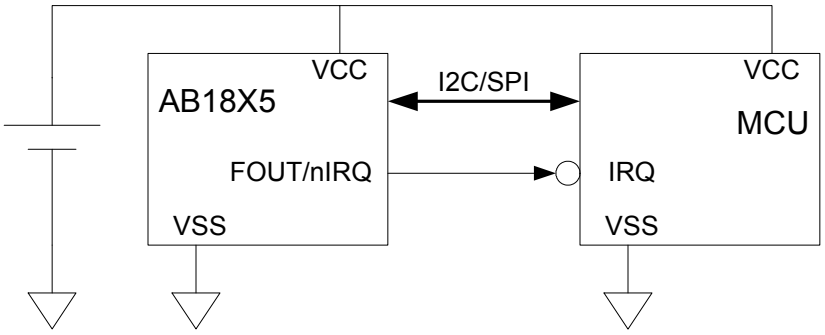


Figure 39. Interrupt Driven Power Control

5.18 Trickle Charger

The devices supporting the VBAT pin include a trickle charging circuit which allows a battery or supercapacitor connected to the VBAT pin to be charged from the power supply connected to the VCC pin. The circuit of the Trickle Charger is shown in Figure 40. The Trickle Charger configuration is controlled by the Trickle register (see 0x20 - Trickle). The Trickle Charger is enabled if a) the TCS field is 1010, b) the DIODE field is 01 or 10 and c) the ROUT field is not 00. A diode, with a typical voltage drop of 0.6V, is inserted in the charging path if DIODE is 10. A Schottky diode, with a typical voltage drop of 0.3V, is

inserted in the charging path if DIODE is 01. The series current limiting resistor is selected by the ROUT field as shown in the figure.

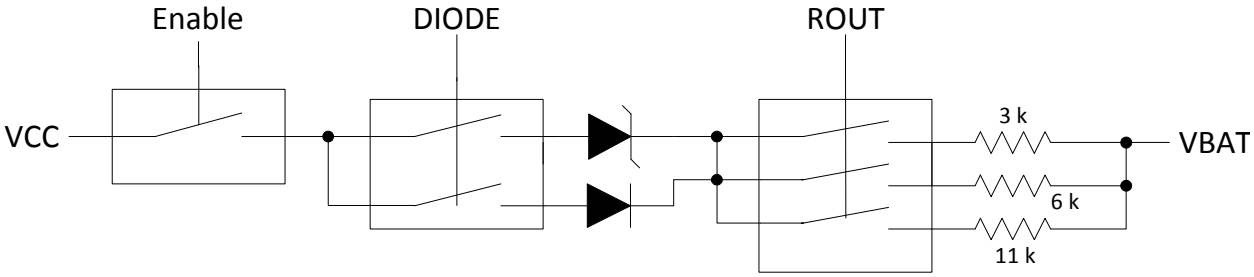


Figure 40. Trickle Charger

6. Registers

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. Table 18 and Table 19 summarize the function of each register. In Table 18, the GPx bits (where x is between 0 and 27) are 28 register bits which may be used as general purpose storage. These bits are described in the sections below. All of the GPx bits are cleared when the AB18X5 powers up and they can therefore be used to allow software to determine if a true Power On Reset has occurred or hold other initialization data.

6.1 Register Definitions and Memory Map

Table 18: Register Definitions (0x00 to 0x0F)

Offset	Register	7	6	5	4	3	2	1	0
0x00	Hundredths	Seconds - Tenths				Seconds - Hundredths			
0x01	Seconds	GP0	Seconds - Tens			Seconds - Ones			
0x02	Minutes	GP1	Minutes - Tens			Minutes - Ones			
0x03	Hours (24 hour)	GP3	GP2	Hours - Tens		Hours - Ones			
0x03	Hours (12 hour)	GP3	GP2	AM/PM	Hours - Tens	Hours - Ones			
0x04	Date	GP5	GP4	Date - Tens		Date - Ones			
0x05	Months	GP8	GP7	GP6	Months - Tens	Months - Ones			
0x06	Years	Years - Tens				Years - Ones			
0x07	Weekdays	GP13	GP12	GP11	GP10	GP9	Weekdays		
0x08	Hundredths Alarm	Hundredths Alarm - Tenths				Hundredths Alarm - Hundredths			
0x09	Seconds Alarm	GP14	Seconds Alarm - Tens			Seconds Alarm - Ones			
0x0A	Minutes Alarm	GP15	Minutes Alarm - Tens			Minutes Alarm - Ones			
0x0B	Hours Alarm (24 hour)	GP17	GP16	Hours Alarm - Tens		Hours Alarm - Ones			
0x0B	Hours Alarm (12 hour)	GP17	GP16	AM/PM	Hours Alarm - Tens	Hours Alarm - Ones			
0x0C	Date Alarm	GP19	GP18	Date Alarm - Tens		Date Alarm - Ones			
0x0D	Months Alarm	GP22	GP21	GP20	Months Alarm - Tens	Months Alarm - Ones			
0x0E	Weekdays Alarm	GP27	GP26	GP25	GP24	GP23	Weekdays Alarm		
0x0F	Status	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1

Table 19: Register Definitions (0x10 to 0xFF)

Offset	Register	7	6	5	4	3	2	1	0
0x10	Control1	STOP	12/24	OUTB	OUT	RSP	ARST	PWR2	WRTC
0x11	Control2	-	-	RS1E	OUT2S			OUT1S	
0x12	IntMask	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E
0x13	SQW	SQWE	-	SQFS					
0x14	Cal_XT	CMDX	OFFSETX						
0x15	Cal_RC_Hi	CMDR	OFFSETR[13:8]						
0x16	Cal_RC_Low	OFFSETR[7:0]							
0x17	Sleep_Control	SLP	SLRES	EX2P	EX1P	SLST	SLTO		
0x18	Timer Control	TE	TM	TRPT	RPT			TFS	
0x19	Timer	Countdown Timer							
0x1A	Timer_Initial	Timer Initial Value							
0x1B	WDT	WDS	BMB					WRB	
0x1C	Osc. Control	OSEL	ACAL		AOS	FOS	PWGT	OFIE	ACIE
0x1D	Osc. Status	XTCAL		LKO2	OMODE	-	-	OF	ACF
0x1E	RESERVED	RESERVED							
0x1F	Configuration Key	Configuration Key							
0x20	Trickle	TCS				DIODE	ROUT		
0x21	BREF Control	BREF				-			
0x22	RESERVED	RESERVED							
0x23	RESERVED	RESERVED							
0x24	RESERVED	RESERVED							
0x25	RESERVED	RESERVED							
0x26	AFCTRL	AFCTRL							
0x27	BATMODE I/O	IOBM	RESERVED						
0x28	ID0 (Read only)	Part Number – MS Byte = 00011000 (0x18)							
0x29	ID1 (Read only)	Part Number – LS Byte (e.g. 00000101 for AB1805)							
0x2A	ID2 (Read only)	Revision – Major = 00010					Revision – Minor = 011		
0x2B	ID3 (Read only)	Lot[7:0]							
0x2C	ID4 (Read only)	Lot[9]	Unique ID[14:8]						
0x2D	ID5 (Read only)	Unique ID[7:0]							
0x2E	ID6 (Read only)	Lot[8]	Wafer					–	–
0x2F	ASTAT	BBOD	BMIN	-	-	-	-	VINIT	-
0x30	OCTRL	WDBM	EXBM	WDDS	EXDS	RSEN	O4EN	O3EN	O1EN
0x3F	Extension Address	O4BM	BPOL	WDIN	EXIN	-	XADA	XADS	
0x40–7F	RAM	Normal RAM Data							
0x80–FF	RAM	Alternate RAM Data (I^2C Mode Only)							

6.2 Time and Date Registers

6.2.1 0x00 - Hundredths

This register holds the count of hundredths of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 99. Note that in order to divide from 32.786 kHz, the hundredths register will not be fully accurate at all times but will be correct every 500 ms. Maximum jitter of this register will be less than 1 ms. The Hundredths Counter is not valid if the 128 Hz RC Oscillator is selected.

Table 20: Hundredths Register

Bit	7	6	5	4	3	2	1	0
Name	Seconds - Tenths				Seconds - Hundredths			
Reset	1	0	0	1	1	0	0	1

Table 21: Hundredths Register Bits

Bit	Name	Function
7:4	Seconds - Tenths	Holds the tenths place in the hundredths counter.
3:0	Seconds - Hundredths	Holds the hundredths place in the hundredths counter.

6.2.2 0x01 - Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Table 22: Seconds Register

Bit	7	6	5	4	3	2	1	0
Name	GP0	Seconds - Tens			Seconds - Ones			
Reset	0	0	0	0	0	0	0	0

Table 23: Seconds Register Bits

Bit	Name	Function
7	GP0	Register bit for general purpose use.
6:4	Seconds - Tens	Holds the tens place in the seconds counter.
3:0	Seconds - Ones	Holds the ones place in the seconds counter.

6.2.3 0x02 - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Table 24: Minutes Register

Bit	7	6	5	4	3	2	1	0
Name	GP1	Minutes - Tens			Minutes - Ones			
Reset	0	0	0	0	0	0	0	0

Table 25: Minutes Register Bits

Bit	Name	Function
7	GP1	Register bit for general purpose use.
6:4	Minutes - Tens	Holds the tens place in the minutes counter.
3:0	Minutes - Ones	Holds the ones place in the minutes counter.

6.2.4 0x03 - Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23 if the 12/24 bit (see 0x10 - Control1) is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will range from 1 to 12.

Table 26: Hours Register (12 Hour Mode)

Bit	7	6	5	4	3	2	1	0
Name	GP3	GP2	AM/PM	Hours - Tens	Hours - Ones			
Reset	0	0	0	0	0	0	0	0

Table 27: Hours Register Bits (12 Hour Mode)

Bit	Name	Function
7	GP3	Register bit for general purpose use.
6	GP2	Register bit for general purpose use.
5	AM/PM	0 = AM hours. 1 = PM hours.
4	Hours - Tens	Holds the tens place in the hours counter.
3:0	Hours - Ones	Holds the ones place in the hours counter.

Table 28: Hours Register (24 Hour Mode)

Bit	7	6	5	4	3	2	1	0
Name	GP3	GP2	Hours - Tens		Hours - Ones			
Reset	0	0	0	0	0	0	0	0

Table 29: Hours Register Bits (24 Hour Mode)

Bit	Name	Function
7	GP3	Register bit for general purpose use.
6	GP2	Register bit for general purpose use.
5:4	Hours - Tens	Holds the tens place in the hours counter.
3:0	Hours - Ones	Holds the ones place in the hours counter.

6.2.5 0x04 - Date

This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

Table 30: Date Register

Bit	7	6	5	4	3	2	1	0
Name	GP5	GP4	Date - Tens		Date - Ones			
Reset	0	0	0	0	0	0	0	1

Table 31: Date Register Bits

Bit	Name	Function
7	GP5	Register bit for general purpose use.
6	GP4	Register bit for general purpose use.
5:4	Date - Tens	Holds the tens place in the date counter.
3:0	Date - Ones	Holds the ones place in the date counter.

6.2.6 0x05 - Months

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

Table 32: Months Register

Bit	7	6	5	4	3	2	1	0
Name	GP8	GP7	GP6	Months - Tens	Months - Ones			
Reset	0	0	0	0	0	0	0	1

Table 33: Months Register Bits

Bit	Name	Function
7	GP8	Register bit for general purpose use.
6	GP7	Register bit for general purpose use.
5	GP6	Register bit for general purpose use.
4	Months - Tens	Holds the tens place in the months counter.
3:0	Months - Ones	Holds the ones place in the months counter.

6.2.7 0x06 - Years

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

Table 34: Years Register

Bit	7	6	5	4	3	2	1	0
Name	Years - Tens				Years - Ones			
Reset	0	0	0	0	0	0	0	0

Table 35: Years Register Bits

Bit	Name	Function
7:4	Years - Tens	Holds the tens place in the years counter.
3:0	Years - Ones	Holds the ones place in the years counter.

6.2.8 0x07 - Weekday

This register holds the current day of the week. Values will range from 0 to 6.

Table 36: Weekdays Register

Bit	7	6	5	4	3	2	1	0
Name	GP13	GP12	GP11	GP10	GP9	Weekdays		
Reset	0	0	0	0	0	0	0	0

Table 37: Weekdays Register Bits

Bit	Name	Function
7	GP13	Register bit for general purpose use.
6	GP12	Register bit for general purpose use.
5	GP11	Register bit for general purpose use.
4	GP10	Register bit for general purpose use.
3	GP9	Register bit for general purpose use.
2:0	Weekdays	Holds the weekday counter value.

6.3 Alarm Registers

6.3.1 0x08 - Hundredths Alarm

This register holds the alarm value for hundredths of seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

Table 38: Hundredths Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	Seconds Alarm - Tenths				Seconds Alarm - Hundredths			
Reset	0	0	0	0	0	0	0	0

Table 39: Hundredths Alarm Register Bits

Bit	Name	Function
7:4	Seconds Alarm - Tenths	Holds the tenths place for the hundredths alarm.
3:0	Seconds Alarm - Hundredths	Holds the hundredths place for the hundredths alarm.

6.3.2 0x09 - Seconds Alarm

This register holds the alarm value for seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Table 40: Seconds Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	GP14	Seconds Alarm - Tens			Seconds Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 41: Seconds Alarm Register Bits

Bit	Name	Function
7	GP14	Register bit for general purpose use.
6:4	Seconds Alarm - Tens	Holds the tens place for the seconds alarm.
3:0	Seconds Alarm - Ones	Holds the ones place for the seconds alarm.

6.3.3 0x0A - Minutes Alarm

This register holds the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Table 42: Minutes Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	GP15	Minutes Alarm - Tens			Minutes Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 43: Minutes Alarm Register Bits

Bit	Name	Function
7	GP15	Register bit for general purpose use.
6:4	Minute Alarm - Tens	Holds the tens place for the minutes alarm.
3:0	Minutes Alarm - Ones	Holds the ones place for the minutes alarm.

6.3.4 0x0B - Hours Alarm

This register holds the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23 if the 12/24 bit (see 0x10 - Control1) is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will be from 1 to 12.

Table 44: Hours Alarm Register (12 Hour Mode)

Bit	7	6	5	4	3	2	1	0
Name	GP17	GP16	AM/PM	Hours Alarm - Tens	Hours Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 45: Hours Alarm Register Bits (12 Hour Mode)

Bit	Name	Function
7	GP17	Register bit for general purpose use.
6	GP16	Register bit for general purpose use.
5	AM/PM	0 = AM hours. 1 = PM hours.
4	Hours Alarm - Tens	Holds the tens place for the hours alarm.
3:0	Hour Alarm - Ones	Holds the ones place for the hours alarm.

Table 46: Hours Alarm Register (24 Hour Mode)

Bit	7	6	5	4	3	2	1	0
Name	GP17	GP16	Hours Alarm - Tens		Hours Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 47: Hours Alarm Register Bits (24 Hour Mode)

Bit	Name	Function
7	GP17	Register bit for general purpose use.
6	GP16	Register bit for general purpose use.
5:4	Hours Alarm - Tens	Holds the tens place for the hours alarm.
3:0	Hours Alarm - Ones	Holds the ones place for the hours alarm.

6.3.5 0x0C - Date Alarm

This register holds alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

Table 48: Date Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	GP19	GP18	Date Alarm - Tens		Date Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 49: Date Alarm Register Bits

Bit	Name	Function
7	GP19	Register bit for general purpose use.
6	GP18	Register bit for general purpose use.
5:4	Date Alarm - Tens	Holds the tens place for the date alarm.
3:0	Date Alarm - Ones	Holds the ones place for the date alarm.

6.3.6 0x0D - Months Alarm

This register holds alarm value for months, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

Table 50: Months Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	GP22	GP21	GP20	Months Alarm - Tens	Months Alarm - Ones			
Reset	0	0	0	0	0	0	0	0

Table 51: Months Alarm Register Bits

Bit	Name	Function
7	GP22	Register bit for general purpose use.
6	GP21	Register bit for general purpose use.
5	GP20	Register bit for general purpose use.
4	Months Alarm - Tens	Holds the tens place for the months alarm.
3:0	Months Alarm - Ones	Holds the ones place for the months alarm.

6.3.7 0x0E - Weekday Alarm

This register holds the alarm value for the day of the week. Values will range from 0 to 6.

Table 52: Weekdays Alarm Register

Bit	7	6	5	4	3	2	1	0
Name	GP27	GP26	GP25	GP24	GP23	Weekdays Alarm		
Reset	0	0	0	0	0	0	0	0

Table 53: Weekdays Alarm Register Bits

Bit	Name	Function
7	GP27	Register bit for general purpose use.
6	GP26	Register bit for general purpose use.
5	GP25	Register bit for general purpose use.
4	GP24	Register bit for general purpose use.
3	GP23	Register bit for general purpose use.
2:0	Weekdays Alarm	Holds the weekdays alarm value.

6.4 Configuration Registers

6.4.1 0x0F - Status (Read Only)

This register holds a variety of status bits. The register may be written at any time to clear or set any status flag. If the ARST bit is set, any read of the Status Register will clear all of the bits except the CB bit.

Table 54: Status Register

Bit	7	6	5	4	3	2	1	0
Name	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1
Reset	0	0	0	0	0	0	0	0

Table 55: Status Register Bits

Bit	Name	Function
7	CB	Century. This bit will be toggled when the Years register rolls over from 99 to 00 if the CEB bit is a 1. A 0 assumes the century is 19xx or 21xx, and a 1 assumes it is 20xx for leap year calculations.
6	BAT	Set when the system switches to the VBAT Power state.
5	WDT	Set when the Watchdog Timer is enabled and is triggered, and the WDS bit is 0.
4	BL	Set if the battery voltage VBAT crosses the reference voltage selected by BREF in the direction selected by BPOL.
3	TIM	Set when the Countdown Timer is enabled and reaches zero.

Table 55: Status Register Bits

Bit	Name	Function
2	ALM	Set when the Alarm function is enabled and all selected Alarm registers match their respective counters.
1	EX2	Set when an external trigger is detected on the WDI pin. The EX2E bit must be set in order for this interrupt to occur, but subsequently clearing EX2E will not automatically clear this flag.
0	EX1	Set when an external trigger is detected on the EXTI pin. The EX1E bit must be set in order for this interrupt to occur, but subsequently clearing EX1E will not automatically clear this flag.

6.4.2 0x10 - Control1

This register holds some major control signals.

Table 56: Control1 Register

Bit	7	6	5	4	3	2	1	0
Name	STOP	12/24	OUTB	OUT	RSP	ARST		WRTC
Reset	0	0	0	1	0	0	1	1

Table 57: Control1 Register Bits

Bit	Name	Function
7	STOP	When 1, stops the clocking system. The XT and RC Oscillators are not stopped. In XT Mode the 32.786 kHz clock output will continue to run. In RC Mode, the 128 Hz clock output will continue to run. Other clock output selections will produce static outputs. This bit allows the clock system to be precisely started, by setting it to 1 and back to 0.
6	12/24	When 0, the Hours register operates in 24 hour mode. When 1, the Hours register operates in 12 hour mode.
5	OUTB	A static value which may be driven on the nIRQ2 pin. The OUTB bit cannot be set to 1 if the LKO2 bit is 1.
4	OUT	A static value which may be driven on the FOUT/nIRQ pin. This bit also defines the default value for the Square Wave output when SQWE is not asserted.
3	RSP	Reset Polarity. When 1, the nRST pin is asserted high. When 0, the nRST pin is asserted low.
2	ARST	Auto reset enable. When 1, a read of the Status register will cause any interrupt bits (TIM, BL, ALM, WDT, XT1, XT2) to be cleared. When 0, the bits must be explicitly cleared by writing the Status register.
1	PWR2	When 1, the PSW/nIRQ2 pin is driven by an approximately 1Ω pull-down which allows the AB18X5 to switch power to other system devices through this pin. When 0, the PSW/nIRQ2pin is a normal open drain output.
0	WRTC	Write RTC. This bit must be set in order to write any of the Counter registers (Hundredths, Seconds, Minutes, Hours, Date, Months, Years or Weekdays).

6.4.3 0x11 - Control2

This register holds additional control and configuration signals for the flexible output pins FOUT/nIRQ and PSW/nIRQ2. Note that PSW/nIRQ2 and FOUT/nIRQ are open drain outputs.

Table 58: Control2 Register

Bit	7	6	5	4	3	2	1	0
Name	RESERVED			OUT2S			OUT1S	
Reset	0	0	1	1	1	1	0	0

Table 59: Control2 Register Bits

Bit	Name	Function
7:6	RESERVED	RESERVED
5		
4:2	OUT2S	Controls the function of the nIRQ2 pin, as shown in Table 60.
1:0	OUT1S	Controls the function of the FOUT/NIRQ pin, as shown in Table 61.

Table 60: PSW/nIRQ2 Pin Control

OUT2S Value	PSW/nIRQ2 Pin Function
000	nIRQ if at least one interrupt is enabled, else OUTB
001	SQW if SQWE = 1, else OUTB
010	RESERVED
011	nAIRQ if AIE is set, else OUTB
100	TIRQ if TIE is set, else OUTB
101	nTIRQ if TIE is set, else OUTB
110	SLEEP
111	OUTB

Table 61: FOUT/nIRQ Pin Control

OUT1S Value	FOUT/nIRQ Pin Function
00	nIRQ if at least one interrupt is enabled, else OUT
01	SQW if SQWE = 1, else OUT
10	SQW if SQWE = 1, else nIRQ if at least one interrupt is enabled, else OUT
11	nAIRQ if AIE is set, else OUT

6.4.4 0x12 - Interrupt Mask

This register holds the interrupt enable bits and other configuration information.

Table 62: Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0
Name	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E
Reset	1	1	1	0	0	0	0	0

Table 63: Interrupt Mask Register Bits

Bit	Name	Function
7	CEB	Century Enable. 0: The CB bit will never be automatically updated. 1: The CB bit will toggle when the Years register rolls over from 99 to 00.
6:5	IM	Interrupt Mode. This controls the duration of the nAIRQ interrupt as shown below. The interrupt output always goes high when the corresponding flag in the Status Register is cleared. In order to minimize current drawn by the AB18X5 this field should be kept at 0x3. 00: Level (static) for both XT mode and RC mode. 01: 1/8192 seconds for XT mode. 1/64 seconds for RC mode. 10: 1/64 seconds for both XT mode and RC mode. 11: 1/4 seconds for both XT mode and RC mode.
4	BLIE	Battery Low Interrupt Enable. 0: Disable the battery low interrupt. 1: The battery low detection will generate an interrupt.
3	TIE	Timer Interrupt Enable. 0: Disable the timer interrupt. 1: The Countdown Timer will generate an IRQ interrupt signal and set the TIM flag when the timer reaches 0.
2	AIE	Alarm Interrupt Enable. 0: Disable the alarm interrupt. 1: A match of all the enabled alarm registers will generate an IRQ interrupt signal.
1	EX2E	XT2 Interrupt Enable. 0: Disable the XT2 interrupt. 1: The WDI input pin will generate the XT2 interrupt when the edge specified by EX2P occurs.
0	EX1E	XT1 Interrupt Enable. 0: Disable the XT1 interrupt. 1: The EXTI input pin will generate the XT1 interrupt when the edge specified by EX1P occurs.

6.4.5 0x13 - SQW

This register holds the control signals for the square wave output. Note that some frequency selections are not valid if the 128 Hz RC Oscillator is selected.

Table 64: SQW Register

Bit	7	6	5	4	3	2	1	0
Name	SQWE	RESERVED		SQFS				
Reset	0	0	1	0	0	1	1	0

Table 65: SQW Register Bits

Bit	Name	Function
7	SQWE	When 1, the square wave output is enabled. When 0, the square wave output is held at the value of OUT.
6:5	RESERVED	RESERVED
4:0	SQFS	Selects the frequency of the square wave output, as shown in Table 66. Note that some selections are not valid if the 128 Hz oscillator is selected. Some selections also produce short pulses rather than square waves, and are intended primarily for test usage.

Table 66: Square Wave Function Select

SQFS Value	Square Wave Output
00000	1 century(2)
00001	32.768 kHz(1)
00010	8.192 kHz(1)
00011	4.096 kHz(1)
00100	2.048 kHz(1)
00101	1.024 kHz(1)
00110	512 Hz(1) – Default value
00111	256 Hz(1)
01000	128 Hz
01001	64 Hz
01010	32 Hz
01011	16 Hz
01100	8 Hz
01101	4 Hz
01110	2 Hz
01111	1 Hz

Table 66: Square Wave Function Select

SQFS Value	Square Wave Output
10000	½ Hz
10001	¼ Hz
10010	1/8 Hz
10011	1/16 Hz
10100	1/32 Hz
10101	1/60 Hz (1 minute)
10110	16.384 kHz (1)
10111	100 Hz (1)(2)
11000	1 hour(2)
11001	1 day(2)
11010	TIRQ
11011	NOT TIRQ
11100	1 year(2)
11101	1 Hz to Counters(2)
11110	1/32 Hz from Acal(2)
11111	1/8 Hz from Acal (2)
(1) NA if 128 Hz Oscillator selected. (2) Pulses for Test Usage.	

6.5 Calibration Registers

6.5.1 0x14 - Calibration XT

This register holds the control signals for a digital calibration function of the XT Oscillator.

Table 67: Calibration XT Register

Bit	7	6	5	4	3	2	1	0
Name	CMDX	OFFSETX						
Reset	0	0	0	0	0	0	0	0

Table 68: Calibration XT Register Bits

Bit	Name	Function
7	CMDX	The calibration adjust mode. When 0 (Normal Mode), each adjustment step is +/- 2 ppm. When 1 (Coarse Mode), each adjustment step is +/- 4 ppm.
6:0	OFFSETX	The amount to adjust the effective time. This is a two's complement number with a range of -64 to +63 adjustment steps.

6.5.2 0x15 - Calibration RC Upper

This register holds the control signals for the fine digital calibration function of the low power RC Oscillator. This register is initialized with a factory value which calibrates the RC Oscillator to 128 Hz.

Table 69: Calibration RC Upper Register

Bit	7	6	5	4	3	2	1	0
Name	CMDR		OFFSETRU					
Reset	Preconfigured		Preconfigured					

Table 70: Calibration RC Upper Register Bits

Bit	Name	Function
7:6	CMDR	The calibration adjust mode for the RC calibration adjustment. CMDR selects the highest frequency used in the RC Calibration process, as shown in Table 71.
5:0	OFFSETRU	The upper 6 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of -2^13 to +2^13-1 adjustment steps.

Table 71: CMDR Function

CMDR	Calibration Period	Minimum Adjustment	Maximum Adjustment
00	8,192 seconds	+/-1.91 ppm	+/-1.56%
01	4,096 seconds	+/-3.82 ppm	+/-3.13%
10	2,048 seconds	+/-7.64 ppm	+/-6.25%
11	1,024 seconds	+/-15.28 ppm	+/-12.5%

6.5.3 0x16 - Calibration RC Lower

This register holds the lower 8 bits of the OFFSETR field for the digital calibration function of the low power RC Oscillator. This register is initialized with a factory value which calibrates the RC Oscillator to 128 Hz.

Table 72: Calibration RC Lower Register

Bit	7	6	5	4	3	2	1	0
Name	OFFSETRL							
Reset	Preconfigured							

Table 73: Calibration RC Lower Register Bits

Bit	Name	Function
7:0	OFFSETRL	The lower 8 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of -2^13 to +2^13-1 adjustment steps.

6.6 Sleep Control Register

6.6.1 0x17 - Sleep Control

This register controls the Sleep function of the Power Control system.

Table 74: Sleep Control Register

Bit	7	6	5	4	3	2	1	0
Name	SLP	SLRES	EX2P	EX1P	SLST	SLTO		
Reset	0	0	0	0	0	0	0	0

Table 75: Sleep Control Register Bits

Bit	Name	Function
7	SLP	When 1, the Power Control SM will transition to the SWAIT state. This bit will be cleared when the SM returns to the RUN state. If either STOP is 1 or no interrupt is enabled, SLP will remain at 0 even after an attempt to set it to 1.
6	SLRES	When 1, assert nRST low when the Power Control SM is in the SLEEP state.
5	EX2P	When 1, the external interrupt XT2 will trigger on a rising edge of the WDI pin. When 0, the external interrupt XT2 will trigger on a falling edge of the WDI pin.
4	EX1P	When 1, the external interrupt XT1 will trigger on a rising edge of the EXTI pin. When 0, the external interrupt XT1 will trigger on a falling edge of the EXTI pin.
3	SLST	Set when the AB18X5 enters Sleep Mode. This allows software to determine if a SLEEP has occurred since the last time this bit was read.
2:0	SLTO	The number of 7.8 ms periods after SLP is set until the Power Control SM goes into the SLEEP state. If SLTO is not 0, the actual delay is guaranteed to be between SLTO and (SLTO + 1) periods. If SLTO is 0, the transition will occur with no delay.

6.7 Timer Registers

6.7.1 0x18 - Countdown Timer Control

This register controls the Countdown Timer function. Note that the 00 frequency selection is slightly different depending on whether the 32.786 kHz XT Oscillator or the 128 Hz RC Oscillator is selected. In some RC Oscillator modes, the interrupt pulse output is specified as RCPLS. In these cases the interrupt

output will be a short negative going pulse which is typically between 100 and 400 µs. This allows control of external devices which require pulses shorter than the minimum 7.8 ms pulse created directly by the RC Oscillator.

Table 76: Countdown Timer Control Register

Bit	7	6	5	4	3	2	1	0
Name	TE	TM	TRPT	RPT			TFS	
Reset	0	0	1	0	0	0	1	1

Table 77: Countdown Timer Control Register Bits

Bit	Name	Function
7	TE	Timer Enable. When 1, the Countdown Timer will count down. When 0, the Countdown Timer retains the current value. If TE is 0, the clock to the Timer is disabled for power minimization.
6	TM	Timer Interrupt Mode. Along with TRPT, this controls the Timer Interrupt function as shown in Table 28. A Level Interrupt will cause the nIRQ signal to be driven low by a Countdown Timer interrupt until the associated flag is cleared. A Pulse interrupt will cause the nIRQ signal to be driven low for the time shown in Table 79 or until the flag is cleared.
5	TRPT	Along with TM, this controls the repeat function of the Countdown Timer. If Repeat is selected, the Countdown Timer reloads the value from the Timer_Initial register upon reaching 0, and continues counting. If Single is selected, the Countdown Timer will halt when it reaches zero. This allows the generation of periodic interrupts of virtually any frequency.
4:2	RPT	These bits enable the Alarm Interrupt repeat function, as shown in Table 78. HA is the Hundredths_Alarm register value.
1:0	TFS	Select the clock frequency and interrupt pulse width of the Countdown Timer, as defined in Table 79. RCPLS is a 100-400 µs pulse.

Table 78: Repeat Function

RPT	HA	Repeat When
7	FF	Once per hundredth (*)
7	F[9-0]	Once per tenth (*)
7	[9-0][9-0]	Hundredths match (once per second)
6		Hundredths and seconds match (once per minute)
5		Hundredths, seconds and minutes match (once per hour)
4		Hundredths, seconds, minutes and hours match (once per day)
3		Hundredths, seconds, minutes, hours and weekday match (once per week)
2		Hundredths, seconds, minutes, hours and date match (once per month)
1		Hundredths, seconds, minutes, hours, date and month match (once per year)
0		Alarm Disabled
(*)Once per second if 128 Hz Oscillator selected		

Table 79: Countdown Timer Function Select

TM	TRPT	TFS	Int	Repeat	Countdown Timer Frequency		Interrupt Pulse Width	
					32.786 kHz Oscillator	128 Hz Oscillator	32.786 kHz Oscillator	128 Hz Oscillator
0	0	00	Pulse	Single	4.096 kHz	128 Hz	1/4096 s	1/128 s
0	0	01	Pulse	Single	64 Hz	64 Hz	1/128 s	1/128 s
0	0	10	Pulse	Single	1 Hz	1 Hz	1/64 s	1/64 s
0	0	11	Pulse	Single	1/60 Hz	1/60 Hz	1/64 s	1/64 s
0	1	00	Pulse	Repeat	4.096 kHz	128 Hz	1/4096 s	1/128 s
0	1	01	Pulse	Repeat	64 Hz	64 Hz	1/128 s	1/128 s
0	1	10	Pulse	Repeat	1 Hz	1 Hz	1/64 s	1/64 s
0	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/64 s	1/64 s
1	0	00	Level	Single	4.096 kHz	128 Hz	N/A	N/A
1	0	01	Level	Single	64 Hz	64 Hz	N/A	N/A
1	0	10	Level	Single	1 Hz	1 Hz	N/A	N/A
1	0	11	Level	Single	1/60 Hz	1/60 Hz	N/A	N/A
1	1	00	Pulse	Repeat	4.096 kHz	128 Hz	1/4096 s	RCPLS
1	1	01	Pulse	Repeat	64 Hz	64 Hz	1/4096 s	RCPLS
1	1	10	Pulse	Repeat	1 Hz	1 Hz	1/4096 s	RCPLS
1	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/4096 s	RCPLS

6.7.2 0x19 - Countdown Timer

This register holds the current value of the Countdown Timer. It may be loaded with the desired starting value when the Countdown Timer is stopped.

Table 80: Countdown Timer Register

Bit	7	6	5	4	3	2	1	0
Name	Countdown Timer							
Reset	0	0	0	0	0	0	0	0

Table 81: Countdown Timer Register Bits

Bit	Name	Function
7:0	Countdown Timer	The current value of the Countdown Timer.

6.7.3 0x1A - Timer Initial Value

This register holds the value which will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1. This allows for periodic timer interrupts, and a period of (Timer_initial + 1) * (1/ Countdown_frequency).

Table 82: Timer Initial Value Register

Bit	7	6	5	4	3	2	1	0
Name	Timer Initial Value							
Reset	0	0	0	0	0	0	0	0

Table 83: Timer Initial Value Register Bits

Bit	Name	Function
7:0	Timer Initial Value	The value reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1.

6.7.4 0x1B - Watchdog Timer

This register controls the Watchdog Timer function.

Table 84: Watchdog Timer Register

Bit	7	6	5	4	3	2	1	0
Name	WDS	BMB					WRB	
Reset	0	0	0	0	0	0	0	0

Table 85: Watchdog Timer Register Bits

Bit	Name	Function
7	WDS	Watchdog Steering. When 0, the Watchdog Timer will generate WIRQ when it times out. When 1, the Watchdog Timer will generate a reset when it times out.
6:2	BMB	The number of clock cycles which must occur before the Watchdog Timer times out. A value of 00000 disables the Watchdog Timer function.
1:0	WRB	The clock frequency of the Watchdog Timer, as shown in Table 86.

Table 86: Watchdog Timer Frequency Select

WRB Value	Watchdog Timer Frequency
00	16 Hz
01	4 Hz
10	1 Hz
11	1/4 Hz

6.8 Oscillator Registers

6.8.1 0x1C - Oscillator Control

This register controls the overall Oscillator function. It may only be written if the Configuration Key register contains the value 0xA1. An Autocalibration cycle is initiated immediately whenever this register is written with a value in the ACAL field which is not zero.

Table 87: Oscillator Control Register

Bit	7	6	5	4	3	2	1	0
Name	OSEL	ACAL		AOS	FOS	PWGT	OFIE	ACIE
Reset	0	0	0	0	0	0	0	0

Table 88: Oscillator Control Register Bits

Bit	Name	Function
7	OSEL	When 1, request the RC Oscillator to generate a 128 Hz clock for the timer circuits. When 0, request the XT Oscillator to generate a 32.786 kHz clock to the timer circuit. Note that if the XT Oscillator is not operating, the oscillator switch will not occur. The OMODE field in the Oscillator Status register indicates the actual oscillator which is selected.
6:5	ACAL	Controls the automatic calibration function, as described in Autocalibration.
4	AOS	When 1, the oscillator will automatically switch to RC oscillator mode when the system is powered from the battery. When 0, no automatic switching occurs.
3	FOS	When 1, the oscillator will automatically switch to RC oscillator mode when an oscillator failure is detected. When 0, no automatic switching occurs.
2	PWGT	When 1, the I/O interface will be disabled when the power switch is active and disabled (PWR2 is a 1 and the OUT2 output is a 1). In order for the I/O interface to be disabled, the PSW pin must be configured for the sleep function by setting the OUT2S field to a value of 6.
1	OFIE	Oscillator Fail interrupt enable. When 1, an Oscillator Failure will generate an IRQ signal.
0	ACIE	When 1, an Autocalibration Failure will generate an interrupt.

6.8.2 0x1D – Oscillator Status Register

This register holds several miscellaneous bits used to control and observe the oscillators.

Table 89: Oscillator Status Register

Bit	7	6	5	4	3	2	1	0
Name	XTCAL		LKO2	OMODE	RESERVED		OF	ACF
Reset	0	0	1	0	0	0	1	0

Table 90: Oscillator Status Register Bits

Bit	Name	Function
7:6	XTCAL	Extended Crystal Calibration. This field defines a value by which the Crystal Oscillator is adjusted to compensate for low capacitance crystals, independent of the normal Crystal Calibration function controlled by the Calibration XT Register. The frequency generated by the Crystal Oscillator is slowed by 122 ppm times the value in the XTCAL field (0, -122,-244 or -366 ppm).
5	LKO2	Lock OUT2. If this bit is a 1, the OUTB register bit (see Section 7.3.2) cannot be set to 1. This is typically used when OUT2 is configured as a power switch, and setting OUTB to a 1 would turn off the switch.
4	OMODE	(read only) – Oscillator Mode. This bit is a 1 if the RC Oscillator is selected to drive the internal clocks, and a 0 if the Crystal Oscillator is selected. If the STOP bit is set, the OMODE bit is invalid.
3:2	RESERVED	RESERVED
1	OF	Oscillator Failure. This bit is set on a power on reset, when both the system and battery voltages have dropped below acceptable levels. It is also set if an Oscillator Failure occurs, indicating that the crystal oscillator is running at less than 8 kHz. It can be cleared by writing a 0 to the bit.
0	ACF	Set when an Autocalibration Failure occurs, indicating that either the RC Oscillator frequency is too different from 128 Hz to be correctly calibrated or the XT Oscillator did not start.

6.9 Miscellaneous Registers

6.9.1 0x1F - Configuration Key

This register contains the Configuration Key, which must be written with specific values in order to access some registers and functions. The Configuration Key is reset to 0x00 on any register write.

Table 91: Configuration Key Register

Bit	7	6	5	4	3	2	1	0
Name	Configuration Key							
Reset	0	0	0	0	0	0	0	0

Table 92: Configuration Key Register Bits

Bit	Name	Function
7:0	Configuration Key	Written with specific values in order to access some registers and functions.

1. Writing a value of 0xA1 enables write access to the Oscillator Control register
2. Writing a value of 0x3C does not update the Configuration Key register, but generates a Software Reset (see Software Reset).
3. Writing a value of 0x9D enables write access to the Trickle Register (0x20), the BREF Register (0x21), the AFCTRL Register (0x26), the Batmode I/O Register (0x27) and the Output Control Register (0x30).

6.10 Analog Control Registers

6.10.1 0x20 - Trickle

This register controls the Trickle Charger. The Key Register must be written with the value 0x9D in order to enable access to this register.

Table 93: Trickle Register

Bit	7	6	5	4	3	2	1	0
Name	TCS				DIODE		ROUT	
Reset	0	0	0	0	0	0	0	0

Table 94: Trickle Register Bits

Bit	Name	Function
7:4	TCS	A value of 1010 enables the trickle charge function. All other values disable the Trickle Charger.
3:2	DIODE	Diode Select. A value of 10 inserts a standard diode into the trickle charge circuit, with a voltage drop of 0.6V. A value of 01 inserts a schottky diode into the trickle charge circuit, with a voltage drop of 0.3V. Other values disable the Trickle Charger.
1:0	ROUT	Output Resistor. This selects the output resistor of the trickle charge circuit, as shown in Table 95.

Table 95: Trickle Charge Output Resistor

ROUT Value	Series Resistor
00	Disable
01	3 KΩ
10	6 KΩ
11	11 KΩ

6.10.2 0x21 - BREF Control

This register controls the reference voltages used in the Wakeup Control system. The Key Register must be written with the value 0x9D in order to enable access to this register.

Table 96: BREF Control Register

Bit	7	6	5	4	3	2	1	0
Name	BREF				RESERVED			
Reset	1	1	1	1	0	0	0	0

Table 97: BREF Control Register Bits

Bit	Name	Function
7:4	BREF	This selects the voltage reference which is compared to the battery voltage VBAT to produce the BBOD signal. Typical values are shown in Table 98. The valid BREF values are 0x7, 0xB, 0xD, and 0xF. The reset value is 0xF. All other values are RESERVED.
3:0	RESERVED	RESERVED

Table 98: VBAT Reference Voltage

BREF Value	VBAT Falling Voltage (TYP)	VBAT Rising Voltage (TYP)
0111	2.5V	3.0V
1011	2.1V	2.5V
1101	1.8V	2.2V
1111	1.4V	1.6V

6.10.3 0x26 – AFCTRL

This register holds the enable code for the Autocalibration Filter (AF) filter capacitor connected to the AF pin. Writing the value 0xA0 to this register enables the AF pin. Writing the value 0x00 to this register disables the AF pin. No other value may be written to this register. The Configuration Key Register must be written with the value 0x9D prior to writing the AFCTRL Register.

Table 99: AFCTRL Register

Bit	7	6	5	4	3	2	1	0
Name	AFCTRL							
Reset	0	0	0	0	0	0	0	0

Table 100: AFCTRL Register Bits

Bit	Name	Function
7:0	AFCTRL	If 0xA0, enable the AF pin. If 0x00, disable the AF pin.

6.10.4 0x27 – Batmode IO Register

This register holds the IOBM bit which controls the enabling and disabling of the I/O interface when a Brownout Detection occurs. It may only be written if the Configuration Key register contains the value 0x9D. All undefined bits must be written with 0.

Table 101: Batmode IO Register

Bit	7	6	5	4	3	2	1	0
Name	IOBM	RESERVED						
Reset	1	0	0	0	0	0	0	0

Table 102: Batmode IO Register Bits

Bit	Name	Function
7	IOBM	If 1, the AB18X5 will not disable the I/O interface even if VCC goes away and VBAT is still present. This allows external access while the AB18X5 is powered by VBAT.
6:0	RESERVED	RESERVED - must write only 0000000.

6.10.5 0x2F – Analog Status Register (Read Only)

This register holds eight status bits which indicate the voltage levels of the VCC and VBAT power inputs.

Table 103: Analog Status Register

Bit	7	6	5	4	3	2	1	0
Name	BBOD	BMIN	RESERVED				VINIT	RESERVED
Reset								

Table 104: Analog Status Register Bits

Bit	Name	Function
7	BBOD	If 1, the VBAT input voltage is above the BREF threshold.
6	BMIN	If 1, the VBAT input voltage is above the minimum operating voltage (1.2 V).
5:2	RESERVED	RESERVED
1	VINIT	If 1, the VCC input voltage is above the minimum power up voltage (1.6 V).
0	RESERVED	RESERVED

6.10.6 0x30 – Output Control Register

This register holds bits which control the behavior of the I/O pins under various power down conditions. The Key Register must be written with the value 0x9D in order to enable access to this register.

Table 105: Output Control Register

Bit	7	6	5	4	3	2	1	0
Name	WDBM	EXBM	WDDS	EXDS	RSEN	O4EN	O3EN	O1EN
Reset	0	0	0	0	0	0	0	0

Table 106: Output Control Register Bits

Bit	Name	Function
7	WDBM	If 1, the WDI input is enabled when the AB18X5 is powered from VBAT. If 0, the WDI input is disabled when the AB18X5 is powered from VBAT.
6	EXBM	If 1, the EXTI input is enabled when the AB18X5 is powered from VBAT. If 0, the EXTI input is disabled when the AB18X5 is powered from VBAT.
5	WDDS	If 1, the WDI input is disabled when the AB18X5 is in Sleep Mode. If 0, the WDI input is enabled when the AB18X5 is in Sleep Mode If WDI is disabled, it will appear as a 1 to the internal logic.
4	EXDS	If 1, the EXTI input is disabled when the AB18X5 is in Sleep Mode. If 0, the EXTI input is enabled when the AB18X5 is in Sleep Mode. If EXTI is disabled, it will appear as a 1 to the internal logic.
3	RSEN	If 1, the nRST output is enabled when the AB18X5 is in Sleep Mode. If 0, the nRST output is completely disconnected when the AB18X5 is in Sleep Mode.
2	O4EN	If 1, the CLKOUT/nIRQ3 output is enabled when the AB18X5 is in Sleep Mode. If 0, the CLKOUT/nIRQ3 output is completely disconnected when the AB18X5 is in Sleep Mode.
1	O3EN	If 1, the nTIRQ output is enabled when the AB18X5 is in Sleep Mode. If 0, the nTIRQ output is completely disconnected when the AB18X5 is in Sleep Mode.
0	O1EN	If 1, the FOUT/nIRQ output is enabled when the AB18X5 is in Sleep Mode. If 0, the FOUT/nIRQ output is completely disconnected when the AB18X5 is in Sleep Mode.

6.11 ID Registers

6.11.1 0x28 – ID0 - Part Number Upper Register (Read Only)

This register holds the upper eight bits of the part number in BCD format, which is always 0x18 for the AB18X5 family.

Table 107: 28 – ID0 – Part Number Upper Register

Bit	7	6	5	4	3	2	1	0
Name	Part Number - Digit 3				Part Number - Digit 2			
Reset	0	0	0	1	1	0	0	0

6.11.2 0x29 – ID1 - Part Number Lower Register (Read Only)

This register holds the lower eight bits of the part number in BCD format.

Table 108: 28 – ID1 – Part Number Lower Register

Bit	7	6	5	4	3	2	1	0
Name	Part Number - Digit 1				Part Number - Digit 0			
Reset	Preconfigured Digit 1				Preconfigured Digit 0			

6.11.3 0x2A – ID2 - Part Revision (Read Only)

This register holds the Revision number of the part.

Table 109: 2A – ID2 – Part Revision Register

Bit	7	6	5	4	3	2	1	0
Name	MAJOR					MINOR		
Reset	0	0	0	1	0	0	1	1

Table 110: 2A – ID2 – Part Revision Register Bits

Bit	Name	Function
7:3	MAJOR	This field holds the major revision of the AB18X5.
2:0	MINOR	This field holds the minor revision of the AB18X5.

6.11.4 0x2B – ID3 – Lot Lower (Read Only)

This register holds the lower 8 bits of the manufacturing lot number.

Table 111: 2B – ID3 – Lot Lower Register

Bit	7	6	5	4	3	2	1	0
Name	Lot[7:0]							
Reset	Preconfigured Lot Number							

Table 112: 2B – ID3 – Lot Lower Register Bits

Bit	Name	Function
7:0	Lot[7:0]	This field holds the lower 8 bits of the manufacturing lot number.

6.11.5 0x2C – ID4 – ID Upper (Read Only)

This register holds part of the manufacturing information of the part, including bit 9 of the manufacturing lot number and the upper 7 bits of the unique part identifier. The 15-bit ID field contains a unique value for each AB18X5 part.

Table 113: 2C – ID4 – ID Upper Register

Bit	7	6	5	4	3	2	1	0
Name	Lot[9]	ID[14:8]						
Reset	Preconfigured Value							

Table 114: 2C – ID4 – ID Upper Register Bits

Bit	Name	Function
7	Lot[9]	This field holds bit 9 of the manufacturing lot number.
1:0	ID[14:8]	This field holds the upper 7 bits of the unique part ID.

6.11.6 0x2D – ID5 – Unique Lower (Read Only)

This register holds the lower 8 bits of the unique part identifier. The 15-bit ID field contains a unique value for each AB18X5 part.

Table 115: 2D – ID5 – ID Lower Register

Bit	7	6	5	4	3	2	1	0
Name	ID]7:0]							
Reset	Preconfigured Value							

Table 116: 2D – ID5 – ID Lower Register Bits

Bit	Name	Function
7:0	ID[7:0]	This field holds the lower 8 bits of the unique part ID.

6.11.7 0x2E – ID6 – Wafer (Read Only)

Table 117: 2E – ID6 – Wafer Register

Bit	7	6	5	4	3	2	1	0
Name	Lot[8]	Wafer					RESERVED	
Reset	Preconfigured Value							

Table 118: 2E – ID6 – Wafer Register Bits

Bit	Name	Function
7	Lot[8]	This field holds bit 8 of the manufacturing lot number.
6:2	Wafer	This field holds the manufacturing wafer number.
1:0	RESERVED	RESERVED

6.12 Ram Registers

6.12.1 0x3F - Extension RAM Address

This register controls access to the Extension RAM, and includes some miscellaneous control bits.

Table 119: 3F – Extension RAM Address Register

Bit	7	6	5	4	3	2	1	0
Name	O4BM	BPOL	WDIN	EXIN	RSVD	XADA	XADS	
Reset	0	0	Read Only		0	0	0	0

Table 120: 3F – Extension RAM Address Register Bits

Bit	Name	Function
7	O4BM	If 1, the CLKOUT/nIRQ3 output is enabled when the AB18X5 is powered from VBAT. If 0, the CLKOUT/nIRQ3 output is completely disconnected when the AB18X5 is powered from VBAT.
6	BPOL	BL Polarity. When 0, the Battery Low flag BL is set when the VBAT voltage goes below the BREF threshold. When 1, the Battery Low flag BL is set when the VBAT voltage goes above the BREF threshold.
5	WDIN	(read only) – this bit supplies the current level of the WDI pin.
4	EXIN	(read only) – this bit supplies the current level of the EXTI pin.
3	RSVD	RESERVED.
2	XADA	This field supplies the upper bit for addresses to the Alternate RAM address space.
1:0	XADS	This field supplies the upper two address bits for the Standard RAM address space.

6.12.2 0x40 - 0x7F – Standard RAM

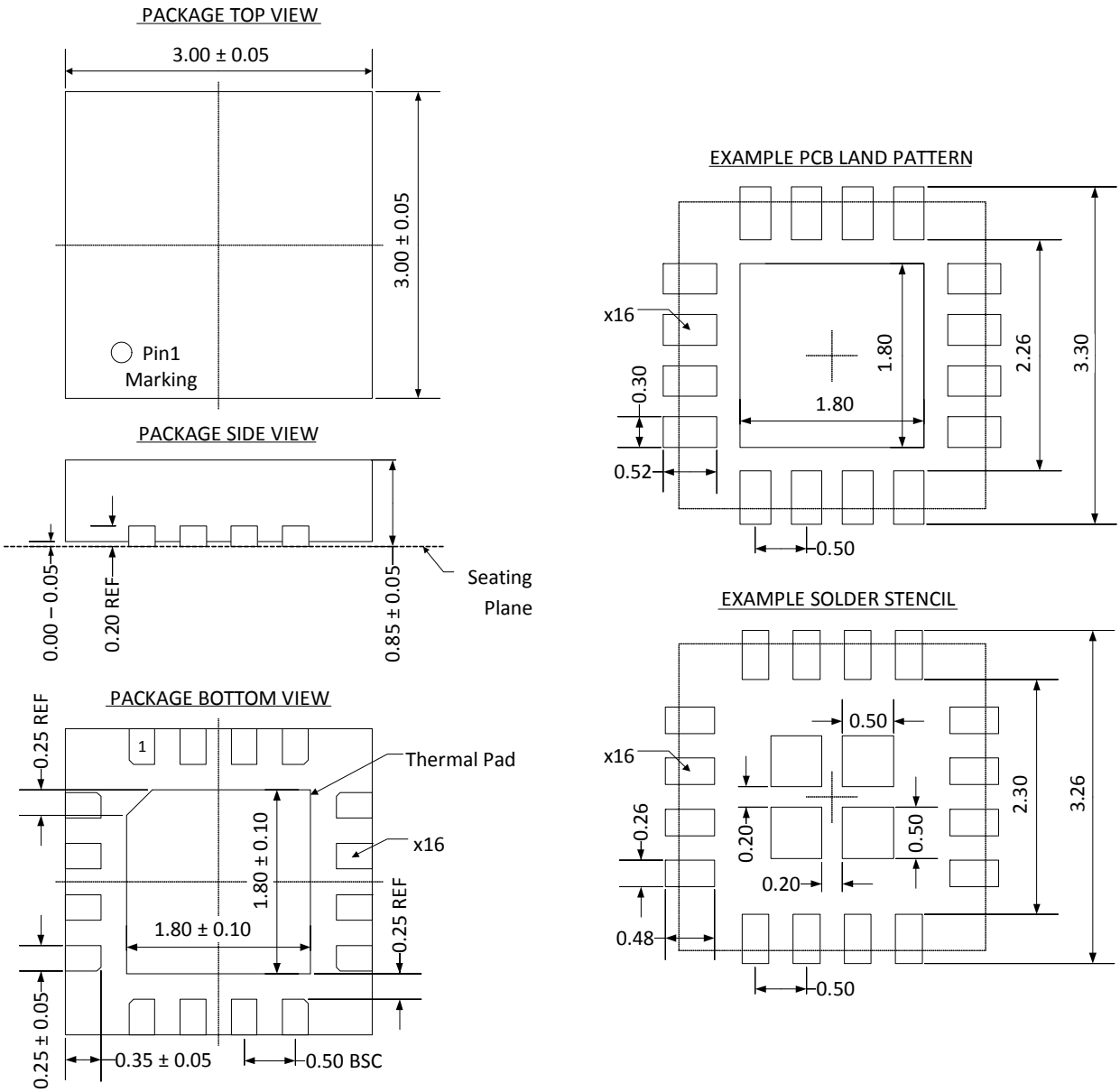
64 bytes of RAM space which may be accessed in either I^2C or SPI interface mode. The data in the RAM is held when using battery power. The upper 2 bits of the RAM address are taken from the XADS field, and the lower 6 bits are taken from the address offset, supporting a total RAM of 256 bytes. The initial values of the RAM locations are undefined.

6.12.3 0x80 - 0xFF – Alternate RAM

128 bytes of RAM which may be accessed only in I^2C interface mode. The data in the RAM is held when using battery power. The upper bit of the RAM address is taken from the XADA field, and the lower 7 bits are taken from the address offset, supporting a total RAM of 256 bytes. The initial values of the RAM locations are undefined.

7. Package Mechanical Information

Figure 41 illustrates the package mechanical information.



Drawing Notes:

1. All dimensions are in millimeters.
2. These drawings are subject to change without notice.
3. Quad Flat-pack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for connectivity and mechanical performance.
5. Customers should contact their board fabricator for minimum solder mask tolerances between signal pads.

Figure 41. Package Mechanical Diagram

8. Reflow Profile

Figure 42 illustrates the reflow soldering requirements.

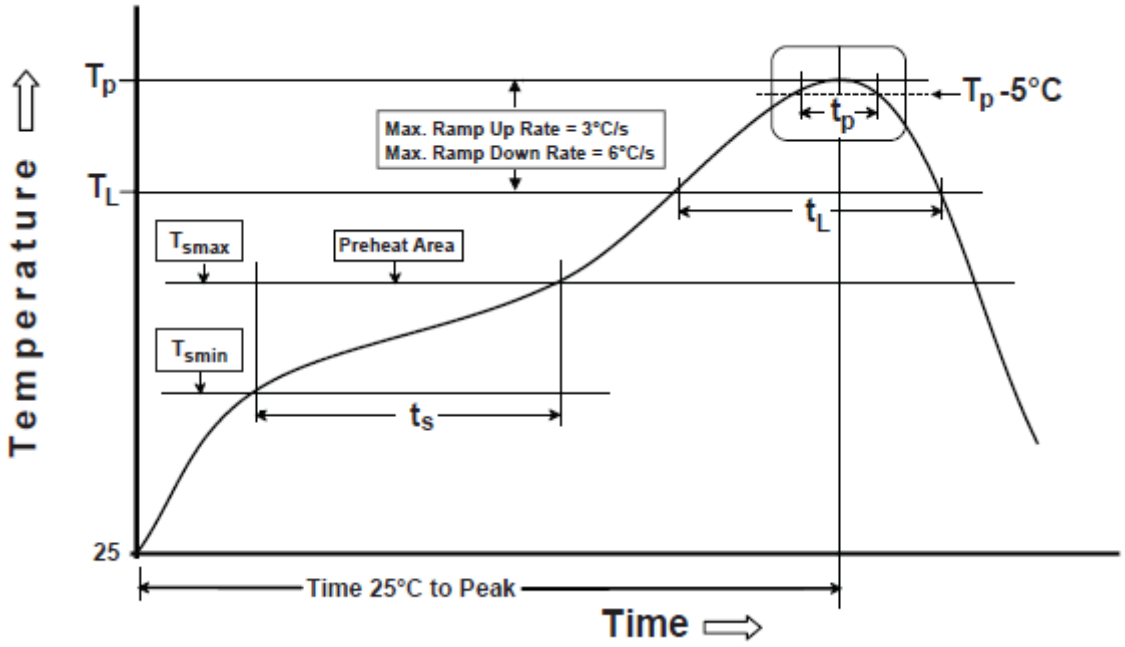


Figure 42. Reflow Soldering Diagram

Table 121: Reflow Soldering Requirements (Pb-free assembly)

Profile Feature	Requirement
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (ts) from (T_{smin} to T_{smax})	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to Tp)	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 °C 60-150 seconds
Peak package body temperature (T_p)	260 °C max.
Time (t_p) within 5 °C of T_p	30 seconds max.
Ramp-down rate (T_p to T_L)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

9. Ordering Information

Table 122: Ordering Information

AB18X5 Orderable Part Numbers		Package	Temperature Range	MSL Level(2)
P/N	Tape and Reel Qty			
AB1805-T3	3000pcs/reel	Pb-Free(1) 16-Pin QFN 3 x 3 mm	-40 to +85 °C	1
AB1815-T3	3000pcs/reel			

(1) Compliant and certified with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in raw homogeneous materials. The package was designed to be soldered at high temperatures (per reflow profile) and can be used in specified lead-free processes.

(2) Moisture Sensitivity Level rating according to the JEDEC J-STD-020D.1 industry standard classifications.

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