2.5 V to 5.5 V, 230 µA, Dual Rail-to-Rail, Voltage Output 8-/10-/12-Bit DACs

AD5302/AD5312/AD5322

FEATURES

- **AD5302: Two 8-bit buffered DACs in 1 package**
  - **A version: ±1 LSB INL, B version: ±0.5 LSB INL**
- **AD5312: Two 10-bit buffered DACs in 1 package**
  - **A version: ±4 LSB INL, B version: ±2 LSB INL**
- **AD5322: Two 12-bit buffered DACs in 1 package**
  - **A version: ±16 LSB INL, B version: ±8 LSB INL**
- **10-lead MSOP**
- **Micropower operation: 300 µA @ 5 V (including reference current)**
- **Power-down to 200 nA @ 5 V, 50 nA @ 3 V**
- **2.5 V to 5.5 V power supply**
- **Double-buffered input logic**
- **Guaranteed monotonic by design over all codes**
- **Buffered/Unbuffered reference input options**
- **0 V to V_{REF} output voltage**
- **Power-on-reset to 0 V**
- **Simultaneous update of DAC outputs via $\overline{LDAC}$**
- **Low power serial interface with Schmitt-triggered inputs**
- **On-chip rail-to-rail output buffer amplifiers**
- **Qualified for automotive applications**

APPLICATIONS

- **Portable battery-powered instruments**
- **Digital gain and offset adjustment**
- **Programmable voltage and current sources**
- **Programmable attenuators**

GENERAL DESCRIPTION

The AD5302/AD5312/AD5322 are dual 8-, 10-, and 12-bit buffered voltage output DACs in a 10-lead MSOP that operate from a single 2.5 V to 5.5 V supply, consuming 230 µA at 3 V. Their on-chip output amplifiers allow the outputs to swing rail-to-rail with a slew rate of 0.7 V/µs. The AD5302/AD5312/AD5322 utilize a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The references for the two DACs are derived from two reference pins (one per DAC). The reference inputs can be configured as buffered or unbuffered inputs. The outputs of both DACs can be updated simultaneously using the asynchronous $\overline{LDAC}$ input. The parts incorporate a power-on reset circuit, which ensures that the DAC outputs power-up to 0 V and remain there until a valid write takes place to the device. The parts contain a power-down feature that reduces the current consumption of the devices to 200 nA at 5 V (50 nA at 3 V) and provides software-selectable output loads while in power-down mode.

The low power consumption of these parts in normal operation makes them ideally suited for portable battery-operated equipment. The power consumption is 1.5 mW at 5 V, 0.7 mW at 3 V, reducing to 1 µW in power-down mode.

FUNCTIONAL BLOCK DIAGRAM

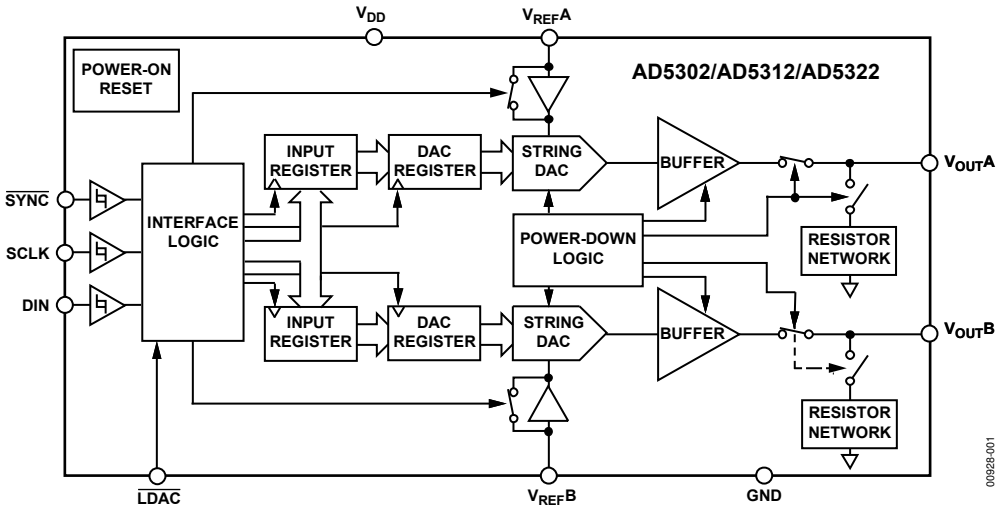


Figure 1.

Rev. D

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SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 2 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Version[1]			B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC PERFORMANCE[3, 4]								
AD5302								
Resolution		8			8		Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.5	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5312								
Resolution		10			10		Bits	
Relative Accuracy		±0.5	±4		±0.5	±2	LSB	
Differential Nonlinearity		±0.05	±0.5		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes
AD5322								
Resolution		12			12		Bits	
Relative Accuracy		±2	±16		±2	±8	LSB	
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3		±0.4	±3	% of FSR	See Figure 3 and Figure 4
Gain Error		±0.15	±1		±0.15	±1	% of FSR	See Figure 3 and Figure 4
Lower Deadband		10	60		10	60	mV	See Figure 3 and Figure 4
Offset Error Drift[5]		−12			−12		ppm of FSR/°C	
Gain Error Drift[5]		−5			−5		ppm of FSR/°C	
Power Supply Rejection Ratio[5]		−60			−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[5]		30			30		µV	
DAC REFERENCE INPUTS[5]								
V_{REF} Input Range	1		V_{DD}	1		V_{DD}	V	Buffered reference mode
	0		V_{DD}	0		V_{DD}	V	Unbuffered reference mode
V_{REF} Input Impedance		>10			>10		MΩ	Buffered reference mode
		180			180		kΩ	Unbuffered reference mode, input impedance = R_{DAC}
Reference Feedthrough		−90			−90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−80			−80		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[5]								
Minimum Output Voltage[6]		0.001			0.001		V min	A measure of the minimum drive capability of the output amplifier
Maximum Output Voltage[6]		V_{DD} − 0.001			V_{DD} − 0.001		V max	A measure of the maximum drive capability of the output amplifier
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		50			50		mA	V_{DD} = 5 V
		20			20		mA	V_{DD} = 3 V
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5			5		µs	Coming out of power-down mode, V_{DD} = 3 V
LOGIC INPUTS[5]								
Input Current			±1			±1	µA	
V_{IL}, Input Low Voltage			0.8			0.8	V	V_{DD} = 5 V ± 10%
			0.6			0.6	V	V_{DD} = 3 V ± 10%
			0.5			0.5	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	2.4			2.4			V	V_{DD} = 5 V ± 10%
	2.1			2.1			V	V_{DD} = 3 V ± 10%
	2.0			2.0			V	V_{DD} = 2.5 V
Pin Capacitance		2	3.5		2	3.5	pF	

Parameter[2]	A Version[1] Min	Typ	Max	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS								
V_{DD}	2.5		5.5	2.5		5.5	V	I_{DD} specification is valid for all DAC codes
I_{DD} (Normal Mode)								Both DACs active and excluding load currents
V_{DD} = 4.5 V to 5.5 V		300	450		300	450	µA	Both DACs in unbuffered mode, $V_{IH} = V_{DD}$ and
V_{DD} = 2.5 V to 3.6 V		230	350		230	350	µA	V_{IL} = GND; in buffered mode, extra current is typically × µA per DAC where x = 5 µA + V_{REF}/R_{DAC}
I_{DD} (Full Power-Down)								
V_{DD} = 4.5 V to 5.5 V		0.2	1		0.2	1	µA	
V_{DD} = 2.5 V to 3.6 V		0.05	1		0.05	1	µA	

[1] Temperature range: A, B version: –40°C to +105°C.
[2] See Terminology section.
[3] DC specifications tested with the outputs unloaded.
[4] Linearity is tested using a reduced code range: AD5302 (Code 8 to 248); AD5312 (Code 28 to 995); AD5322 (Code 115 to 3981).
[5] Guaranteed by design and characterization, not production tested.
[6] In order for the amplifier output to reach its minimum voltage, offset error must be negative. In order for the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and offset plus gain error must be positive.

AC SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter[3]	A, B Version[2] Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
AD5302		6	8	µs	¼ Scale to ¾ Scale Change (0 × 40 to 0 × C0)
AD5312		7	9	µs	¼ Scale to ¾ Scale Change (0 × 100 to 0 × C300)
AD5322		8	10	µs	¼ Scale to ¾ Scale Change (0 × 400 to 0 × C00)
Slew Rate		0.7		V/µs	
Major-Code Transition Glitch Energy		12		nV-s	1 LSB Change Around Major Carry (011…11 to 100…00)
Digital Feedthrough		0.10		nV-s	
Analog Crosstalk		0.01		nV-s	
DAC-to-DAC Crosstalk		0.01		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p, Unbuffered Mode
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p, Frequency = 10 kHz

[1] Guaranteed by design and characterization, not production tested.
[2] Temperature range: A, B version: –40°C to +105°C.
[3] See Terminology section.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1, 2, 3]

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Version)	Unit	Conditions/Comments
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK Active Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	100	ns min	Minimum $\overline{SYNC}$ High Time
t_9	20	ns min	$\overline{LDAC}$ Pulse Width
t_{10}	20	ns min	SCLK Falling Edge to $\overline{LDAC}$ Rising Edge

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] See Figure 2.

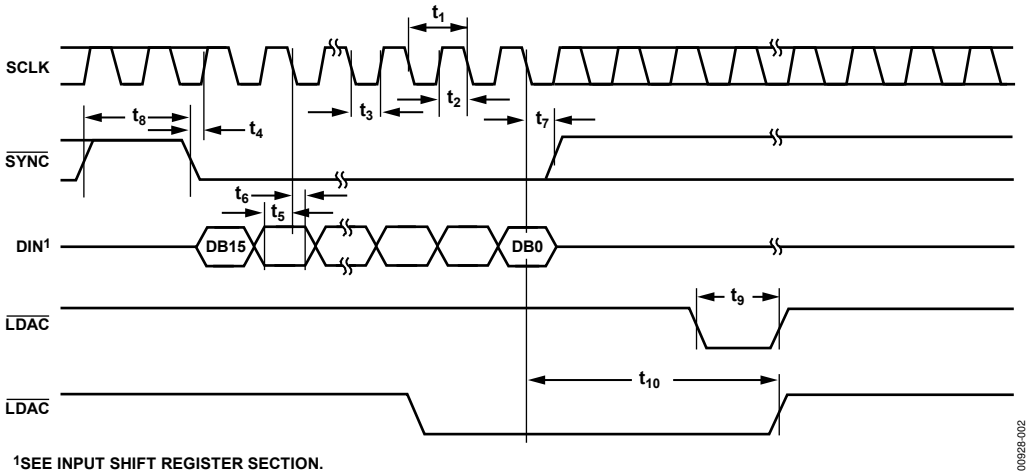


Figure 2. Serial Interface Timing Diagram

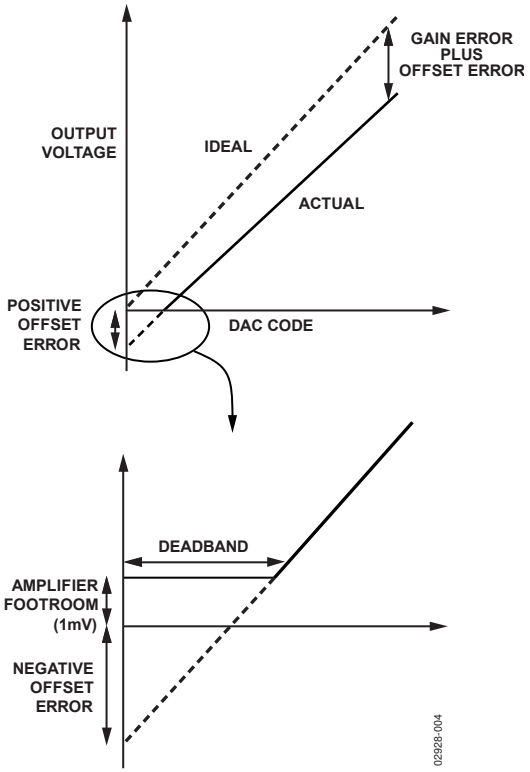


Figure 3. Transfer Function with Negative Offset

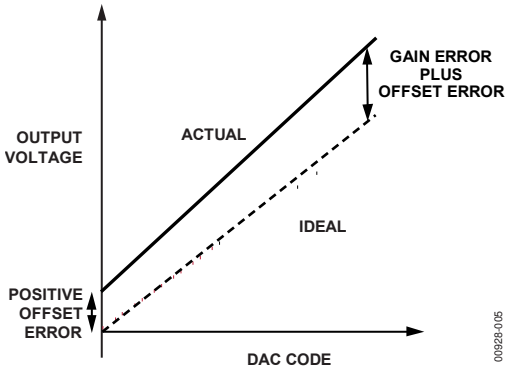


Figure 4. Transfer Function with Positive Offset

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT}A, V_{OUT}B to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A, B Version)	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	+150°C
10-Lead MSOP	
Power Dissipation	(T_J max – T_A)/θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

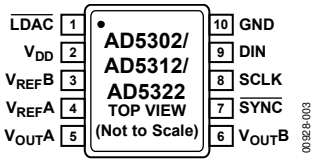


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Active Low Control Input. This pin transfers the contents of the input registers to their respective DAC registers. Pulsing $\overline{\text{LDAC}}$ low allows either or both DAC registers to be updated if the input registers have new data. This allows simultaneous updating of both DAC outputs.
2	V_{DD}	Power Supply Input. The parts can be operated from 2.5 V to 5.5 V, and the supply should be decoupled to GND.
3	$V_{REF}B$	Reference Input Pin for DAC B. This is the reference for DAC B. It can be configured as a buffered or an unbuffered input, depending on the BUF bit in the control word of DAC B. It has an input range of 0 V to V_{DD} in unbuffered mode and 1 V to V_{DD} in buffered mode.
4	$V_{REF}A$	Reference Input Pin for DAC A. This is the reference for DAC A. It can be configured as a buffered or an unbuffered input depending on the BUF bit in the control word of DAC A. It has an input range of 0 V to V_{DD} in unbuffered mode and 1 V to V_{DD} in buffered mode.
5	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
6	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
7	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 16 clocks. If $\overline{\text{SYNC}}$ is taken high before the 16th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz. The SCLK input buffer is powered down after each write cycle.
9	DIN	Serial Data Input. This device has a 16-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
10	GND	Ground Reference Point for All Circuitry on the Part.

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSB, from a straight line passing through the actual endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 6.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 9.

Offset Error
This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift
This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Major-Code Transition Glitch Energy
Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-sec and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s and vice versa.

Analog Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a change in the output of the other DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high, then pulsing $\overline{\text{LDAC}}$ low, and monitoring the output of the DAC whose digital code is not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of the other DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ low and monitoring the output of the other DAC. The area of the glitch is expressed in nV-sec.

DC Crosstalk
This is the dc change in the output level of one DAC in response to a change in the output of the other DAC. It is measured with a full-scale output change on one DAC while monitoring the other DAC. It is expressed in μV.

Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

Reference Feedthrough
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in dB.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dB.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Channel-to-Channel Isolation Definition
This is a ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of the other DAC. It is measured in dB.

TYPICAL PERFORMANCE CHARACTERISTICS

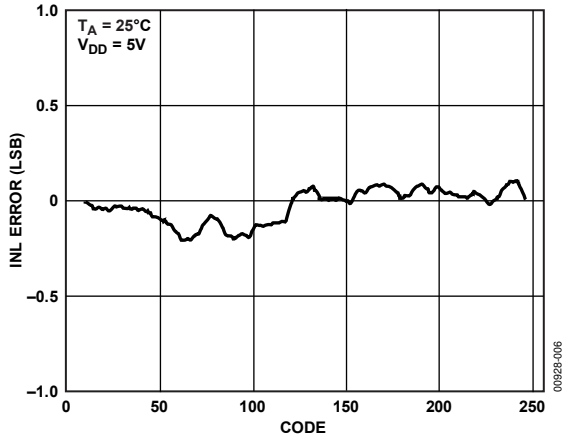


Figure 6. AD5302 Typical INL Plot

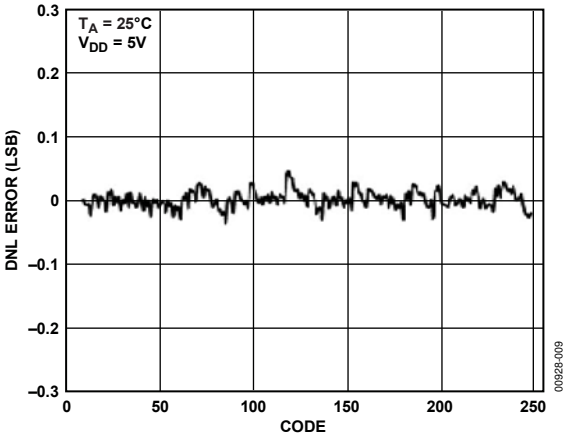


Figure 9. AD5302 Typical DNL Plot

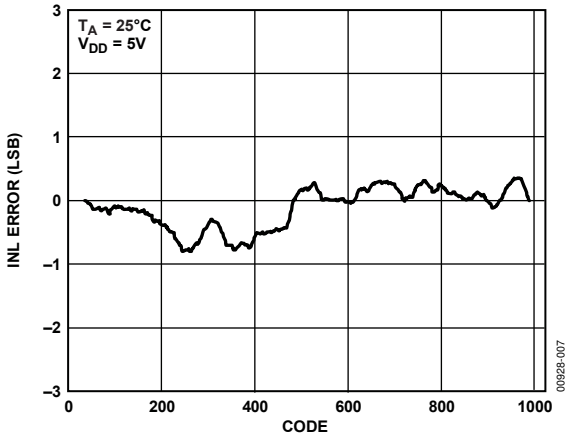


Figure 7. AD5312 Typical INL Plot

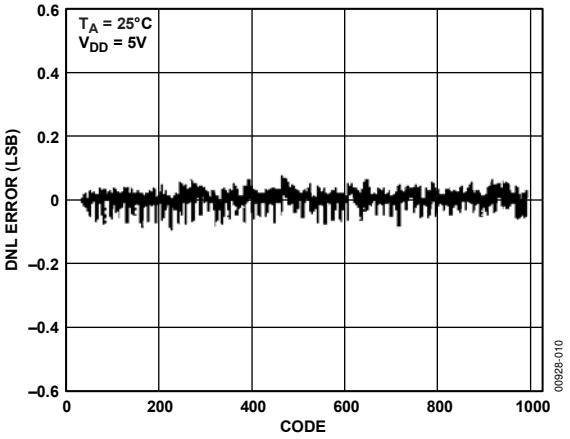


Figure 10. AD5312 Typical DNL Plot

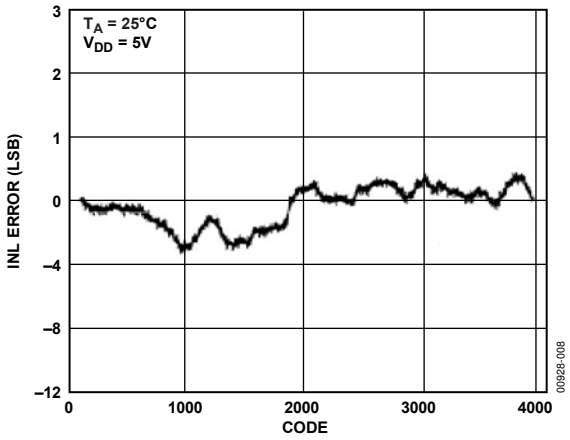


Figure 8. AD5322 Typical INL Plot

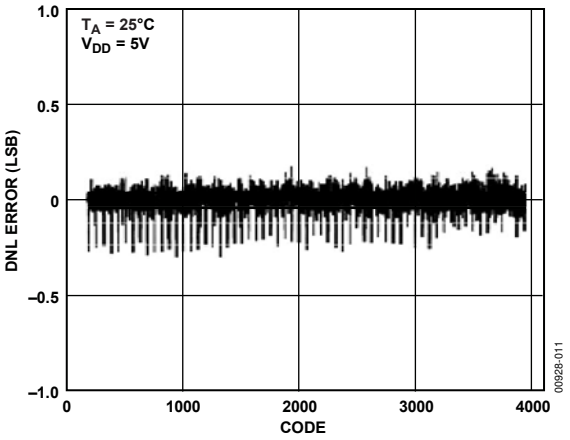


Figure 11. AD5322 Typical DNL Plot

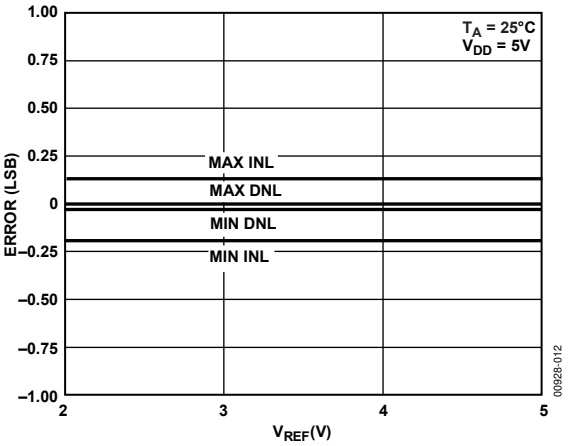


Figure 12. AD5302 INL and DNL Error vs. V_{REF}

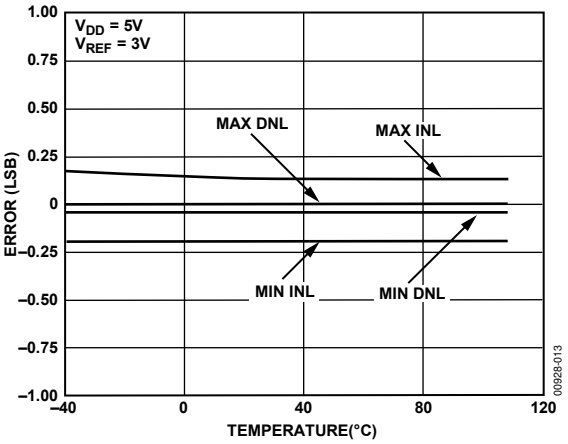


Figure 13. AD5302 INL Error and DNL Error vs. Temperature

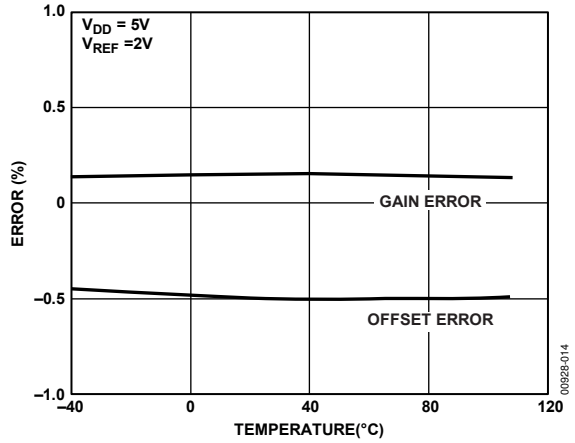


Figure 14. Offset Error and Gain Error vs. Temperature

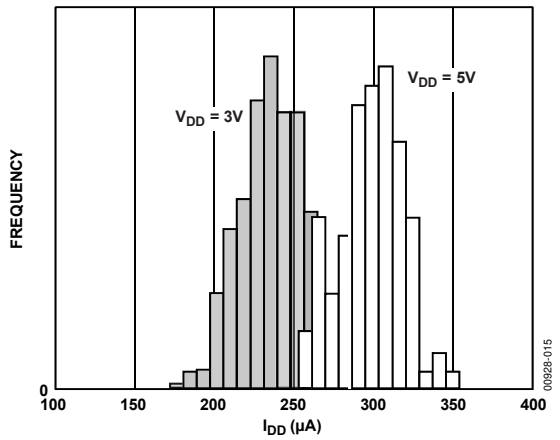


Figure 15. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

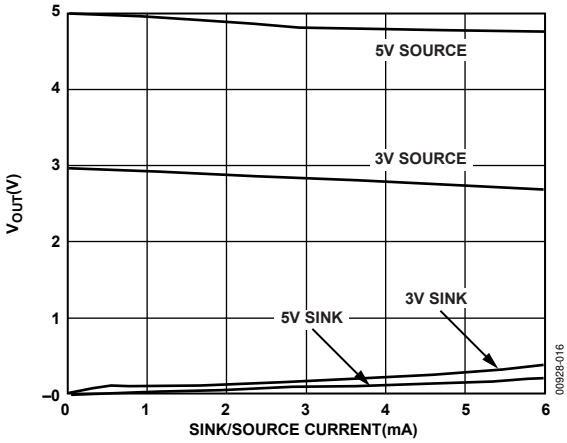


Figure 16. Source and Sink Current Capability

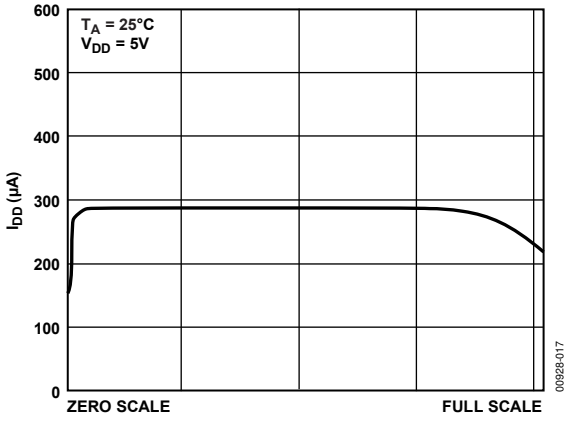


Figure 17. Supply Current vs. Code

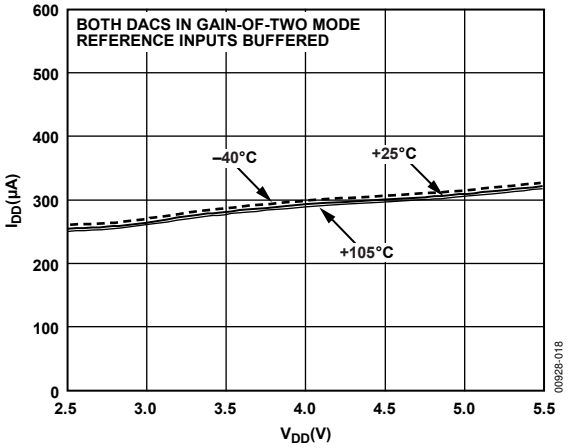


Figure 18. Supply Current vs. Supply Voltage

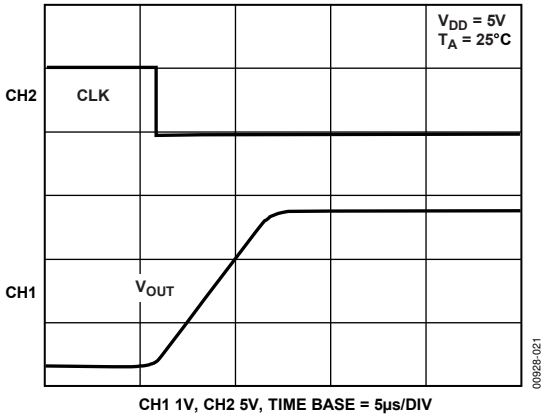


Figure 21. Half-Scale Setting (¼ to ¾ Scale Code Change)

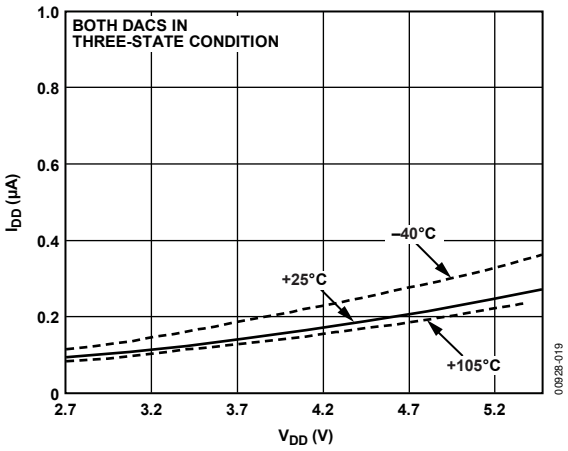


Figure 19. Power-Down Current vs. Supply Voltage

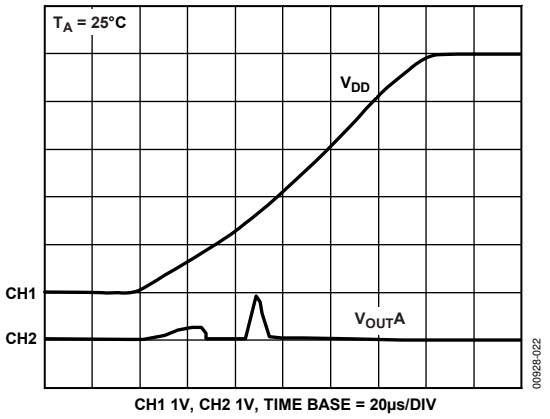


Figure 22. Power-On Reset to 0 V

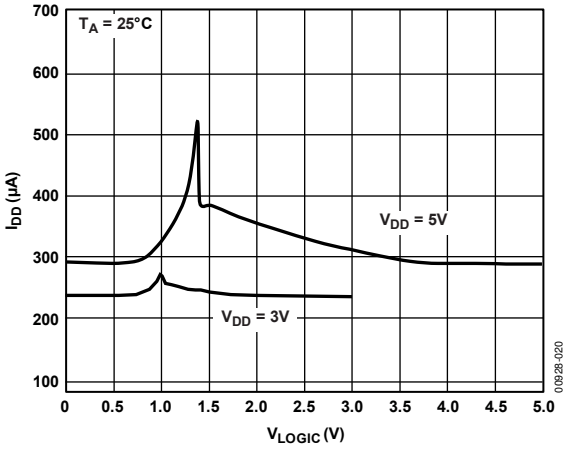


Figure 20. Supply vs. Logic Input Voltage

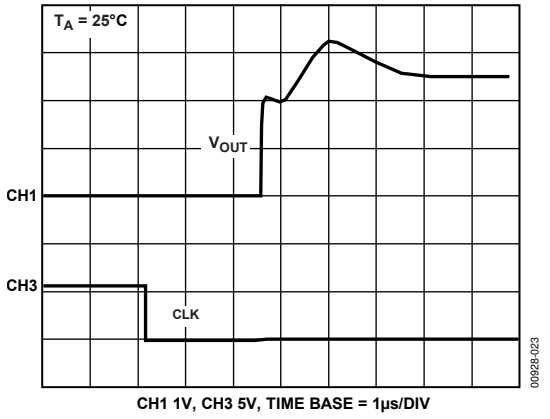


Figure 23. Existing Power-Down to Midscale

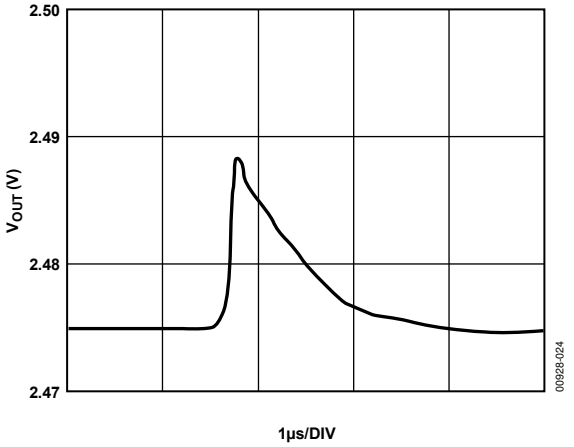


Figure 24. AD5322 Major-Code Transition

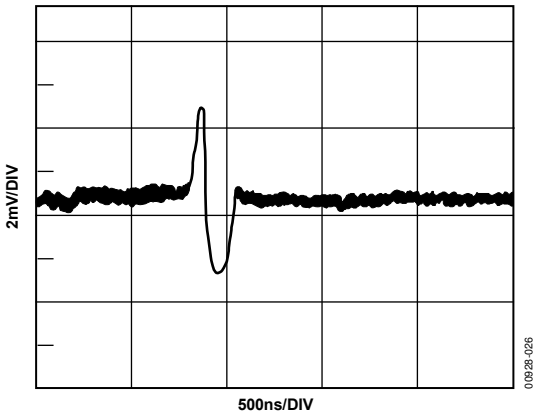


Figure 26. DAC-to-DAC Crosstalk

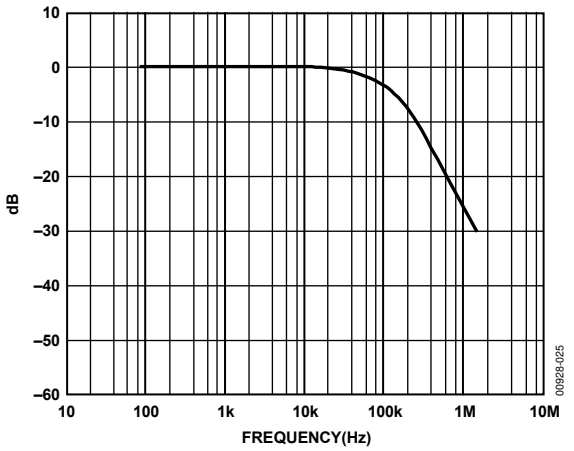


Figure 25. Multiplying Bandwidth (Small-Signal Frequency Response)

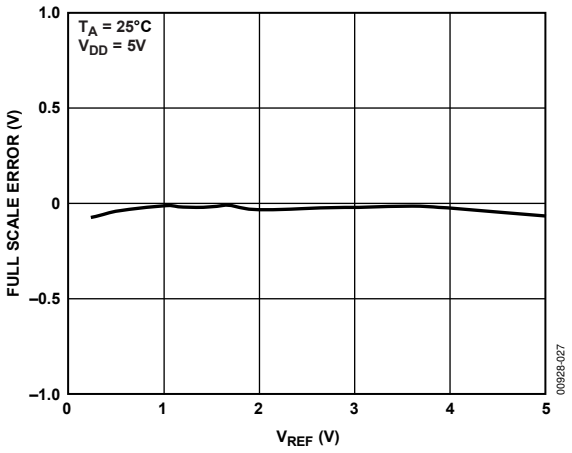


Figure 27. Full-Scale Error vs. V_{REF} (Buffered)

FUNCTIONAL DESCRIPTION

The AD5302/AD5312/AD5322 are dual resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. They contain reference buffers and output buffer amplifiers, and are written to via a 3-wire serial interface. They operate from single supplies of 2.5 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. Each DAC is provided with a separate reference input, which can be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from GND to V_{DD}. The devices have three programmable power-down modes, in which one or both DACs can be turned off completely with a high impedance output, or the output can be pulled low by an on-chip resistor.

DIGITAL-TO-ANALOG SECTION

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 28 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:

D = decimal equivalent of the binary code that is loaded to the DAC register:

0 to 255 for AD5302 (8 bits)
0 to 1023 for AD5312 (10 bits)
0 to 4095 for AD5322 (12 bits)

N = DAC resolution.

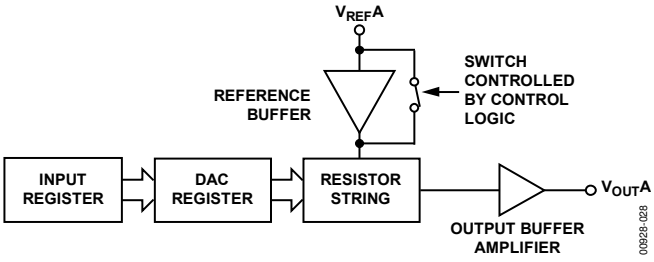


Figure 28. Single DAC Channel Architecture

RESISTOR STRING

The resistor-string section is shown in Figure 29. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

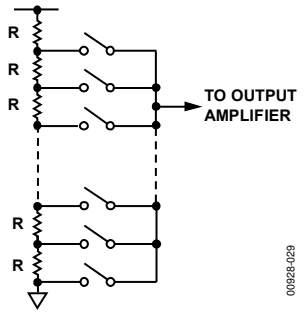


Figure 29. Resistor String

DAC REFERENCE INPUTS

There is a reference input pin for each of the two DACs. The reference inputs are buffered but can also be configured as unbuffered. The advantage of the buffered input is the high impedance it presents to the voltage source driving it.

However, if the unbuffered mode is used, the user can have a reference voltage as low as GND and as high as V_{DD} because there is no restriction due to headroom and footroom of the reference amplifier. If there is a buffered reference in the circuit (for example, REF192), there is no need to use the on-chip buffers of the AD5302/AD5312/AD5322. In unbuffered mode, the impedance is still large (180 kΩ per reference input).

The buffered/unbuffered option is controlled by the BUF bit in the control word (see the Serial Interface section for a description of the register contents).

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail, which gives an output range of 0.001 V to V_{DD} – 0.001 V when the reference is V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 500 pF to GND and V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 16.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at eight bits) of 6 µs. See Figure 21.

POWER-ON RESET

The AD5302/AD5312/AD5322 are provided with a power-on reset function to power them up in a defined state. The power-on state is

- Normal operation
- Reference inputs unbuffered
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

SERIAL INTERFACE

The AD5302/AD5312/AD5322 are controlled over a versatile, 3-wire serial interface, which operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 30 to Figure 32). Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 2. The 16-bit word consists of four control bits followed by 8, 10, or 12 bits of DAC data, depending on the device type. The first bit loaded is the MSB (Bit 15), which determines whether the data is for DAC A or DAC B. Bit 14 determines if the reference input is buffered or unbuffered. Bit 13 and Bit 12 control the operating mode of the DAC.

Table 6. Control Bits

Bit	Name	Function	Power-On Default
15	$\overline{A}$/B	0: Data Written to DAC A 1: Data Written to DAC B	N/A
14	BUF	0: Reference Is Unbuffered 1: Reference Is Buffered	0
13	PD1	Mode Bit	0
12	PD0	Mode Bit	0

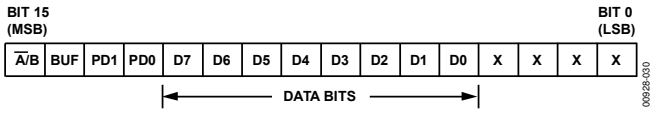


Figure 30. AD5302 Input Shift Register Contents

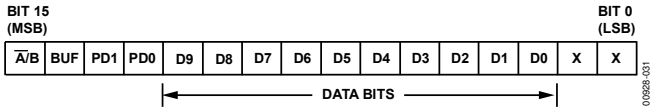


Figure 31. AD5312 Input Shift Register Contents

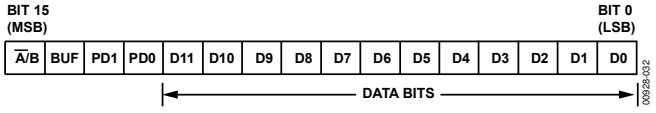


Figure 32. AD5322 Input Shift Register Contents

The remaining bits are DAC data bits, starting with the MSB and ending with the LSB. The AD5322 uses all 12 bits of DAC data, the AD5312 uses 10 bits and ignores the 2 LSB. The AD5302 uses eight bits and ignores the last four bits. The data format is straight binary, with all 0s corresponding to 0 V output, and all 1s corresponding to full-scale output (VREF – 1 LSB).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low observing the minimum $\overline{SYNC}$ to SCLK active edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. Any data and clock pulses after the 16th are ignored, and no further serial data transfers occur until $\overline{SYNC}$ is taken high and low again.

$\overline{SYNC}$ can be taken high after the falling edge of the 16th SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t_7.

After the end of serial data transfer, data is automatically transferred from the input shift register to the input register of the selected DAC. If $\overline{SYNC}$ is taken high before the 16th falling edge of SCLK, the data transfer is aborted and the input registers are not updated.

When data has been transferred into both input registers, the DAC registers of both DACs can be simultaneously updated by taking $\overline{LDAC}$ low.

LOW POWER SERIAL INTERFACE

To reduce the power consumption of the device even further, the interface only powers up fully when the device is being written to. As soon as the 16-bit control word has been written to the part, the SCLK and DIN input buffers are powered down. They only power up again following a falling edge of $\overline{SYNC}$.

DOUBLE-BUFFERED INTERFACE

The AD5302/AD5312/AD5322 DACs all have double-buffered interfaces consisting of two banks of registers—input registers and DAC registers. The input register is connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register can change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it.

This is useful if the user requires simultaneous updating of both DAC outputs. The user can write to both input registers individually and then, by pulsing the $\overline{LDAC}$ input low, both outputs update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5302/AD5312/AD5322, the part only updates the DAC register if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODES

The AD5302/AD5312/AD5322 have very low power consumption, dissipating only 0.7 mW with a 3 V supply and 1.5 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into one of three power-down modes, which are selected by Bit 13 and Bit 12 (PD1 and PD0) of the control word. Table 7 shows how the state of the bits corresponds to the mode of operation of that particular DAC.

Table 7. PD1/PD0 Operating Modes

PD1	PDO	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ Load to GND)
1	0	Power-Down (100 kΩ Load to GND)
1	1	Power-Down (High Impedance Output)

When both bits are set to 0, the DACs work normally with their normal power consumption of 300 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. There are three different options.

- The output is connected internally to GND through a 1 kΩ resistor,
- The output is connected internally to GND through a 100 kΩ resistor, or
- The output is left open-circuited (three-state).

The output stage is illustrated in Figure 33.

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs when V_{DD} = 3 V. See Figure 23 for a plot.

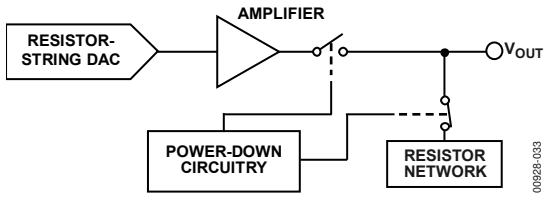


Figure 33. Output Stage During Power-Down

MICROPROCESSOR INTERFACING

AD5302/AD5312/AD5322 TO ADSP-2101/ADSP-2103 INTERFACE

Figure 34 shows a serial interface between the AD5302/AD5312/AD5322 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 sport is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. The data is clocked out on each falling edge of the DSP's serial clock and clocked into the AD5302/AD5312/AD5322 on the rising edge of the DSP's serial clock. This corresponds to the falling edge of the DAC's SCLK.

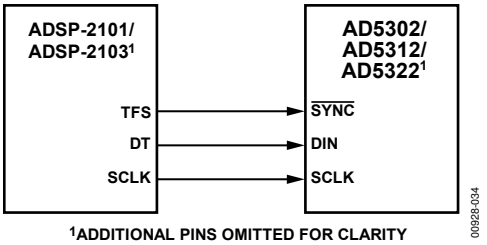


Figure 34. AD5302/AD5312/AD5322 to ADSP-2101/ADSP-2103 Interface

AD5302/AD5312/AD5322 TO 68HC11/68L11 INTERFACE

Figure 35 shows a serial interface between the AD5302/AD5312/AD5322 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5302/AD5312/AD5322, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit = 0 and its CPHA bit = 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 are configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/ 68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5302/AD5312/AD5322, PC7 is left low after the first eight bits are transferred and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

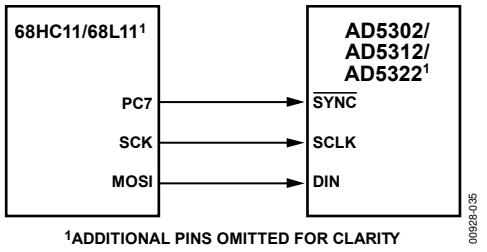


Figure 35. AD5302/AD5312/AD5322 to 68HC11/68L11 Interface

AD5302/AD5312/AD5322 TO 80C51/80L51 INTERFACE

Figure 36 shows a serial interface between the AD5302/AD5312/AD5322 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5302/AD5312/AD5322, while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5302/AD5312/AD5322, P3.3 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5302/AD5312/AD5322 require their data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

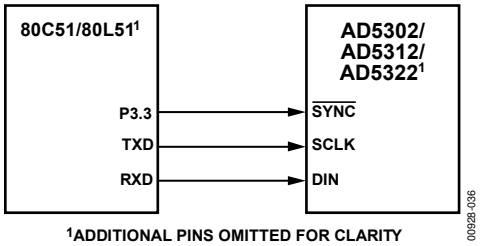


Figure 36. AD5302/AD5312/AD5322 to 80C51/80L51 Interface

AD5302/AD5312/AD5322 TO MICROWIRE INTERFACE

Figure 37 shows an interface between the AD5302/AD5312/AD5322 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5302/AD5312/AD5322 on the rising edge of the SK.

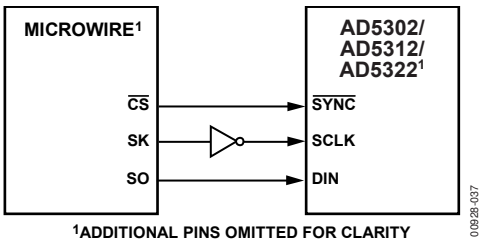


Figure 37. AD5302/AD5312/AD5322 to MICROWIRE Interface

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

The AD5302/AD5312/AD5322 can be used with a wide range of reference voltages, especially if the reference inputs are configured to be unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0 V to V_{DD}. More typically, the AD5302/AD5312/AD5322 can be used with a fixed, precision reference voltage. Figure 38 shows a typical setup for the AD5302/AD5312/AD5322 when using an external reference. If the reference inputs are unbuffered, the reference input range is from 0 V to V_{DD}, but if the on-chip reference buffers are used, the reference range is reduced. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference would be the REF191, a 2.048 V reference.

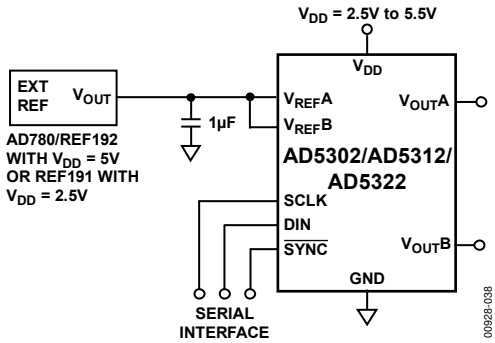


Figure 38. AD5302/AD5312/AD5322 Using External Reference

If an output range of 0 V to V_{DD} is required when the reference inputs are configured as unbuffered (for example, 0 V to 5 V), the simplest solution is to connect the reference inputs to V_{DD}. As this supply cannot be very accurate and can be noisy, the AD5302/AD5312/AD5322 can be powered from the reference voltage, for example, a 5 V reference such as the REF195, as shown in Figure 39. The REF195 outputs a steady supply voltage for the AD5302/AD5312/AD5322. The current required from the REF195 is 300 µA supply current and approximately 30 µA into each reference input. This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10 kΩ load on each output) is

$$360\ \mu A + 2\left(\frac{5\ V}{10\ k\Omega}\right) = 1.36\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.7 ppm (13.5 µV) for the 1.36 mA current drawn from it. This corresponds to a 0.0007 LSB error at eight bits and a 0.011 LSB error at 12 bits.

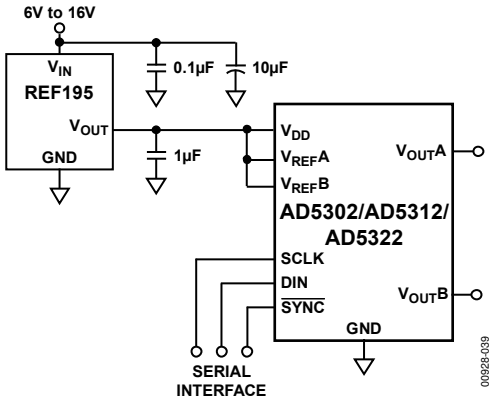


Figure 39. Using a REF195 as Power and Reference to the AD5302/AD5312/AD5322

BIPOLAR OPERATION USING THE AD5302/AD5312/AD5322

The AD5302/AD5312/AD5322 are designed for single-supply operation, but bipolar operation is also achievable using the circuit shown in Figure 40. This circuit is configured to achieve an output voltage range of –5 V < V_{OUT} < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

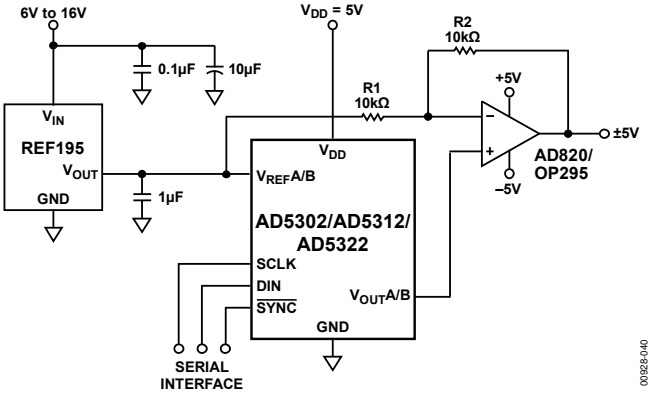


Figure 40. Bipolar Operation Using the AD5302/AD5312/AD5322

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = \left[\frac{\left(V_{REF} \times D / 2^N\right) \times (R1 + R2)}{R1}\right] - V_{REF} \times (R2 / R1)$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
V_{REF} is the reference voltage input.

If V_{REF} = 5 V, *R*1 = *R*2 = 1 kΩ, and V_{DD} = 5 V:

$$V_{OUT} = \left(10 \times D / 2^N\right) - 5\ V$$

OPTO-ISOLATED INTERFACE FOR PROCESS CONTROL APPLICATIONS

Each AD5302/AD5312/AD5322 has a versatile 3-wire serial interface, making them ideal for generating accurate voltages in process control and industrial applications. Due to noise, safety requirements, or distance, it can be necessary to isolate the AD5302/AD5312/AD5322 from the controller. This can easily be achieved by using opto-isolators, which provide isolation in excess of 3 kV. The serial loading structure of the AD5302/AD5312/AD5322 makes them ideally suited for use in opto-isolated applications. Figure 41 shows an opto-isolated interface to the AD5302/AD5312/AD5322 where DIN, SCLK, and $\overline{\text{SYNC}}$ are driven from opto-couplers. The power supply to the part also needs to be isolated by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5302/AD5312/AD5322.

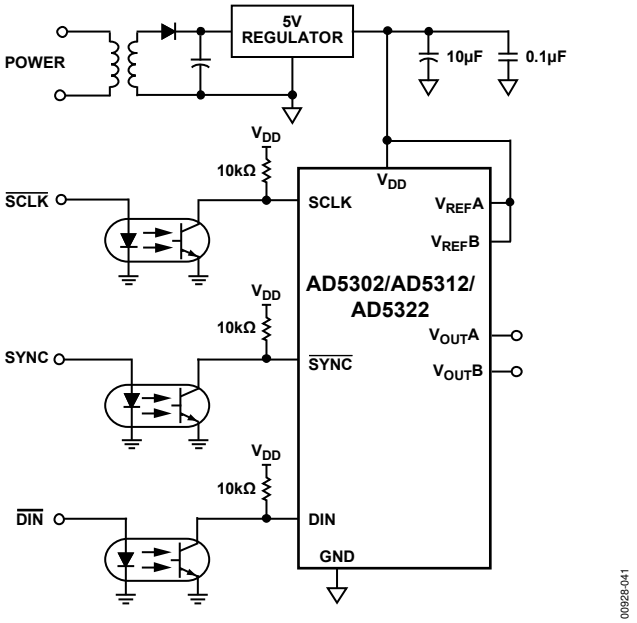


Figure 41. AD5302/AD5312/AD5322 in an Opto-Isolated Interface

DECODING MULTIPLE AD5302/AD5312/AD5322s

The $\overline{\text{SYNC}}$ pin on the AD5302/AD5312/AD5322 can be used in applications to decode a number of DACs. In this application, all the DACs in the system receive the same serial clock and serial data, but only the $\overline{\text{SYNC}}$ to one of the devices is active at any one time, allowing access to two channels in this eight-channel system.

The 74HC139 is used as a 2-to-4 line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 42 shows a diagram of a typical setup for decoding multiple AD5302/AD5312/AD5322 devices in a system.

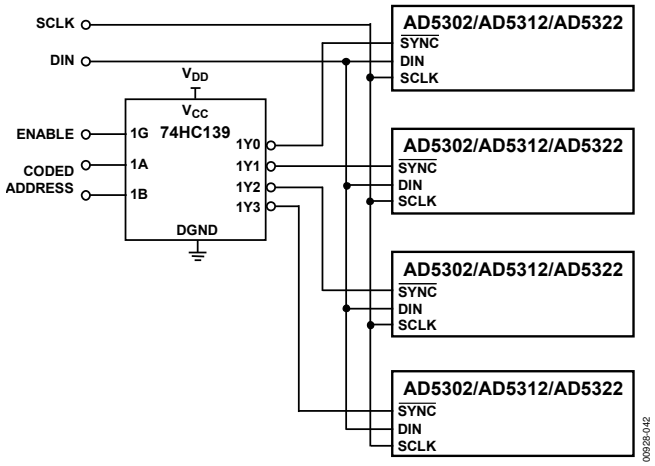


Figure 42. Decoding Multiple AD5302/AD5312/AD5322 Devices in a System

AD5302/AD5312/AD5322 AS A DIGITALLY PROGRAMMABLE WINDOW DETECTOR

Figure 43 shows a digitally programmable upper-/lower-limit detector using the two DACs in the AD5302/AD5312/AD5322. The upper and lower limits for the test are loaded to DAC A and DAC B, which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, an LED indicates the fail condition.

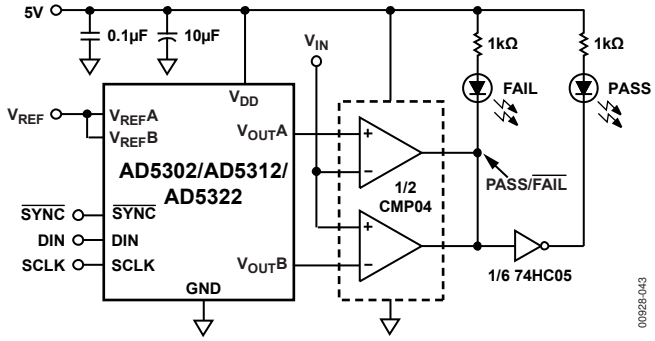


Figure 43. Window Detector Using AD5302/AD5312/AD5322

COARSE AND FINE ADJUSTMENT USING THE AD5302/AD5312/AD5322

The DACs in the AD5302/AD5312/AD5322 can be paired together to form a coarse and fine adjustment function, as shown in Figure 44. DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 changes the relative effect of the coarse and fine adjustments. With the resistor values and external reference shown, the output amplifier has unity gain for the DAC A output, so the output range is 0 V to 2.5 V − 1 LSB. For DAC B, the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range equal to 19 mV.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} can be used. The op amps indicated allow a rail-to-rail output swing.

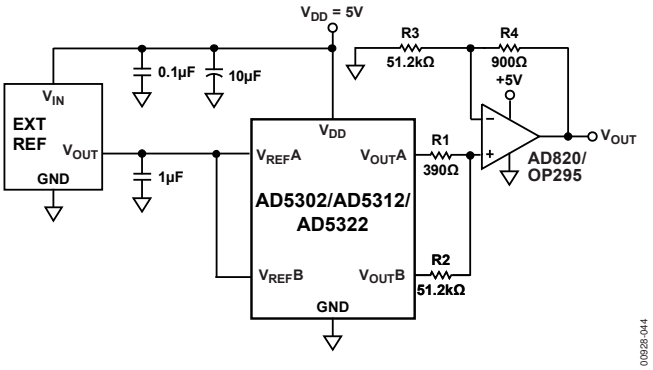


Figure 44. Coarse/Fine Adjustment

POWER SUPPLY BYPASSING AND GROUNDING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5302/AD5312/AD5322 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5302/AD5312/AD5322 are in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the AD5302/AD5312/AD5322. The part should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close as possible to the package, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), similar to the common ceramic types that provide a low impedance path to ground at high frequencies that handle transient currents due to internal logic switching.

The power supply lines of the AD5302/AD5312/AD5322 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

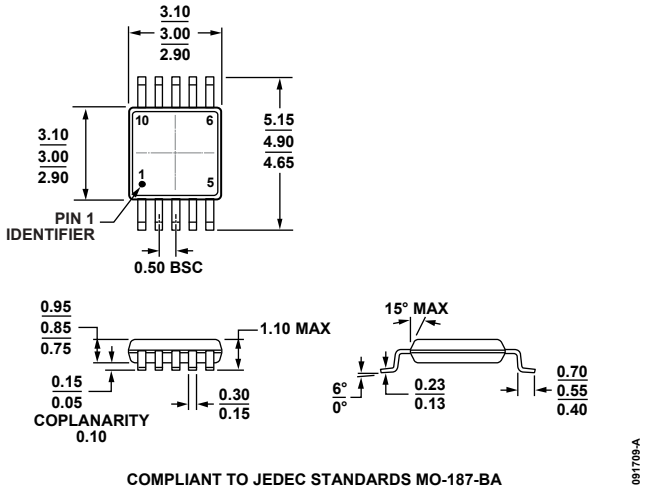


Figure 45. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
AD5302ARM	−40°C to +105°C	10-Lead MSOP	RM-10	D5A
AD5302ARM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D5A
AD5302ARMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D5A#
AD5302ARMZ-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D5A#
AD5302ARMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D5A#
AD5302BRM	−40°C to +105°C	10-Lead MSOP	RM-10	D5B
AD5302BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D5B
AD5302BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D5B
AD5302BRMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D5B#
AD5302BRMZ-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D5B#
AD5302BRMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D5B#
AD5312ARM	−40°C to +105°C	10-Lead MSOP	RM-10	D6A
AD5312ARMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D6A#
AD5312ARMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D6A#
AD5312BRM	−40°C to +105°C	10-Lead MSOP	RM-10	D6B
AD5312BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D6B
AD5312BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D6B
AD5312BRMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D6B#
AD5312BRMZ-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D6B#
AD5312BRMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D6B#
AD5322ARM	−40°C to +105°C	10-Lead MSOP	RM-10	D7A
AD5322ARM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D7A
AD5322ARMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D6T
AD5322ARMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D6T
AD5322BRM	−40°C to +105°C	10-Lead MSOP	RM-10	D7B
AD5322BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D7B
AD5322BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D7B
AD5322BRMZ	−40°C to +105°C	10-Lead MSOP	RM-10	D7B#
AD5322BRMZ-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	D7B#
AD5322BRMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D7B#
AD5312WARMZ-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	D6A#

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD5312WARMZ-REEL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability report for this model.

NOTES

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