Dual 8-/10-/12-Bit, High Bandwidth, Multiplying DACs with Serial Interface

Data Sheet

AD5429/AD5439/AD5449

FEATURES

10 MHz multiplying bandwidth
INL of ±0.25 LSB at 8 bits
16-lead TSSOP package
2.5 V to 5.5 V supply operation
±10 V reference input
50 MHz serial interface
2.47 MSPS update rate
Extended temperature range: −40°C to +125°C
4-quadrant multiplication
Power-on reset
0.5 µA typical current consumption
Guaranteed monotonic
Daisy-chain mode
Readback function

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation applications
Programmable amplifiers and attenuators
Digitally controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5429/AD5439/AD5449[1] are CMOS, 8-, 10-, and 12-bit, dual-channel, current output digital-to-analog converters (DAC), respectively. These devices operate from a 2.5 V to 5.5 V power supply, making them suited to battery-powered and other applications.

As a result of being manufactured on a CMOS submicron process, these parts offer excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (RFB) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

These DACs use a double-buffered, 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE™, and most DSP interface standards. In addition, a serial data out (SDO) pin allows daisy-chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with 0s, and the DAC outputs are at zero scale.

The AD5429/AD5439/AD5449 DACs are available in 16-lead TSSOP packages. The EV-AD5415/49SDZ evaluation board is available for evaluating DAC performance. For more information, see the UG-297 evaluation board user guide.

FUNCTIONAL BLOCK DIAGRAM

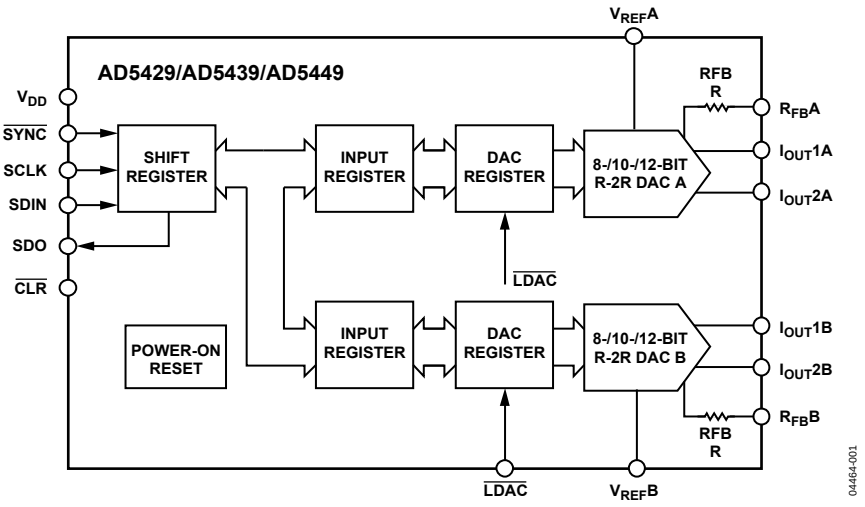


Figure 1.

[1] U.S. Patent Number 5,689,257.

Rev. F Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2004–2016 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Timing Characteristics ... 5
Timing Diagrams ... 5
Absolute Maximum Ratings ... 7
ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Typical Performance Characteristics ... 9
Terminology ... 14
Theory of Operation ... 15
Digital-to-Analog Converter ... 15
Circuit Operation ... 15
Single-Supply Applications ... 17
Adding Gain ... 18
Divider or Programmable Gain Element ... 18
Reference Selection ... 19
Amplifier Selection ... 19
Serial Interface ... 20
Microprocessor Interfacing ... 22
PCB Layout and Power Supply Decoupling ... 24
Overview of Multiplying DAC Devices ... 25
Outline Dimensions ... 26
Ordering Guide ... 26

REVISION HISTORY

1/16—Rev. E to Rev. F

Changed AD54xx to AD5429/AD5439/AD5449 ... Throughout
Changed ADSP-21xx to ADSP-2191M and Family ... Throughout
Changed ADSP-2101/ADSP-2103/ADSP-2191 to ADSP-2191M ... Throughout
Changed ADSP-BF5xx to ADSP-BF534 ... Throughout
Deleted Positive Output Voltage Section and Figure 41; Renumbered Sequentially ... 17
Changes to Adding Gain Section ... 18
Changed Overview of AD54xx Devices Section to Overview of Multiplying DAC Devices Section ... 26

5/13—Rev. D to Rev. E

Changes to General Description ... 1
Changes to Ordering Guide ... 26

6/11—Rev. C to Rev. D

Changes to General Description ... 1
Deleted Evaluation Board for the DAC Section ... 24
Changes to Ordering Guide ... 30

4/10—Rev. B to Rev. C

Added to Figure 4 ... 6

3/08—Rev. A to Rev. B

Added t_{13} and t_{14} Parameters to Table 2 ... 5
Changes to Figure 2 ... 5
Changes to Figure 3 ... 6
Changes to Figure 38 ... 16
Changes to Ordering Guide ... 30

7/05—Rev. 0 to Rev. A

Changes to Features List ... 1
Changes to Specifications ... 3
Changes to Timing Characteristics ... 5
Changes to Absolute Maximum Ratings Section ... 7
Changes to General Description Section ... 15
Changes to Table 5 ... 15
Changes to Table 6 ... 16
Changes to Single-Supply Applications Section ... 17
Changes to Divider or Programmable Gain Element Section ... 18
Changes to Table 7 Through Table 10 ... 20
Added ADSP-BF5xx-to-AD5429/AD5439/AD5449 Interface Section ... 23
Change to PCB Layout and Power Supply Decoupling Section ... 25
Changes to Power Supplies for the Evaluation Board Section ... 25
Changes to Table 13 ... 29
Updated Outline Dimensions ... 30
Changes to Ordering Guide ... 30

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. Temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance is measured with the OP177, and ac performance is measured with the AD8038, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
AD5429					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5439					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5449					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±25	mV	
Gain Error Temperature Coefficient		±5		ppm FSR/°C	
Output Leakage Current			±5	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±15	nA	Data = 0x0000, $I_{OUT}1$
REFERENCE INPUT					
Reference Input Range		±10		V	
$V_{REF}A$, $V_{REF}B$ Input Resistance	9	11	13	kΩ	Input resistance temperature coefficient = −50 ppm/°C
$V_{REF}A$-to-$V_{REF}B$ Input Resistance Mismatch		1.6	2.5	%	Typical = 25°C, maximum = 125°C
Input Capacitance					
Code 0		3.5		pF	
Code 4095		3.5		pF	
DIGITAL INPUTS/OUTPUT					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 3.6 V to 5.5 V
	1.7			V	V_{DD} = 2.5 V to 3.6 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5.5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5.5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE					
Reference-Multiplying Bandwidth		10		MHz	V_{REF} = ±3.5 V p-p, DAC loaded all 1s
Output Voltage Settling Time					R_{LOAD} = 100 Ω, C_{LOAD} = 15 pF, V_{REF} = 10 V, DAC latch alternately loaded with 0s and 1s
Measured to ±1 mV of FS		80	120	ns	
Measured to ±4 mV of FS		35	70	ns	
Measured to ±16 mV of FS		30	60	ns	
Digital Delay		20	40	ns	
Digital-to-Analog Glitch Impulse		3		nV-sec	1 LSB change around major carry, V_{REF} = 0 V

Parameter[1]	Min	Typ	Max	Unit	Conditions
Multiplying Feedthrough Error					DAC latches loaded with all 0s, V_{REF} = ±3.5 V
			70	dB	1 MHz
			48	dB	10 MHz
Output Capacitance		12	17	pF	DAC latches loaded with all 0s
		25	30	pF	DAC latches loaded with all 1s
Digital Feedthrough		3	5	nV-sec	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz
Analog THD		81		dB	V_{REF} = 3. 5 V p-p, all 1s loaded, f = 1 kHz
Digital THD					Clock = 10 MHz, V_{REF} = 3.5 V
100 kHz f_{OUT}		61		dB	
50 kHz f_{OUT}		66		dB	
SFDR Performance (Wide Band)					AD5449, 65k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					AD5449, 65k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50 kHz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					AD5449, 65k codes, V_{REF} = 3.5 V
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	Clock = 10 MHz
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	Clock = 25 MHz
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.7	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.5	10	µA	T_A = −40°C to +125°C, logic inputs = 0 V or V_{DD}
Power Supply Sensitivity			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V, temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments[2]
f_{SCLK}	50	MHz max	Maximum clock frequency
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	5	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_8	30	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{10}	12	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{12}[3]	25	ns min	SCLK active edge to SDO valid, strong SDO driver
	60	ns min	SCLK active edge to SDO valid, weak SDO driver
t_{13}	12	ns min	$\overline{CLR}$ pulse width
t_{14}	4.5	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
Update Rate	2.47	MSPS	Consists of cycle time, $\overline{SYNC}$ high time, data setup, and output voltage settling time

[1] Guaranteed by design and characterization, not subject to production test.
[2] Falling or rising edge as determined by the control bits of the serial word. Strong or weak SDO driver selected via the control register.
[3] Daisy-chain and readback modes cannot operate at maximum clock frequency. SDO timing specifications are measured with a load circuit, as shown in Figure 5.

TIMING DIAGRAMS

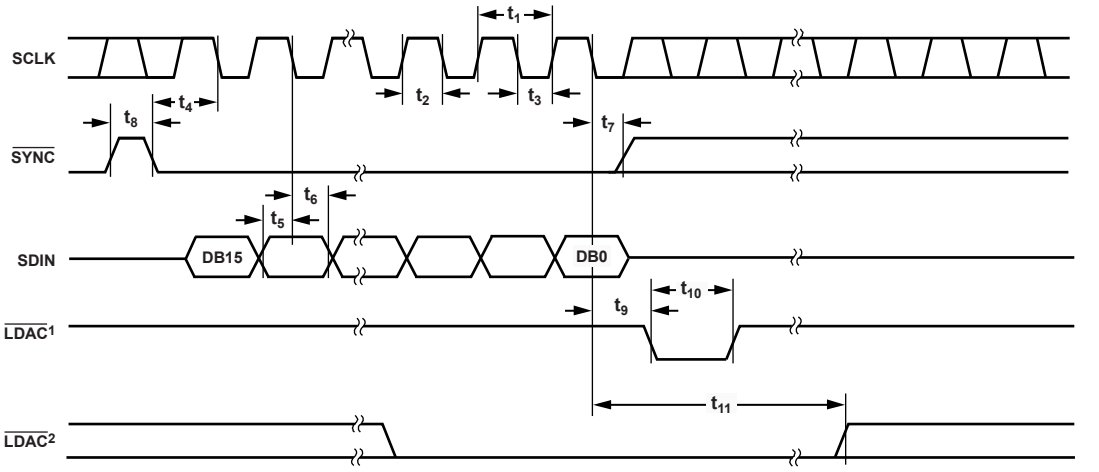
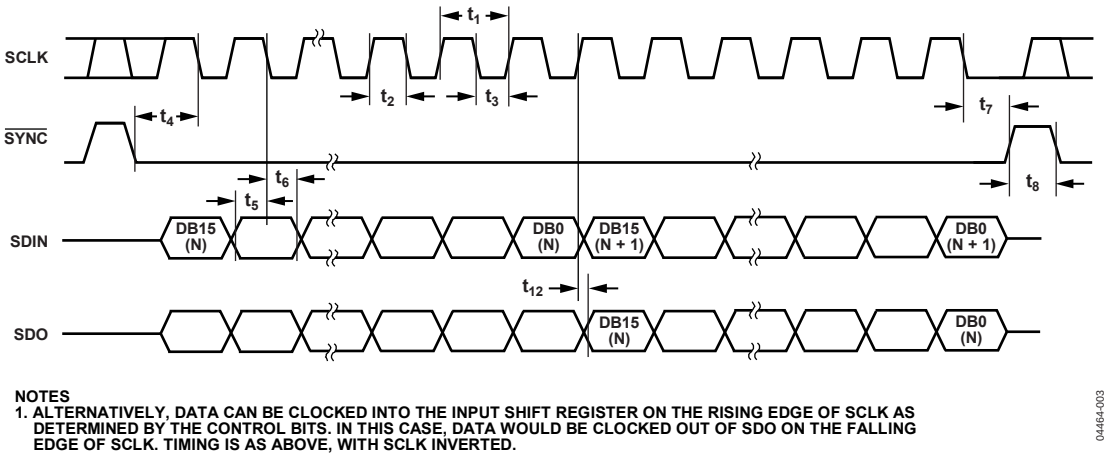


Figure 2. Standalone Mode Timing Diagram



NOTES
1. ALTERNATIVELY, DATA CAN BE CLOCKED INTO THE INPUT SHIFT REGISTER ON THE RISING EDGE OF SCLK AS DETERMINED BY THE CONTROL BITS. IN THIS CASE, DATA WOULD BE CLOCKED OUT OF SDO ON THE FALLING EDGE OF SCLK. TIMING IS AS ABOVE, WITH SCLK INVERTED.

Figure 3. Daisy-Chain Timing Diagram

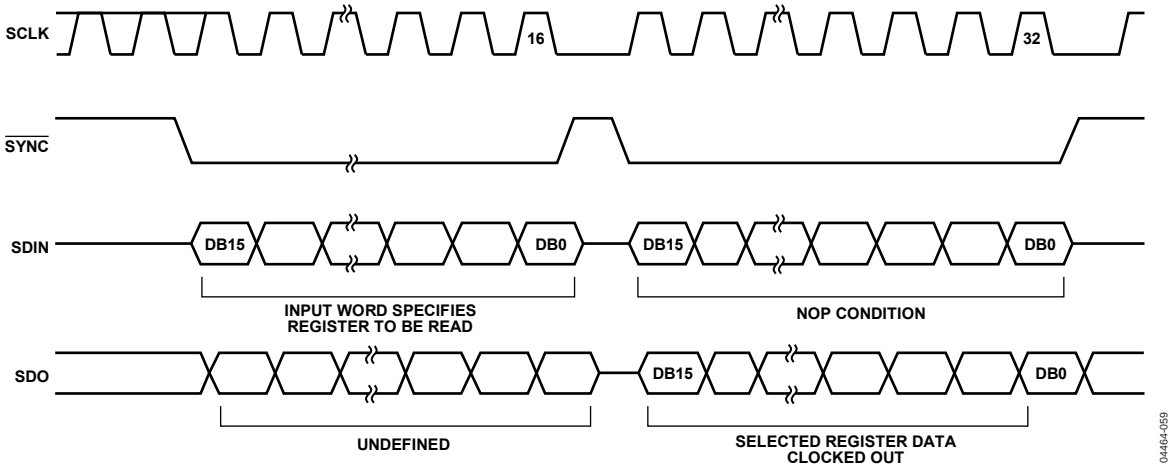


Figure 4. Readback Mode Timing Diagram

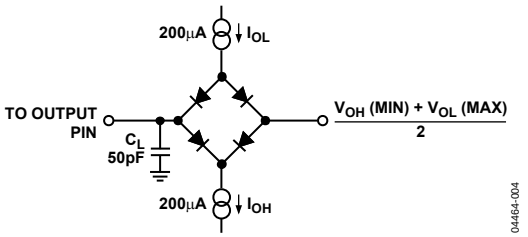


Figure 5. Load Circuit for SDO Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.
T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
$V_{REF}x$, $R_{FB}x$ to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to +7 V
Input Current to Any Pin Except Supplies	±10 mA
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance	150°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at SCLK, $\overline{SYNC}$, and SDIN are clamped by internal diodes.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

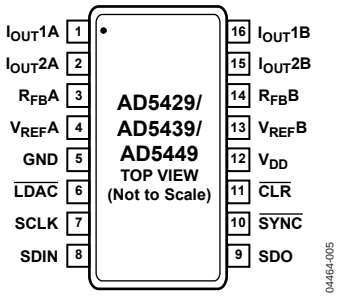


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$I_{OUT}1A$	DAC A Current Output.
2	$I_{OUT}2A$	DAC A Analog Ground. This pin should typically be tied to the analog ground of the system, but it can be biased to achieve single-supply operation.
3	$R_{FB}A$	DAC Feedback Resistor Pin. This pin establishes voltage output for the DAC by connecting to an external amplifier output.
4	$V_{REF}A$	DAC A Reference Voltage Input Pin.
5	GND	Ground Pin.
6	$\overline{LDAC}$	Load DAC Input. This pin allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected, whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of $\overline{SYNC}$ when in daisy-chain mode.
7	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device can be configured such that data is clocked into the shift register on the rising edge of SCLK.
8	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, data is clocked at power-on into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to a rising edge.
9	SDO	Serial Data Output. This pin allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and clocked out via SDO on the rising edge of SCLK. Data is always clocked out on the alternate edge to loading data to the shift register. Writing the readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, and they are clocked out on the next 16 opposite clock edges to the active clock edge.
10	$\overline{SYNC}$	Active Low Control Input. This pin provides the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded into the shift register on the active edge of the subsequent clocks. In standalone mode, the serial interface counts the clocks, and data is latched into the shift register on the 16th active clock edge.
11	$\overline{CLR}$	Active Low Control Input. This pin clears the DAC output, input, and DAC registers. Configuration mode allows the user to enable the hardware $\overline{CLR}$ pin as a clear-to-zero scale or midscale, as required.
12	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
13	$V_{REF}B$	DAC B Reference Voltage Input Pin.
14	$R_{FB}B$	DAC B Feedback Resistor Pin. This pin establishes voltage output for the DAC by connecting to an external amplifier output.
15	$I_{OUT}2B$	DAC B Analog Ground. This pin typically should be tied to the analog ground of the system, but it can be biased to achieve single-supply operation.
16	$I_{OUT}1B$	DAC B Current Output.

TYPICAL PERFORMANCE CHARACTERISTICS

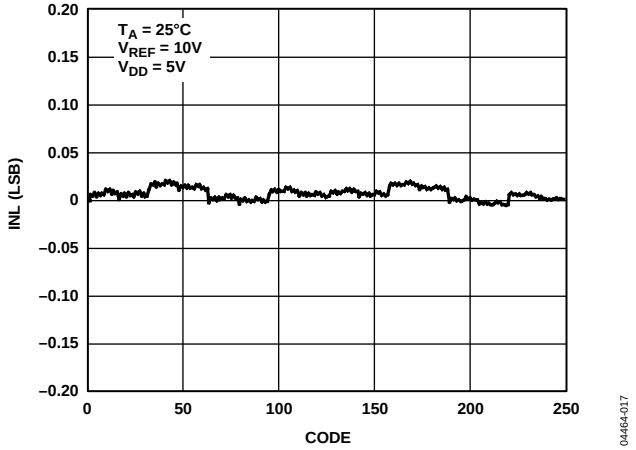


Figure 7. INL vs. Code (8-Bit DAC)

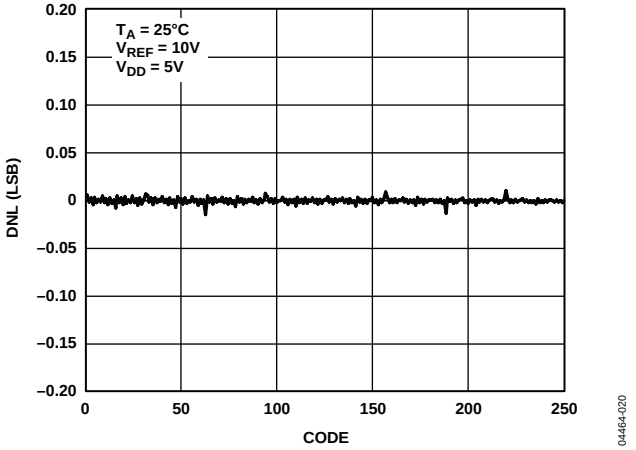


Figure 10. DNL vs. Code (8-Bit DAC)

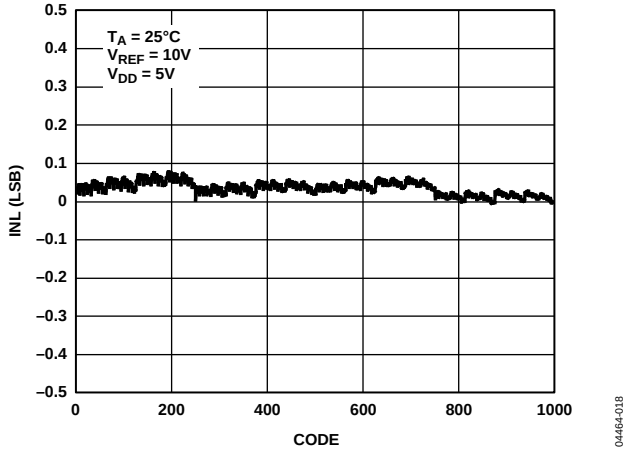


Figure 8. INL vs. Code (10-Bit DAC)

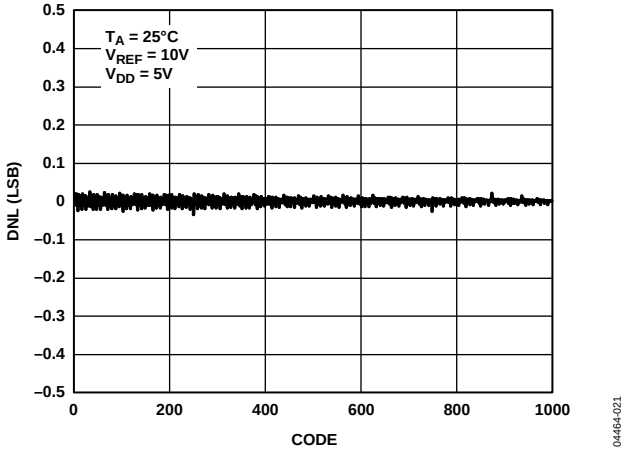


Figure 11. DNL vs. Code (10-Bit DAC)

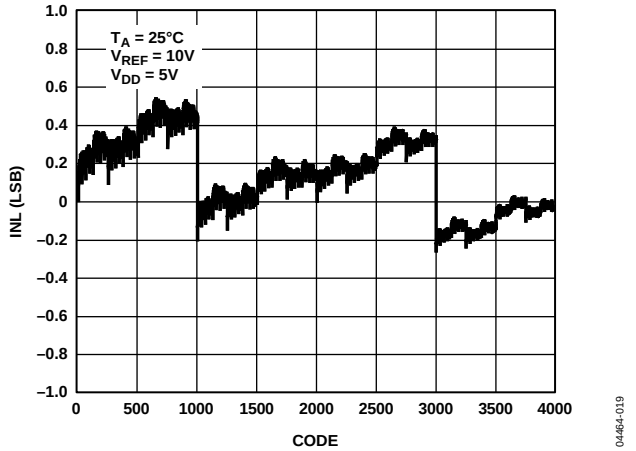


Figure 9. INL vs. Code (12-Bit DAC)

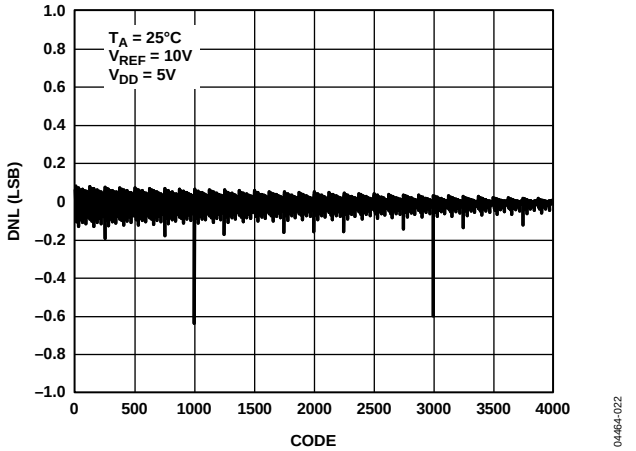


Figure 12. DNL vs. Code (12-Bit DAC)

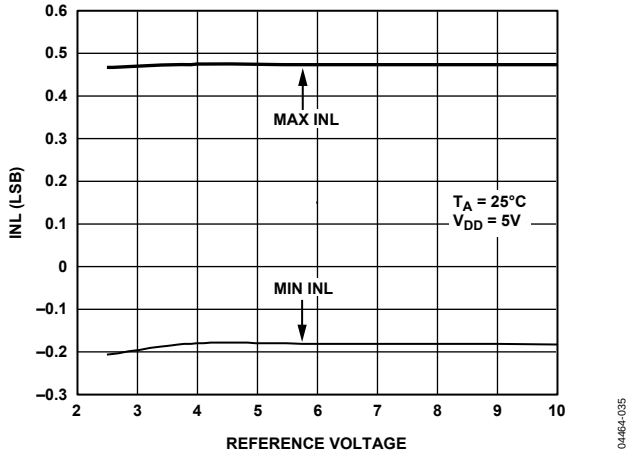


Figure 13. INL vs. Reference Voltage

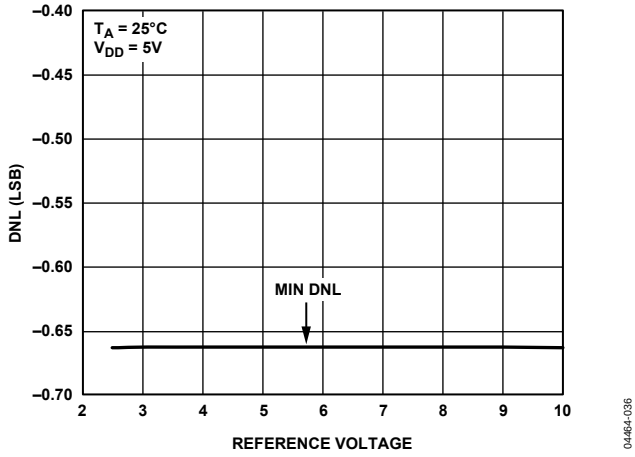


Figure 14. DNL vs. Reference Voltage

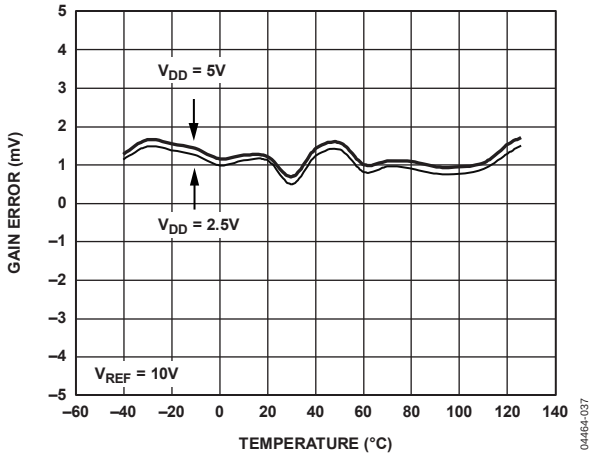


Figure 15. Gain Error vs. Temperature

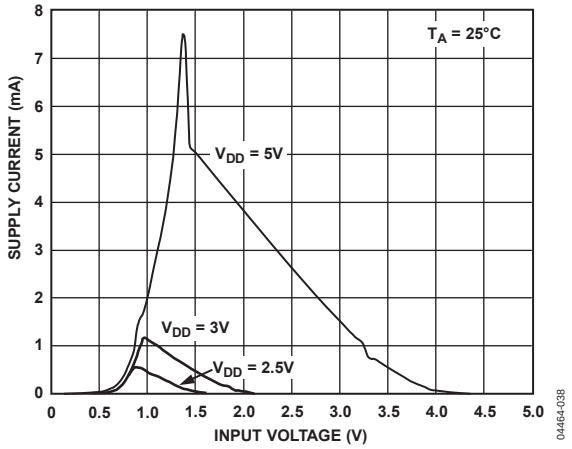


Figure 16. Supply Current vs. Logic Input Voltage

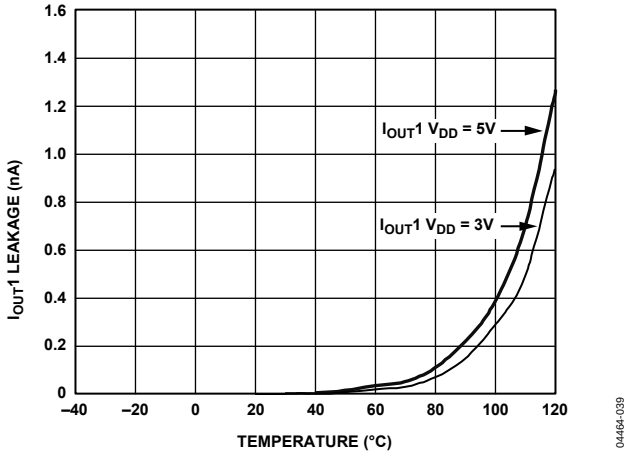


Figure 17. I_{OUT}1 Leakage Current vs. Temperature

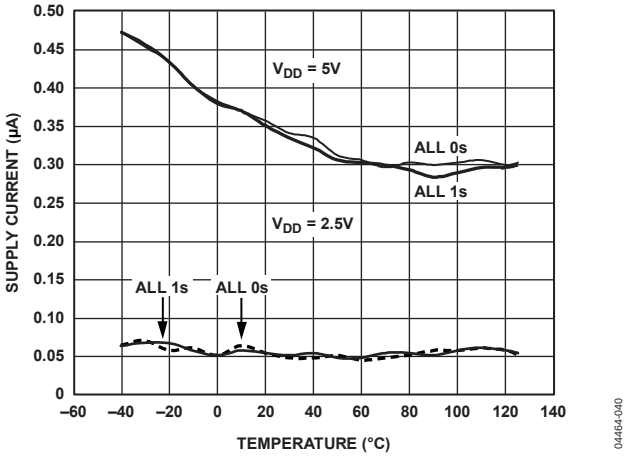


Figure 18. Supply Current vs. Temperature

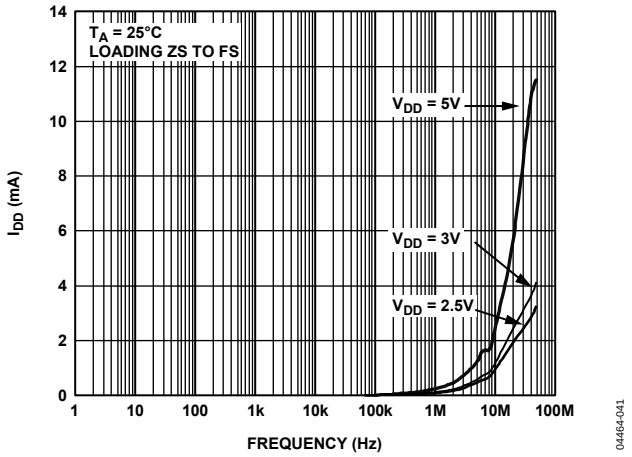


Figure 19. Supply Current vs. Update Rate

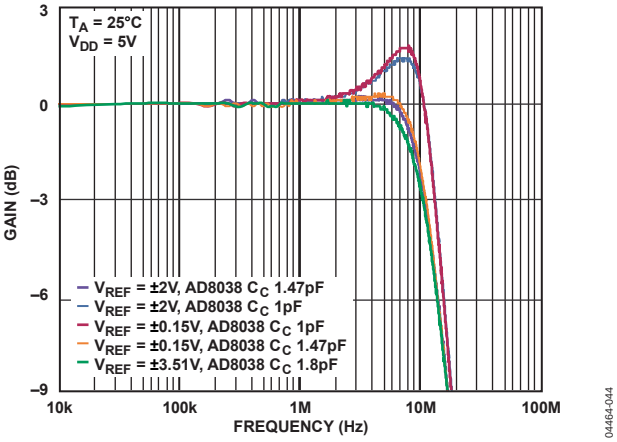


Figure 22. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

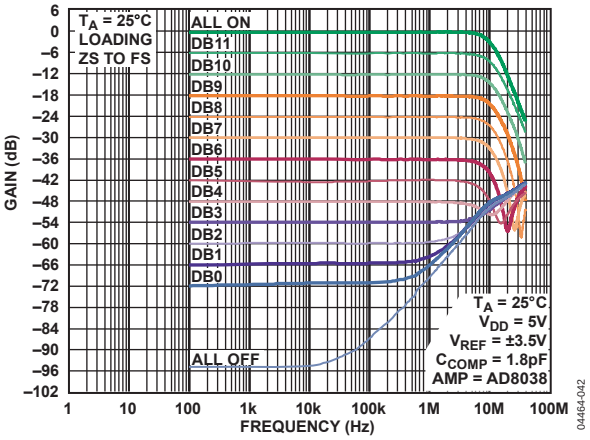


Figure 20. Reference Multiplying Bandwidth vs. Frequency and Code

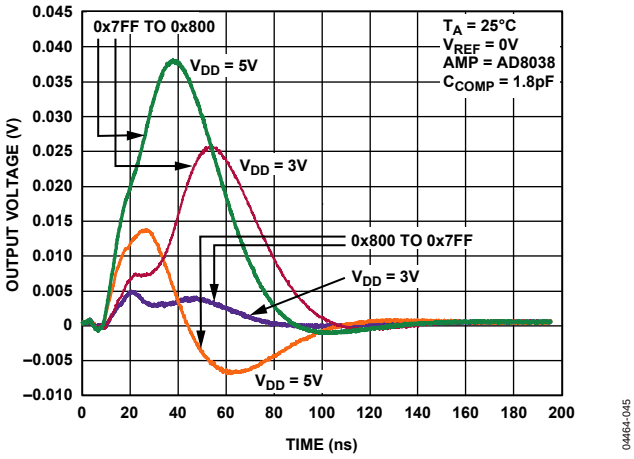


Figure 23. Midscale Transition, V_{REF} = 0 V

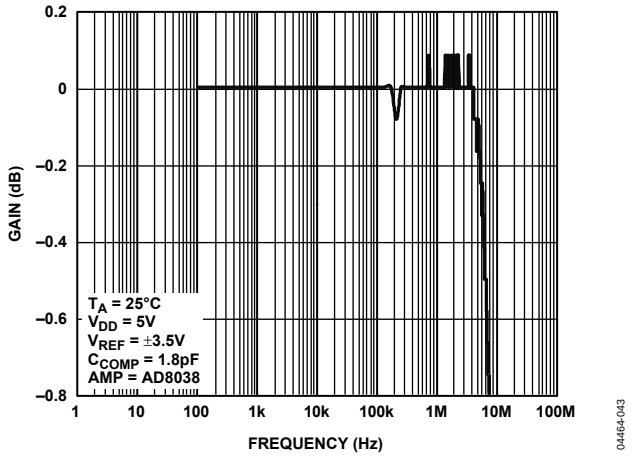


Figure 21. Reference Multiplying Bandwidth—All 1s Loaded

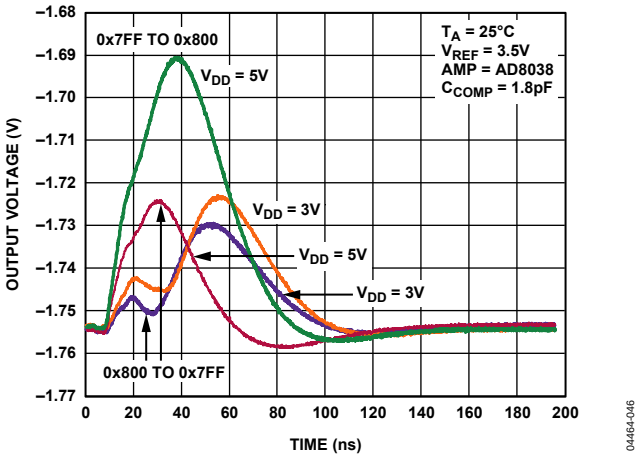


Figure 24. Midscale Transition, V_{REF} = 3.5 V

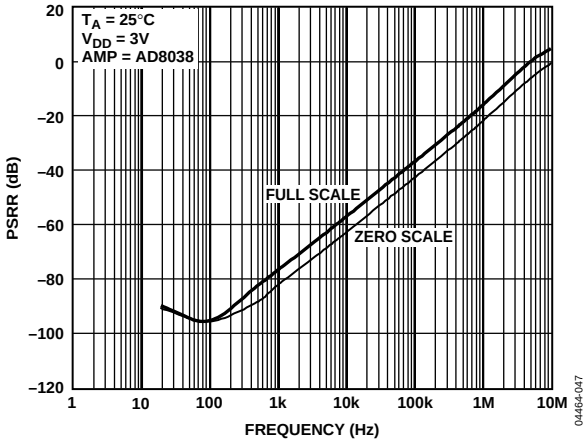


Figure 25. Power Supply Rejection Ratio vs. Frequency

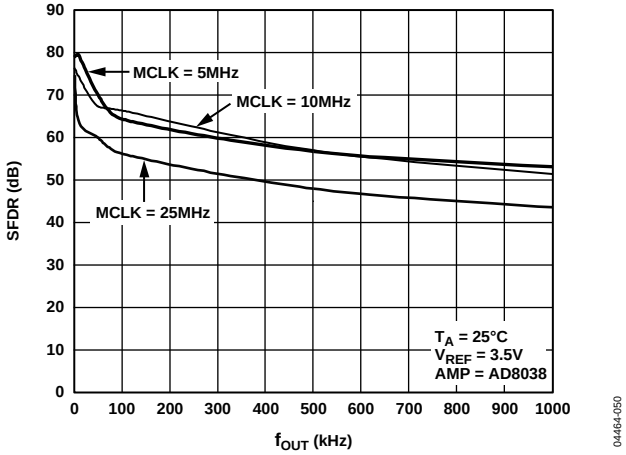


Figure 28. Wideband SFDR vs. f_{OUT} Frequency

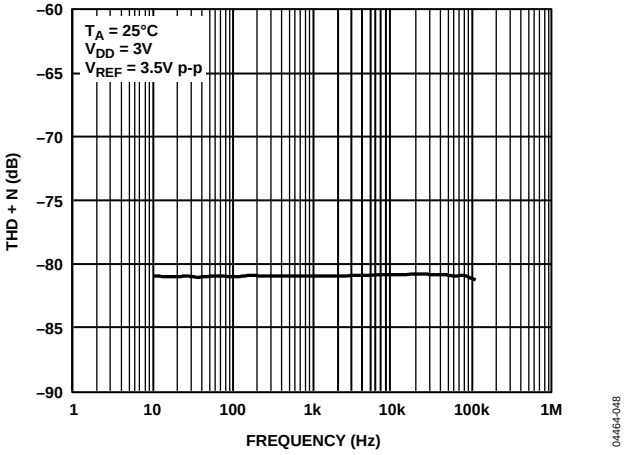


Figure 26. THD + Noise vs. Frequency

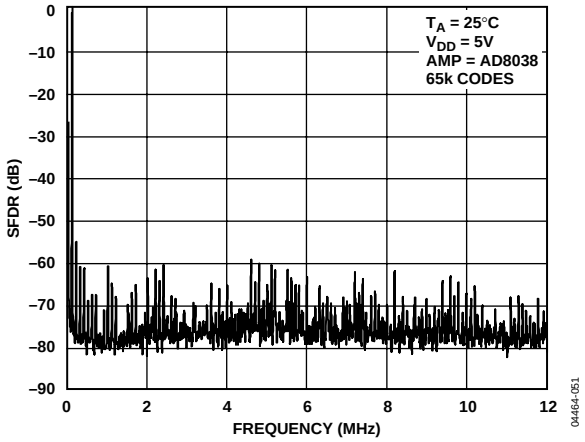


Figure 29. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

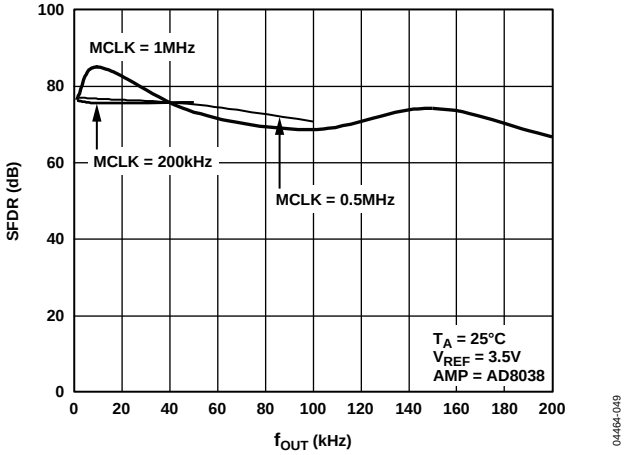


Figure 27. Wideband SFDR vs. f_{OUT} Frequency

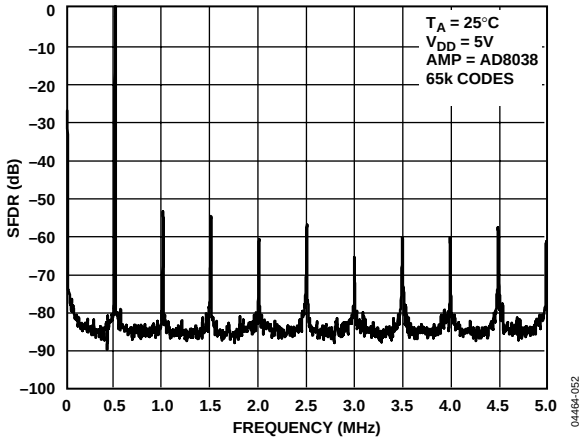


Figure 30. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz

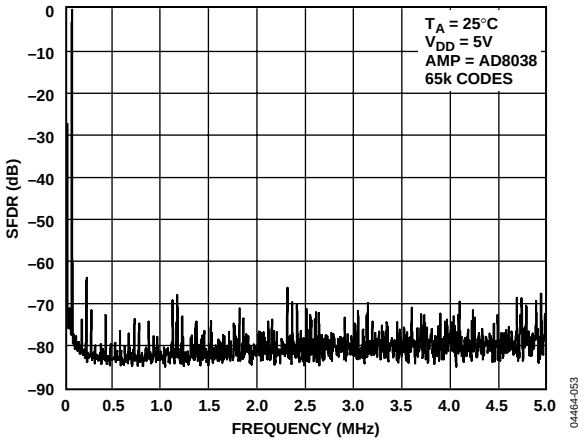


Figure 31. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz

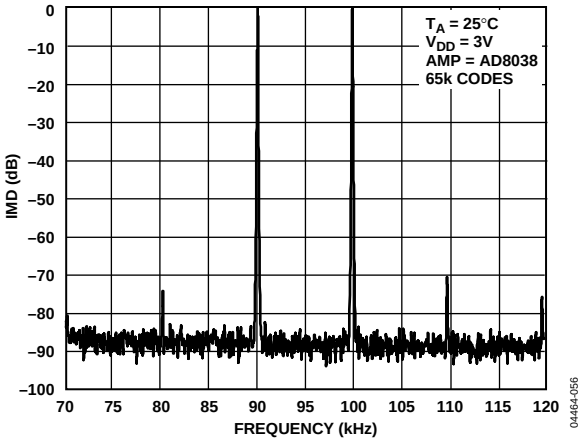


Figure 34. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz

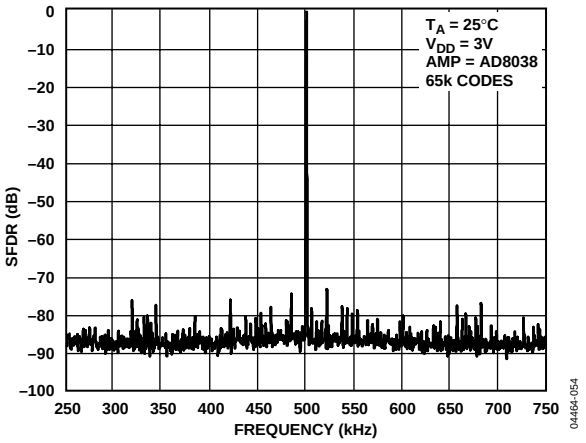


Figure 32. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz

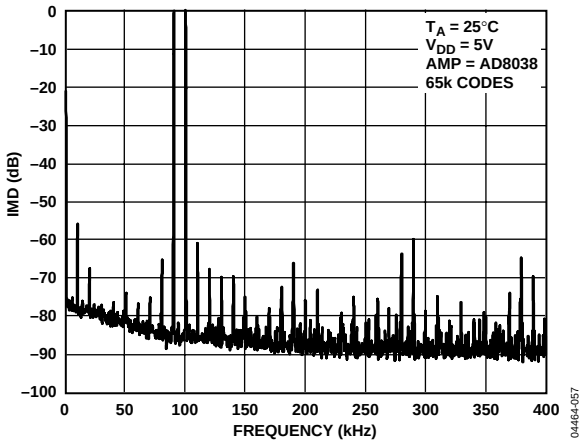


Figure 35. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz

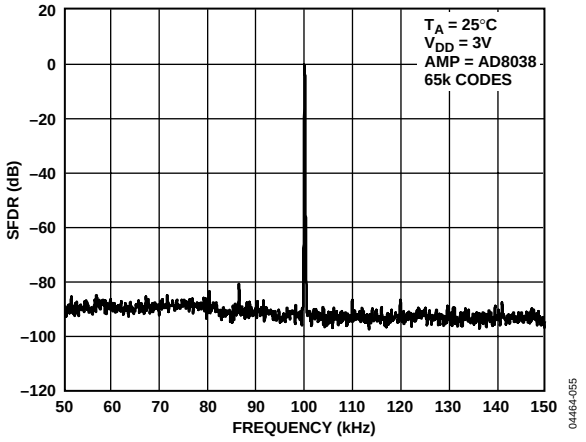


Figure 33. Narrow-Band SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

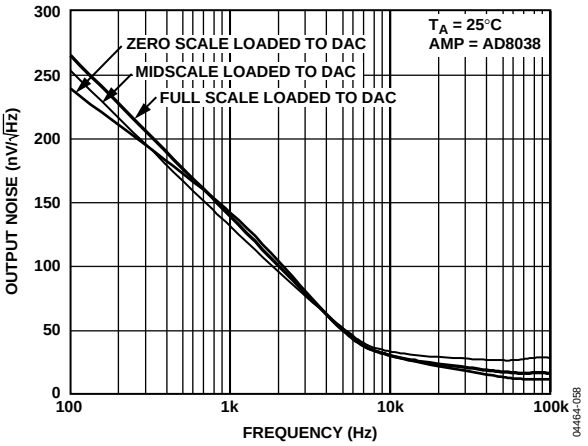


Figure 36. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy (Endpoint Nonlinearity)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is typically expressed in LSBs or as a percentage of the full-scale reading.

Differential Nonlinearity
The difference in the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of –1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error (Full-Scale Error)
A measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. The gain error of the DACs is adjustable to zero with an external resistance.

Output Leakage Current
The current that flows into the DAC ladder switches when they are turned off. For the $I_{OUT}1x$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows into the $I_{OUT}2x$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
The amount of time for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-sec or nV-sec, depending on whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the digital inputs of the device is capacitively coupled through the device and produces noise on the I_{OUT} pins and, subsequently, on the circuitry that follows. This noise is digital feedthrough.

Multiplying Feedthrough Error
The error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1x$ terminal when all 0s are loaded to the DAC.

Digital Crosstalk
The glitch impulse transferred to the outputs of one DAC in response to a full-scale code change (all 0s to all 1s, or vice versa) in the input register of the other DAC. It is expressed in nV-sec.

Analog Crosstalk
The glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s, or vice versa) while keeping $\overline{LDAC}$ high and then pulsing $\overline{LDAC}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-sec.

Channel-to-Channel Isolation
The portion of input signal from the reference input of a DAC that appears at the output of another DAC. It is expressed in dB.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as the second to fifth harmonics.

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

Intermodulation Distortion (IMD)
The DAC is driven by two combined sine wave references of Frequency fa and Frequency fb. Distortion products are produced at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 … Intermodulation terms are those for which m or n is not equal to 0. The second-order terms include (fa + fb) and (fa − fb), and the third-order terms are (2fa + fb), (2fa − fb), (f + 2fa + 2fb), and (fa − 2fb). IMD is defined as

$$IMD = 20 \log \frac{RMS\ Sum\ of\ the\ Sum\ and\ Diff\ Distortion\ Products}{RMS\ Amplitude\ of\ the\ Fundamental}$$

Compliance Voltage Range

The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5429/AD5439/AD5449 are 8-, 10-, and 12-bit, dual-channel, current output DACs consisting of a standard inverting R-2R ladder configuration. Figure 37 shows a simplified diagram for a single channel of the AD5449. The feedback resistor, $R_{FB}A$, has a value of R. The value of R is typically 10 kΩ (with a minimum of 8 kΩ and a maximum of 12 kΩ). If $I_{OUT}1A$ and $I_{OUT}2A$ are kept at the same potential, a constant current flows into each ladder leg, regardless of digital input code. Therefore, the input resistance presented at $V_{REF}A$ is always constant.

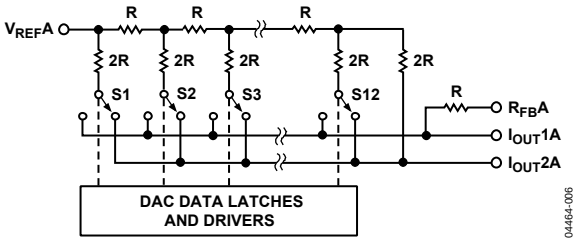


Figure 37. Simplified Ladder

Access is provided to the $V_{REF}x$, $R_{FB}x$, $I_{OUT}1x$, and $I_{OUT}2x$ terminals of the DACs, making the devices extremely versatile and allowing them to be configured in several operating modes, such as unipolar mode, bipolar output mode, or single-supply mode.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 38.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times D/2^n$$

where:

D is the fractional representation of the digital word loaded to the DAC.

D = 0 to 255 (AD5429)
= 0 to 1023 (AD5439)
= 0 to 4095 (AD5449)

n is the number of bits.

With a fixed 10 V reference, the circuit shown in Figure 38 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between digital code and the expected output voltage for unipolar operation using the 8-bit AD5429 DAC.

Table 5. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

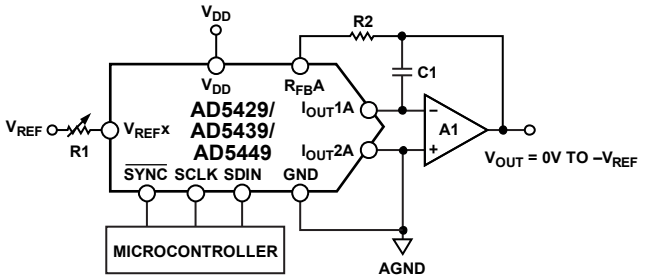


Figure 38. Unipolar Operation

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can easily be accomplished by using another external amplifier and three external resistors, as shown in Figure 39.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. When connected in bipolar mode, the output voltage is

$$V_{OUT} = \left(V_{REF} \times D / 2^{n-1}\right) - V_{REF}$$

where:
D is the fractional representation of the digital word loaded to the DAC.

D = 0 to 255 (AD5429)
= 0 to 1023 (AD5439)
= 0 to 4095 (AD5449)

n is the number of bits.

Table 6 shows the relationship between digital code and the expected output voltage for bipolar operation with the AD5429.

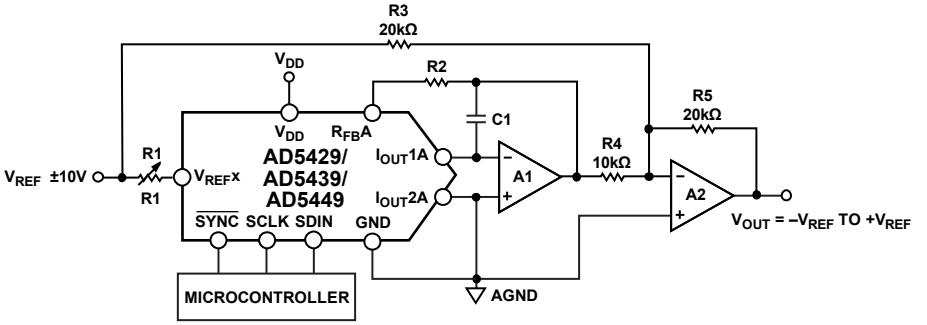
Table 6. Bipolar Code

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (255/256)
1000 0000	0
0000 0001	$-V_{REF}$ (255/256)
0000 0000	$-V_{REF}$ (256/256)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as closely as possible, and proper PCB layout techniques must be used. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in the closed-loop applications circuit.

As shown in Figure 38 and Figure 39, an optional compensation capacitor, C1, can be added in parallel with $R_{FB}x$ for stability. Too small a value of C1 can produce ringing at the output, whereas too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.



NOTES
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR V_{OUT} = 0V WITH CODE 10000000 LOADED TO DAC.
2. MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R3 AND R4.
3. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER.
4. DAC B AND ADDITIONAL PINS OMITTED FOR CLARITY.

04464-008

Figure 39. Bipolar Operation

SINGLE-SUPPLY APPLICATIONS

Voltage-Switching Mode

Figure 40 shows the DACs operating in voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1A$ pin; $I_{OUT}2A$ is connected to AGND; and the output voltage is available at the $V_{REF}A$ terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Therefore, an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance; instead, it sees one that varies with code. Therefore, the voltage input should be driven from a low impedance source.

Note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V, or an internal diode turns on, causing the device to exceed the maximum ratings. In this type of application, the full range of multiplying capability of the DAC is lost.

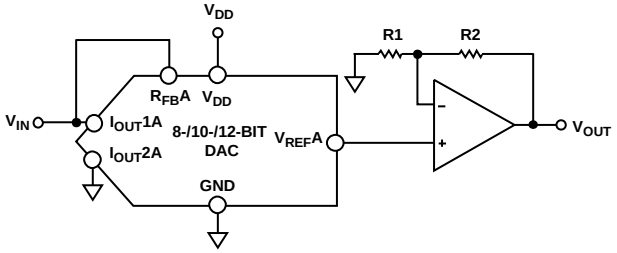


Figure 40. Single-Supply Voltage-Switching Mode

ADDING GAIN

In applications in which the output voltage must be greater than V_{IN}, gain can be added with an additional external amplifier, or it can be achieved in a single stage. Consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the RFB resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit in Figure 41 shows the recommended method of increasing the gain of the circuit. R1, R2, and R3 should have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits in which gains of greater than 1 are required. Note that R_{FB} >> R2||R3 and a gain error percentage of 100 × (R2||R3)/R_{FB} must be taken into consideration.

DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB}A is used as the input resistor, as shown in Figure 42, the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$, the output voltage is

$$V_{OUT} = -V_{IN} / D = -V_{IN} / \left(1 - 2^{-n}\right)$$

As D is reduced, the output voltage increases. For small values of the Digital Fraction D, it is important to ensure that the amplifier does not saturate and the required accuracy is met. For example, an 8-bit DAC driven with binary code of 0x10 (0001 0000)—that is, 16 decimal—in the circuit of Figure 42 should cause the output voltage to be 16 × V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB, D can have a weight in the range of 15.5/256 to 16.5/256, so that the possible output voltage is in the range of 15.5 V_{IN} to 16.5 V_{IN}. This range represents an error of 3%, even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction, D, of the current into the V_{REF}x terminal is routed to the I_{OUT}1 terminal, the output voltage changes as follows:

Output Error Voltage Due to DAC Leakage = (Leakage × R)/D

where *R* is the DAC resistance at the V_{REF}x terminal.

For a DAC leakage current of 10 nA, R = 10 kΩ, and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

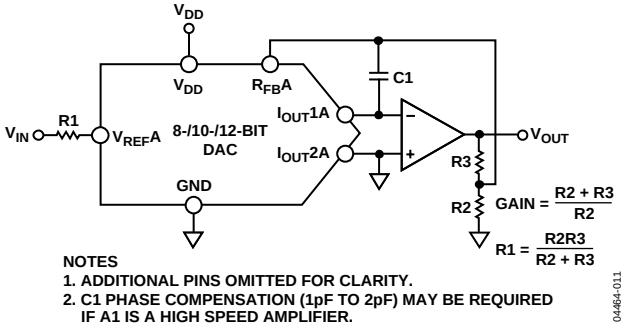


Figure 41. Increasing Gain of Current Output DAC

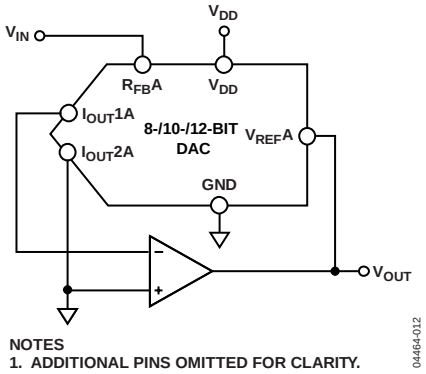


Figure 42. Current-Steering DAC Used as a Divider or Programmable Gain Element

REFERENCE SELECTION

When selecting a reference for use with the AD5429/AD5439/AD5449 series of current output DACs, pay attention to the reference output voltage temperature coefficient specification. This parameter affects not only the full-scale error, but it can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range of 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with a low output temperature coefficient, this error source can be minimized. Table 7 lists some references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, RFB. Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 8-, 10-, and 12-bit resolution.

If the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which, in turn, requires an amplifier that can handle rail-to-rail signals. Analog Devices offers a wide range of single-supply amplifiers (see Table 8 and Table 9).

Table 7. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC
ADR01	10	0.05	9	1	20	TSOT, SC70
ADR02	5	0.06	3	1	10	SOIC
ADR02	5	0.06	9	1	10	TSOT, SC70
ADR03	2.5	0.10	3	1	6	SOIC
ADR03	2.5	0.10	9	1	6	TSOT, SC70
ADR06	3	0.10	3	1	10	SOIC
ADR06	3	0.10	9	1	10	TSOT, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC
ADR435	5	0.04	3	0.8	8	SOIC
ADR391	2.5	0.16	9	0.12	5	TSOT
ADR395	5	0.10	9	0.12	8	TSOT

Table 8. Suitable Analog Devices Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC

Table 9. Suitable Analog Devices High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1500	6000	SOIC, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1000	10,500	SOIC, MSOP
AD8038	3 to 12	350	425	3000	750	SOIC, SC70
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC

SERIAL INTERFACE

The AD5429/AD5439/AD5449 have an easy-to-use, 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and most DSP interface standards. Data is written to the device in 16-bit words. Each 16-bit word consists of four control bits and eight, 10, or 12 data bits, as shown in Figure 43 through Figure 45.

Low Power Serial Interface

To minimize the power consumption of the device, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$. The SCLK and SDIN input buffers are powered down on the rising edge of $\overline{\text{SYNC}}$.

DAC Control Bit C3 to Control Bit C0

Control Bit C3 to Control Bit C0 allow control of various functions of the DAC, as shown in Table 11. The default settings of the DAC at power-on are such that data is clocked into the shift register on falling clock edges and daisy-chain mode is enabled. The device powers on with a zero-scale load to the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features at power-on. For example, daisy-chaining can be disabled if not in use, an active clock edge can be changed to a rising edge, and DAC output can be cleared to either zero scale or midscale. The user can also initiate a readback of the DAC register contents for verification.

Control Register (Control Bits = 1101)

While maintaining software compatibility with single-channel current output DACs (AD5426/AD5432/AD5443), these DACs also feature additional interface functionality. Set the control bits to 1101 to enter control register mode. Figure 46 shows the contents of the control register, the functions of which are described in the following sections.

SDO Control (SDO1 and SDO2)

The SDO bits enable the user to control the SDO output driver strength, disable the SDO output, or configure it as an open-drain driver. The strength of the SDO driver affects the timing of t_{12}, and, when stronger, allows a faster clock cycle.

Table 10. SDO Control Bits

SDO2	SDO1	Function Implemented
0	0	Full SDO driver
0	1	Weak SDO driver
1	0	SDO configured as open drain
1	1	Disable SDO output

Daisy-Chain Control (DSY)

DSY allows the enabling or disabling of daisy-chain mode. A 1 enables daisy-chain mode; a 0 disables daisy-chain mode. When disabled, a readback request is accepted; SDO is automatically enabled; the DAC register contents of the relevant DAC are clocked out on SDO; and, when complete, SDO is disabled again.

Hardware $\overline{\text{CLR}}$ Bit (HCLR)

The default setting for the hardware $\overline{\text{CLR}}$ bit is to clear the registers and DAC output to zero code. A 1 in the HCLR bit allows the $\overline{\text{CLR}}$ pin to clear the DAC outputs to midscale, and a 0 clears to zero scale.

Active Clock Edge (SCLK)

The default active clock edge is a falling edge. Write a 1 to this bit to clock data in on the rising edge, or a 0 to clock it in on the falling edge.

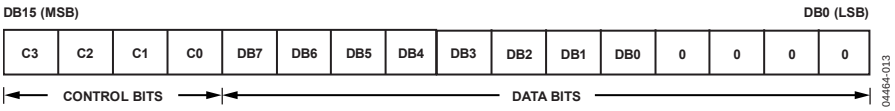


Figure 43. AD5429 8-Bit Input Shift Register Contents

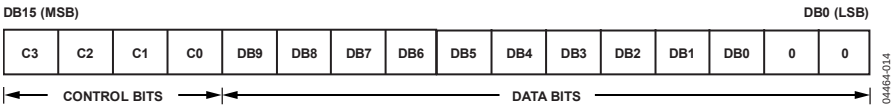


Figure 44. AD5439 10-Bit Input Shift Register Contents

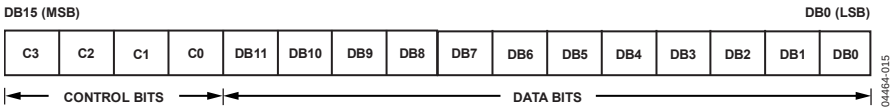


Figure 45. AD5449 12-Bit Input Shift Register Contents



Figure 46. Control Register Loading Sequence

$\overline{\text{SYNC}}$ Function

$\overline{\text{SYNC}}$ is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low, observing the minimum $\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time, t_4.

Daisy-Chain Mode

Daisy-chain mode is the default power-on mode. To disable the daisy-chain function, write 1001 to the control word. In daisy-chain mode, the internal gating on SCLK is disabled. SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK (this is the default; use the control word to change the active edge) and is valid for the next device on the falling edge of SCLK (default). By connecting this line to the SDIN input on the next device in the chain, a multidevice interface is constructed. For each device in the system, 16 clock pulses are required. Therefore, the total number of clock cycles must equal 16*n,* where *n* is the total number of devices in the chain. See Figure 4.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents additional data from being clocked into the input shift register. A burst clock containing the exact number of clock cycles can be used, after which $\overline{\text{SYNC}}$ can be taken high. After the rising edge of $\overline{\text{SYNC}}$, data is automatically transferred from the input shift register of each device to the addressed DAC.

When control bits = 0000, the device is in no operation mode. This may be useful in daisy-chain applications in which the user does not want to change the settings of a particular DAC in the chain. Write 0000 to the control bits for that DAC; subsequent data bits are ignored.

Standalone Mode

After power-on, write 1001 to the control word to disable daisy-chain mode. The first falling edge of $\overline{\text{SYNC}}$ resets the serial clock counter to ensure that the correct number of bits are shifted in and out of the serial shift registers. A $\overline{\text{SYNC}}$ edge during the 16-bit write cycle causes the device to abort the current write cycle.

After the falling edge of the 16th SCLK pulse, data is automatically transferred from the input shift register to the DAC. For another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

$\overline{\text{LDAC}}$ Function

The $\overline{\text{LDAC}}$ function allows asynchronous and synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected, whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of $\overline{\text{SYNC}}$ when the device is in daisy-chain mode.

Software $\overline{\text{LDAC}}$ Function

Load-and-update mode can also serve as a software update function, irrespective of the voltage level on the $\overline{\text{LDAC}}$ pin.

Table 11. DAC Control Bits

C3	C2	C1	C0	DAC	Function Implemented
0	0	0	0	A and B	No operation (power-on default)
0	0	0	1	A	Load and update
0	0	1	0	A	Initiate readback
0	0	1	1	A	Load input register
0	1	0	0	B	Load and update
0	1	0	1	B	Initiate readback
0	1	1	0	B	Load input register
0	1	1	1	A and B	Update DAC outputs
1	0	0	0	A and B	Load input registers
1	0	0	1	N/A	Disable daisy-chain
1	0	1	0	N/A	Clock data to shift register on rising edge
1	0	1	1	N/A	Clear DAC output to zero scale
1	1	0	0	N/A	Clear DAC output to midscale
1	1	0	1	N/A	Control word
1	1	1	0	N/A	Reserved
1	1	1	1	N/A	No operation

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5429/AD5439/AD5449 DACs is through a serial bus that uses standard protocol and is compatible with microcontrollers and DSP processors. The communication channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5429/AD5439/AD5449 require a 16-bit word, with the default being data valid on the falling edge of SCLK; however, this is changeable using the control bits in the data-word.

ADSP-2191M and Family-to-AD5429/AD5439/AD5449 Interface

The ADSP-2191M family of DSPs is easily interfaced to an AD5429/AD5439/AD5449 DAC without the need for extra glue logic. Figure 47 is an example of a serial peripheral interface (SPI) between the DAC and the ADSP-2191M. The MOSI (master output, slave input) pin of the DSP drives the serial data line, SDIN. SYNC is driven from a port line, in this case SPIxSEL.

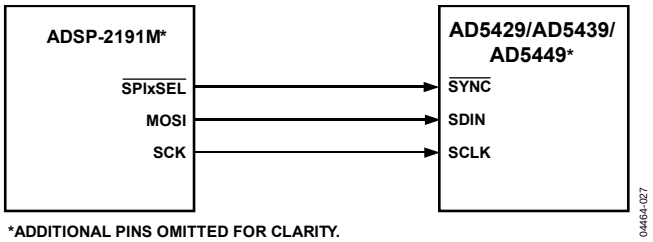


Figure 47. ADSP-2191M SPI-to-AD5429/AD5439/AD5449 Interface

The ADSP-2191M processor incorporates channel synchronous serial ports (SPORT). A serial interface between the DAC and DSP SPORT is shown in Figure 48. In this interface example, SPORT0 is used to transfer data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP serial clock and clocked into the DAC input shift register on the falling edge of its SCLK. Updating of the DAC output takes place on the rising edge of the SYNC signal.

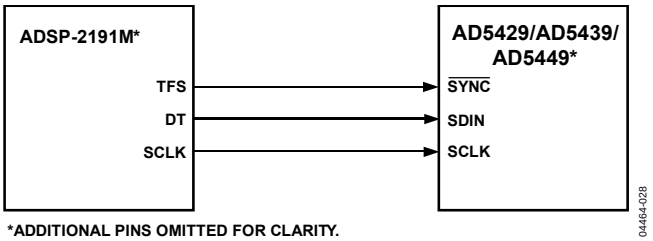


Figure 48. ADSP-2191M SPORT-to-AD5429/AD5439/AD5449 Interface

Communication between two devices at a given clock speed is possible when the following specifications are compatible: frame SYNC delay and frame SYNC setup-and-hold, data delay and data setup-and-hold, and SCLK width. The DAC interface expects a t_4 (SYNC falling edge to SCLK falling edge setup time) of 13 ns minimum.

See the ADSP-2191M user manual at www.analog.com for details on clock and frame SYNC frequencies for the SPORT register. Table 12 shows the setup for the SPORT control register.

Table 12. SPORT Control Register Setup

Name	Setting	Description
TFSW	1	Alternate framing
INVTFS	1	Active low frame signal
DTYPE	00	Right-justify data
ISCLK	1	Internal serial clock
TFSR	1	Frame every word
ITFS	1	Internal framing signal
SLEN	1111	16-bit data-word

ADSP-BF534-to-AD5429/AD5439/AD5449 Interface

The ADSP-BF534 family of processors has an SPI-compatible port that enables the processor to communicate with SPI-compatible devices. A serial interface between the BlackFin® processor and the AD5429/AD5439/AD5449 DAC is shown in Figure 49. In this configuration, data is transferred through the MOSI pin. SYNC is driven by the SPIxSEL pin, which is a reconfigured programmable flag pin.

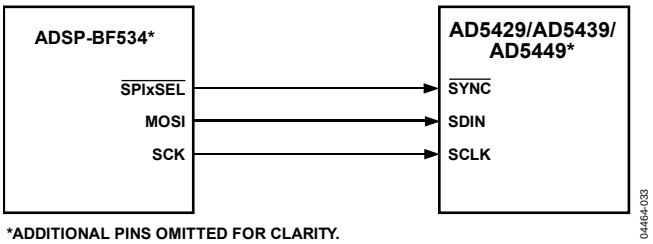


Figure 49. ADSP-BF534-to-AD5429/AD5439/AD5449 Interface

A serial interface between the DAC and the DSP SPORT is shown in Figure 50. When SPORT is enabled, initiate transmission by writing a word to the Tx register. The data is clocked out on each rising edge of the DSP serial clock and clocked into the DAC input shift register on the falling edge of its SCLK. The DAC output is updated by using the transmit frame synchronization (TFS) line to provide a SYNC signal.

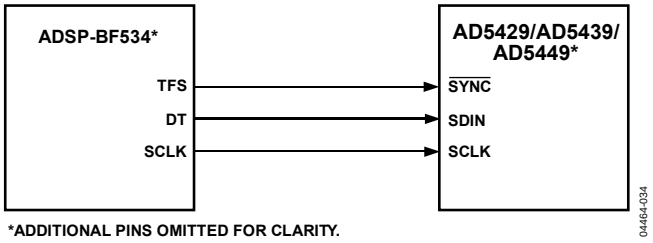
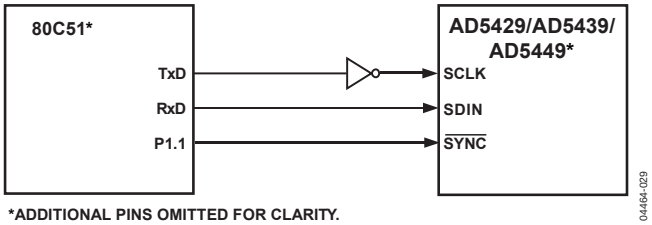


Figure 50. ADSP-BF534 SPORT-to-AD5429/AD5439/AD5449 Interface

80C51/80L51-to-AD5429/AD5439/AD5449 Interface

A serial interface between the DAC and the 80C51/80L51 is shown in Figure 51. TxD of the 80C51/80L51 drives SCLK of the DAC serial interface, and RxD drives the serial data line, SDIN. P1.1 is a bit-programmable pin on the serial port and is used to drive $\overline{\text{SYNC}}$. When data is to be transmitted to the switch, P1.1 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; therefore, only eight falling clock edges occur in the transmit cycle.

To load data correctly to the DAC, P1.1 is left low after the first eight bits are transmitted, and then a second write cycle is initiated to transmit the second byte of data. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge of TxD. As a result, no glue logic is required between the DAC and microcontroller interface. P1.1 is taken high following the completion of this cycle. The 80C51/80L51 provide the LSB of the SBUF register as the first bit in the data stream. The DAC input register requires its data with the MSB as the first bit received. The transmit routine should take this requirement into account.

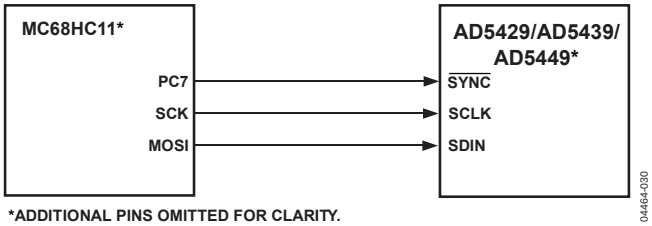


*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 51. 80C51/80L51-to-AD5429/AD5439/AD5449 Interface

MC68HC11-to-AD5429/AD5439/AD5449 Interface

Figure 52 is an example of a serial interface between the DAC and the MC68HC11 microcontroller. The SPI on the MC68HC11 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, and clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR); see the MC68HC11 user manual. The SCK of the MC68HC11 drives the SCLK of the DAC interface; the MOSI output drives the serial data line (SDIN) of the AD5429/AD5439/AD5449.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 52. MCH68HC11/68L11-to-AD5429/AD5439/AD5449 Interface

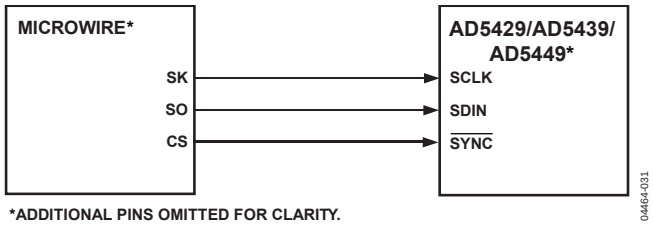
The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5429/AD5439/AD5449, the $\overline{\text{SYNC}}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first.

To load data to the DAC, leave PC7 low after the first eight bits are transferred and perform a second serial write operation to the DAC. PC7 is taken high at the end of this procedure.

If the user wants to verify the data previously written to the input shift register, the SDO line can be connected to MISO of the MC68HC11, and, with $\overline{\text{SYNC}}$ low, the shift register clocks data out on the rising edges of SCLK.

MICROWIRE-to-AD5429/AD5439/AD5449 Interface

Figure 53 shows an interface between the DAC and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the DAC input shift register on the rising edge of SK, which corresponds to the falling edge of the DAC SCLK.

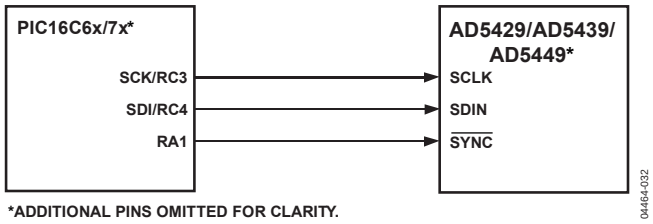


*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 53. MICROWIRE-to-AD5429/AD5439/AD5449 Interface

PIC16C6x/7x-to-AD5429/AD5439/AD5449 Interface

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit (CKP) = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the PIC16/17 microcontroller user manual for more information. In this example, the I/O port, RA1, is used to provide a $\overline{\text{SYNC}}$ signal and enable the serial port of the DAC. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are required. Figure 54 shows the connection diagram.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 54. PIC16C6x/7x-to-AD5429/AD5439/AD5449 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5429/AD5439/AD5449 is mounted should be designed so that the analog and digital sections are separate and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The DAC should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply, located as close as possible to the package, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types of capacitors that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR, 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Components, such as clocks, that produce fast-switching signals, should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This layout reduces the effects of feedthrough on the board. A microstrip technique is by far the best method, but its use is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the soldered side.

It is good practice to use compact, minimum lead-length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between $V_{REF}x$ and $R_{FB}x$ should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close as possible to the device.

OVERVIEW OF MULTIPLYING DAC DEVICES

Table 13.

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package[1]	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

[1] RU = TSSOP, CP = LFCSP, RM = MSOP, UJ = TSOT.

OUTLINE DIMENSIONS

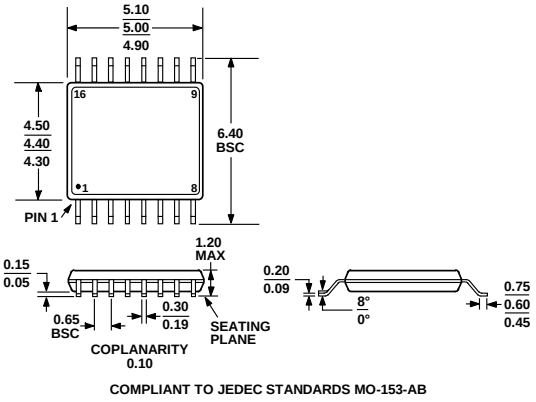


Figure 55. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	INL (LSB)	Temperature Range	Package Description	Package Option
AD5429YRU-REEL7	8	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5429YRUZ	8	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5429YRUZ-REEL7	8	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5439YRU-REEL	10	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5439YRU-REEL7	10	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5439YRUZ	10	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5439YRUZ-REEL7	10	±0.5	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRU	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRU-REEL	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRU-REEL7	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRUZ	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRUZ-REEL	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5449YRUZ-REEL7	12	±1	−40°C to +125°C	16-Lead TSSOP	RU-16
EV-AD5415/49SDZ				Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

©2004–2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D04464-0-1/16(F)