Voltage-to-Frequency and Frequency-to-Voltage Converter

Data Sheet

AD650

FEATURES

- V/F conversion to 1 MHz
- Reliable monolithic construction
- Very low nonlinearity
  - 0.002% typ at 10 kHz
  - 0.005% typ at 100 kHz
  - 0.07% typ at 1 MHz
- Input offset trimmable to zero
- CMOS- or TTL-compatible
- Unipolar, bipolar, or differential V/F
- V/F or F/V conversion
- Available in surface mount
- MIL-STD-883 compliant versions available

FUNCTIONAL BLOCK DIAGRAM

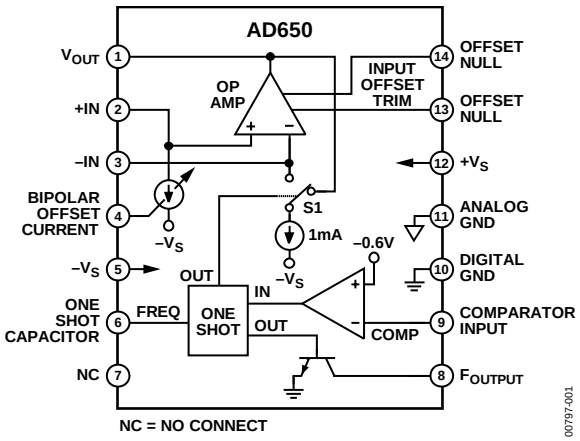


Figure 1.

PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20 ppm (0.002% of full scale) and 50 ppm (0.005%) maximum at 10 kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1 MHz full scale, linearity is guaranteed less than 1000 ppm (0.1%) on the AD650KN, BD, and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in plastic 14-lead DIP packages. The AD650JP is available in a 20-lead plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commercial temperature range (0°C to 70°C). For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in ceramic packages. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. Can operate at full-scale output frequencies up to 1 MHz (in addition to having very high linearity).
2. Can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved by using an open collector frequency output. The pull-up resistor can be connected to voltages up to 30 V.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. Separate analog and digital grounds prevent ground loops in real-world applications.
6. Available in versions compliant with MIL-STD-883.

Rev. E
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REVISION HISTORY

3/13—Rev. D to Rev. E

Changes to Figure 13 ... 11
Updated Outline Dimensions ... 19
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3/06—Rev. C to Rev. D

Updated Format ... Universal
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SPECIFICATIONS

T = 25°C, V_S = ±15 V, unless otherwise noted.

Table 1.

	AD650J/AD650A			AD650K/AD650B			AD650S			
Model	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
DYNAMIC PERFORMANCE										
Full-Scale Frequency Range			1			1			1	MHz
Nonlinearity[1]										
f_{MAX} = 10 kHz		0.002	0.005		0.002	0.005		0.002	0.005	%
f_{MAX} = 100 kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
f_{MAX} = 500 kHz		0.02	0.05		0.02	0.05		0.02	0.05	%
f_{MAX} = 1 MHz		0.1			0.05	**0.1**		0.05	**0.1**	%
Full-Scale Calibration Error[2]										
100 kHz		± 5			± 5			± 5		%
1 MHz		± 10			± 10			± 10		%
vs. Supply[3]	−0.015		**+0.015**	−0.015		**+0.015**	−0.015		**+0.015**	% of FSR/V
vs. Temperature										
A, B, and S Grades										
at 10 kHz			±75			±75			**±75**	ppm/°C
at 100 kHz			±150			±150			**±200**	ppm/°C
J and K Grades										
at 10 kHz		±75			±75					ppm/°C
at 100 kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24 kΩ Between Pin 4 and Pin 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full-Scale Step Input	1 pulse of new frequency plus 1 µs			1 pulse of new frequency plus 1 µs			1 pulse of new frequency plus 1 µs			
Overload Recovery Time Step Input	1 pulse of new frequency plus 1 µs			1 pulse of new frequency plus 1 µs			1 pulse of new frequency plus 1 µs			
ANALOG INPUT AMPLIFIER (V/F CONVERSION)										
Current Input Range (Figure 4)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 12)	−10		0	−10		0	−10		0	V
Differential Impedance		2 MΩ||10 pF			2 MΩ||10 pF			2 MΩ||10 pF		
Common-Mode Impedance		1000 MΩ||10 pF			1000 MΩ||10 pF			1000 MΩ||10 pF		
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	**±20**		±8	**±20**		±8	**±20**	nA
Input Offset Voltage (Trimmable to Zero)			**±4**			**±4**			**±4**	mV
vs. Temperature (T_{MIN} to T_{MAX})		±30				±30			±30	µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		V
COMPARATOR (F/V CONVERSION)										
Logic 0 Level	$-V_S$		−1	$-V_S$		−1	$-V_S$		−1	V
Logic 1 Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F CONVERSION)										
Output Voltage in Logic 0										
$I_{SINK} \leq 8$ mA, T_{MIN} to T_{MAX}			0.4			0.4			0.4	V
Output Leakage Current in Logic 1			**100**			**100**			**100**	nA
Voltage Range[5]	0		36	0		36	0		36	V

Model	AD650J/AD650A Min	Typ	Max	AD650K/AD650B Min	Typ	Max	AD650S Min	Typ	Max	Units
AMPLIFIER OUTPUT (F/V CONVERSION)										
Voltage Range (1500 Ω Min Load Resistance)	0		10	0		10	0		10	V
Source Current (750 Ω Max Load Resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9		**±18**	±9		**±18**	±9		**±18**	V
Quiescent Current			**8**			**8**			**8**	mA
TEMPERATURE RANGE										
Rated Performance										
N Package	0		+70	0		+70				°C
D Package	−25		+85	−25		+85	−55		+125	°C

[1] Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[2] Full-scale calibration error adjustable to zero.
[3] Measured at full-scale output frequency of 100 kHz.
[4] Refer to F/V conversion section of the text.
[5] Referred to digital ground.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Total Supply Voltage	36 V
Storage Temperature Range	−55°C to +150°C
Differential Input Voltage	±10 V
Maximum Input Voltage	$\pm V_S$
Open Collector Output Voltage Above Digital GND	36 V
Current	50 mA
Amplifier Short Circuit to Ground	Indefinite
Comparator Input Voltage	$\pm V_S$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

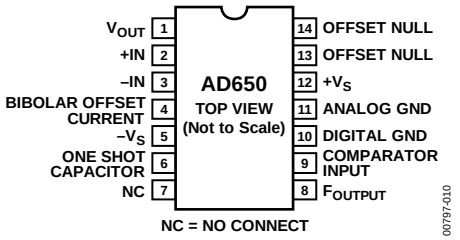


Figure 2. D-14, N-14 Pin Configurations

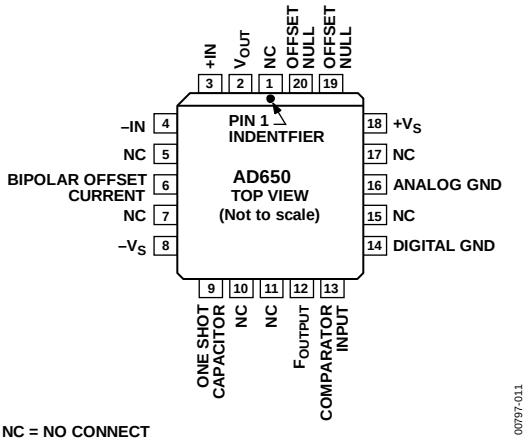


Figure 3. P-20 Pin Configuration

Table 2. Pin Function Descriptions

Pin No.			
D-14, N-14	**P-20**	**Mnemonic**	**Description**
1	2	V_{OUT}	Output of Operational Amplifier. The operational amplifier, along with C_{INT}, is used in the integrate stage of the V to F conversion.
2	3	+IN	Positive Analog Input.
3	4	–IN	Negative Analog Input.
4	6	BIPOLAR OFFSET CURRENT	On-Chip Current Source. This can be used in conjunction with an external resistor to remove the operational amplifier's offset.
5	8	$–V_S$	Negative Power Supply Input.
6	9	ONE-SHOT CAPACITOR	The Capacitor, C_{OS}, is Connected to This Pin. C_{OS} determines the time period for the one shot.
7	1, 5, 7, 10, 11, 15, 17	NC	No Connect.
8	12	F_{OUTPUT}	Frequency Output from AD650.
9	13	COMPARATOR INPUT	Input to Comparator. When the input voltage reaches –0.6 V, the one shot is triggered.
10	14	DIGITAL GND	Digital Ground.
11	16	ANALOG GND	Analog Ground.
12	18	$+V_S$	Positive Power Supply Input.
13, 14	19, 20	OFFSET NULL	Offset Null Pins. Using an external potentiometer, the offset of the operational amplifier can be removed.

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a charge balance voltage-to-frequency converter. In the connection diagram shown in Figure 4, or the block diagram of Figure 5, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is exactly balanced by an internal feedback current delivered in short, timed bursts from the switched 1 mA internal current source. These bursts of current can be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Because the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation is accomplished. The frequency output is furnished via an open collector transistor.

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V-to-F converter is shown in Figure 5. The unit is comprised of an input integrator, a current source and steering switch, a comparator, and a one shot. When the output of the one shot is low, the current steering switch S_1 diverts all the current to the output of the op amp; this is called the integration period. When the one shot has been triggered and its output is high, the switch S_1 diverts all the current to the summing junction of the op amp; this is called the reset period. The two different states are shown in Figure 6 and Figure 7 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

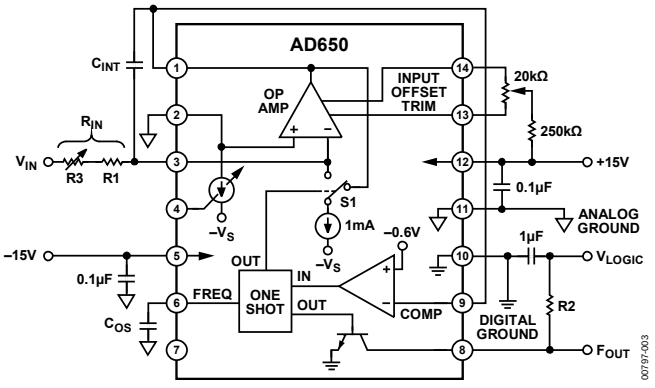


Figure 4. Connection Diagram for V/F Conversion, Positive Input Voltage

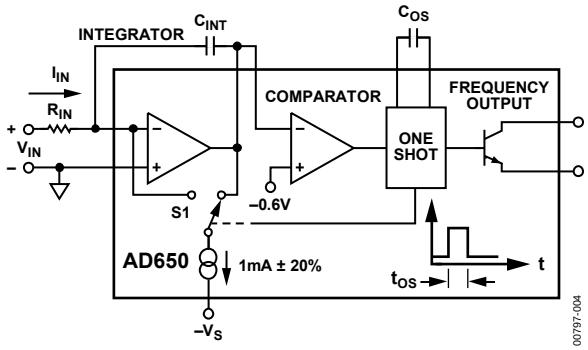


Figure 5. Block Diagram

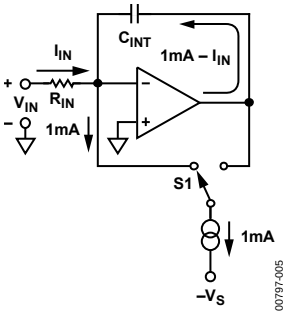


Figure 6. Reset Mode

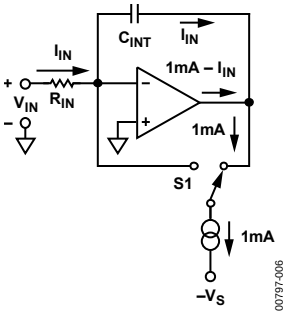


Figure 7. Integrate Mode

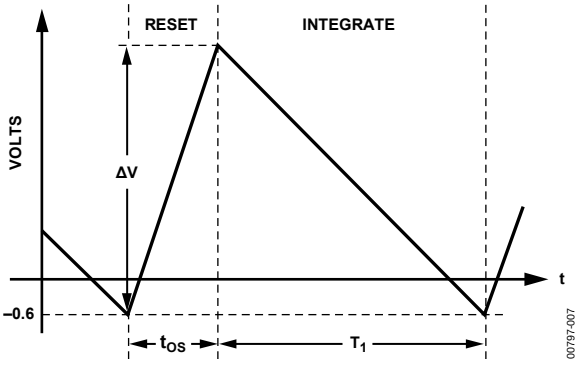


Figure 8. Voltage Across C_{INT}

The positive input voltage develops a current ($I_{IN} = V_{IN}/R_{IN}$) that charges the integrator capacitor C_{INT}. As charge builds up on C_{INT}, the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (Pin 1) crosses the comparator threshold (–0.6 V) the comparator triggers the one shot, whose time period, t_{OS} is determined by the one-shot capacitor C_{OS}.

Specifically, the one-shot time period is

$$t_{OS} = C_{OS} \times 6.8 \times 10^{3} \text{ sec/F} + 3.0 \times 10^{-7} \text{ sec} \quad (1)$$

The reset period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount

$$\Delta V = t_{OS} \times \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}}\left(1 \text{ mA} - I_{IN}\right) \quad (2)$$

After the reset period has ended, the device starts another integration period, as shown in Figure 8, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as

$$T1 = \frac{\Delta V}{\frac{dV}{dt}} = \frac{\frac{t_{OS}}{C_{INT}}\left(1\text{mA} - I_{IN}\right)}{\frac{I_N}{C_{INT}}} = t_{OS}\left(\frac{1\text{mA}}{I_{IN}} - 1\right) \quad (3)$$

The output frequency is now given as

$$f_{OUT} = \frac{1}{t_{OS} + T_1} = \frac{I_{IN}}{t_{OS} \times 1\text{mA}} = 0.15\frac{F \times \text{Hz}}{A}\frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} F} \quad (4)$$

Note that C_{INT}, the integration capacitor, has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

One-Shot Timing

A key part of the preceding analysis is the one-shot time period given in Equation 1. This time period can be broken down into approximately 300 ns of propagation delay and a second time segment dependent linearly on timing capacitor C_{OS}. When the one shot is triggered, a voltage switch that holds Pin 6 at analog ground is opened, allowing that voltage to change. An internal 0.5 mA current source connected to Pin 6 then draws its current out of C_{OS}, causing the voltage at Pin 6 to decrease linearly. At approximately –3.4 V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one-shot time period can be written mathematically as

$$t_{OS} = \frac{\Delta V\, C_{OS}}{I_{DISCHARGE}} + T_{GATE\ DELAY} \quad (5)$$

substituting actual values quoted in Equation 5,

$$t_{OS} = \frac{-3.4\text{ V} \times C_{OS}}{-0.5 \times 10^{-3}\text{ A}} + 300 \times 10^{-9} \text{ sec} \quad (6)$$

This simplifies into the timed period equation (see Equation 1).

COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance R_{IN}, timing capacitor C_{OS}, logic resistor R2, and integration capacitor C_{INT}. The first two determine the input voltage and full-scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R2 is the easiest to define. As a pull-up resistor, it should be chosen to limit the current through the output transistor to 8 mA if a TTL maximum V_{OL} of 0.4 V is desired. For example, if a 5 V logic supply is used, R2 should be no smaller than 5 V/8 mA or 625 Ω. A larger value can be used if desired.

R_{IN} and C_{OS} are the only two parameters available to set the full-scale frequency to accommodate the given signal range. The swing variable that is affected by the choice of R_{IN} and C_{OS} is nonlinearity. The selection guides of Figure 9 and Figure 10 show this quite graphically. In general, larger values of C_{OS} and lower full-scale input currents (higher values of R_{IN}) provide better linearity. In Figure 10, the implications of four different choices of R_{IN} are shown. Although the selection guide is set up for a unipolar configuration with a 0 V to 10 V input signal range, the results can be extended to other configurations and input signal ranges. For a full-scale frequency of 100 kHz (corresponding to 10 V input), among the available choices R_{IN} = 20 kΩ and C_{OS} = 620 pF gives the lowest nonlinearity, 0.0038%. In addition, the highest frequency that gives the 20 ppm minimum nonlinearity is approximately 33 kHz (40.2 kΩ and 1000 pF).

For input signal spans other than 10 V, the input resistance must be scaled proportionately. For example, if 100 kΩ is called out for a 0 V to 10 V span, 10 kΩ would be used with a 0 V to 1 V span, or 200 kΩ with a ±10 V bipolar connection.

The last component to be selected is the integration capacitor C_{INT}. In almost all cases, the best value for C_{INT} can be calculated using the equation

$$C_{INT} = \frac{10^{-4} F/\text{sec}}{f_{MAX}}\left(1000 \text{ pF minimum}\right) \quad (7)$$

When the proper value for C_{INT} is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, therefore, large amounts of noise and interference can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal-mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, then the continuous integration of the signal is interrupted, allowing the noise to appear at the output.

If the approximate amount of noise that appears on C_{INT} is known (V_{NOISE}), then the value of C_{INT} can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS} \times 1 \times 10^{-3}\ A}{+V_S - 3\text{V} - V_{NOISE}} \quad (8)$$

For example, consider an application calling for a maximum frequency of 75 kHz, a 0 V to 1 V signal range, and supply voltages of only ±9 V. The component selection guide of Figure 9 is used to select 2.0 kΩ for R_{IN} and 1000 pF for C_{OS}. This results in a one-shot time period of approximately 7 µs. Substituting 75 kHz into Equation 7 yields a value of 1300 pF for C_{INT}. When the input signal is near zero, 1 mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across C_{INT} to increase by approximately 5.5 V. Because the integrator output stage requires approximately 3 V headroom for proper operation, only 0.5 V margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time could saturate the integrator, causing an error in signal integration. Increasing C_{INT} to 1500 pF or 2000 pF provides much more noise margin, thereby eliminating this potential trouble spot.

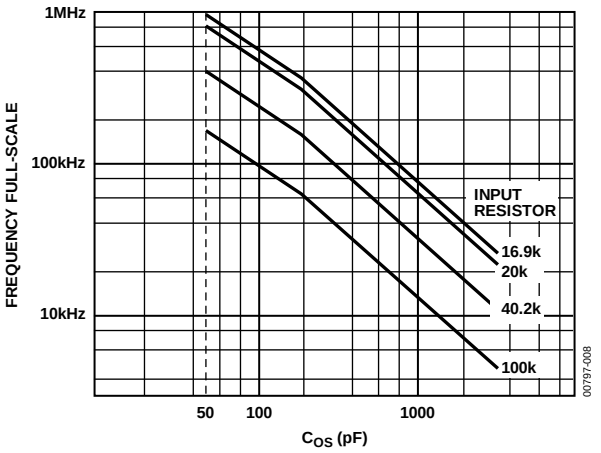


Figure 9. Full-Scale Frequency vs. C_{OS}

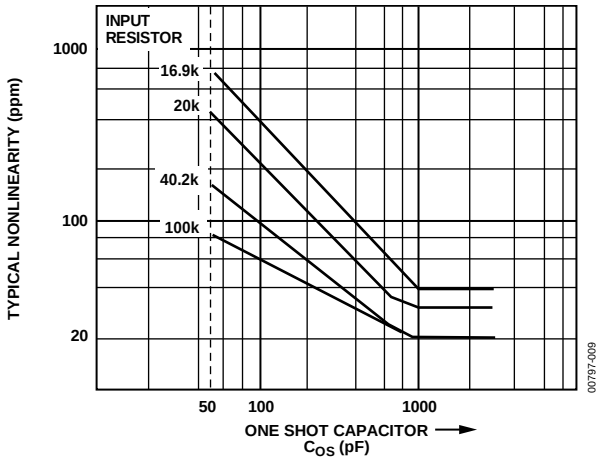


Figure 10. Typical Nonlinearity vs. C_{OS}

BIPOLAR V/F

Figure 11 shows how the internal bipolar current sink is used to provide a half-scale offset for a ±5 V signal range, while providing a 100 kHz maximum output frequency. The nominally 0.5 mA (±10%) offset current sink is enabled when a 1.24 kΩ resistor is connected between Pin 4 and Pin 5. Thus, with the grounded 10 kΩ nominal resistance shown, a −5 V offset is developed at Pin 2. Because Pin 3 must also be at −5 V, the current through R_{IN} is 10 V/40 kΩ = +0.25 mA at V_{IN} = +5 V, and 0 mA at V_{IN} = −5 V.

Components are selected using the same guidelines outlined for the unipolar configuration with one alteration. The voltage across the total signal range must be equated to the maximum input voltage in the unipolar configuration. In other words, the value of the input resistor R_{IN} is determined by the input voltage span, not the maximum input voltage. A diode from Pin 1 to ground is also recommended. This is further discussed in the Other Circuit Considerations section.

As in the unipolar circuit, R_{IN} and C_{OS} must have low temperature coefficients to minimize the overall gain drift. The 1.24 kΩ resistor used to activate the 0.5 mA offset current should also have a low temperature coefficient. The bipolar offset current has a temperature coefficient of approximately −200 ppm/°C.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 12 shows the connection diagram for V/F conversion of negative input voltages. In this configuration, full-scale output frequency occurs at negative full-scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source can be used because it only drives the noninverting integrator input. Typical input impedance at this terminal is 1 GΩ or higher. For V/F conversion of positive input signals using the connection diagram of Figure 4, the signal generator must be able to source the integration current to drive the AD650. For the negative V/F conversion circuit of Figure 12, the integration current is drawn from ground through R1 and R3, and the active input is high impedance.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in the Unipolar Configuration section. For best operating results use Equation 7 and Equation 8 in the Component Selection section.

F/V CONVERSION

The AD650 also makes a very linear frequency-to-voltage converter. Figure 13 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1 mA into the integrator input for a measured time period (determined by C_{OS}). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage that is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the Bipolar V/F section.

For a more complete description of this application, refer to Analog Devices' Application Note AN-279.

HIGH FREQUENCY OPERATION

Proper RF techniques must be observed when operating the AD650 at or near its maximum frequency of 1 MHz. Lead lengths must be kept as short as possible, especially on the one shot and integration capacitors, and at the integrator summing junction. In addition, at maximum output frequencies above 500 kHz, a 3.6 kΩ pull-down resistor from Pin 1 to $-V_S$ is required (see Figure 14). The additional current drawn through the pulldown resistor reduces the op amp's output impedance and improves its transient response.

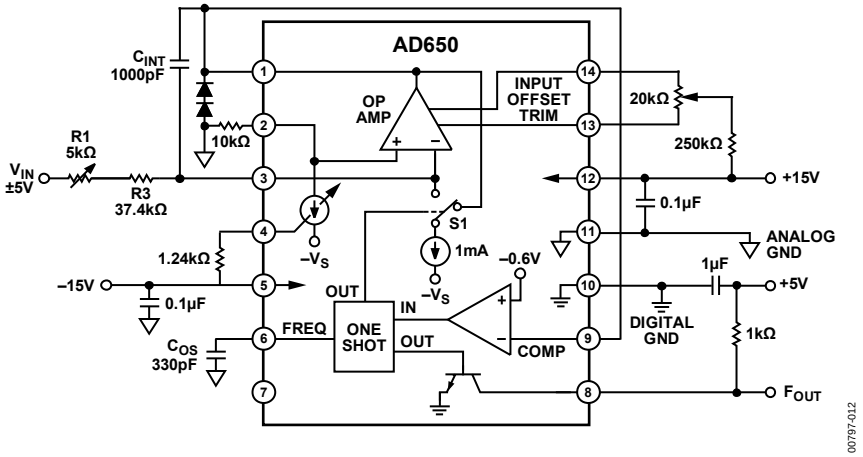


Figure 11. Connections for ±5 V Bipolar V/F with 0 kHz to 100 kHz TTL Output

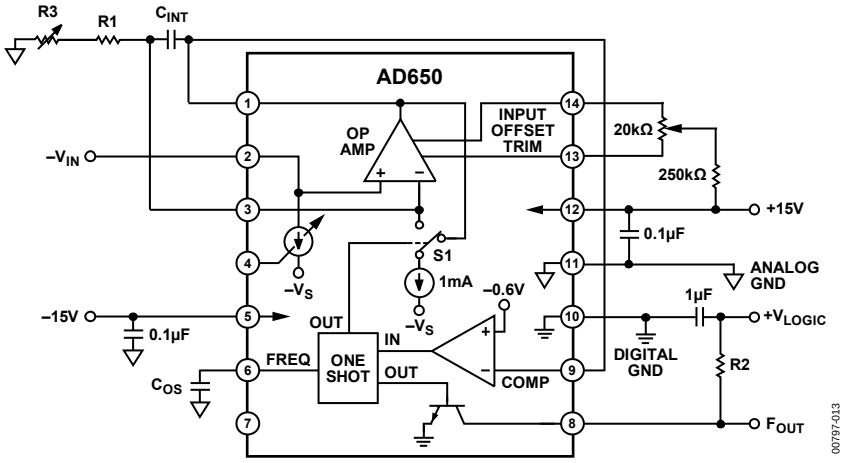


Figure 12. Connection Diagram for V/F Conversion, Negative Input Voltage

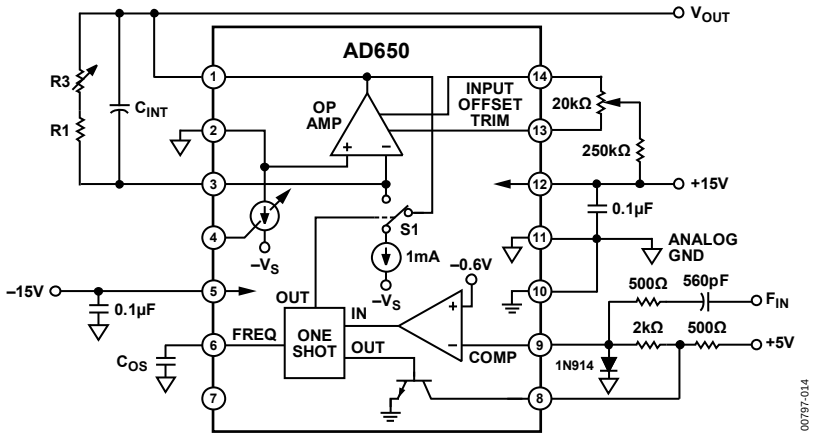


Figure 13. Connection Diagram for F/V Conversion

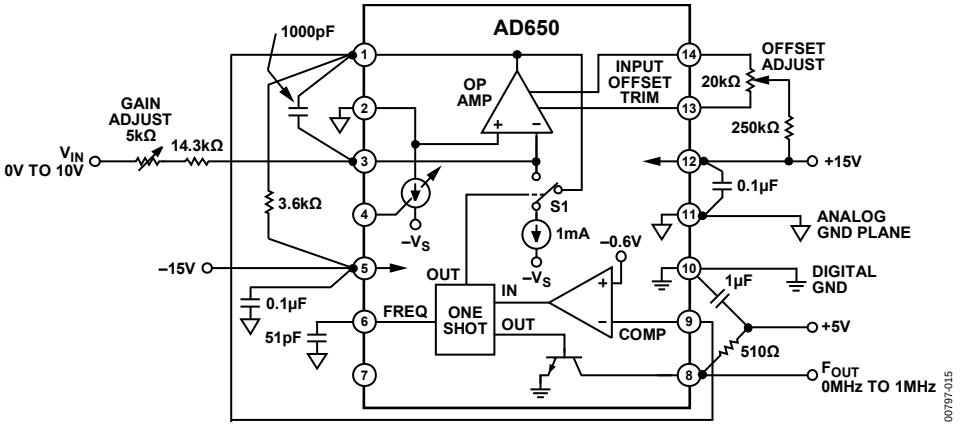


Figure 14. 1 MHz V/F Connection Diagram

DECOUPLING AND GROUNDING

It is effective engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 Ω to 100 Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1 µF to 1.0 µF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1 µF to 10 µF should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution, data acquisition applications where users expect to exploit the full linearity and dynamic range of the AD650. Although some types of circuits can operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1 MHz full scale, it is necessary to use a pull-up resistor of about 500 Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 V logic supply, for example, the open collector output draws 10 mA.

This much current being switched causes ringing on long ground runs due to the self-inductance of the wires. For instance, 20 gauge wire has an inductance of about 20 nH per inch; a current of 10 mA being switched in 50 ns at the end of 12 inches of 20 gauge wire produces a voltage spike of 50 mV. The separate digital ground of the AD650 easily handles these types of switching transients.

A problem remains from interference caused by radiation of electromagnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A 1 µF to 10 µF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground (Pin 10). The pull-up resistor should be connected directly to the frequency output (Pin 8). The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor supplies (or absorbs) the current transients, and large ac signals flows in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop does not radiate RFI efficiently.

The digital ground (Pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There can also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This does not cause any problem. In fact, the AD650 tolerates as much as 0.25 V dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (Pin 11) at the package. All of the signal grounds should be tied directly to Pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in "Noise Reduction Techniques in Electronic Systems, 2nd edition" by Henry W. Ott, (John Wiley & Sons, Inc., 1988).

TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_{OS} directly affect the overall temperature stability. In the application of Figure 5, a 10 ppm/°C input resistor used with a 100 ppm/°C capacitor can result in a maximum overall circuit gain drift of:

150 ppm/°C (AD650A) + 100 ppm/°C (C_{OS})
+ 10 ppm/°C (R_{IN}) = 260 ppm/°C

In bipolar configuration, the drift of the 1.24 kΩ resistor used to activate the internal bipolar offset current source directly affects the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input, Pin 2 (see Figure 11). That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp noninverting input is solely determined by the AD650. Under these conditions, the TC of the bipolar offset voltage is typically −200 ppm/°C and is a maximum of −300 ppm/°C. The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not as different from the nominal value as to preclude operation. This includes the integration capacitor C_{INT}. A change in the capacitance value of C_{INT} simply results in a different rate of voltage change across the capacitor. During the integration phase (see Figure 8), the rate of voltage change across C_{INT} has the opposite effect that it does during the reset phase. The result is that the conversion accuracy is unchanged by either drift or tolerance of C_{INT}. The net effect of a change in the integrator capacitor is simply to change the peak-to-peak amplitude of the sawtooth waveform at the output of the integrator.

The gain temperature coefficient of the AD650 is not a constant value. Rather, the gain TC is a function of both the full-scale frequency and the ambient temperature. At a low full-scale frequency, the gain TC is determined primarily by the stability of the internal reference (a buried Zener reference). This low speed gain TC can be quite effective; at 10 kHz full scale, the gain TC near 25°C is typically 0 ± 50 ppm/°C. Although the gain TC changes with ambient temperature (tending to be more positive at higher temperatures), the drift remains within a ±75 ppm/°C window over the entire military temperature range. At full-scale frequencies higher than 10 kHz, dynamic errors become much more important than the static drift of the dc reference. At a full-scale frequency of 100 kHz and above, these timing errors dominate the gain TC. For example, at 100 kHz full-scale frequency (R_{IN} = 40 kΩ and C_{OS} = 330 pF) the gain TC near room temperature is typically −80 ±50 ppm/°C, but at an ambient temperature near 125°C, the gain TC tends to be more positive and is typically 15 ±50 ppm/°C. This information is presented in a graphical form in Figure 15. The gain TC always tends to become more positive at higher temperatures. Therefore, it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100 kHz full-scale frequency. An average drift of −100 ppm/°C means that as temperature is increased, the circuit produces a lower frequency in response to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of −100 ppm/°C. Now consider the 1 MHz full-scale frequency.

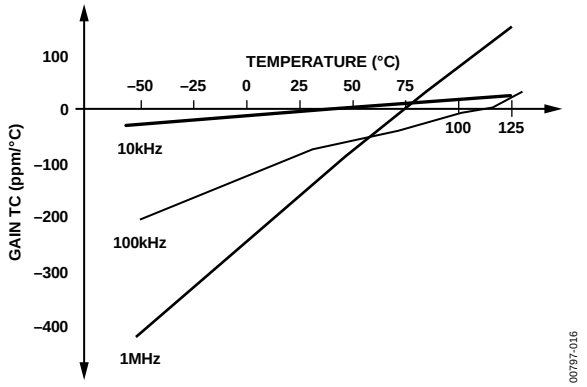


Figure 15. Gain TC vs. Temperature

It is not possible to achieve much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately −20°C), a C_{OS} with a drift of −310 ppm/°C is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of 75°C, then the C_{OS} capacitor would change the gain TC from approximately 0 ppm to 310 ppm/°C.

The temperature effects of these components are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the endpoint method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and zero. The nonlinearity varies with the choice of one-shot capacitor and input resistor (see Figure 10). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20 ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it is not usually necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated bench-top tester proves useful. Such a system based on Analog Devices' LTS-2010 is described in "V-F Converters Demand Accurate Linearity Testing," by L. DeVito, (Electronic Design, March 4, 1982).

The voltage-to-frequency transfer relation is shown in Figure 16 and Figure 17 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the endpoints of the operating range (typically at 10 mV and 10 V) with a straight line. This straight line is then the ideal relationship that is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the endpoints—typically ten intermediate points suffices. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full-scale frequency and expressed either as parts per million of full scale (ppm) or parts per hundred of full scale (%). For example, on a 100 kHz full scale, if the maximum frequency error is 5 Hz, the nonlinearity is specified as 50 ppm or 0.005%. Typically on the 100 kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 16). At higher full-scale frequencies, (500 kHz to 1 MHz), the nonlinearity becomes "S" shaped and the maximum value can be either positive or negative. Typically, on the 1 MHz scale (R_{IN} = 16.9 kΩ, C_{OS} = 51 pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 17.

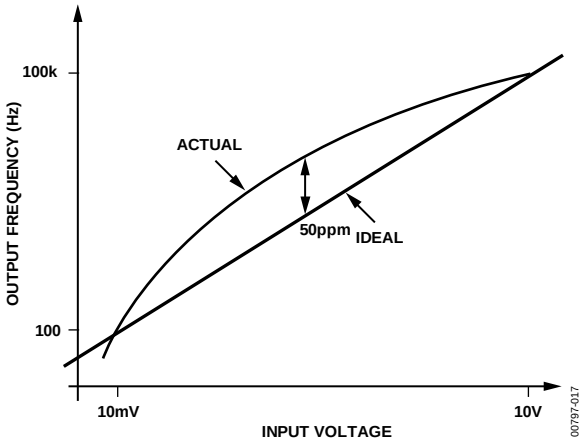


Figure 16. Exaggerated Nonlinearity at 100 kHz Full Scale

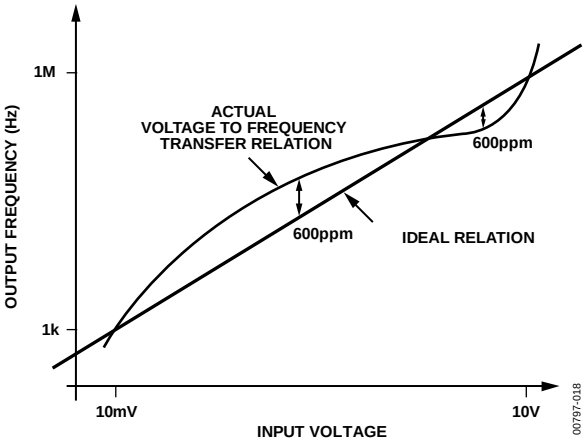


Figure 17. Exaggerated Nonlinearity at 1 MHz Full Scale

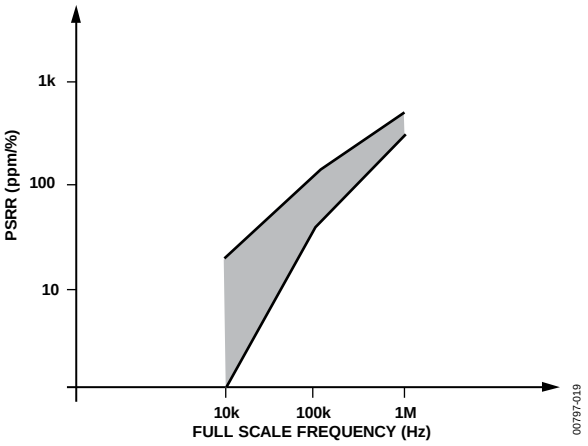


Figure 18. PSRR vs. Full-Scale Frequency

PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply (ppm/%). For example, consider a VFC with a 10 V input applied and an output frequency of exactly 100 kHz when the power supply potential is ±15 V. Changing the power supply to ±12.5 V is a 5 V change out of 30 V, or 16.7%. If the output frequency changes to 99.9 kHz, then the gain has changed 0.1% or 1000 ppm. The PSRR is 1000 ppm divided by 16.7%, which equals 60 ppm/%.

The PSRR of the AD650 is a function of the full-scale operating frequency. At low full-scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very effective. At higher frequencies, there are dynamic errors that become more important than the static reference signals, and consequently the PSRR is not quite as effective. The values of PSRR are typically 0 ± 20 ppm/% at 10 kHz full-scale frequency (R_{IN} = 40 kΩ, C_{OS} = 3300 pF). At 100 kHz (R_{IN} = 40 kΩ, C_{OS} = 330 pF) the PSRR is typically +80 ± 40 ppm/%, and at 1 MHz (R_{IN} = 16.9 kΩ, C_{OS} = 51 pF) the PSRR is +350 ± 50 ppm/%. This information is summarized graphically in Figure 18.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to Pin 1, Pin 2, and Pin 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently, the voltage on the output (Pin 1) must always be more positive than 2 V below the inputs (Pin 2 and Pin 3). For example, in the F-to-V conversion mode (Figure 13) the noninverting input of the op amp (Pin 2) is grounded, which means that the output (Pin 1) is not able to go below –2 V. Normal operation of the circuit shown in Figure 13 never calls for a negative voltage at the output, but users can imagine an arrangement calling for a bipolar output voltage (for example, ±10 V) by connecting an extra resistor from Pin 3 to a positive voltage. However, this does not work.

Care should be taken under conditions where a high positive input voltage exists at or before power up. These situations can cause a latch up at the integrator output (Pin 1). This is a nondestructive latch and, as such, normal operation can be restored by cycling the power supply. Latch up can be prevented by connecting two diodes (for example, 1N914 or 1N4148) as shown in Figure 11, thereby preventing Pin 1 from swinging below Pin 2.

A second major difference is that the output only sinks 1 mA to the negative supply. There is no pulldown stage at the output other than the 1 mA current source used for the V-to-F conversion. The op amp sources a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp can be driven to within 3 V of the positive supply when it is not sourcing external current. When sourcing 10 mA the output voltage can be driven to within 6 V of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, Pin 3, is bias current compensated and the noninverting input is not bias-current compensated. The bias current at the inverting input is nominally zero, but can be as much as 20 nA in either direction. The noninverting input typically has a bias current of 40 nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20 kΩ is connected from Pin 13 to Pin 14 and the wiper is connected to the positive supply through a 250 kΩ resistor. A potential of about 0.6 V is established across the 250 kΩ resistor, and the 3 μA current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and by using a bipolar current either into or out of the null pin. The amount of current required is very small—typically less than 3 μA. This technique is shown in the Applications section of this data sheet; the autozero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24 kΩ resistor between Pin 4 and the negative supply. The resulting current delivered to the op amp noninverting input is nominally 0.5 mA and has a tolerance of ±10%. This current is then used to provide an offset voltage when Pin 2 is tied to ground through a resistor. The 0.5 mA that appears at Pin 2 is also flowing through the 1.24 kΩ resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resulting offset voltage. It is possible to use other values of resistance between Pin 4 and $-V_S$ to obtain a bipolar offset current different from 0.5 mA. Figure 19 shows the relationship between the bipolar offset current and the value of the resistor used to activate the source.

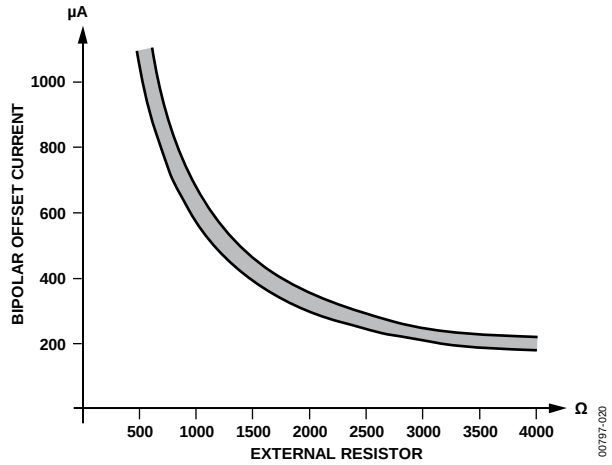


Figure 19. Bipolar Offset Current vs. External Resistor

APPLICATIONS

DIFFERENTIAL VOLTAGE-TO-FREQUENCY CONVERSION

The circuit in Figure 20 accepts a true floating differential input signal. The common-mode input, V_{CM}, can be in the range +15 V to −5 V with respect to analog ground. The signal input, V_{IN}, can be ±5 V with respect to the common-mode input. Both inputs are low impedance; the source that drives the common-mode input must supply the 0.5 mA drawn by the bipolar offset current source, and the source that drives the signal input must supply the integration current.

If less common-mode voltage range is required, then a lower voltage Zener can be used. For example, if a 5 V Zener is used, the V_{CM} input can be in the range +10 V to −5 V. If the Zener is not used at all, the common-mode range is ±5 V with respect to analog ground. If no Zener is used, the 10 kΩ pulldown resistor is not needed and the integrator output (Pin 1) is connected directly to the comparator input (Pin 9).

AUTOZERO CIRCUIT

In order to exploit the full dynamic range of the AD650 VFC, very small input voltages need to be converted. For example, a six decade dynamic range based on a full scale of 10 V requires accurate measurement of signals down to 10 µV. In these situations, a well-controlled input offset voltage is imperative. A constant offset voltage does not affect dynamic range but simply shifts all of the frequency readings by a few hertz. However, if the offset should change, it is not possible to distinguish between a small change in a small input voltage and a drift of the offset voltage. Therefore, the usable dynamic range is less. The circuit shown in Figure 21 provides automatic adjustment of the op amp offset voltage. The circuit uses an AD582 sample-and-hold amplifier to control the offset, and the input voltage to the VFC is switched between ground and the signal to be measured via an AD7512DI analog switch. The offset of the AD650 is adjusted by injecting a current into—or drawing a current out of—Pin 13. Note that only one of the offset null pins is used. During the VFC norm mode, the SHA is in the hold mode and the hold capacitor is very large, 0.1 µF, which holds the AD650 offset constant for a long period of time.

When the circuit is in the autozero mode, the SHA is in sample mode and behaves like an op amp. The circuit is a variation of the classical two amplifier servo loop, where the output of the device under test (DUT)—here the DUT is the AD650 op amp—is forced to ground by the feedback action of the control amplifier—the SHA. Because the input of the VFC circuit is connected to ground during the autozero mode, the input current that can flow is determined by the offset voltage of the AD650 op amp. Because the output of the integrator stage is forced to ground, it is known that the voltage is not changing (it is equal to ground potential). Therefore, if the output of the integrator is constant, its input current must be zero, so the offset voltage has been forced to be zero. Note that the output of the DUT could have been forced to any convenient voltage other than ground. All that is required is that the output voltage be known to be constant. Note also that the effect of the bias current at the inverting input of the AD650 op amp is also mulled in this circuit. The 1000 pF capacitor shunting the 200 kΩ resistor is compensation for the two amplifier servo loop. Two integrators in a loop require a single zero for compensation. The 3.6 kΩ resistor from Pin 1 of the AD650 to the negative supply is not part of the autozero circuit, but rather, it is required for VFC operation at 1 MHz.

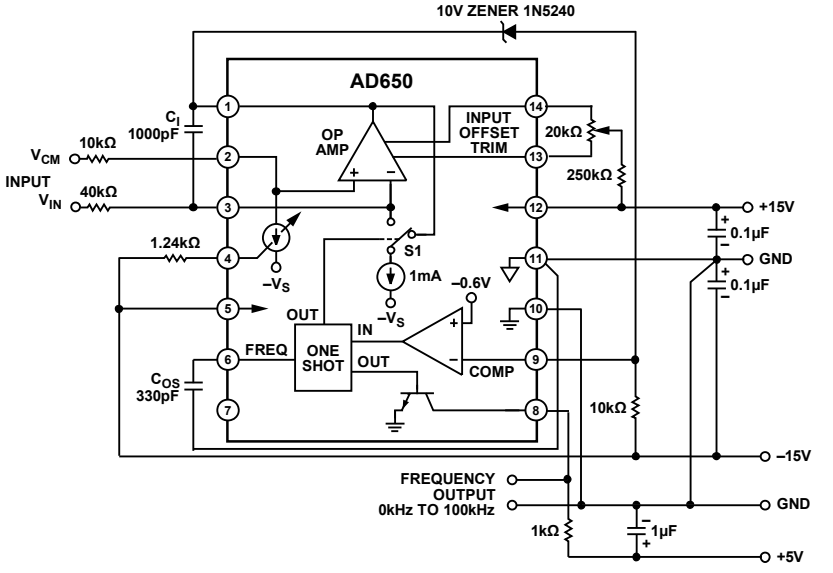


Figure 20. Differential Input

PHASE-LOCKED LOOP F/V CONVERSION

Although the F/V conversion technique shown in Figure 13 is quite accurate and uses only a few extra components, it is very limited in terms of signal frequency response and carrier feedthrough. If the carrier (or input) frequency changes instantaneously, then the output cannot change very rapidly due to the integrator time constant formed by C_{INT} and R_{IN}. While it is possible to decrease the integrator time constant to provide faster settling of the F-to-V output voltage, the carrier feedthrough then becomes larger. For signal frequency response in excess of 2 kHz, a phase-locked F/V conversion technique such as the one shown in Figure 22 is recommended.

In a phase-locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable "divide by N" before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to "N times" the reference frequency. It is this frequency output that is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

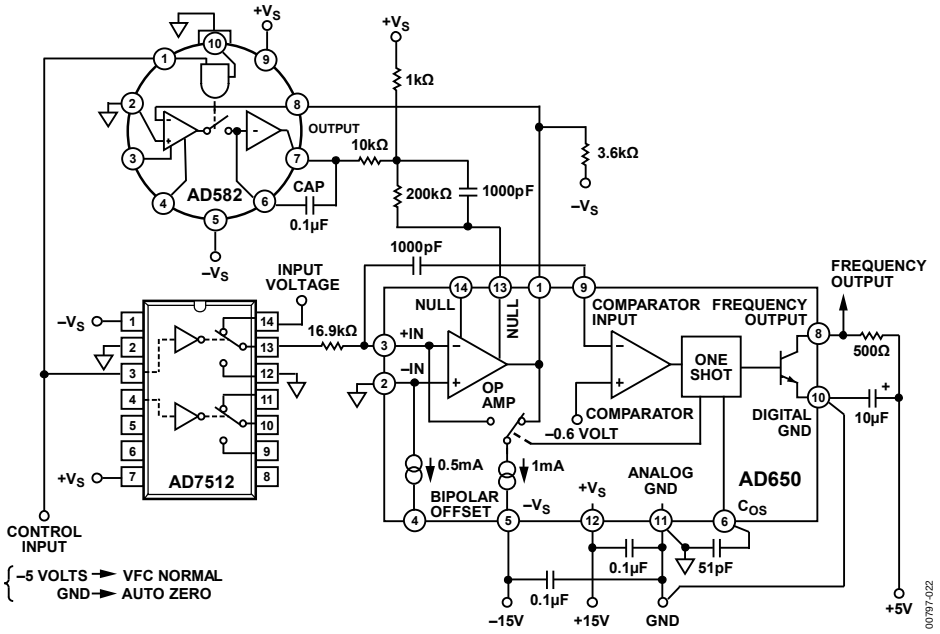


Figure 21. Autozero Circuit

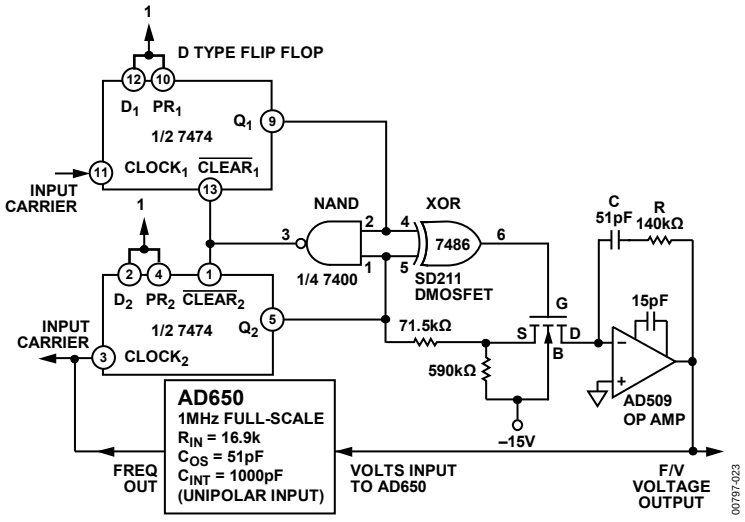


Figure 22. Phase-Locked Loop F/V Conversion

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations, a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 22 uses a digital phase detector that also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFDs) are available in integrated form. For a full discussion of phase-lock loop circuits see "Phase Lock Techniques," 3rd Edition, by F.M. Gardner, (John Wiley & Sons, Inc., 1979).

An analysis of this circuit must begin at the 7474 Dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops rise at exactly the same time. With two zeros, and then two ones on the inputs of the exclusive or (XOR) gate, the output remains low keeping the DMOS FET switched off. Also, the NAND gate goes low resetting the flip-flops to zero. Throughout this entire cycle, the DMOS integrator gate remains off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate is turned on for the short time span that the two signals are mismatched. Because Q_2 is low during the mismatch time, a negative current is fed into the integrator, causing its output voltage to rise. This in turn increases the frequency of the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator is forced down slightly to synchronize the two signals.

Using a mathematical approach, the ±25 μA pulses from the phase detector are incorporated into the phase-detector gain (K_d).

$$K_d = \frac{25\mu A}{2\pi} = 4\times10^{-6} \text{ amperes / radian} \quad (9)$$

Also, the V/F converter is configured to produce 1 MHz in response to a 10 V input so its gain (Ko) is

$$K_O = \frac{2\pi\times1\times10^6 \text{ Hz}}{10 \text{ V}} = 6.3\times10^5 \frac{\text{radians}}{\text{volt}\times\text{sec}} \quad (10)$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency (ω_n).

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \quad (11)$$

and damping factor (ζ) is

$$\zeta = \frac{R\sqrt{CK_o K_d}}{2} \quad (12)$$

For the values shown in Figure 22, these relations simplify to a natural frequency of 35 kHz with a damping factor of 0.8.

For a simple approach to determine component values for other PLL frequencies and VFC full-scale voltage, follow these steps:

1. Determine K_o (in units of radians per volt second) from the maximum input carrier frequency f_{MAX} (in hertz) and the maximum output voltage V_{MAX}.

$$K_o = \frac{2\pi\times F_{MAX}}{V_{MAX}} \quad (13)$$

2. Calculate a value for C based upon the desired loop bandwidth f_n. Note that this is the desired frequency range of the output signal. The loop bandwidth (f_n) is not the maximum carrier frequency (f_{MAX}). The signal can be very narrow even though it is transmitted over a 1 MHz carrier.

$$C = \frac{K_o}{f_n^{\,2}}\times1\times10^{-7} \frac{V\times F}{\text{Rad}\times\text{sec}} \quad (14)$$

where:
C units = farads
f_n units = hertz
K_o units = rad/volt × sec

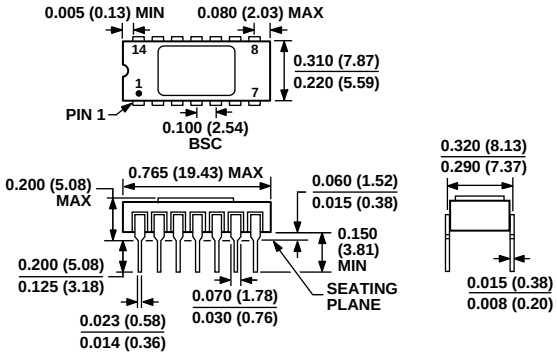
3. Calculate R to yield a damping factor of approximately 0.8 using this equation:

$$R = \frac{f_n}{K_o}\times2.5\times10^6 \frac{\text{Rad}\times\Omega}{V} \quad (15)$$

where:
R units = ohms
f_n units = hertz
K_o units = rad/volt × sec

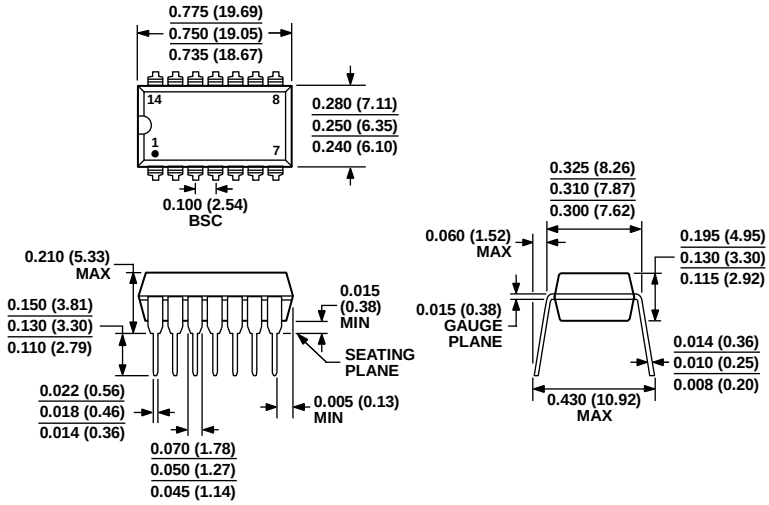
If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor can be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]
(D-14)
Dimensions shown in inches and (millimeters)

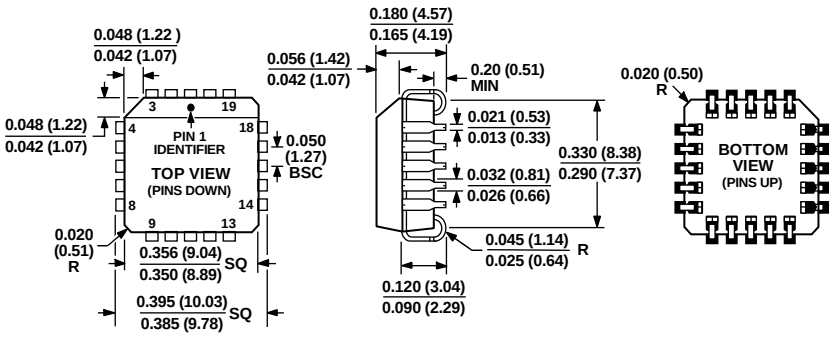


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 24. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Gain Tempco ppm/°C 100 kHz	1 MHz Linearity	Temperature Range	Package Description	Package Option
AD650JN	150 typ	0.1% typ	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD650JNZ	150 typ	0.1% typ	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD650KN	150 typ	0.1% max	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD650KNZ	150 typ	0.1% max	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD650JP	150 typ	0.1% typ	0°C to 70°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
AD650JPZ	150 typ	0.1% typ	0°C to 70°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
AD650AD	150 max	0.1% typ	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD650BD	150 max	0.1% max	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD650SD	200 max	0.1% max	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD650SD/883B	200 max	0.1% max	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD650ACHIPS				Die	

[1] Z = RoHS Compliant Part.

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