LC²MOS 12-Bit DACPORTs

AD7245A/AD7248A

FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Improved AD7245/AD7248:
12 V to 15 V Operation
±1/2 LSB Linearity Grade
Faster Interface—30 ns Typ Data Setup Time
Extended Plastic Temperature Range (–40°C to +85°C)
Single or Dual Supply Operation
Low Power—65 mW Typ in Single Supply
Parallel Loading Structure: AD7245A
(8+4) Loading Structure: AD7248A

GENERAL DESCRIPTION

The AD7245A/AD7248A is an enhanced version of the industry standard AD7245/AD7248. Improvements include operation from 12 V to 15 V supplies, a ±1/2 LSB linearity grade, faster interface times and better full scale and reference variations with V_{DD}. Additional features include extended temperature range operation for commercial and industrial grades.

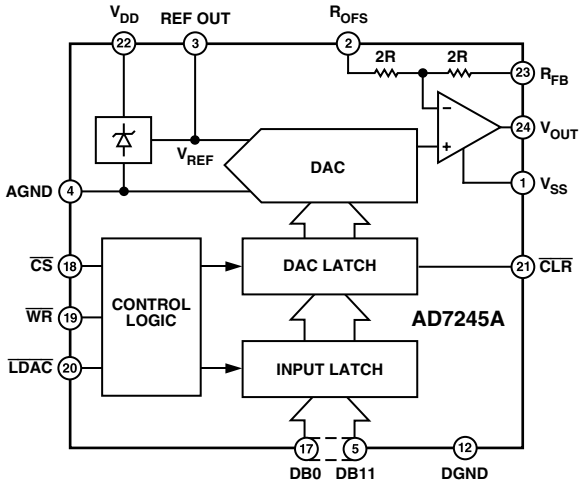
The AD7245A/AD7248A is a complete, 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and double-buffered interface logic. The AD7245A accepts 12-bit parallel data that is loaded into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248A has an 8-bit-wide data bus with data loaded to the input latch in two write operations. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch and updates the analog output. The AD7245A also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented.

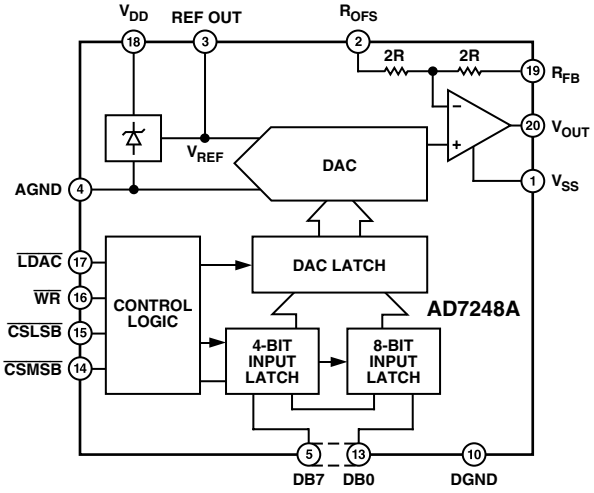
The on-chip 5 V buried Zener diode provides a low noise, temperature compensated reference for the DAC. For single supply operation, two output ranges of 0 V to 5 V and 0 V to 10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing 10 V across a 2 kΩ load to GND.

The AD7245A/AD7248A is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7245A is available in a small, 0.3" wide, 24-lead DIP and SOIC and in 28-terminal surface mount packages. The AD7248A is packaged in a small, 0.3" wide, 20-lead DIP and SOIC and in 20-terminal surface mount packages.

AD7245A FUNCTIONAL BLOCK DIAGRAM



AD7248A FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7245A/AD7248A is a 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times on the part allows easy, direct interfacing to most modern microprocessors.
3. The AD7245A/AD7248A features a wide power supply range allowing operation from 12 V supplies.

DACPORT is a registered trademark of Analog Devices, Inc.

REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2001

AD7245A/AD7248A–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2] Version	B[2] Version	T[2] Version	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy @ 25°C[3]	±3/4	±1/2	±1/2	LSB max	
T_{MIN} to T_{MAX}	±1	±3/4	±3/4	LSB max	
T_{MIN} to T_{MAX}		±1/2		LSB max	V_{DD} = 15 V ± 10%
Differential Nonlinearity[3]	±1	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error @ 25°C[3]	±3	±3	±3	LSB max	V_{SS} = 0 V or –12 V to –15 V[4]
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
Bipolar Zero Error @ 25°C[3]	±3	±2	±2	LSB max	R_{OFS} connected to REF OUT; V_{SS} = –12 V to –15 V[4]
T_{MIN} to T_{MAX}	±5	±4	±4	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
DAC Gain Error[3, 6]	±2	±2	±2	LSB max	
Full-Scale Output Voltage Error[7] @ 25°C	±0.2	±0.2	±0.2	% of FSR max	V_{DD} = 15 V
ΔFull Scale/ΔV_{DD}	±0.06	±0.06	±0.06	% of FSR/V max	V_{DD} = +12 V to +15 V[4]
ΔFull Scale/ΔV_{SS}	±0.01	±0.01	±0.01	% of FSR/V max	V_{SS} = –12 V to –15 V[4]
Full-Scale Temperature Coefficient[8]	±40	±30	±40	ppm of FSR/°C max	V_{DD} = 15 V
REFERENCE OUTPUT					
REF OUT @ 25°C	4.99/5.01	4.99/5.01	4.99/5.01	V min/V max	V_{DD} = 15 V
ΔREF OUT/ΔV_{DD}	2	2	2	mV/V max	V_{DD} = 12 V to 15 V[4]
Reference Temperature Coefficient	±25	±25	±35	ppm/°C typ	
Reference Load Change					
(ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Reference Load Current Change (0–100 μA)
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[9]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges[10]	5, 10	5, 10	5, 10	V	V_{SS} = 0 V; Pin Strappable
	5, 10,	5, 10,	5, 10,		V_{SS} = –12 V to –15 V;[4] Pin Strappable
	±5	±5	±5	V	
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[9]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	7	7	10	μs max	DAC Latch All 0s to All 1s
Negative Full-Scale Change	7	7	10	μs max	DAC Latch All 1s to All 0s; V_{SS} = –12 V to –15 V[4]
Output Voltage Slew Rate	2	2	1.5	V/μs min	
Digital Feedthrough[3]	10	10	10	nV-s typ	
Digital-to-Analog Glitch Impulse	30	30	30	nV-s typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/	+10.8/	+10.8/	V min/	For Specified Performance Unless Otherwise Stated
	+16.5	+16.5	+16.5	V max	
V_{SS}	–10.8/	–10.8/	–10.8/	V min/	For Specified Performance Unless Otherwise Stated
	–16.5	–16.5	–16.5	V max	
I_{DD} @ 25°C	9	9	9	mA max	Output Unloaded; Typically 5 mA
T_{MIN} to T_{MAX}	10	10	12	mA max	Output Unloaded
I_{SS} (Dual Supplies)	3	3	5	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Power supply tolerance is ±10%.
[2]Temperature ranges are as follows: A/B Versions; –40°C to +85°C; T Version; –55°C to +125°C.
[3]See Terminology.
[4]With appropriate power supply tolerances.
[5]FSR means Full-Scale Range and is 5 V for the 0 V to 5 V output range and 10 V for both the 0 V to 10 V and ±5 V output ranges.
[6]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.
[7]This error is calculated with respect to an ideal 4.9988 V on the 0 V to 5 V and ±5 V ranges; it is calculated with respect to an ideal 9.9976 V on the 0 V to 10 V range. It includes the effects of internal voltage reference, gain and offset errors.
[8]Full-Scale TC = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
[9]Guaranteed by design and characterization, not production tested.
[10]0 V to 10 V output range is available only when V_{DD} ≥ +14.25 V.

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1] (V_{DD} = +12 V to +15 V;[2] V_{SS} = 0 V to –12 V to –15 V;[2] See Figures 5 and 7.)

Parameter	A, B Versions	T Version	Unit	Conditions
t_1				
@ 25°C	55	55	ns typ	Chip Select Pulsewidth
T_{MIN} to T_{MAX}	80	100	ns min	
t_2				
@ 25°C	40	40	ns typ	Write Pulsewidth
T_{MIN} to T_{MAX}	80	100	ns min	
t_3				
@ 25°C	0	0	ns min	Chip Select to Write Setup Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_4				
@ 25°C	0	0	ns min	Chip Select to Write Hold Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_5				
@ 25°C	40	40	ns typ	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	80	80	ns min	
t_6				
@ 25°C	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	ns min	
t_7				
@ 25°C	40	40	ns typ	Load DAC Pulsewidth
T_{MIN} to T_{MAX}	80	100	ns min	
t_8 (AD7245A Only)				
@ 25°C	40	40	ns typ	Clear Pulsewidth
T_{MIN} to T_{MAX}	80	100	ns min	

NOTES
[1]Sample tested at 25°C to ensure compliance.
[2]Power supply tolerance is ±10%.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND ..... –0.3 V to +17 V
V_{DD} to DGND ..... –0.3 V to +17 V
V_{DD} to V_{SS} ..... –0.3 V to +34 V
AGND to DGND ..... –0.3 V, V_{DD}
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND[2] ..... V_{SS}, V_{DD}
V_{OUT} to V_{SS}[2] ..... 0 V, 24 V
V_{OUT} to V_{DD}[2] ..... –32 V, 0 V
REF OUT[2] to AGND ..... 0 V, V_{DD}
Power Dissipation (Any Package) to 75°C ..... 450 mW
Derates above 75°C by ..... 6 mW/°C
Operating Temperature
Commercial (A, B Versions) ..... –40°C to +85°C
Extended (S Version) ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. V_{OUT} short circuit current is typically 80 mA.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7245A/AD7248A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD7245A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7245AAN	–40°C to +85°C	±3/4 LSB	N-24
AD7245ABN	–40°C to +85°C	±1/2 LSB	N-24
AD7245AAQ	–40°C to +85°C	±3/4 LSB	Q-24
AD7245ATQ[3]	–55°C to +125°C	±3/4 LSB	Q-24
AD7245AAP	–40°C to +85°C	±3/4 LSB	P-28A
AD7245AAR	–40°C to +85°C	±3/4 LSB	R-24
AD7245ABR	–40°C to +85°C	±1/2 LSB	R-24
AD7245ATE[3]	–55°C to +125°C	±3/4 LSB	E-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.
[3]This grade will be available to /883B processing only.

AD7248A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7248AAN	–40°C to +85°C	±3/4 LSB	N-20
AD7248ABN	–40°C to +85°C	±1/2 LSB	N-20
AD7248AAQ	–40°C to +85°C	±3/4 LSB	Q-20
AD7248ATQ[3]	–55°C to +125°C	±3/4 LSB	Q-20
AD7248AAP	–40°C to +85°C	±3/4 LSB	P-20A
AD7248AAR	–40°C to +85°C	±3/4 LSB	R-20
AD7248ABR	–40°C to +85°C	±1/2 LSB	R-20

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.
[3]This grade will be available to /883B processing only.

TERMINOLOGY

RELATIVE ACCURACY
Relative Accuracy, or endpoint nonlinearity, is a measure of the actual deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH
Digital Feedthrough is the glitch impulse injected from the digital inputs to the analog output when the inputs change state. It is measured with $\overline{LDAC}$ high and is specified in nV-s.

DAC GAIN ERROR
DAC Gain Error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been allowed for. It is, therefore defined as:

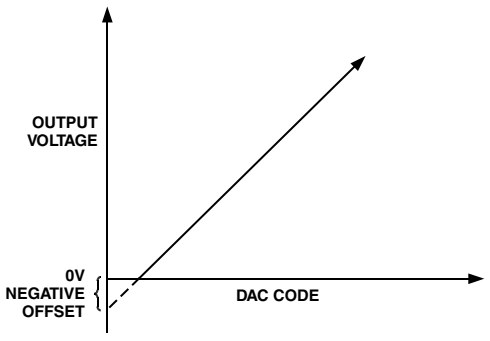
Measured Value—Offset—Ideal Value

where the ideal value is calculated relative to the actual reference value.

UNIPOLAR OFFSET ERROR
Unipolar Offset Error is a combination of the offset errors of the voltage mode DAC and the output amplifier and is measured when the part is configured for unipolar outputs. It is present for all codes and is measured with all 0s in the DAC register.

BIPOLAR ZERO OFFSET ERROR
Bipolar Zero Offset Error is measured when the part is configured for bipolar output and is a combination of errors from the DAC and output amplifier. It is present for all codes and is measured with a code of 2048 (decimal) in the DAC register.

SINGLE SUPPLY LINEARITY AND GAIN ERROR
The output amplifier of the AD7245A/AD7248A can have a true negative offset even when the part is operated from a single positive power supply. However, because the lower supply rail to the part is 0 V, the output voltage cannot actually go negative. Instead the output voltage sits on the lower rail and this results in the transfer function shown. This is an offset effect and the transfer function would have followed the dotted line if the output voltage could have gone negative. Normally, linearity is measured after offset and full scale have been adjusted or allowed for. On the AD7245A/AD7248A the negative offset is allowed for by calculating the linearity from the code which the amplifier comes off the lower rail. This code is given by the negative offset specification. For example, the single supply linearity specification applies between Code 3 and Code 4095 for the 25°C specification and between Code 5 and Code 4095 over the T_{MIN} to T_{MAX} temperature range. Since gain error is also measured after offset has been allowed for, it is calculated between the same codes as the linearity error. Bipolar linearity and gain error are measured between Code 0 and Code 4095.

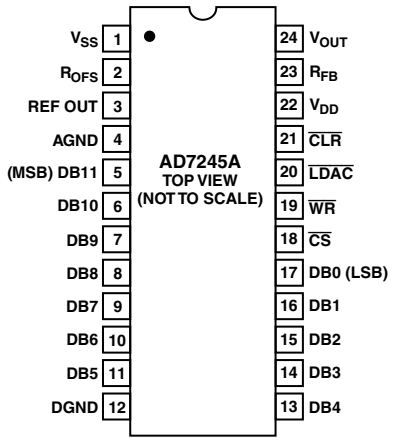


AD7245A PIN FUNCTION DESCRIPTIONS
(DIP PIN NUMBERS)

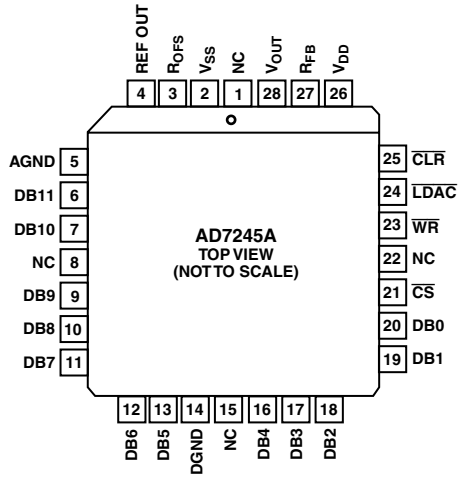
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB11	Data Bit 11. Most Significant Bit (MSB).
6–11	DB10–DB5	Data Bit 10 to Data Bit 5.
12	DGND	Digital Ground.
13–16	DB4–DB1	Data Bit 4 to Data Bit 1.
17	DB0	Data Bit 0. Least Significant Bit (LSB).
18	$\overline{CS}$	Chip Select Input (Active LOW). The device is selected when this input is active.
19	$\overline{WR}$	Write Input (Active LOW). This is used in conjunction with $\overline{CS}$ to write data into the input latch of the AD7245A.
20	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
21	$\overline{CLR}$	Clear Input (Active LOW). When this input is active the contents of the DAC latch are reset to all 0s.
22	V_{DD}	Positive Supply Voltage.
23	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
24	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 V to 5 V, 0 V to 10 V or –5 V to +5 V.

AD7245A PIN CONFIGURATIONS

DIP and SOIC

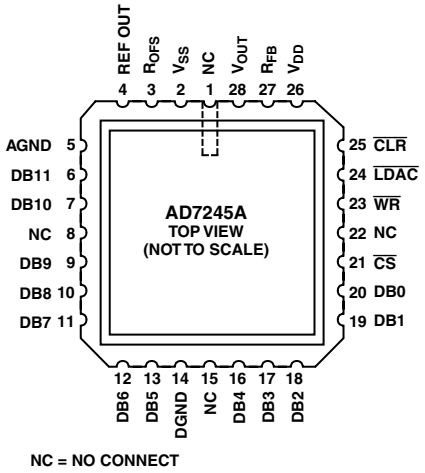


PLCC



NC = NO CONNECT

LCCC



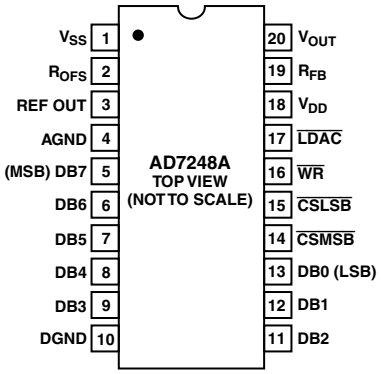
NC = NO CONNECT

AD7248A PIN FUNCTION DESCRIPTIONS
(ANY PACKAGE)

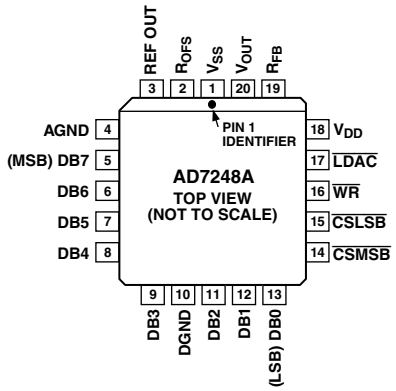
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0 V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB7	Data Bit 7.
6	DB6	Data Bit 6.
7	DB5	Data Bit 5.
8	DB4	Data Bit 4.
9	DB3	Data Bit 3.
10	DGND	Digital Ground.
11	DB2	Data Bit 2/Data Bit 10.
12	DB1	Data Bit 1/Data Bit 9.
13	DB0	Data Bit 0 (LSB)/Data Bit 8.
14	$\overline{CSMSB}$	Chip Select Input for MS Nibble. (Active LOW). This selects the upper 4 bits of the input latch. Input data is right justified.
15	$\overline{CSLSB}$	Chip Select Input for LS byte. (Active LOW). This selects the lower 8 bits of the input latch.
16	$\overline{WR}$	Write Input. This is used in conjunction with $\overline{CSMSB}$ and $\overline{CSLSB}$ to load data into the input latch of the AD7248A.
17	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
18	V_{DD}	Positive Supply Voltage.
19	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
20	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 V to 5 V, 0 V to 10 V or –5 V to +5 V.

AD7248A PIN CONFIGURATIONS

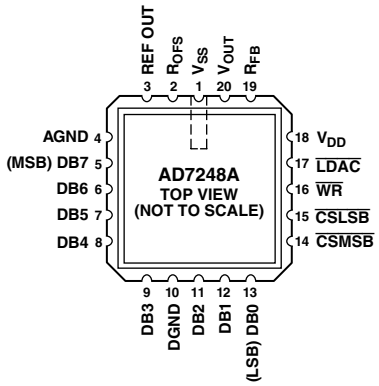
DIP and SOIC

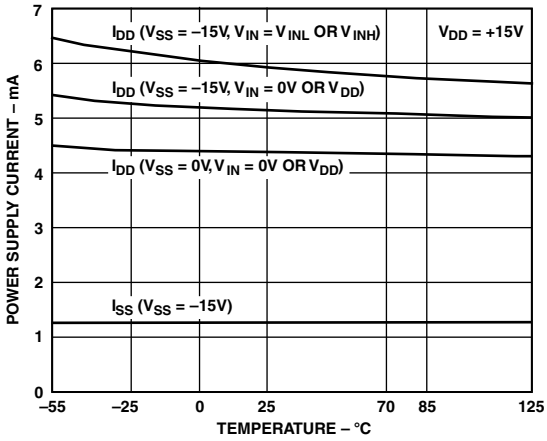


PLCC

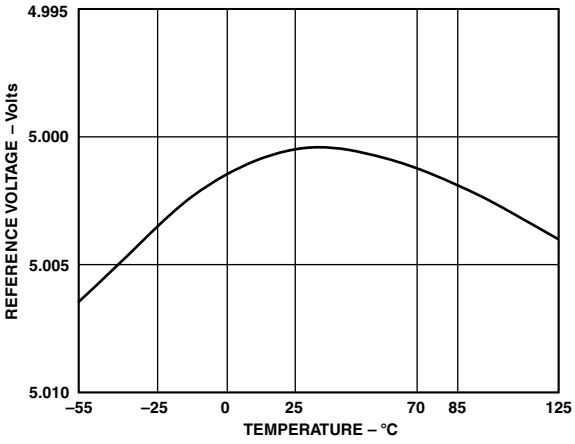


LCCC

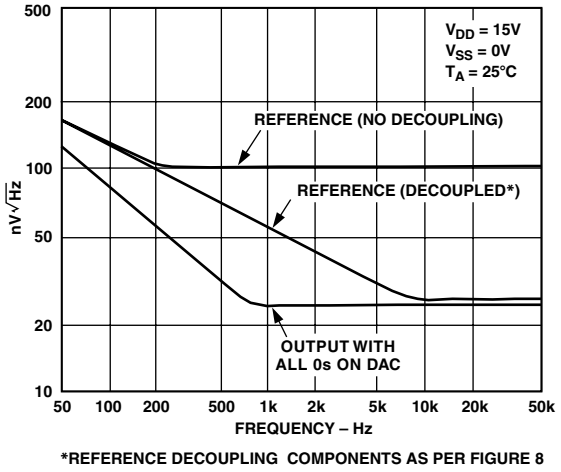




TPC 1. Power Supply Current vs. Temperature

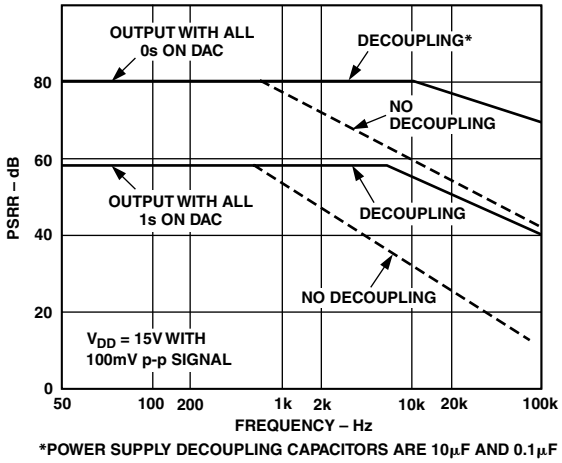


TPC 4. Reference Voltage vs. Temperature



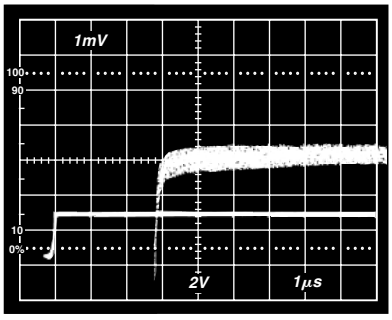
*REFERENCE DECOUPLING COMPONENTS AS PER FIGURE 8

TPC 2. Noise Spectral Density vs. Frequency

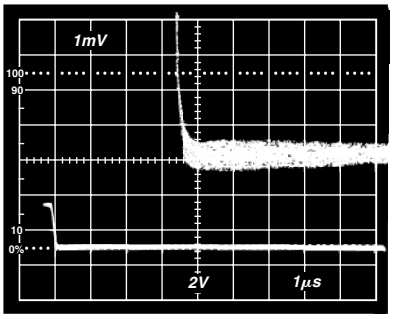


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF AND 0.1μF

TPC 5. Power Supply Rejection Ration vs. Frequency



TPC 3. Positive-Going Settling Time
(V_{DD} = +15 V, V_{SS} = –15 V)



TPC 6. Negative Going Settling Time
(V_{DD} = +15 V, V_{SS} = –15 V)

CIRCUIT INFORMATION

D/A SECTION

The AD7245A/AD7248A contains a 12-bit voltage mode digital-to-analog converter. The output voltage from the converter has the same positive polarity as the reference voltage allowing single supply operation. The reference voltage for the DAC is provided by an on-chip buried Zener diode.

The DAC consists of a highly stable, thin-film, R–2R ladder and twelve high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

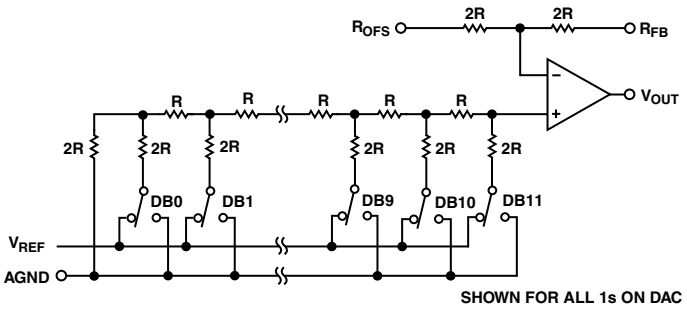


Figure 1. D/A Simplified Circuit Diagram

The input impedance of the DAC is code dependent and can vary from 8 kΩ to infinity. The input capacitance also varies with code, typically from 50 pF to 200 pF.

OP AMP SECTION

The output of the voltage mode D/A converter is buffered by a noninverting CMOS amplifier. The user has access to two gain setting resistors which can be connected to allow different output voltage ranges (discussed later). The buffer amplifier is capable of developing up to 10 V across a 2 kΩ load to GND.

The output amplifier can be operated from a single positive power supply by tying V_{SS} = AGND = 0 V. The amplifier can also be operated from dual supplies to allow a bipolar output range of –5 V to +5 V. The advantages of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0 V, full sink capability of 2.5 mA maintained over the entire output range and elimination of the effects of negative offset on the transfer characteristic (outlined previously). Figure 2 shows the sink capability of the amplifier for single supply operation.

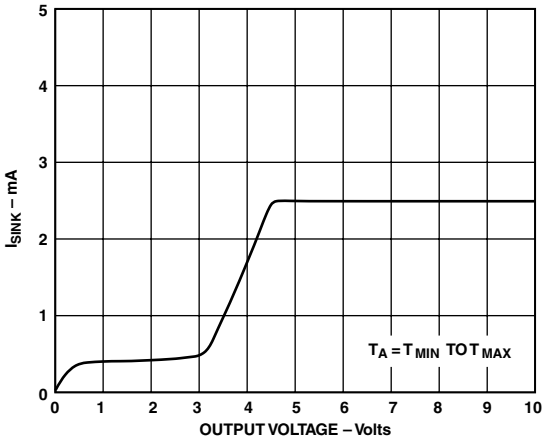


Figure 2. Typical Single Supply Sink Current vs. Output Voltage

The small signal (200 mV p-p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 25 nV/√Hz at a frequency of 1 kHz. The broadband noise from the amplifier has a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. There is no significant difference in the output noise between single and dual supply operation.

VOLTAGE REFERENCE

The AD7245A/AD7248A contains an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. The reference is internally connected to the DAC. Since the DAC has a variable input impedance at its reference input the Zener diode reference is buffered. This buffered reference is available to the user to drive the circuitry required for bipolar output ranges. It can be used as a reference for other parts in the system provided it is externally buffered. The reference will give long-term stability comparable with the best discrete Zener reference diodes. The performance of the AD7245A/AD7248A is specified with internal reference, and all the testing and trimming is done with this reference. The reference should be decoupled at the REF OUT pin and recommended decoupling components are 10 μF and 0.1 μF capacitors in series with a 10 Ω resistor. A simplified schematic of the reference circuitry is shown in Figure 3.

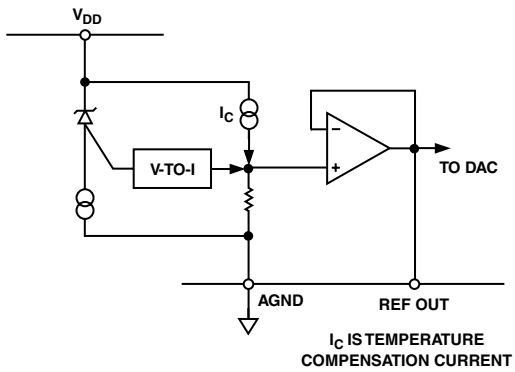


Figure 3. Internal Reference

DIGITAL SECTION

The AD7245A/AD7248A digital inputs are compatible with either TTL or 5 V CMOS levels. All data inputs are static protected MOS gates with typical input currents of less than 1 nA. The control inputs sink higher currents (150 μA max) as a result of the fast digital interfacing. Internal input protection of all logic inputs is achieved by on-chip distributed diodes.

The AD7245A/AD7248A features a very low digital feedthrough figure of 10 nV-s in a 5 V output range. This is due to the voltage mode configuration of the DAC. Most of the impulse is actually as a result of feedthrough across the package.

INTERFACE LOGIC INFORMATION—AD7245A

Table I shows the truth table for AD7245A operation. The part contains two 12-bit latches, an input latch and a DAC latch. $\overline{CS}$ and $\overline{WR}$ control the loading of the input latch while $\overline{LDAC}$ controls the transfer of information from the input latch to the DAC latch. All control signals are level triggered; and therefore, either or both latches may be made transparent, the input latch by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC latch by keeping $\overline{LDAC}$ "LOW." Input data is latched on the rising edge of $\overline{WR}$.

The data held in the DAC latch determines the analog output of the converter. Data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. This $\overline{LDAC}$ signal is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. For example, if $\overline{LDAC}$ goes LOW while $\overline{WR}$ is "LOW," then the $\overline{LDAC}$ signal must stay LOW for t_7 or longer after $\overline{WR}$ goes high to ensure correct data is latched through to the output.

Table I. AD7245A Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Latches are Transparent
H	H	H	X	Both Latches are Latched
H	H	X	H	Both Latches are Latched
H	H	L	L	Input Latches Transparent
H	H	↓	L	Input Latches Latched
H	L	H	H	DAC Latches Transparent
H	↓	H	H	DAC Latches Latched
L	X	X	X	DAC Latches Loaded with all 0s
↓	H	H	H	DAC Latches Latched with All 0s and Output Remains at 0 V or –5 V
↓	L	L	L	Both Latches are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

The contents of the DAC latch are reset to all 0s by a low level on the $\overline{CLR}$ line. With both latches transparent, the $\overline{CLR}$ line functions like a zero override with the output brought to 0 V in the unipolar mode and –5 V in the bipolar mode for the duration of the $\overline{CLR}$ pulse. If both latches are latched, a "LOW" pulse on the $\overline{CLR}$ input latches all 0s into the DAC latch and the output remains at 0 V (or –5 V) after the $\overline{CLR}$ line has returned "HIGH." The $\overline{CLR}$ line can be used to ensure power-up to 0 V on the AD7245A output in unipolar operation and is also useful, when used as a zero override, in system calibration cycles.

Figure 4 shows the input control logic for the AD7245A and the write cycle timing for the part is shown in Figure 5.

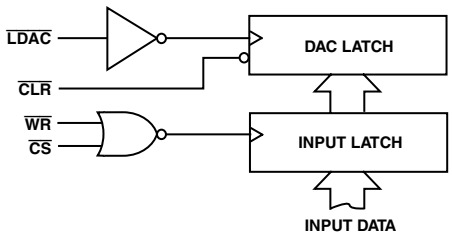


Figure 4. AD7245A Input Control Logic

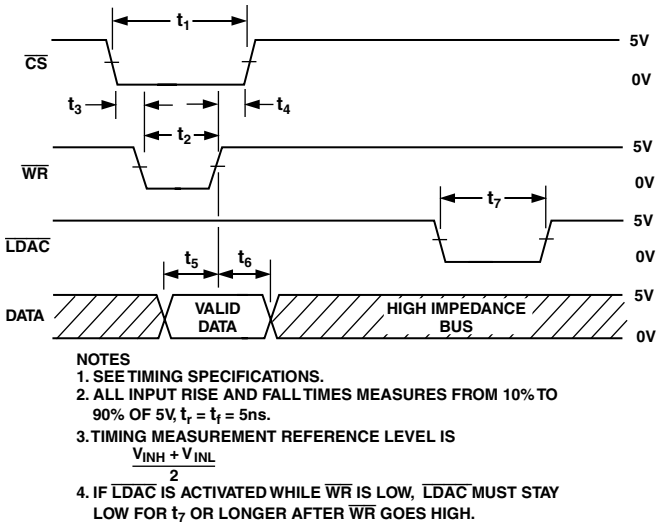


Figure 5. AD7245A Write Cycle Timing Diagram

INTERFACE LOGIC INFORMATION—AD7248A

The input loading structure on the AD7248A is configured for interfacing to microprocessors with an 8-bit wide data bus. The part contains two 12-bit latches—an input latch and a DAC latch. Only the data held in the DAC latch determines the analog output from the converter. The truth table for AD7248A operation is shown in Table II, while the input control logic diagram is shown in Figure 6.

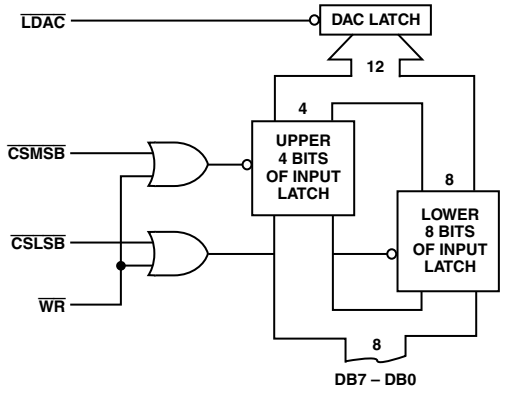


Figure 6. AD7248A Input Control Logic

$\overline{CSMSB}$, $\overline{CSLSB}$ and $\overline{WR}$ control the loading of data from the external data bus to the input latch. The eight data inputs on the AD7248A accept right justified data. This data is loaded to the input latch in two separate write operations. $\overline{CSLSB}$ and $\overline{WR}$ control the loading of the lower 8-bits into the 12-bit wide latch. The loading of the upper 4-bit nibble is controlled by $\overline{CSMSB}$ and $\overline{WR}$. All control inputs are level triggered, and input data for either the lower byte or upper 4-bit nibble is latched into the input latches on the rising edge of $\overline{WR}$ (or either $\overline{CSMSB}$ or $\overline{CSLSB}$). The order in which the data is loaded to the input latch (i.e., lower byte or upper 4-bit nibble first) is not important.

The $\overline{\text{LDAC}}$ input controls the transfer of 12-bit data from the input latch to the DAC latch. This $\overline{\text{LDAC}}$ signal is also level triggered, and data is latched into the DAC latch on the rising edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ input is asynchronous and independent of $\overline{\text{WR}}$. This is useful in many applications especially in the simultaneous updating of multiple AD7248A outputs. However, in systems where the asynchronous LDAC can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if LDAC goes low while WR and either CS input are low (or WR and either CS go low while LDAC is low), then the LDAC signal must stay low for t_7 or longer after WR returns high to ensure correct data is latched through to the output. The write cycle timing diagram for the AD7248A is shown in Figure 7.

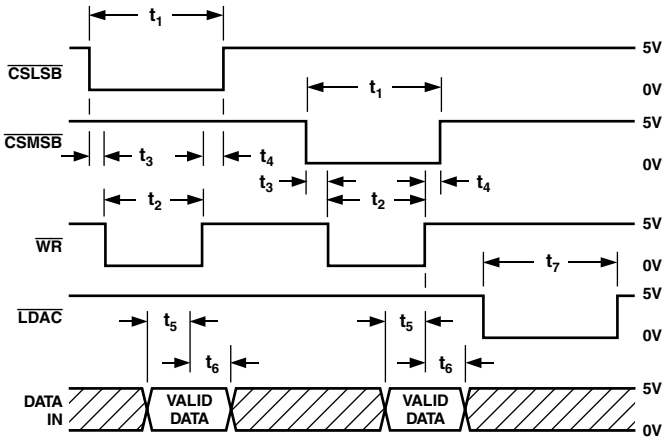


Figure 7. AD7248A Write Cycle Timing Diagram

An alternate scheme for writing data to the AD7248A is to tie the $\overline{\text{CSMSB}}$ and $\overline{\text{LDAC}}$ inputs together. In this case exercising $\overline{\text{CSLSB}}$ and $\overline{\text{WR}}$ latches the lower 8 bits into the input latch. The second write, which exercises $\overline{\text{CSMSB}}$, $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ loads the upper 4-bit nibble to the input latch and at the same time transfers the 12-bit data to the DAC latch. This automatic transfer mode updates the output of the AD7248A in two write operations. This scheme works equally well for $\overline{\text{CSLSB}}$ and $\overline{\text{LDAC}}$ tied together provided the upper 4-bit nibble is loaded to the input latch followed by a write to the lower 8 bits of the input latch.

Table II. AD7248A Truth Table

$\overline{\text{CSLSB}}$	$\overline{\text{CSMSB}}$	$\overline{\text{WR}}$	$\overline{\text{LDAC}}$	Function
L	H	L	H	Load LS Byte into Input Latch
L	H	↓	H	Latches LS Byte into Input Latch
↓	H	L	H	Latches LS Byte into Input Latch
H	L	L	H	Loads MS Nibble into Input Latch
H	L	↓	H	Latches MS Nibble into Input Latch
H	↓	L	H	Latches MS Nibble into Input Latch
H	H	H	L	Loads Input Latch into DAC Latch
H	H	H	↓	Latches Input Latch into DAC Latch
H	L	L	L	Loads MS Nibble into Input Latch and Loads Input Latch into DAC Latch
H	H	H	H	No Data Transfer Operation

H = High State, L = Low State

APPLYING THE AD7245A/AD7248A

The internal scaling resistors provided on the AD7245A/AD7248A allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to 5 V or 0 V to 10 V and a bipolar output range of –5 V to +5 V. Connections for the various ranges are outlined below.

UNIPOLAR (0 V TO 10 V) CONFIGURATION

The first of the configurations provides an output voltage range of 0 V to 10 V. This is achieved by connecting the bipolar offset resistor, R_{OFS}, to AGND and connecting R_{FB} to V_{OUT}. In this configuration the AD7245A/AD7248A can be operated single supply (V_{SS} = 0 V = AGND). If dual supply performance is required, a V_{SS} of –12 V to –15 V should be applied. Figure 8 shows the connection diagram for unipolar operation while the table for output voltage versus the digital code in the DAC latch is shown in Table III.

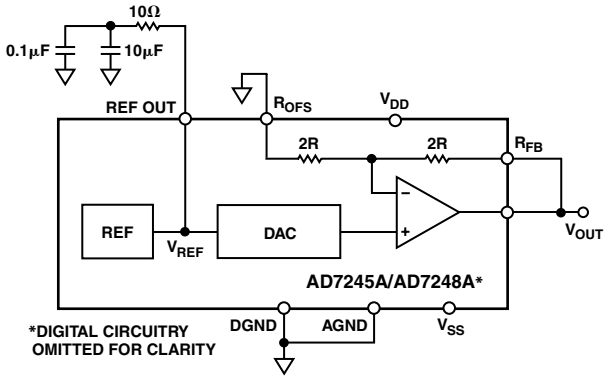


Figure 8. Unipolar (0 to 10 V) Configuration

Table III. Unipolar Code Table (0 V to 10 V Range)

DAC Latch Contents MSB		LSB	Analog Output, V_{OUT}
1 1 1 1	1 1 1 1	1 1 1 1	$+2\ V_{REF} \times \left(\frac{4095}{4096}\right)$
			$V_{REF} \times \left(\frac{2049}{4096}\right)$
			$V_{REF} \times \left(\frac{2048}{4096}\right) = +V_{REF}$
			$V_{REF} \times \left(\frac{2047}{4096}\right)$
			$V_{REF} \times \left(\frac{1}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 0	0 V

NOTE: $1\ LSB = 2 \times V_{REF}(2^{-12}) = V_{REF}\left(\frac{1}{2048}\right)$

UNIPOLAR (0 V TO 5 V) CONFIGURATION

The 0 V to 5 V output voltage range is achieved by tying R_{OFS}, R_{FB} and V_{OUT} together. For this output range the AD7245A/AD7248A can be operated single supply (V_{SS} = 0 V) or dual supply. The table for output voltage versus digital code is as in Table III, with 2 × V_{REF} replaced by V_{REF}. Note that for this range

$$1\ LSB = V_{REF}(2^{-12}) = V_{REF} \times \left(\frac{1}{4096}\right)$$

BIPOLAR CONFIGURATION

The bipolar configuration for the AD7245A/AD7248A, which gives an output voltage range from –5 V to +5 V, is achieved by connecting the R_{OFS} input to REF OUT and connecting R_{FB} and V_{OUT}. The AD7245A/AD7248A must be operated from dual supplies to achieve this output voltage range. The code table for bipolar operation is shown in Table IV.

Table IV. Bipolar Code Table

DAC Latch Contents MSB		LSB	Analog Output, V_{OUT}
1 1 1 1	1 1 1 1	1 1 1 1	$+V_{REF} \times \left(\frac{2047}{2048}\right)$
			$V_{REF} \times \left(\frac{1}{2048}\right)$
0 1 1 1	1 1 1 1	1 1 1 1	$-V_{REF} \times \left(\frac{1}{2048}\right)$
			$-V_{REF} \times \left(\frac{2047}{2048}\right)$
0 0 0 0	0 0 0 0	0 0 0 0	$-V_{REF} \times \left(\frac{2048}{2048}\right) = -V_{REF}$

$$LSB = 2 \times V_{REF}(2^{-11}) = V_{REF}\left(\frac{1}{2048}\right)$$

The AD7245A/AD7248A AGND pin can be biased above system GND (AD7245A/AD7248A DGND) to provide an offset "zero" analog output voltage level. With unity gain on the amplifier (R_{OFS} = V_{OUT} = R_{FB}) the output voltage, V_{OUT} is expressed as:

$$V_{OUT} = V_{BIAS} + D \times V_{REF}$$

where D is a fractional representation of the digital word in the DAC latch and V_{BIAS} is the voltage applied to the AD7245A/AD7248A AGND pin.

Because the current flowing out of the AGND pin varies with digital code, the AGND pin should be driven from a low impedance source. A circuit configuration is outlined for AGND bias in Figure 9 using the AD589, a +1.23 V bandgap reference.

If a gain of 2 is used on the buffer amplifier the output voltage, V_{OUT} is expressed as

$$V_{OUT} = 2(V_{BIAS} + D \times V_{REF})$$

In this case care must be taken to ensure that the maximum output voltage is not greater than V_{DD} –3 V. The V_{DD}–V_{OUT} overhead must be greater than 3 V to ensure correct operation of the part. Note that V_{DD} and V_{SS} for the AD7245A/AD7248A must be referenced to DGND (system GND). The entire circuit can be operated in single supply with the V_{SS} pin of the AD7245A/AD7248A connected to system GND.

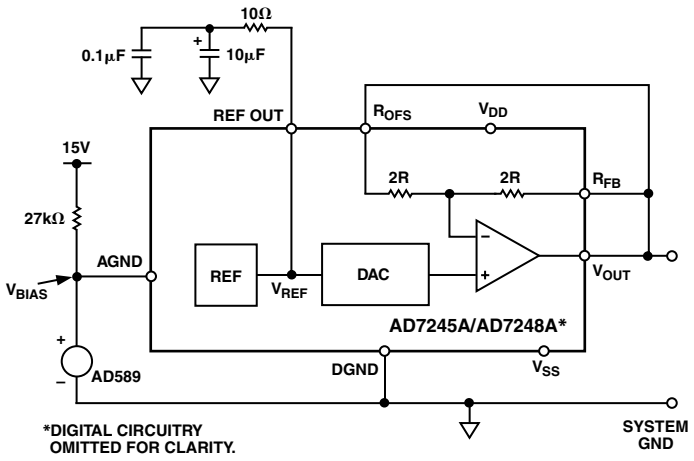


Figure 9. AGND Bias Circuit

PROGRAMMABLE CURRENT SINK

Figure 10 shows how the AD7245A/AD7248A can be configured with a power MOSFET transistor, the VN0300M, to provide a programmable current sink from V_{DD} or V_{SOURCE}. The VN0300M is placed in the feedback of the AD7245A/AD7248A amplifier. The entire circuit can be operated in single supply by tying the V_{SS} of the AD7245A/AD7248A to AGND. The sink current, I_{SINK}, can be expressed as:

$$I_{SINK} = \frac{D \times V_{REF}}{R1}$$

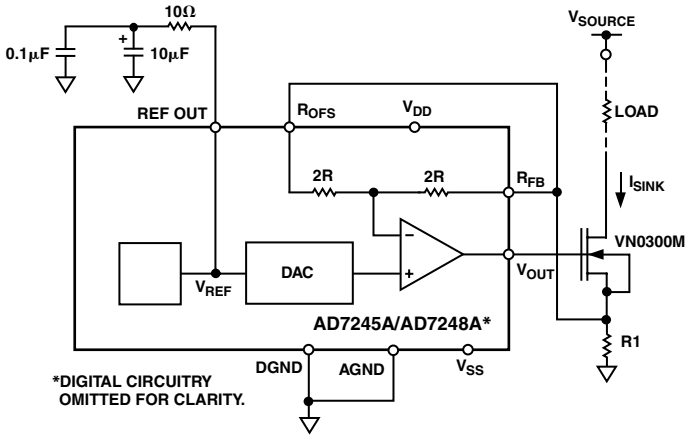


Figure 10. Programmable Current Sink

Using the VN0300M, the voltage drop across the load can typically be as large as V_{SOURCE} –6 V) with V_{OUT} of the DAC at 5 V. Therefore, for a current of 50 mA flowing in the R1 (with all 1s in the DAC register) the maximum load is 200 Ω with V_{SOURCE} = 15 V. The VN0300M can actually handle currents up to 500 mA and still function correctly in the circuit, but in practice the circuit must be used with larger values of V_{SOURCE} otherwise it requires a very small load.

Since the tolerance value on the reference voltage of the AD7245A/AD7248A is ±0.2%, then the absolute value of I_{SINK} can vary by ±0.2% from device to device for a fixed value of R1.

Because the input bias current of the AD7245A/AD7248A's op amp is only of the order of picoamps, its effect on the sink current is negligible. Tying the R_{OFS} input to R_{FB} input reduces this effect even further and prevents noise pickup which could occur if the R_{OFS} pin was left unconnected.

The circuit of Figure 10 can be modified to provide a programmable current source to AGND or $-V_{SINK}$ (for $-V_{SINK}$, dual supplies are required on the AD7245A/AD7248A). The AD7245A/AD7248A is configured as before. The current through R1 is mirrored with a current mirror circuit to provide the programmable source current (see CMOS DAC Application Guide, Publication No. G872-30-10/84, for suitable current mirror circuit). As before the absolute value of the source current will be affected by the ±0.2% tolerance on V_{REF}. In this case the performance of the current mirror will also affect the value of the source current.

FUNCTION GENERATOR WITH PROGRAMMABLE FREQUENCY

Figure 11 shows how the AD7245A/AD7248A with the AD537, voltage-to-frequency converter and the AD639, trigonometric function generator to provide a complete function generator with programmable frequency. The circuit provides square wave, triwave and sine wave outputs, each output of ±10 V amplitude.

The AD7245A/AD7248A provides a programmable voltage to the AD537 input. Since both the AD7245A/AD7248A and AD537 are guaranteed monotonic, the output frequency will always increase with increasing digital code. The AD537 provides a square wave output which is conditioned for ±10 V by amplifier A1. The AD537 also provides a differential triwave output. This is conditioned by amplifiers A2 and A3 to provide the ±1.8 V triwave required at the input of the AD639. The triwave is further scaled by amplifier A4 to provide a ±10 V output.

Adjusting the triwave applied to the AD639 adjust the distortion performance of the sine wave output, (10 V in configuration shown). Amplitude, offset and symmetry of the triwave can affect the distortion. By adjusting these, via VR1 and VR2, an output sine wave with harmonic distortion of better than –50 dB can be achieved at low and intermediate frequencies.

Using the capacitor value shown in Figure 11 for C_F (i.e., 680 pF) the output frequency range is 0 to 100 kHz over the digital input code range. The step size for frequency increments is 25 Hz. The accuracy of the output frequency is limited to 8 or 9 bits by the AD537, but is guaranteed monotonic to 12 bits.

MICROPROCESSOR INTERFACING—AD7245

AD7245A—8086 INTERFACE

Figure 12 shows the 8086 16-bit processor interfacing to the AD7245A. In the setup shown in Figure 12, the double buffering feature of the DAC is not used and the $\overline{LDAC}$ input is tied LOW. AD0–AD11 of the 16-bit data bus are connected to the AD7245A data bus (DB0–DB11). The 12-bit word is written to the AD7245A in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 12 is given in Table V.

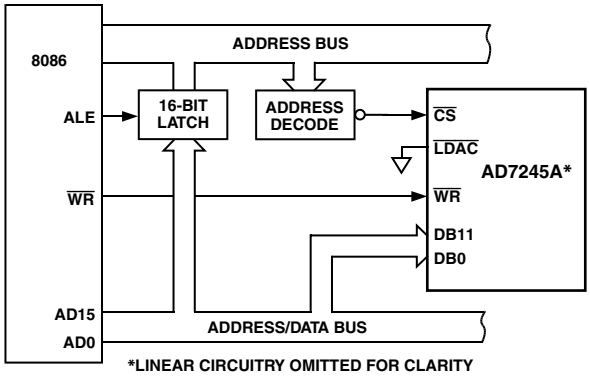


Figure 12. AD7245A to 8086 Interface

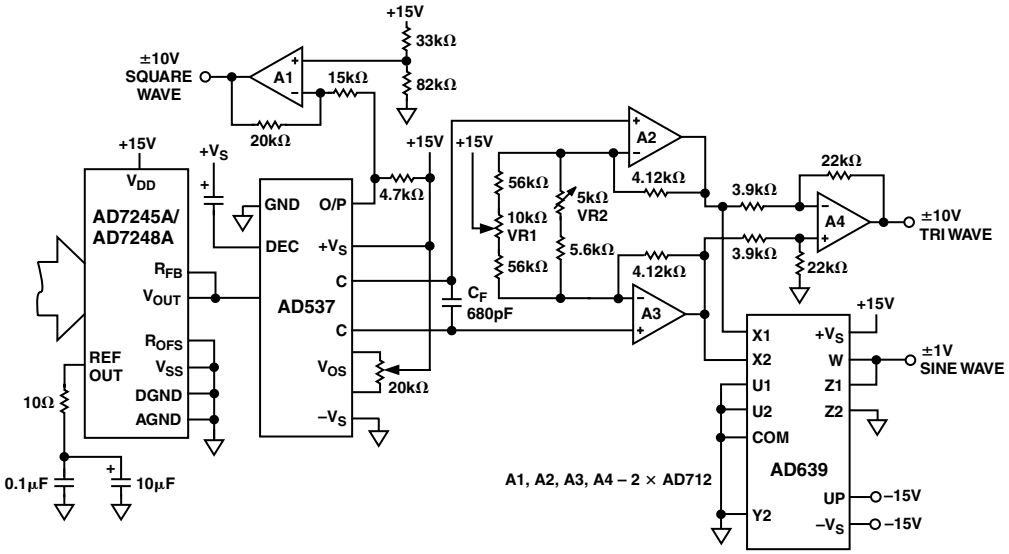


Figure 11. Programmable Function Generator

Table V. Sample Program for Loading AD7245A from 8086

ASSUME DS: DACLOAD, CS: DACLOAD DACLOAD SEGMENT AT 000			
00	8CC9	MOV CS, CS	: DEFINE DATA SEGMENT REGISTER
02	8ED9	MOV DS, CX	: EQUAL TO CODE SEGMENT REGISTER
04	BF00D0	0MOV DI, #D000	: LOAD DI WITH D000
07	C705 "YZWX"	MOV MEM, #YZWX	: DAC LOADED WITH WXYZ
0B 0E	EA00 00 00 FF		: CONTROL IS RETURNED TO THE MONITOR PROGRAM

In a multiple DAC system the double buffering of the AD7245A allows the user to simultaneously update all DACs. In Figure 13, a 12-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought LOW, updating all the DACs simultaneously.

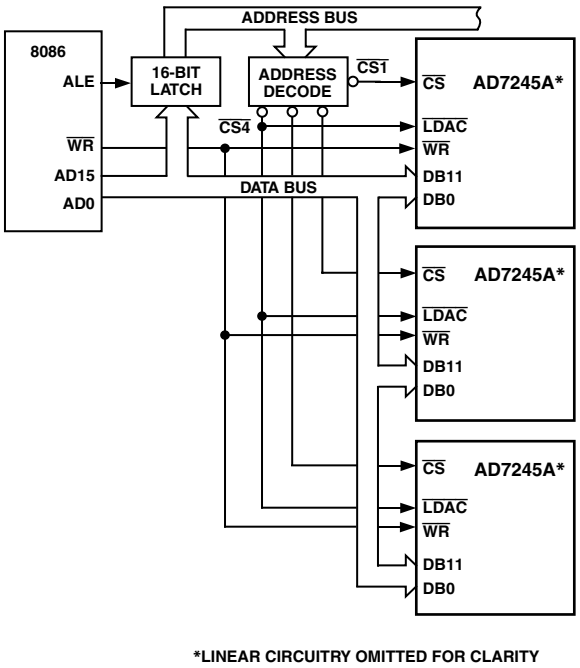


Figure 13. AD7245A to 8086 Multiple DAC Interface

AD7245A—MC68000 INTERFACE

Interfacing between the MC68000 and the AD7245A is accomplished using the circuit of Figure 14. Once again the AD7245A is used in the single buffered mode. A software routine for loading data to the AD7245A is given in Table VI. In this example the AD7245A is located at address E000, and the 12-bit word is written to the DAC in one MOVE instruction.

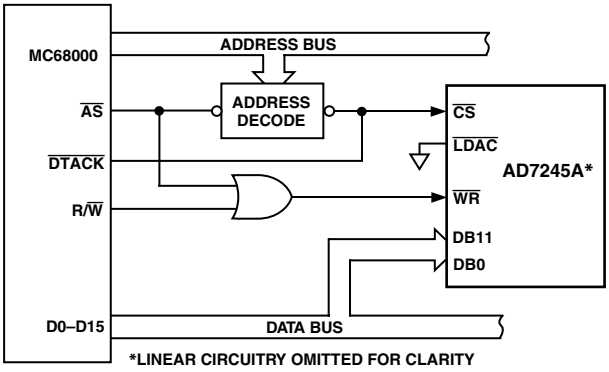


Figure 14. AD7245A to MC68000 Interface

Table VI. Sample Routine for Loading AD7245A from 68000

01000	MOVE.W	#X,D0	The desired DAC data, X, is loaded into Data Register 0. X may be any value between 0 and 4094 (decimal) or 0 and OFFF (hexadecimal).
	MOVE.W	D0,$E000	The Data X is transferred between D0 and the DAC Latch.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	#14	

MICROPROCESSOR INTERFACE—AD7248A

Figure 15 shows the connection diagram for interfacing the AD7248A to both the 8085A and 8088 microprocessors. This scheme is also suited to the Z80 microprocessor, but the Z80 address/data bus does not have to be demultiplexed. Data to be loaded to the AD7248A is right justified. The AD7248A is memory mapped with a separate memory address for the input latch high byte, the input latch low byte and the DAC latch. Data is first written to the AD7248A input latch in two write operations. Either the high byte or the low byte data can be written first to the AD7248A input latch. A write to the AD7248A DAC latch address transfers the input latch data to the DAC latch and updates the output voltage. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7248As for simultaneous updating of a number of voltage channels.

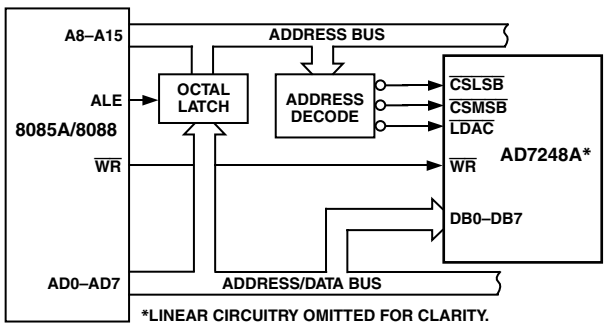


Figure 15. AD7248A to 8085A/8088 Interface

A connection diagram for the interface between the AD7248A and 68008 microprocessor is shown in Figure 16. Once again the AD7248A acts as a memory mapped device and data is right justified. In this case the AD7248A is configured in the automatic transfer mode which means that the high byte of the input latch has the same address as the DAC latch. Data is written to the AD7248A by first writing data to the AD7248A low byte. Writing data to the high byte of the input latch also transfers the input latch contents to the DAC latch and updates the output.

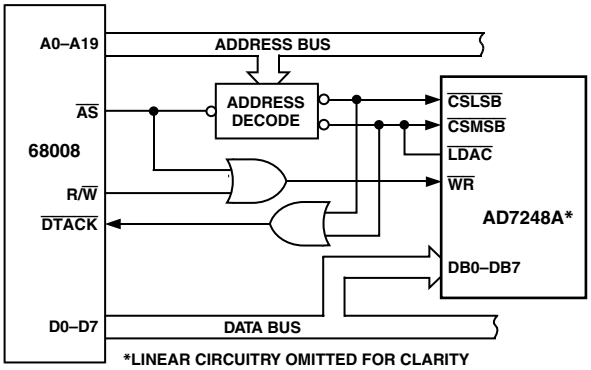


Figure 16. AD7248A to 68008 Interface

An interface circuit for connections to the 6502 or 6809 microprocessors is shown in Figure 17. Once again, the AD7248A is memory mapped and data is right justified. The procedure for writing data to the AD7248A is as outlined for the 8085A/8088. For the 6502 microprocessor the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

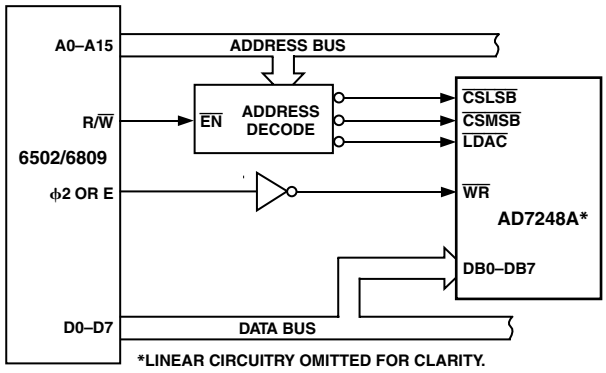


Figure 17. AD7248A to 6502/6809 Interface

Figure 18 shows a connection diagram between the AD7248A and the 8051 microprocessor. The AD7248A is port mapped in this interface and is configured in the automatic transfer mode. Data to be loaded to the input latch low byte is output to Port 1. Output Line P3.0, which is connected to $\overline{CSLSB}$ of the AD7248A, is pulsed to load data into the low byte of the input latch. Pulsing the P3.1 line, after the high byte data has been set up on Port 1, updates the output of the AD7248A. The $\overline{WR}$ input of the AD7248A can be hardwired low in this application because spurious address strobes on $\overline{CSLSB}$ and $\overline{CSMSB}$ do not occur.

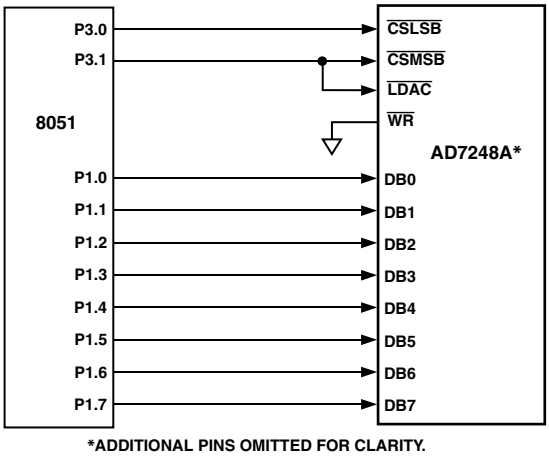


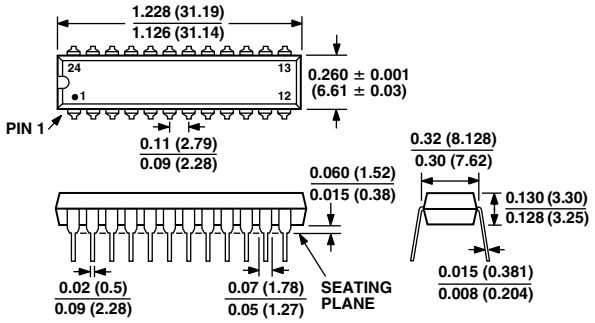
Figure 18. AD7248A to MCS-51 Interface

MECHANICAL INFORMATION—AD7245A

OUTLINE DIMENSIONS

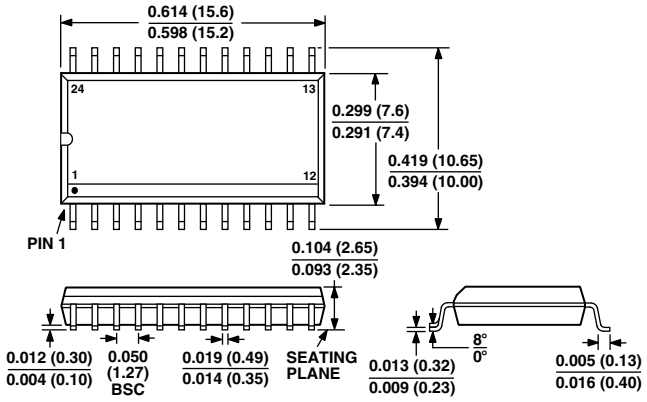
Dimensions shown in inches and (mm).

24-Lead Plastic DIP
(N-24)

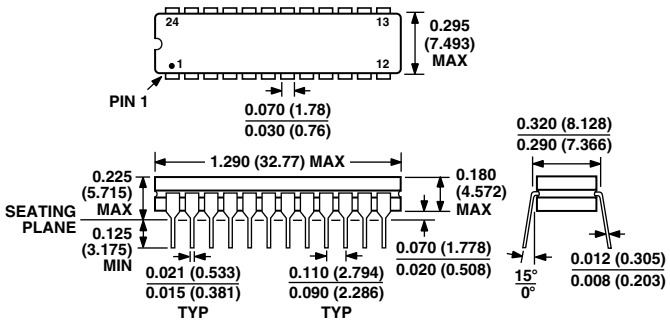


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

24-Lead SOIC
(R-24)

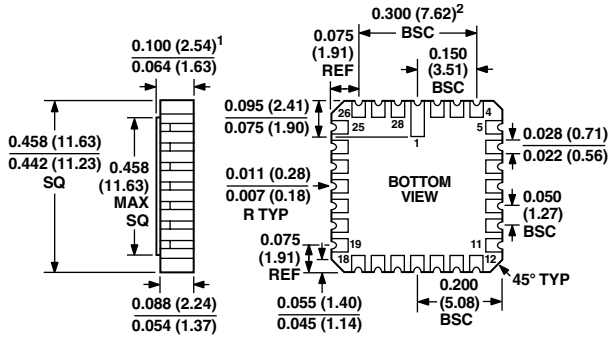


(Q-24)



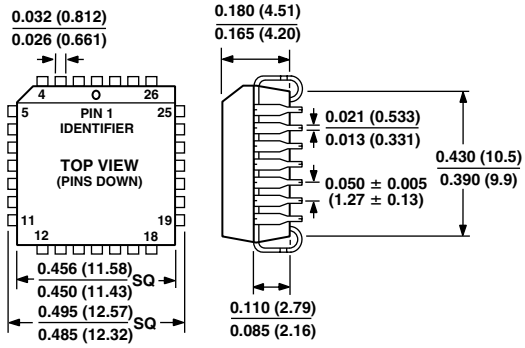
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

Leadless Ceramic Chip Carrier
(E-28A)



NOTES
[1]THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2]APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED

Plastic Leaded Chip Carrier
(P-28A)

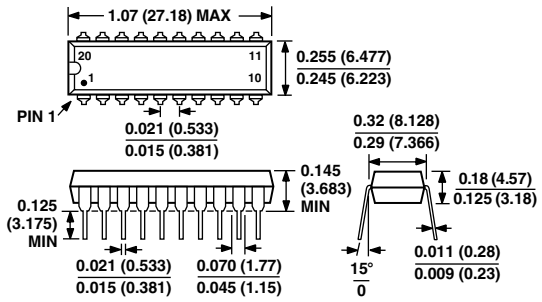


MECHANICAL INFORMATION —AD7248A

OUTLINE DIMENSIONS

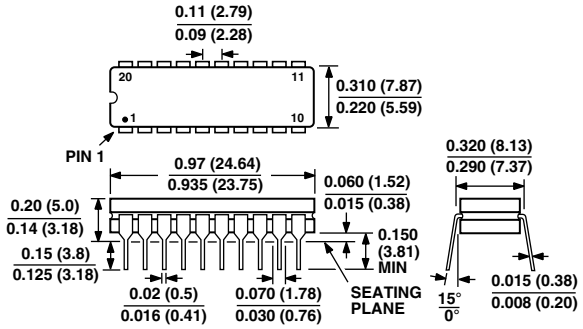
Dimensions shown in inches and (mm).

20-Lead Plastic DIP
(N-20)



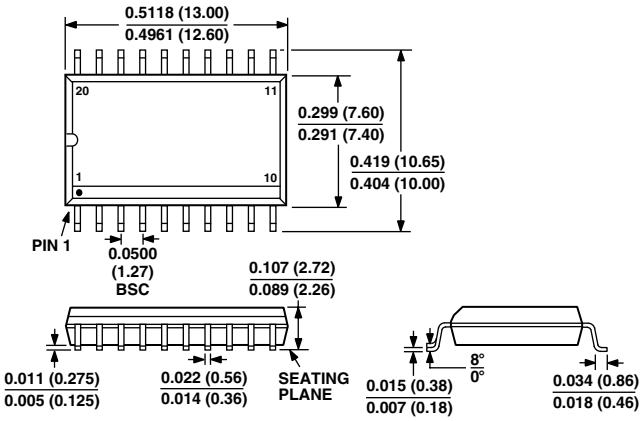
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

(Q-20)

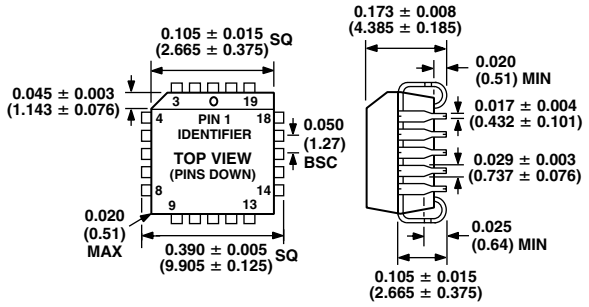


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

(R-20)



Plastic Leaded Chip Carrier
(P-20A)



Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Changed V_{DD} = 15 V ± 5% to V_{DD} = 15 V ± 10% in Static Performance section in Test Conditions/Comments column	2
Changed A Version of Full-Scale Temperature Coefficient from ±30 to ±40	2
Changed B and T Versions of V_{DD} Power Requirements from +11.4/+15.75 to +10.8/+16.5 for V min. Changed B and T Versions of V_{SS} Power Requirements from –11.4/–15.75 to –10.8/–16.5 for V max	2
Change to Note 1 and Note 9 of Specifications table	2
Change to Note 2 in Switching Characteristics	3
Changes to R-24 Package Outline	15

PRINTED IN U.S.A.