Low Cost, Low Power CMOS General Purpose Analog Front End

AD73311L

FEATURES

16-Bit A/D Converter
16-Bit D/A Converter
Programmable Input/Output Sample Rates
76 dB ADC SNR
77 dB DAC SNR
Programmable Sampling Rate
64 kS/s Maximum Sample Rate
–90 dB Crosstalk
Low Group Delay (25 ms Typ per ADC Channel, 50 ms Typ per DAC Channel)
Programmable Input/Output Gain
Flexible Serial Port Which Allows Up to Eight Devices to Be Connected in Cascade
Single (+3 V) Supply Operation
33 mW Max Power Consumption at 2.7 V
On-Chip Reference
20-Lead SOIC/SSOP/TSSOP Packages

APPLICATIONS

General Purpose Analog I/O
Speech Processing
Cordless and Personal Communications
Telephony
Active Control of Sound and Vibration
Data Communications

GENERAL DESCRIPTION

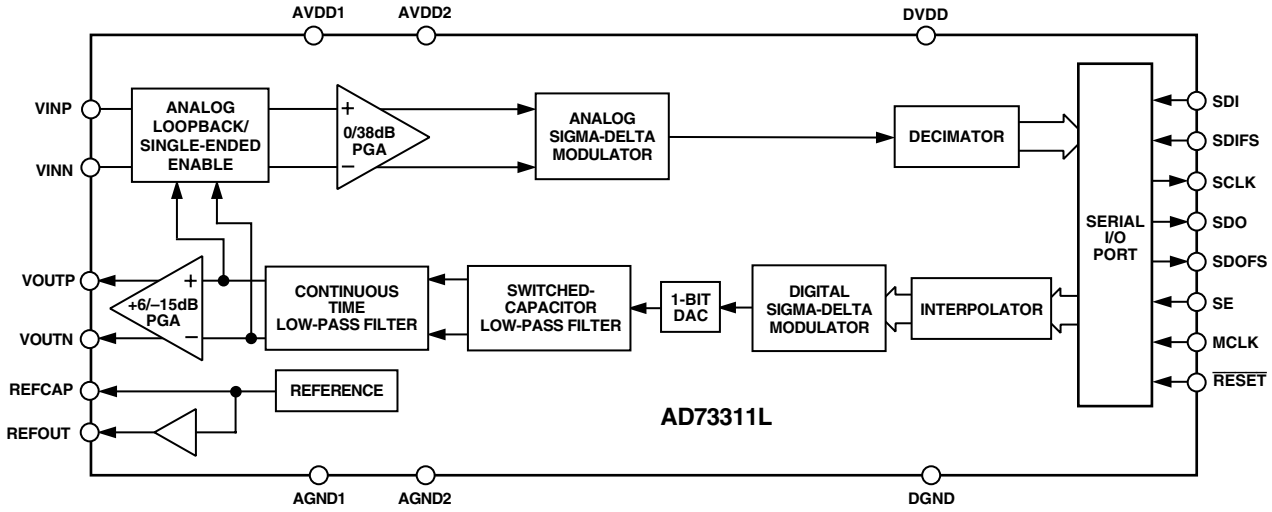
The AD73311L is a complete front-end processor for general purpose applications including speech and telephony. It features a 16-bit A/D conversion channel and a 16-bit D/A conversion channel. Each channel provides 70 dB signal-to-noise ratio over a voiceband signal bandwidth. The final channel bandwidth can be reduced, and signal-to-noise ratio improved, by external digital filtering in a DSP engine.

The AD73311L is suitable for a variety of applications in the speech and telephony area, including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multichannel active control applications.

The gains of the A/D and D/A conversion channels are programmable over 38 dB and 21 dB ranges respectively. An on-chip reference voltage is included to allow single supply operation. A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines.

The AD73311L is available in 20-lead SOIC, SSOP and TSSOP packages.

FUNCTIONAL BLOCK DIAGRAM



REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2000

AD73311L–SPECIFICATIONS[1] (AVDD = DVDD = 2.7 V to 3.3 V; DGND = AGND = 0 V, f_{DMCLK} = 16.384 MHz, F_S = 8 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD73311LA Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE					
REFCAP					
Absolute Voltage, V_{REFCAP}	1.08	1.2	1.32	V	
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from
REFOUT					REFCAP to AGND2
Typical Output Impedance		145		Ω	
Absolute Voltage, V_{REFOUT}	1.08	1.2	1.32	V	Unloaded
Minimum Load Resistance	1			kΩ	
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]		1.578		V p-p	Measured Differentially
		–2.85		dBm	Max Input = (1.578/1.2) × V_{REFCAP}
Nominal Reference Level at VIN		1.0954		V p-p	Measured Differentially
(0 dBm0)		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–2.2	–0.6	+1.0	dB	1.0 kHz, 0 dBm0
PGA = 38 dB		–1.0		dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					Refer to Figure 5a
PGA = 0 dB	71	76		dB	300 Hz to 3400 Hz
	70	74		dB	0 Hz to f_{SAMP}/2
		72		dB	300 Hz to 3400 Hz; f_{SAMP} = 64 kHz
		56		dB	0 Hz to f_{SAMP}/2; f_{SAMP} = 64 kHz
PGA = 38 dB		60		dB	300 Hz to 3.4 kHz
		59		dB	0 Hz to f_{SAMP}/2
Total Harmonic Distortion					
PGA = 0 dB		–85	–75	dB	300 Hz to 3.4 kHz
PGA = 38 dB		–85		dB	300 Hz to 3.4 kHz
Intermodulation Distortion		–82		dB	PGA = 0 dB
Idle Channel Noise		–76		dBm0	PGA = 0 dB
Crosstalk		–100		dB	ADC Input Signal Level: 1.0 kHz, 0 dBm0
					DAC Input at Idle
DC Offset	–20	+2	+25	mV	PGA = 0 dB
Power Supply Rejection		–84		dB	Input Signal Level at AVDD and DVDD
					Pins 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	64 kHz Output Sample Rate
Input Resistance at VIN[2, 4]		45		kΩ[6]	DMCLK = 16.384 MHz
DAC SPECIFICATIONS					
Maximum Voltage Output Swing[2]					
Single-Ended		1.578		V p-p	PGA = 6 dB
		–2.85		dBm	Max Output = (1.578/1.2) × V_{REFCAP}
Differential		3.156		V p-p	PGA = 6 dB
		3.17		dBm	Max Output = 2 × ((1.578/1.2) × V_{REFCAP}
Nominal Voltage Output Swing (0 dBm0)					
Single-Ended		1.0954		V p-p	PGA = 6 dB
		–6.02		dBm	
Differential		2.1909		V p-p	PGA = 6 dB
		0		dBm	
Output Bias Voltage[4]	1.08	1.2	1.32	V	REFOUT Unloaded
Absolute Gain	–1.8	–0.7	+0.4	dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					Refer to Figure 5b
PGA = 0 dB	70	77		dB	300 Hz to 3.4 kHz Frequency Range
		76		dB	300 Hz to 3400 Hz; f_{SAMP} = 64 kHz
PGA = 6 dB		77		dB	300 Hz to 3.4 kHz Frequency Range
		77		dB	300 Hz to 3400 Hz; f_{SAMP} = 64 kHz
Total Harmonic Distortion					
PGA = 0 dB		–80	–70	dB	
PGA = 6 dB		–80		dB	
Intermodulation Distortion		–76		dB	PGA = 0 dB
Idle Channel Noise		–82		dBm0	PGA = 0 dB
Crosstalk		–100		dB	ADC Input Signal Level: AGND; DAC
					Output Signal Level: 1.0 kHz, 0 dBm0

Parameter	AD73311LA Min	Typ	Max	Unit	Test Conditions/Comments
DAC SPECIFICATIONS (Continued)					
Power Supply Rejection		–81		dB	Input Signal Level at AVDD and DVDD Pins: 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	64 kHz Input Sample Rate, Interpolator Bypassed (CRE:5 = 1)
Output DC Offset[2, 7]	–30	+5	+50	mV	PGA = 6 dB
Minimum Load Resistance, R_L[2, 8]					
Single-Ended	150			Ω	
Differential	150			Ω	
Maximum Load Capacitance, C_L[2, 8]					
Single-Ended			500	pF	
Differential			100	pF	
FREQUENCY RESPONSE					
(ADC AND DAC)[9] Typical Output					Normalized to f_{SAMP}
0		0		dB	
0.03125		–0.1		dB	
0.0625		–0.25		dB	
0.125		–0.6		dB	
0.1875		–1.4		dB	
0.25		–2.8		dB	
0.3125		–4.5		dB	Channel Frequency Response Is
0.375		–7.0		dB	Programmable by Means of External
0.4375		–9.5		dB	Digital Filtering
> 0.5		< –12.5		dB	
LOGIC INPUTS					
V_{INH}, Input High Voltage	V_{DD} – 0.8		V_{DD}	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current			10	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	V_{DD} – 0.4		V_{DD}	V	|IOUT| ≤ 100 µA
V_{OL}, Output Low Voltage	0		0.4	V	|IOUT| ≤ 100 µA
Three-State Leakage Current	–10		+10	µA	
POWER SUPPLIES					
AVDD1, AVDD2	2.7		3.3	V	
DVDD	2.7		3.3	V	
I_{DD}[10]					See Table I

NOTES
[1]Operating temperature range is as follows: –40°C to +105°C. Therefore, T_{MIN} = –40°C and T_{MAX} = +105°C.
[2]Test conditions: Input PGA set for 0 dB gain, Output PGA set for 6 dB gain, no load on analog outputs (unless otherwise noted).
[3]At input to sigma-delta modulator of ADC.
[4]Guaranteed by design.
[5]Overall group delay will be affected by the sample rate and the external digital filtering.
[6]The ADC's input impedance is inversely proportional to DMCLK and is approximated by: (4×10^{11})/DMCLK.
[7]Between VOUTP and VOUTN.
[8]At VOUT output.
[9]Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.
[10]Test Conditions: no load on digital inputs, analog inputs ac coupled to ground, no load on analog outputs.
Specifications subject to change without notice.

Table I. Current Summary (AVDD = DVDD = 3.3 V)

Conditions	Analog Current	Internal Digital Current	External Interface Current	Total Current (Max)	SE	MCLK ON	Comments
ADC Only On	2	4.5	0.5	8.0	1	YES	REFOUT Disabled
ADC and DAC On	5.6	4.8	0.5	12.5	1	YES	REFOUT Disabled
REFCAP Only On	0.65	0	0	1.0	0	NO	REFOUT Disabled
REFCAP and REFOUT Only On	2.7	0	0	3.8	0	NO	
All Sections Off	0	0.6	0	0.75	0	YES	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	1 µA	0.5 µA	0	20 µA	0	NO	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA and are typical values unless otherwise noted.

Table II. Signal Ranges

Parameter	Condition	Signal Range
V_{REFCAP}		1.2 V ± 10%
V_{REFOUT}		1.2 V ± 10%
ADC	Maximum Input Range at V_{IN}	1.578 V p-p
	Nominal Reference Level	1.0954 V p-p
DAC	Maximum Voltage	
	Output Swing	
	Single-Ended	1.578 V p-p
	Differential	3.156 V p-p
	Nominal Voltage	
	Output Swing	
	Single-Ended	1.0954 V p-p
	Differential	2.1909 V p-p
	Output Bias Voltage	V_{REFOUT}

TIMING CHARACTERISTICS (AVDD = DVDD = 2.7 V to 3.6 V; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +105°C	Unit	Description
Clock Signals			See Figure 1
t_1	61	ns min	MCLK Period
t_2	24.4	ns min	MCLK Width High
t_3	24.4	ns min	MCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period
t_5	$0.4 \times t_1$	ns min	SCLK Width High
t_6	$0.4 \times t_1$	ns min	SCLK Width Low
t_7	20	ns min	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns min	SDI/SDIFS Hold After SCLK Low
t_9	10	ns max	SDOFS Delay from SCLK High
t_{10}	10	ns min	SDOFS Hold After SCLK High
t_{11}	10	ns min	SDO Hold After SCLK High
t_{12}	10	ns max	SDO Delay from SCLK High
t_{13}	30	ns max	SCLK Delay from MCLK

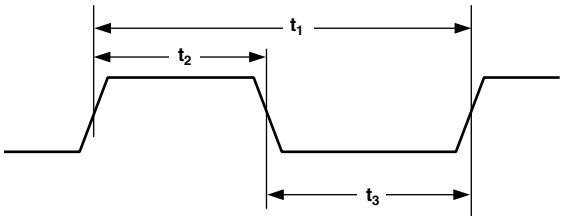


Figure 1. MCLK Timing

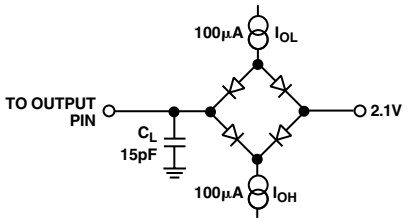
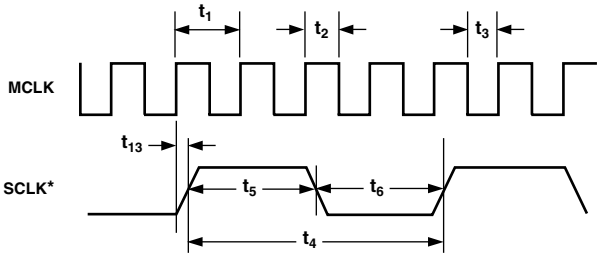


Figure 2. Load Circuit for Timing Specifications



*SCLK IS INDIVIDUALLY PROGRAMMABLE IN FREQUENCY (MCLK/4 SHOWN HERE).

Figure 3. SCLK Timing

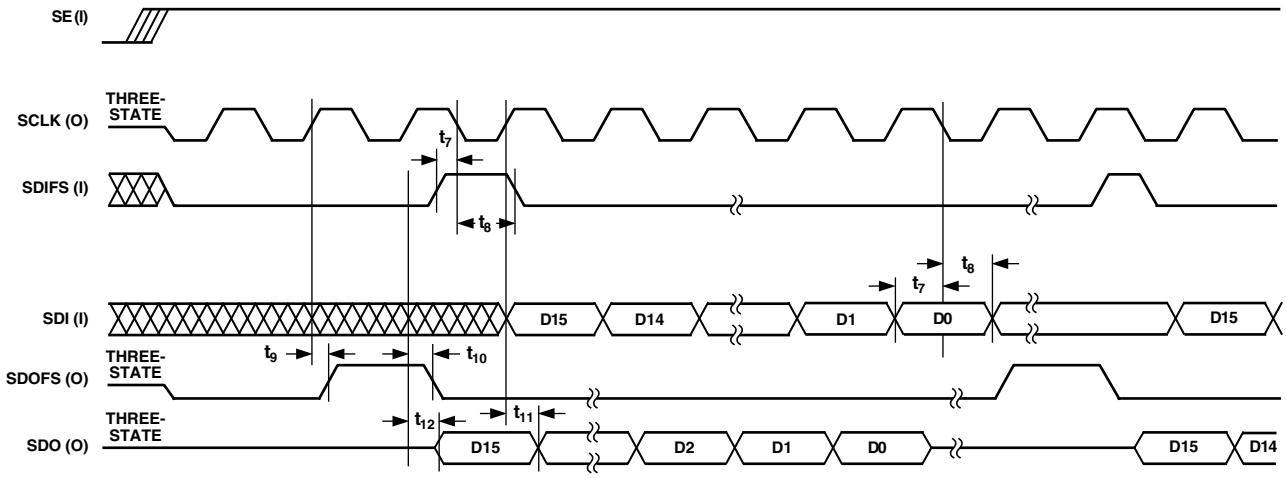


Figure 4. Serial Port (SPORT)

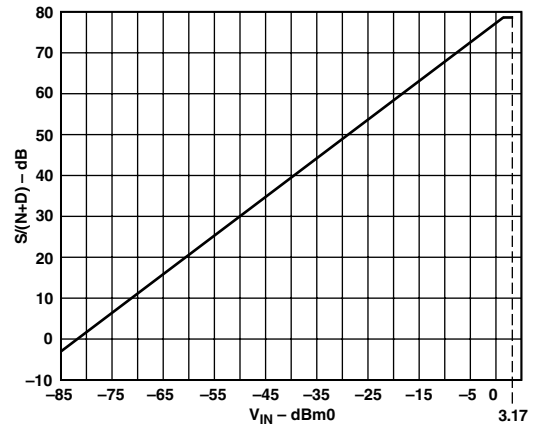


Figure 5a. S/(N+D) vs. V_{IN} (ADC @ 3 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

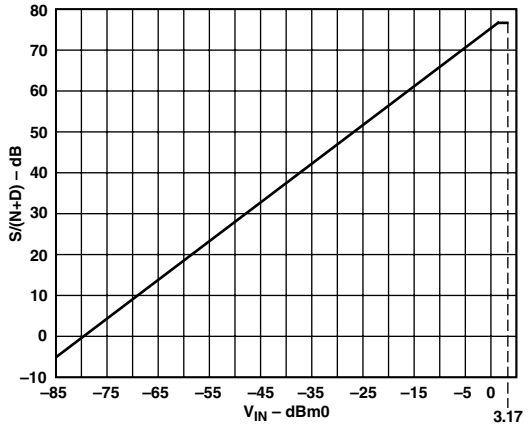


Figure 5b. S/(N+D) vs. V_{IN} (DAC @ 3 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

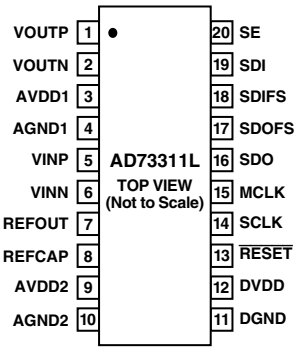
ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

AVDD, DVDD to GND . . . . . –0.3 V to +4.6 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . –0.3 V to (DVDD + 0.3 V)
Analog I/O Voltage to AGND . . . –0.3 V to (AVDD + 0.3 V)
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
SOIC, θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
SSOP, θ_{JA} Thermal Impedance . . . . . 126°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
TSSOP, θ_{JA} Thermal Impedance . . . . . 143°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD73311LAR	–40°C to +105°C	R-20
AD73311LARS	–40°C to +105°C	RS-20
AD73311LARU	–40°C to +105°C	RU-20
EVAL-AD73311LEB	Evaluation Board[2]	

NOTES
[1]R = 0.3' Small Outline IC (SOIC), RS = Shrink Small Outline Package (SSOP), RU = Thin Small Shrink Outline Package (TSSOP).
[2]The AD73311L evaluation board features a cascade of two codecs interfaced to an ADSP-2185L DSP. The board features a DSP software monitor which allows interface to a PC serial port.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73311L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1	VOUTP	Analog Output from the Positive Terminal of the Output Channel.
2	VOUTN	Analog Output from the Negative Terminal of the Output Channel.
3	AVDD1	Analog Power Supply Connection for the Output Driver.
4	AGND1	Analog Ground Connection for the Output Driver.
5	VINP	Analog Input to the Positive Terminal of the Input Channel.
6	VINN	Analog Input to the Negative Terminal of the Input Channel.
7	REFOUT	Buffered Reference Output, which has a nominal value of 1.2 V.
8	REFCAP	A Bypass Capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin.
9	AVDD2	Analog Power Supply Connection.
10	AGND2	Analog Ground/Substrate Connection.
11	DGND	Digital Ground/Substrate Connection.
12	DVDD	Digital Power Supply Connection.
13	$\overline{\text{RESET}}$	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
14	SCLK	Output Serial Clock whose rate determines the serial transfer rate to/from the codec. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider.
15	MCLK	Master Clock Input. MCLK is driven from an external clock signal.
16	SDO	Serial Data Output of the Codec. Both data and control information may be output on this pin and are clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
17	SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is on bit wide and is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
18	SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one bit wide and is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and ignored when SE is low.
19	SDI	Serial Data Input of the Codec. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.
20	SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low); however, the timing counters and other internal registers are at their reset values.

TERMINOLOGY

Absolute Gain
Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured (differentially) with a 1 kHz sine wave at 0 dBm0 for the DAC and with a 1 kHz sine wave at 0 dBm0 for the ADC. The absolute gain specification is used for gain tracking error specification.

Crosstalk
Crosstalk is due to coupling of signals from a given channel to an adjacent channel. It is defined as the ratio of the amplitude of the coupled signal to the amplitude of the input signal. Crosstalk is expressed in dB.

Gain Tracking Error
Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 0 dBm0 (equal to absolute gain) at 1 kHz for the DAC and 0 dBm0 (equal to absolute gain) at 1 kHz for the ADC. Gain tracking error at 0 dBm0 (ADC) and 0 dBm0 (DAC) is 0 dB by definition.

Group Delay
Group delay is defined as the derivative of radian phase with respect to radian frequency, dø(f)/df. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay from a constant indicates the degree of nonlinear phase response of the system.

Idle Channel Noise
Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300 Hz–3400 Hz).

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For final testing, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Power Supply Rejection
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Sample Rate
The sample rate is the rate at which the ADC updates its output register and the DAC updates its output from its input register. It is fixed relative to the DMCLK (= DMCLK/256) and therefore may only be changed by changing the DMCLK.

SNR+THD
Signal-to-noise ratio plus harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300 Hz–3400 Hz, including harmonics but excluding dc.

ABBREVIATIONS

ADC	Analog-to-Digital Converter.
ALB	Analog Loop-Back.
BW	Bandwidth.
CRx	A Control Register where *x* is a placeholder for an alphabetic character (A–E). There are five read/write control registers on the AD73311L—designated CRA through CRE.
CRx:n	A bit position, where *n* is a placeholder for a numeric character (0–7), within a control register; where *x* is a placeholder for an alphabetic character (A–E). Position 7 represents the MSB and Position 0 represents the LSB.
DAC	Digital-to-Analog Converter.
DLB	Digital Loop-Back.
DMCLK	Device (Internal) Master Clock. This is the internal master clock resulting from the external master clock (MCLK) being divided by the on-chip master clock divider.
FSLB	Frame Sync Loop-Back—where the SDOFS of the final device in a cascade is connected to the RFS and TFS of the DSP and the SDIFS of first device in the cascade. Data input and output occur simultaneously. In the case of nonFSLB, SDOFS and SDO are connected to the Rx Port of the DSP while SDIFS and SDI are connected to the Tx Port.
PGA	Programmable Gain Amplifier.
SC	Switched Capacitor.
SNR	Signal-to-Noise Ratio.
SPORT	Serial Port.
THD	Total Harmonic Distortion.
VBW	Voice Bandwidth.

FUNCTIONAL DESCRIPTION

Encoder Channel

The encoder channel consists of an input configuration block, a switched capacitor PGA and a sigma-delta analog-to-digital converter (ADC). An on-board digital filter, which forms part of the sigma-delta ADC, also performs critical system-level filtering. Due to the high level of oversampling, the input anti-alias requirements are reduced such that a simple single pole RC stage is sufficient to give adequate attenuation in the band of interest.

Input Configuration Block

The input configuration block consists of a multiplexing arrangement that allows selection of various input configurations. This includes ADC input selection from either the VINP, VINN pins or from the DAC output via the Analog Loop-Back (ALB) arrangement. Differential inputs can be inverted and it is also possible to use the device in single-ended mode, which allows the option of using the VINP, VINN pins as two separate single-ended inputs, either of which can be selected under software control.

Programmable Gain Amplifier

The encoder section's analog front end comprises a switched capacitor PGA that also forms part of the sigma-delta modulator. The SC sampling frequency is DMCLK/8. The PGA, whose programmable gain settings are shown in Table III, may be used to increase the signal level applied to the ADC from low output sources such as microphones, and can be used to avoid placing external amplifiers in the circuit. The input signal level to the sigma-delta modulator should not exceed the maximum input voltage permitted.

The PGA gain is set by bits IGS0, IGS1 and IGS2 (CRD:0–2) in Control Register D.

Table III. PGA Settings for the Encoder Channel

IGS2	IGS1	IGS0	Gain (dB)
0	0	0	0
0	0	1	6
0	1	0	12
0	1	1	18
1	0	0	20
1	0	1	26
1	1	0	32
1	1	1	38

ADC

The ADC consists of an analog sigma-delta modulator and a digital antialiasing decimation filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a DMCLK/8 rate. This bitstream, representing the analog input signal, is input to the antialiasing decimation filter. The decimation filter reduces the sample rate and increases the resolution.

Analog Sigma-Delta Modulator

The AD73311L input channel employs a sigma-delta conversion technique, which provides a high resolution 16-bit output with system filtering being implemented on-chip.

Sigma-delta converters employ a technique known as oversampling, where the sampling rate is many times the highest frequency of interest. In the case of the AD73311L, the initial sampling rate of the sigma-delta modulator is DMCLK/8. The main effect of oversampling is that the quantization noise is spread over a very wide bandwidth, up to $F_S/2$ = DMCLK/16 (Figure 6a). This means that the noise in the band of interest is much reduced. Another complementary feature of sigma-delta converters is the use of a technique called noise-shaping. This technique has the effect of pushing the noise from the band of interest to an out-of-band position (Figure 6b). The combination of these techniques, followed by the application of a digital filter, reduces the noise in band sufficiently to ensure good dynamic performance from the part (Figure 6c).

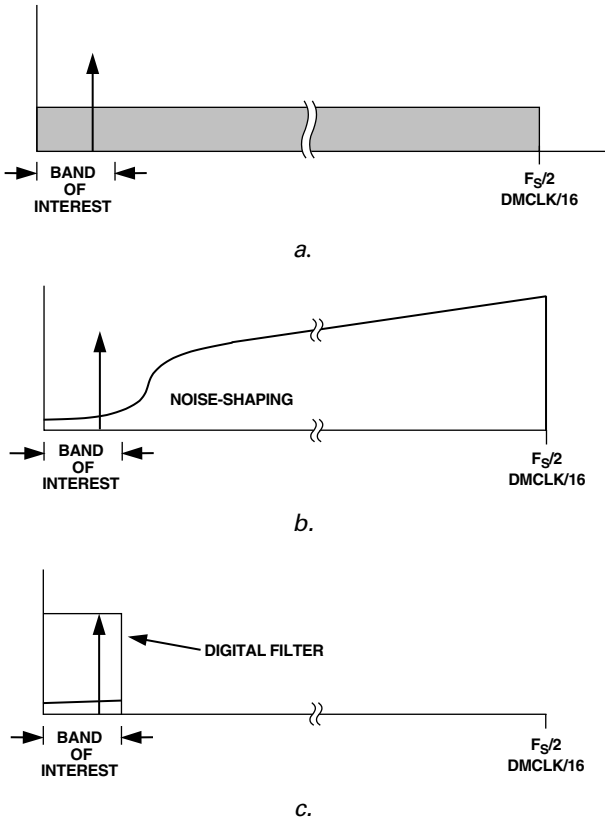
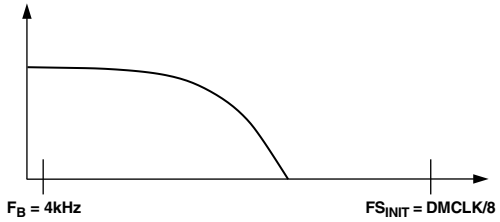
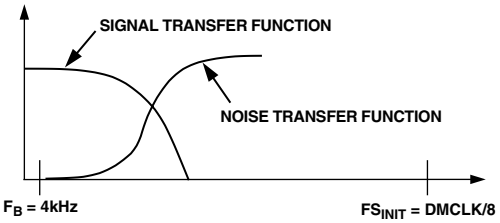


Figure 6. Sigma-Delta Noise Reduction

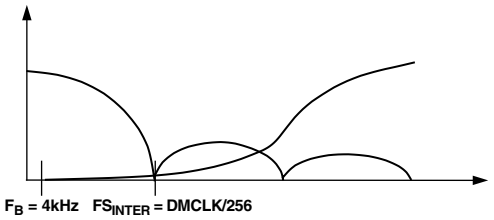
Figure 7 shows the various stages of filtering that are employed in a typical AD73311L application. In Figure 7a we see the transfer function of the external analog antialias filter. Even though it is a single RC pole, its cutoff frequency is sufficiently far away from the initial sampling frequency (DMCLK/8) that it takes care of any signals that could be aliased by the sampling frequency. This also shows the major difference between the initial oversampling rate and the bandwidth of interest. In Figure 7b, the signal and noise-shaping responses of the sigma-delta modulator are shown. The signal response provides further rejection of any high frequency signals while the noise-shaping will push the inherent quantization noise to an out-of-band position. The detail of Figure 7c shows the response of the digital decimation filter (Sinc-cubed response) with nulls every multiple of DMCLK/256, which is the decimation filter update rate. The final detail in Figure 7d shows the application of a final antialias filter in the DSP engine. This has the advantage of being implemented according to the user's requirements and available MIPS. The filtering in Figures 7a through 7c is implemented in the AD73311L.



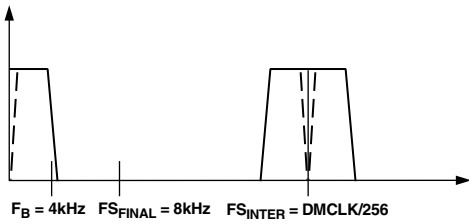
a. Analog Antialias Filter Transfer Function



b. Analog Sigma-Delta Modulator Transfer Function



c. Digital Decimator Transfer Function



d. Final Filter LPF (HPF) Transfer Function

Figure 7. AD73311L ADC Frequency Responses

Decimation Filter

The digital filter used in the AD73311L carries out two important functions. Firstly, it removes the out-of-band quantization noise, which is shaped by the analog modulator and secondly, it decimates the high frequency bitstream to a lower rate 15-bit word.

The antialiasing decimation filter is a sinc-cubed digital filter that reduces the sampling rate from DMCLK/8 at the modulator to an output rate at the SPORT of DMCLK/M (where M depends on the sample rate setting—M = 256 @ 64 kHz; M = 512 @ 32 kHz, M = 1024 @ 16 kHz, M = 2048 @ 8 kHz), and increases the resolution from a single bit to 15 bits. Its Z transform is given as: $[(1–Z^{–N})/(1–Z^{–1})]^3$ where N is determined by the sampling rate (N = 32 @ 64 kHz, N = 64 @ 32 kHz, N = 128 @ 16 kHz, N = 256 @ 8 kHz). This ensures a minimal group delay of 25 µs at the 64 kHz sampling rate.

ADC Coding

The ADC coding scheme is in twos complement format (see Figure 8). The output words are formed by the decimation filter, which grows the word length from the single-bit output of the sigma-delta modulator to a 15-bit word, which is the 16-bit transfer being used as a flag bit to indicate either control or data in the frame.

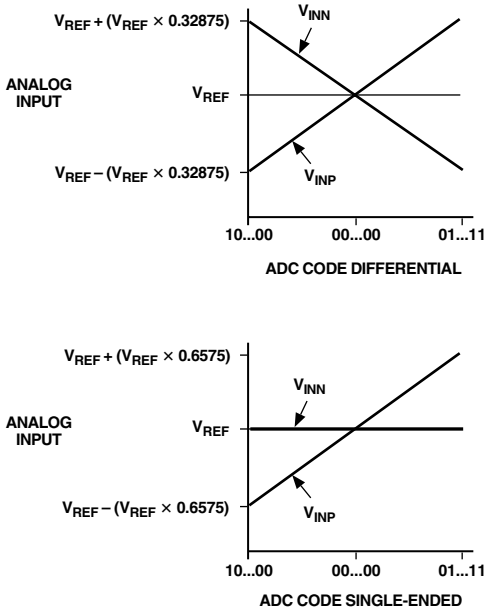


Figure 8. ADC Transfer Function

Decoder Channel

The decoder channel consists of a digital interpolator, digital sigma-delta modulator, a single bit digital-to-analog converter (DAC), an analog smoothing filter and a programmable gain amplifier with differential output.

DAC Coding

The DAC coding scheme is in twos complement format with 0x7FFF being full-scale positive and 0x8000 being full-scale negative.

Interpolation Filter

The anti-imaging interpolation filter is a sinc-cubed digital filter which up-samples the 16-bit input words from the SPORT input rate of DMCLK/M (where M depends on the sample rate setting—M = 256 @ 64 kHz; M = 512 @ 32 kHz, M = 1024 @ 16 kHz, M = 2048 @ 8 kHz), to a rate of DMCLK/8 while filtering to attenuate images produced by the interpolation process. Its Z transform is given as: $[(1–Z^{–N})/(1–Z^{–1})]^3$ where N is determined by the sampling rate (N = 32 @ 64 kHz, N = 64 @ 32 kHz, N = 128 @ 16 kHz, N = 256 @ 8 kHz). The DAC receives 16-bit samples from the host DSP processor at a rate of DMCLK/M. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered by the anti-imaging interpolation filter, but there is an option to bypass the interpolator for the minimum group delay configuration by setting the IBYP bit (CRE:5) of Control Register E. The interpolation filter has the same characteristics as the ADC's antialiasing decimation filter.

The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples at a rate of DMCLK/8. The modulator noise-shapes the signal so that errors inherent to the process are minimized in the passband of the converter. The bitstream output of the sigma-delta modulator is fed to the single bit DAC where it is converted to an analog voltage.

Analog Smoothing Filter and PGA

The output of the single-bit DAC is sampled at DMCLK/8, therefore it is necessary to filter the output to reconstruct the low frequency signal. The decoder's analog smoothing filter consists of a continuous-time filter preceded by a third-order switched-capacitor filter. The continuous-time filter forms part of the output programmable gain amplifier (PGA). The PGA can be used to adjust the output signal level from –15 dB to +6 dB in 3 dB steps, as shown in Table IV. The PGA gain is set by bits OGS0, OGS1 and OGS2 (CRD:4-6) in Control Register D.

Table IV. PGA Settings for the Decoder Channel

OGS2	OGS1	OGS0	Gain (dB)
0	0	0	+6
0	0	1	+3
0	1	0	0
0	1	1	–3
1	0	0	–6
1	0	1	–9
1	1	0	–12
1	1	1	–15

Differential Output Amplifiers

The decoder has a differential analog output pair (VOUTP and VOUTN). The output channel can be muted by setting the MUTE bit (CRD:7) in Control Register D. The output signal is dc-biased to the codec's on-chip voltage reference.

Voltage Reference

The AD73311L reference, REFCAP, is a bandgap reference that provides a low noise, temperature-compensated reference to the DAC and ADC. A buffered version of the reference is also made available on the REFOUT pin and can be used to bias other external analog circuitry. The reference has a default nominal value of 1.2 V.

The reference output (REFOUT) can be enabled for biasing external circuitry by setting the RU bit (CRC:6) of CRC.

Serial Port (SPORT)

The codec communicates with a host processor via the bidirectional synchronous serial port (SPORT) which is compatible with most modern DSPs. The SPORT is used to transmit and receive digital data and control information.

In both transmit and receive modes, data is transferred at the serial clock (SCLK) rate with the MSB being transferred first. Due to the fact that the SPORT uses a common serial register for serial input and output, communications between an AD73311L codec and a host processor (DSP engine) must always be initiated by the codec itself. This ensures that there is no danger of the information being sent to the codec being corrupted by ADC samples being output by the codec.

SPORT Overview

The AD73311L SPORT is a flexible, full-duplex, synchronous serial port whose protocol has been designed to allow up to eight AD73311L devices to be connected, in cascade, to a single DSP via a six-wire interface. It has a very flexible architecture that can be configured by programming two of the internal control registers. The AD73311L SPORT has three distinct modes of operation: Control Mode, Data Mode and Mixed Control/Data Mode.

In Control Mode (CRA:0 = 0), the device's internal configuration can be programmed by writing to the five internal control registers. In this mode, control information can be written to or read from the codec. In Data Mode (CRA:0 = 1), information that is sent to the device is used to update the decoder section (DAC), while the encoder section (ADC) data is read from the device. In this mode, only DAC and ADC data is written to or read from the device. Mixed mode (CRA:0 = 1 and CRA:1 = 1) allows the user to choose whether the information being sent to the device contains either control information or DAC data. This is achieved by using the MSB of the 16-bit frame as a flag bit. Mixed mode reduces the resolution to 15 bits with the MSB being used to indicate whether the information in the 16-bit frame is control information or DAC/ADC data.

The SPORT features a single 16-bit serial register that is used for both input and output data transfers. As the input and output data must share the same register there are some precautions that must be observed. The primary precaution is that no information must be written to the SPORT without reference to an output sample event, which is when the serial register will be overwritten with the latest ADC sample word. Once the SPORT starts to output the latest ADC word then it is safe for the DSP to write new control or data words to the codec. In certain configurations, data can be written to the device to coincide with the output sample being shifted out of the serial register—see section on interfacing devices. The serial clock rate (CRB:2–3) defines how many 16-bit words can be written to a device before the next output sample event will happen.

The SPORT block diagram, shown in Figure 9, details the six control registers (A–F), external MCLK to internal DMCLK divider and serial clock divider. The divider rates are controlled by the setting of Control Register B. The AD73311L features a master clock divider that allows users the flexibility of dividing externally available high frequency DSP or CPU clocks to generate a lower frequency master clock internally in the codec which may be more suitable for either serial transfer or sampling rate requirements. The master clock divider has five divider options (÷1 default condition, ÷2, ÷3, ÷4, ÷5) that are set by loading the master clock divider field in Register B with the appropriate code. Once the internal device master clock (DMCLK) has been set using the master clock divider, the sample rate and serial clock settings are derived from DMCLK.

The SPORT can work at four different serial clock (SCLK) rates: chosen from DMCLK, DMCLK/2, DMCLK/4 or DMCLK/8, where DMCLK is the internal or device master clock resulting from the external or pin master clock being divided by the master clock divider. When working at the lower SCLK rate of DMCLK/8, which is intended for interfacing with slower DSPs, the SPORT will support a maximum of two devices in cascade with the sample rate of DMCLK/256.

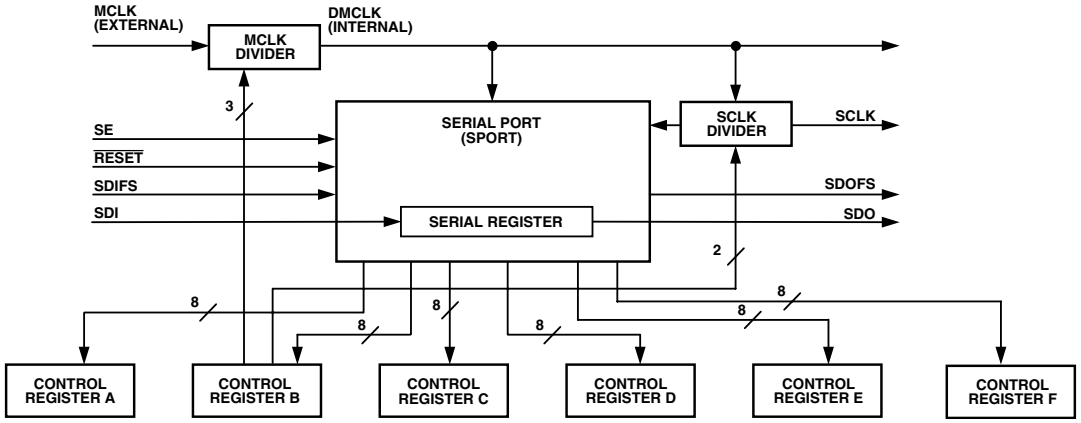


Figure 9. SPORT Block Diagram

SPORT Register Maps

There are two register banks for the AD73311L: the control register bank and the data register bank. The control register bank consists of six read/write registers, each eight bits wide. Table IX shows the control register map for the AD73311L. The first two control registers, CRA and CRB, are reserved for controlling the SPORT. They hold settings for parameters such as bit rate, internal master clock rate and device count (used when more than one AD73311L is connected in cascade from a single SPORT). The other three registers; CRC, CRD and CRE are used to hold control settings for the ADC, DAC, Reference and Power Control sections of the device. Control registers are written to on the negative edge of SCLK. The data register bank consists of two 16-bit registers that are the DAC and ADC registers.

Master Clock Divider

The AD73311L features a programmable master clock divider that allows the user to reduce an externally available master clock, at pin MCLK, by one of the ratios 1, 2, 3, 4 or 5 to produce an internal master clock signal (DMCLK) that is used to calculate the sampling and serial clock rates. The master clock divider is programmable by setting CRB:4-6. Table V shows the division ratio corresponding to the various bit settings. The default divider ratio is divide-by-one.

Table V. DMCLK (Internal) Rate Divider Settings

MCD2	MCD1	MCD0	DMCLK Rate
0	0	0	MCLK
0	0	1	MCLK/2
0	1	0	MCLK/3
0	1	1	MCLK/4
1	0	0	MCLK/5
1	0	1	MCLK
1	1	0	MCLK
1	1	1	MCLK

Serial Clock Rate Divider

The AD73311L features a programmable serial clock divider that allows users to match the serial clock (SCLK) rate of the data to that of the DSP engine or host processor. The maximum SCLK rate available is DMCLK and the other available rates are: DMCLK/2, DMCLK/4 and DMCLK/8. The slowest rate (DMCLK/8) is the default SCLK rate. The serial clock divider is programmable by setting bits CRB:2–3. Table VI shows the serial clock rate corresponding to the various bit settings.

Table VI. SCLK Rate Divider Settings

SCD1	SCD0	SCLK Rate
0	0	DMCLK/8
0	1	DMCLK/4
1	0	DMCLK/2
1	1	DMCLK

Sample Rate Divider

The AD73311L features a programmable sample rate divider that allows users flexibility in matching the codec's ADC and DAC sample rates to the needs of the DSP software. The maximum sample rate available is DMCLK/256 which offers the lowest conversion group delay, while the other available rates are: DMCLK/512, DMCLK/1024 and DMCLK/2048. The slowest rate (DMCLK/2048) is the default sample rate. The sample rate divider is programmable by setting bits CRB:0-1. Table VII shows the sample rate corresponding to the various bit settings.

Table VII. Sample Rate Divider Settings

DIR1	DIR0	SCLK Rate
0	0	DMCLK/2048
0	1	DMCLK/1024
1	0	DMCLK/512
1	1	DMCLK/256

DAC Advance Register

The loading of the DAC is internally synchronized with the unloading of the ADC data in each sampling interval. The default DAC load event happens one SCLK cycle before the SDOFS flag is raised by the ADC data being ready. However, this DAC load position can be advanced before this time by modifying the contents of the DAC Advance field in Control Register E (CRE:0–4). The field is five bits wide, allowing 31 increments of weight 1/(DMCLK/8); see Table VIII. In certain circumstances this can reduce the group delay when the ADC and DAC are used to process data in series. Appendix E details how the DAC advance feature can be used.

NOTE: The DAC advance register should be changed before the DAC section is powered up.

Table VIII. DAC Timing Control

DA4	DA3	DA2	DA1	DA0	Time Advance*
0	0	0	0	0	0 ns
0	0	0	0	1	488.2 ns
0	0	0	1	0	976.5 ns
—	—	—	—	—	—
1	1	1	1	0	14.64 μs
1	1	1	1	1	15.13 μs

*DMCLK = 16.384 MHz.

OPERATION

Resetting the AD73311L

The pin $\overline{\text{RESET}}$ resets all the control registers. All registers are reset to zero indicating that the default SCLK rate (DMCLK/8) and sample rate (DMCLK/2048) are at a minimum to ensure that slow speed DSP engines can communicate effectively. As well as resetting the control registers using the $\overline{\text{RESET}}$ pin, the device can be reset using the $\overline{\text{RESET}}$ bit (CRA:7) in Control Register A. Both hardware and software resets require 4 DMCLK cycles. On reset, DATA/$\overline{\text{PGM}}$ (CRA:0) is set to 0 (default condition) thus enabling Program Mode. The reset conditions ensure that the device must be programmed to the correct settings after power-up or reset. Following a reset, the SDOFS will be asserted 2048 DMCLK cycles after $\overline{\text{RESET}}$ going high. The data that is output following $\overline{\text{RESET}}$ and during Program Mode is random and contains no valid information until either Data or Mixed Mode is set.

Power Management

The individual functional blocks of the AD73311L can be enabled separately by programming the power control register CRC. It allows certain sections to be powered down if not required, which adds to the device's flexibility in that the user need not incur the penalty of having to provide power for a certain section if it is not necessary to their design. The power control register provides individual control settings for the major functional blocks and also a global override that allows all sections to be powered up by setting the bit. Using this method the user could, for example, individually enable a certain section, such as the reference (CRC:5), and disable all others. The global power-up (CRC:0) can be used to enable all sections but if power-down is required using the global control, the reference will still be enabled, in this case, because its individual bit is set. Refer to Table XIII for details of the settings of CRC.

Table IX. Control Register Map

Address (Binary)	Name	Description	Type	Width	Reset Setting (Hex)
000	CRA	Control Register A	R/$\overline{\text{W}}$	8	0x00
001	CRB	Control Register B	R/$\overline{\text{W}}$	8	0x00
010	CRC	Control Register C	R/$\overline{\text{W}}$	8	0x00
011	CRD	Control Register D	R/$\overline{\text{W}}$	8	0x00
100	CRE	Control Register E	R/$\overline{\text{W}}$	8	0x00
101	CRF	Control Register F	R/$\overline{\text{W}}$	8	0x00
110 to 111		Reserved			

Table X. Control Word Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C/$\overline{\text{D}}$	R/$\overline{\text{W}}$	Device Address			Register Address			Register Data							

Control	Frame	Description
Bit 15	Control/$\overline{\text{Data}}$	When set high, it signifies a control word in Program or Mixed Program/Data Modes. When set low, it signifies a data word in Mixed Program/Data Mode or an invalid control word in Program Mode.
Bit 14	Read/$\overline{\text{Write}}$	When set low, it tells the device that the data field is to be written to the register selected by the register field setting provided the address field is zero. When set high, it tells the device that the selected register is to be written to the data field in the input serial register and that the new control word is to be output from the device via the serial output.
Bits 13–11	Device Address	This 3-bit field holds the address information. Only when this field is zero is a device selected. If the address is not zero, it is decremented and the control word is passed out of the device via the serial output.
Bits 10–8	Register Address	This 3-bit field is used to select one of the five control registers on the AD73311L.
Bits 7–0	Register Data	This 8-bit field holds the data that is to be written to or read from the selected register provided the address field is zero.

Table XI. Control Register A Description

CONTROL REGISTER A

7	6	5	4	3	2	1	0
$\overline{\text{RESET}}$	DC2	DC1	DC0	SLB	DLB	MM	DATA/$\overline{\text{PGM}}$

Bit	Name	Description
0	DATA/$\overline{\text{PGM}}$	Operating Mode (0 = Program; 1 = Data Mode)
1	MM	Mixed Mode (0 = Off; 1 = Enabled)
2	DLB	Digital Loop-Back Mode (0 = Off; 1 = Enabled)
3	SLB	SPORT Loop-Back Mode (0 = Off; 1 = Enabled)
4	DC0	Device Count (Bit 0)
5	DC1	Device Count (Bit 1)
6	DC2	Device Count (Bit 2)
7	$\overline{\text{RESET}}$	Software Reset (0 = Off; 1 = Initiates Reset)

Table XII. Control Register B Description

CONTROL REGISTER B

7	6	5	4	3	2	1	0
CEE	MCD2	MCD1	MCD0	SCD1	SCD0	DIR1	DIR0

Bit	Name	Description
0	DIR0	Decimation/Interpolation Rate (Bit 0)
1	DIR1	Decimation/Interpolation Rate (Bit 1)
2	SCD0	Serial Clock Divider (Bit 0)
3	SCD1	Serial Clock Divider (Bit 1)
4	MCD0	Master Clock Divider (Bit 0)
5	MCD1	Master Clock Divider (Bit 1)
6	MCD2	Master Clock Divider (Bit 2)
7	CEE	Control Echo Enable (0 = Off; 1 = Enabled)

Table XIII. Control Register C Description

CONTROL REGISTER C

7	6	5	4	3	2	1	0
–	RU	PUREF	PUDAC	PUADC	–	–	PU

Bit	Name	Description
0	PU	Power-Up Device (0 = Power Down; 1 = Power On)
1	Reserved	Must Be Programmed to Zero (0)
2	Reserved	Must Be Programmed to Zero (0)
3	PUADC	ADC Power (0 = Power Down; 1 = Power On)
4	PUDAC	DAC Power (0 = Power Down; 1 = Power On)
5	PUREF	REF Power (0 = Power Down; 1 = Power On)
6	RU	REFOUT Use (0 = Disable REFOUT; 1 = Enable REFOUT)
7	Reserved	Must Be Programmed to Zero (0)

Table XIV. Control Register D Description

CONTROL REGISTER D

7	6	5	4	3	2	1	0
MUTE	**OGS2**	**OGS1**	**OGS0**	**RMOD**	**IGS2**	**IGS1**	**IGS0**

Bit	Name	Description
0	IGS0	Input Gain Select (Bit 0)
1	IGS1	Input Gain Select (Bit 1)
2	IGS2	Input Gain Select (Bit 2)
3	RMOD	Reset ADC Modulator (0 = Off; 1 = Reset Enabled)
4	OGS0	Output Gain Select (Bit 0)
5	OGS1	Output Gain Select (Bit 1)
6	OGS2	Output Gain Select (Bit 2)
7	MUTE	Output Mute (0 = Mute Off; 1 = Mute Enabled)

Table XV. Control Register E Description

CONTROL REGISTER E

7	6	5	4	3	2	1	0
–	**–**	**IBYP**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**

Bit	Name	Description
0	DA0	DAC Advance Setting (Bit 0)
1	DA1	DAC Advance Setting (Bit 1)
2	DA2	DAC Advance Setting (Bit 2)
3	DA3	DAC Advance Setting (Bit 3)
4	DA4	DAC Advance Setting (Bit 4)
5	IBYP	Interpolator Bypass (0 = Bypass Disabled; 1 = Bypass Enabled)
6	Reserved	Must Be Programmed to Zero (0)
7	Reserved	Must Be Programmed to Zero (0)

Table XVI. Control Register F Description

CONTROL REGISTER F

7	6	5	4	3	2	1	0
ALB	**INV**	**SEEN**	**–**	**–**	**–**	**–**	**–**

Bit	Name	Description
0	Reserved	Must Be Programmed to Zero (0)
1	Reserved	Must Be Programmed to Zero (0)
2	Reserved	Must Be Programmed to Zero (0)
3	Reserved	Must Be Programmed to Zero (0)
4	Reserved	Must Be Programmed to Zero (0)
5	SEEN	Single-Ended Enable (0 = Disabled; 1 = Enabled)
6	INV	Input Invert (0 = Disabled; 1 = Enabled)
7	ALB	Analog Loopback of Output to Input (0 = Disabled; 1 = Enabled)

Operating Modes

There are five operating modes available on the AD73311L. Two of these—Digital Loop-Back and Sport Loop-Back—are provided as diagnostic modes with the other three, Program, Data and Mixed Program/Data, being available for general purpose use. The device configuration—register settings—can be changed only in Program and Mixed Program/Data Modes. In all modes, transfers of information to or from the device occur in 16-bit packets, therefore the DSP engine's SPORT will be programmed for 16-bit transfers.

Program (Control) Mode

In Program Mode, CRA:0 = 0, the user writes to the control registers to set up the device for desired operation—SPORT operation, cascade length, power management, input/output gain, etc. In this mode, the 16-bit information packet sent to the device by the DSP engine is interpreted as a control word whose format is shown in Table X. In this mode, the user must address the device to be programmed using the address field of the control word. This field is read by the device and if it is zero (000 bin) then the device recognizes the word as being addressed to it. If the address field is not zero, it is then decremented and the control word is passed out of the device—either to the next device in a cascade or back to the DSP engine. This 3-bit address format allows the user to uniquely address any one of up to eight devices in a cascade; please note that this addressing scheme is valid only in sending control information to the device —a different format is used to send DAC data to the device(s). In a single codec configuration, all control word addresses must be zero, otherwise they will not be recognized; in a multi-codec configuration all addresses from zero to N-1 (where *N* = number of devices in cascade) are valid.

Following reset, when the SE pin is enabled, the codec responds by raising the SDOFS pin to indicate that an output sample event has occurred. Control words can be written to the device to coincide with the data being sent out of the SPORT, as shown in Figure 10, or they can lag the output words by a time interval that should not exceed the sample interval. After reset, output frame sync pulses will occur at a slower default sample rate, which is DMCLK/2048, until Control Register B is programmed after which the SDOFS pulses will occur at a rate set by the DIR0-1 bits of CRB. This is to allow slow controller devices to establish communication with the AD73311L. During Program Mode, the data output by the device is random and should not be interpreted as ADC data.

Data Mode

Once the device has been configured by programming the correct settings to the various control registers, the device may exit Program Mode and enter Data Mode. This is done by programming the DATA/$\overline{\text{PGM}}$ (CRA:0) bit to a 1 and MM (CRA:1) to 0. Once the device is in Data Mode, the 16-bit input data frame is now interpreted as DAC data rather than a control frame. This data is therefore loaded directly to the DAC register. In Data Mode, as the entire input data frame contains DAC data, the device relies on counting the number of input frame syncs received at the SDIFS pin. When that number equals the device count stored in the device count field of CRA, the device knows that the present data frame being received is its own DAC update data. When the device is in normal Data Mode (i.e., mixed mode disabled), it must receive a hardware reset to reprogram any of the control register settings. In a single codec configuration, each 16-bit data frame sent from the DSP to the device is interpreted as DAC data. The default device count is 1, therefore each input frame sync will cause the 16-bit data frame to be loaded to the DAC register.

Mixed Program/Data Mode

This mode allows the user to send control words to the device along with the DAC data. This permits adaptive control of the device whereby control of the input/output gains can be effected by interleaving control words along with the normal flow of DAC data. The standard data frame remains 16 bits, but now the MSB is used as a flag bit to indicate whether the remaining 15 bits of the frame represent DAC data or control information. In the case of DAC data, the 15 bits are loaded with MSB justification and LSB set to 0 to the DAC register. Mixed mode is enabled by setting the MM bit (CRA:1) to 1 and the DATA/$\overline{\text{PGM}}$ bit (CRA:0) to 1. In the case where control setting changes will be required during normal operation, this mode allows the ability to load both control and data information with the slight inconvenience of formatting the data. Note that the output samples from the ADC will also have the MSB set to zero to indicate it is a data word.

Digital Loop-Back

This mode can be used for diagnostic purposes and allows the user to feed the ADC samples from the ADC register directly to the DAC register. This forms a loop-back of the analog input to the analog output by reconstructing the encoded signal using the decoder channel. The serial interface will continue to work, which allows the user to control gain settings, etc. Only when DLB is enabled with Mixed Mode operation can the user disable the DLB, otherwise the device must be reset.

Sport Loop-Back

This mode allows the user to verify the DSP interfacing and connection by writing words to the SPORT of the device and have them returned back unchanged at the next sample interval. The frame sync and data word that are sent to the device are returned via the output port. Again, SLB mode can only be disabled when used in conjunction with mixed mode, otherwise the device must be reset.

Analog Loop-Back

In Analog Loop-Back mode, the differential DAC output is connected, via a loop-back switch, to the ADC input (see Figure 12). This mode allows the ADC channel to check functionality of the DAC channel as the reconstructed output signal can be monitored using the ADC as a sampler. Analog Loop-Back is enabled by setting the ALB bit (CRF:7).

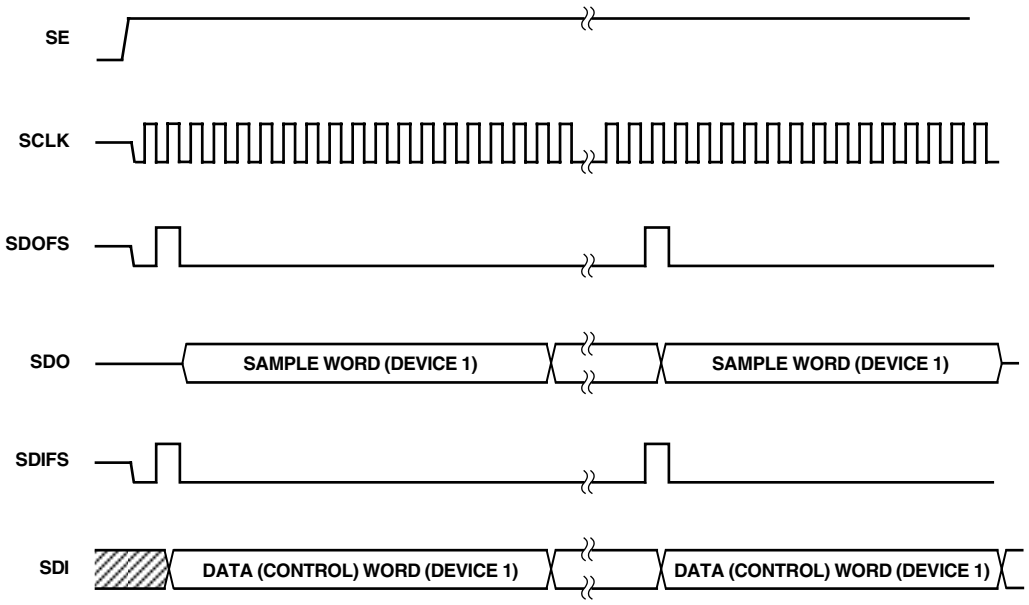


Figure 10. Interface Signal Timing for Single Device Operation

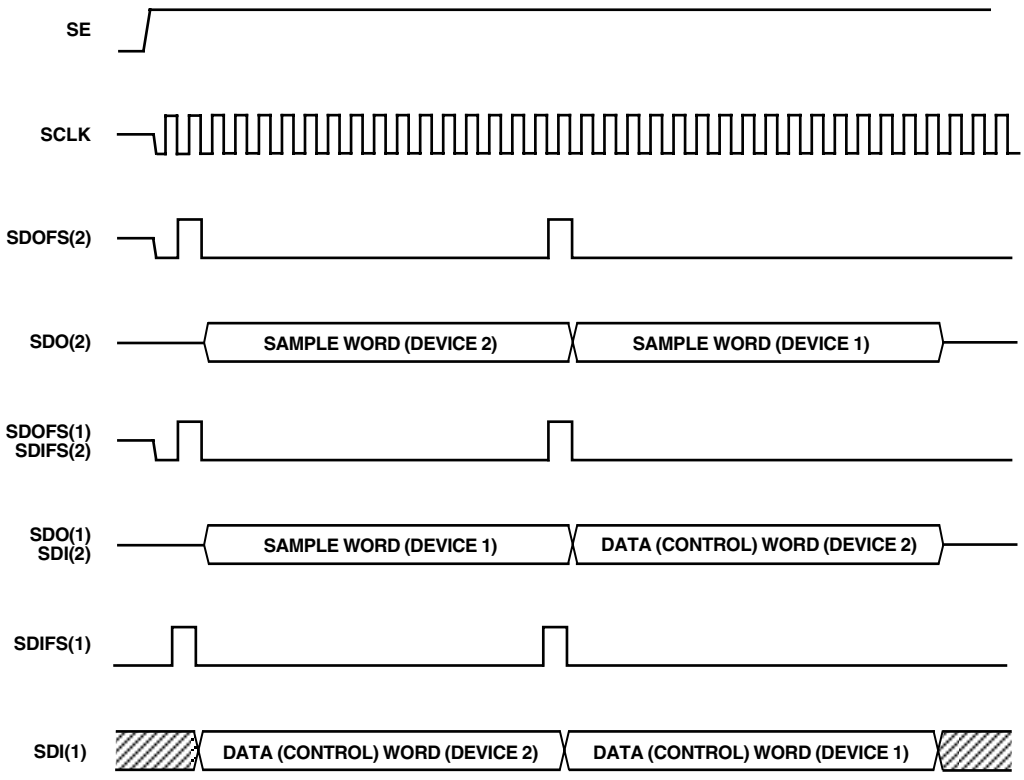


Figure 11. Interface Signal Timing for Cascade of Two Devices

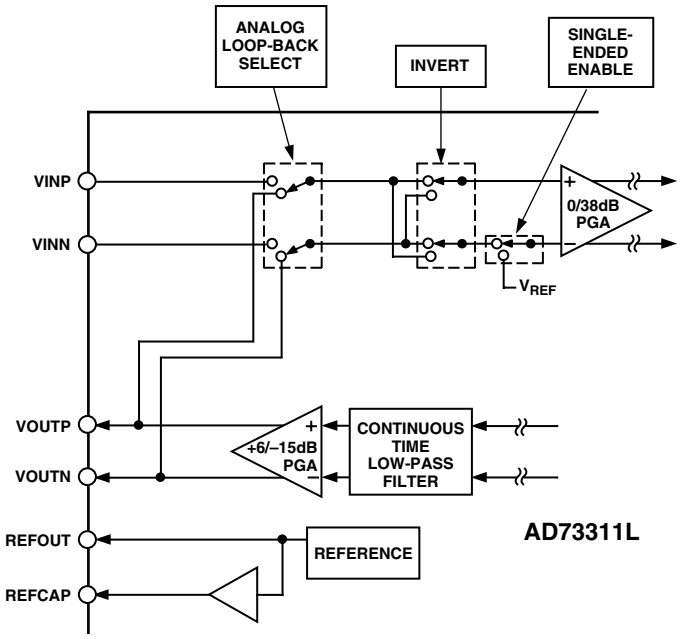


Figure 12. Analog Loop-Back Connectivity

INTERFACING

The AD73311L can be interfaced to most modern DSP engines using conventional serial port connections and an extra enable control line. Both serial input and output data use an accompanying frame synchronization signal which is active high one clock cycle before the start of the 16-bit word or during the last bit of the previous word if transmission is continuous. The serial clock (SCLK) is an output from the codec and is used to define the serial transfer rate to the DSP's Tx and Rx ports. Two primary configurations can be used: the first is shown in Figure 13, where the DSP's Tx data, Tx frame sync, Rx data and Rx frame sync are connected to the codec's SDI, SDIFS, SDO and SDOFS, respectively. This configuration, referred to as indirectly coupled or nonframe sync loop-back, has the effect of decoupling the transmission of input data from the receipt of output data. The delay between receipt of codec output data and transmission of input data for the codec is determined by the DSP's software latency. When programming the DSP serial port for this configuration, it is necessary to set the Rx F_S as an input and the Tx F_S as an output generated by the DSP. This configuration is most useful when operating in mixed mode, as the DSP has the ability to decide how many words (either DAC or control) can be sent to the codec(s). This means that full control can be implemented over the device configuration as well as updating the DAC in a given sample interval. The second configuration (shown in Figure 14) has the DSP's Tx data and Rx data connected to the codec's SDI and SDO, respectively while the DSP's Tx and Rx frame syncs are connected to the codec's SDIFS and SDOFS. In this configuration, referred to as directly coupled or frame sync loop-back, the frame sync signals are connected together and the input data to the codec is forced to be synchronous with the output data from the codec. The DSP must be programmed so that both the Tx F_S and Rx F_S are inputs as the codec SDOFS will be input to both. This configuration guarantees that input and output events occur simultaneously and is the simplest configuration for operation in normal Data Mode. Note that when programming the DSP in this configuration it is advisable to preload the Tx register with the first control word to be sent before the codec is taken out of reset. This ensures that this word will be transmitted to coincide with the first output word from the device(s).

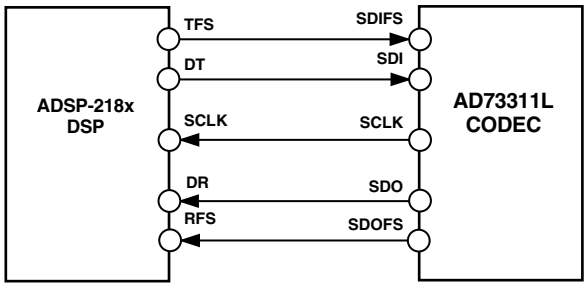


Figure 13. Indirectly Coupled or Nonframe Sync Loop-Back Configuration

Cascade Operation

The AD73311L has been designed to support up to eight codecs in a cascade connected to a single serial port (see Figure 37). The SPORT interface protocol has been designed so that device addressing is built into the packet of information sent to the device. This allows the cascade to be formed with no extra hardware overhead for control signals or addressing. A cascade can be formed in either of the two modes previously discussed.

There may be some restrictions in cascade operation due to the number of devices configured in the cascade and the serial clock rate chosen. Table XVII details the requirements for SCLK rate for cascade lengths from 1 to 8 devices. This assumes a directly coupled frame sync arrangement as shown in Figure 13.

Table XVII. Cascade Options

	Number of Devices in Cascade							
SCLK	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
DMCLK	✓	✓	✓	✓	✓	✓	✓	✓
DMCLK/2	✓	✓	✓	✓	✓	✓	✓	✓
DMCLK/4	✓	✓	✓	✓	X	X	X	X
DMCLK/8	✓	✓	X	X	X	X	X	X

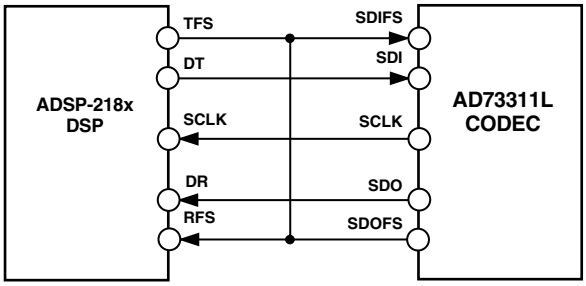


Figure 14. Directly Coupled or Frame Sync Loop-Back Configuration

When using the indirectly coupled frame sync configuration in cascaded operation it is necessary to be aware of the restrictions in sending data to all devices in the cascade. Effectively the time allowed is given by the sampling interval (256/DMCLK) which is 15.625 µs for a sample rate of 64 kHz. In this interval, the DSP must transfer N × 16 bits of information where N is the number of devices in the cascade. Each bit will take 1/SCLK and, allowing for any latency between the receipt of the Rx interrupt and the transmission of the Tx data, the relationship for successful operation is given by:

$$256/DMCLK > ((N \times 16/SCLK) + T_{INTERRUPT\ LATENCY})$$

The interrupt latency will include the time between the ADC sampling event and the Rx interrupt being generated in the DSP—this should be 16 SCLK cycles.

In Cascade Mode, each device must know the number of devices in the cascade because the Data and Mixed modes use a method of counting input frame sync pulses to decide when they should update the DAC register from the serial input register. Control Register A contains a 3-bit field (DC0–2) that is programmed by the DSP during the programming phase. The default condition is that the field contains 000b, which is equivalent to a single device in cascade (see Table XVIII). However, for cascade operation this field must contain a binary value that is one less than the number of devices in the cascade.

Table XVIII. Device Count Settings

DC2	DC1	DC0	Cascade Length
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

PERFORMANCE

As the AD73311L is designed to provide high performance, low cost conversion, it is important to understand the means by which this high performance can be achieved in a typical application. This section will, by means of spectral graphs, outline the typical performance of the device and highlight some of the options available to users in achieving their desired sample rate, either directly in the device or by doing some post-processing in the DSP, while also showing the advantages and disadvantages of the different approaches.

Encoder Section

The AD73311L offers a variable sampling rate from a fixed MCLK frequency—with 64 kHz, 32 kHz, 16 kHz and 8 kHz being available with a 16.384 MHz external clock. Each of these sampling rates preserves the same sampling rate in the ADC's sigma-delta modulator, which ensures that the noise performance is optimized in each case. The examples below will show the performance of a 1 kHz sine wave when converted at the various sample rates.

The range of sampling rates is aimed to offer the user a degree of flexibility in deciding how their analog front end is to be implemented. The high sample rates of 64 kHz and 32 kHz are suited to those applications, such as active control, where low conversion group delay is essential. On the other hand, the lower sample rates of 16 kHz and 8 kHz are better suited for applications such as telephony, where the lower sample rates result in lower DSP overhead.

Figure 15 shows the spectrum of the 1 kHz test tone sampled at 64 kHz. The plot shows the characteristic shaped noise floor of a sigma-delta converter, which is initially flat in the band of interest but then rises with increasing frequency. If a suitable digital filter is applied to this spectrum, it is possible to eliminate the noise floor in the higher frequencies. This signal can then be used in DSP algorithms or can be further processed in a decimation algorithm to reduce the effective sample rate. Figure 16 shows the resulting spectrum following the filtering and decimation of the spectrum of Figure 15 from 64 kHz to an 8 kHz rate.

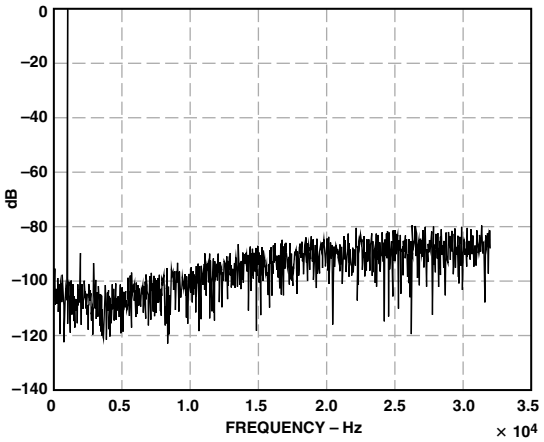


Figure 15. FFT (ADC 64 kHz Sampling)

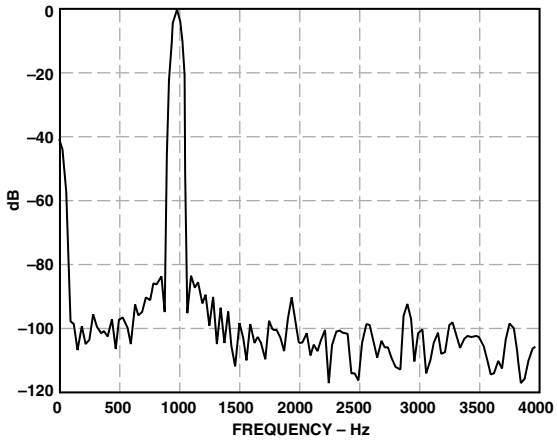


Figure 16. FFT (ADC 8 kHz Filtered and Decimated from 64 kHz)

The AD73311L also features direct sampling at the lower rate of 8 kHz. This is achieved by the use of extended decimation registers within the decimator block, which allows for the increased word growth associated with the higher effective oversampling ratio. Figure 17 details the spectrum of a 1 kHz test tone converted at an 8 kHz rate.

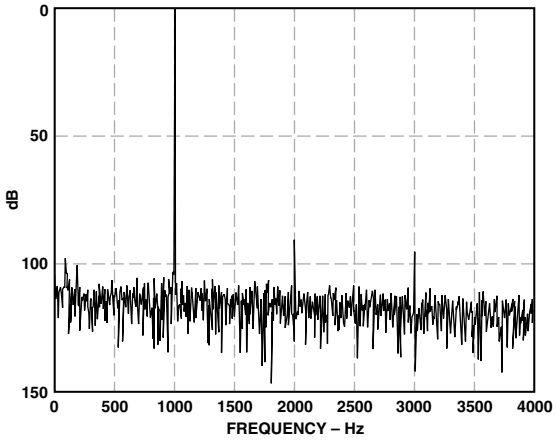


Figure 17. FFT (ADC 8 kHz Direct Sampling)

The device features an on-chip master clock divider circuit that allows the sample rate to be reduced as the sampling rate of the sigma-delta converter is proportional to the output of the MCLK Divider (whose default state is divide by 1).

The decimator's frequency response (Sinc3) gives some pass-band attenuation (up to $F_S/2$) which continues to roll off above the Nyquist frequency. If it is required to implement a digital filter to create a sharper cutoff characteristic, it may be prudent to use an initial sample rate of greater than twice the Nyquist rate in order to avoid aliasing due to the smooth roll-off of the Sinc3 filter response.

In the case of voiceband processing where 4 kHz represents the Nyquist frequency, if the signal to be measured were externally bandlimited, an 8 kHz sampling rate would suffice. However, if it is required to limit the bandwidth using a digital filter, it may be more appropriate to use an initial sampling rate of 16 kHz and to process this sample stream with a filtering and decimating algorithm to achieve a 4 kHz bandlimited signal at an 8 kHz rate. Figure 18 details the initial 16 kHz sampled tone.

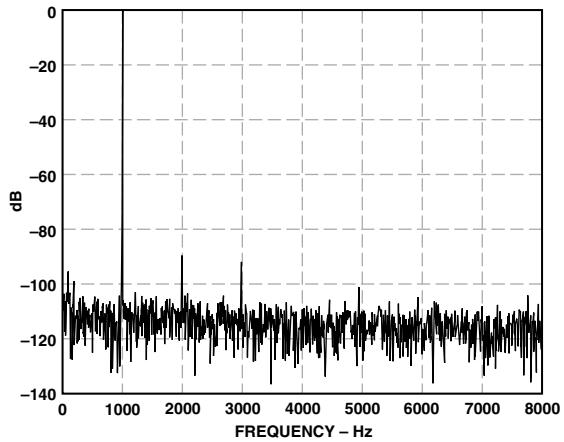


Figure 18. FFT (ADC 16 kHz Direct Sampling)

Figure 19 details the spectrum of the final 8 kHz sampled filtered tone.

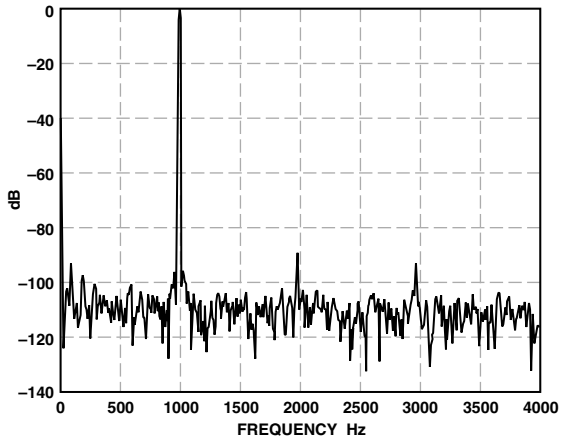


Figure 19. FFT (ADC 8 kHz Filtered and Decimated from 16 kHz)

Encoder Group Delay

When programmed for high sampling rates, the AD73311L offers a very low level of group delay, which is given by the following relationship:

$$Group\ Delay\ (Decimator) = Order \times ((M - 1)/2) \times T_{DEC}$$

where:

Order is the order of the decimator (= 3),

M is the decimation factor (= 32 @ 64 kHz, = 64 @ 32 kHz, = 128 @ 16 kHz , = 256 @ 8 kHz) and

T_{DEC} is the decimation sample interval (= 1/2.048e6) (based on DMCLK = 16.384 MHz) => Group Delay (Decimator @ 64 kHz) = 3 × (32 – 1)/2 × (1/2.048e6) = 22.7 µs

If final filtering is implemented in the DSP, the final filter's group delay must be taken into account when calculating overall group delay.

Decoder Section

The decoder section updates (samples) at the same rate as the encoder section. This rate is programmable as 64 kHz, 32 kHz, 16 kHz or 8 kHz (from a 16.384 MHz MCLK). The decoder section represents a reverse of the process that was described in the encoder section. In the case of the decoder section, signals are applied in the form of samples at an initial low rate. This sample rate is then increased to the final digital sigma-delta modulator rate of DMCLK/8 by interpolating new samples between the original samples. The interpolating filter also has the action of canceling images due to the interpolation process using spectral nulls that exist at integer multiples of the initial sampling rate. Figure 20 shows the spectral response of the decoder section sampling at 64 kHz. Again, its sigma-delta modulator shapes the noise so it is reduced in the voice bandwidth dc–4 kHz. For improved voiceband SNR, the user can implement an initial anti-imaging filter, preceded by 8 kHz to 64 kHz interpolation, in the DSP.

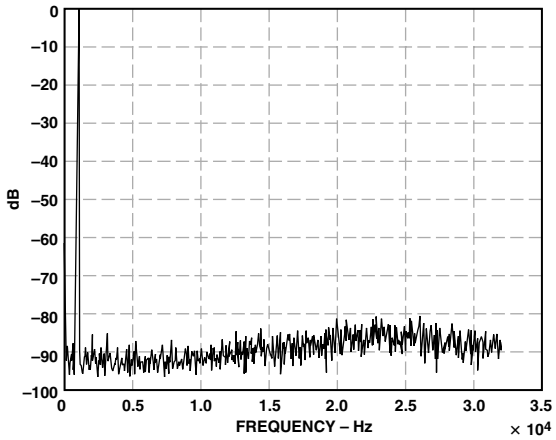


Figure 20. FFT (DAC 64 kHz Sampling)

As the AD73311L can be operated at 8 kHz (see Figure 21) or 16 kHz sampling rates, which make it particularly suited for voiceband processing, it is important to understand the action of the interpolator's Sinc3 response. As was the case with the encoder section, if the output signal's frequency response is not bounded by the Nyquist frequency it may be necessary to perform some initial digital filtering to eliminate signal energy above Nyquist to ensure that it is not imaged at the integer multiples of the sampling frequency. If the user chooses to bypass the interpolator, perhaps to reduce group delay, images of the original signal will be generated at integer intervals of the sampling frequency. In this case these images must be removed by external analog filtering.

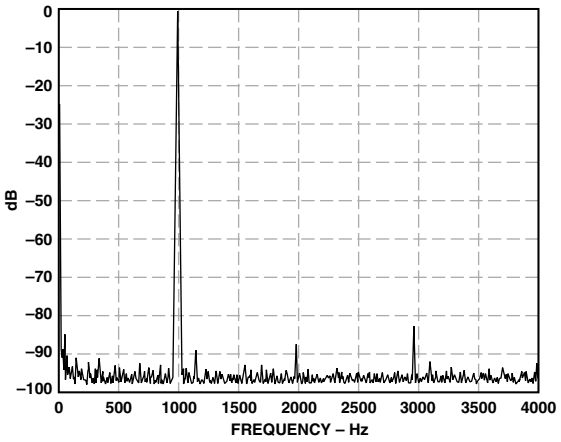


Figure 21. FFT (DAC 8 kHz Sampling)

Figure 22 shows the output spectrum of a 1 kHz tone being generated at an 8 kHz sampling rate with the interpolator bypassed.

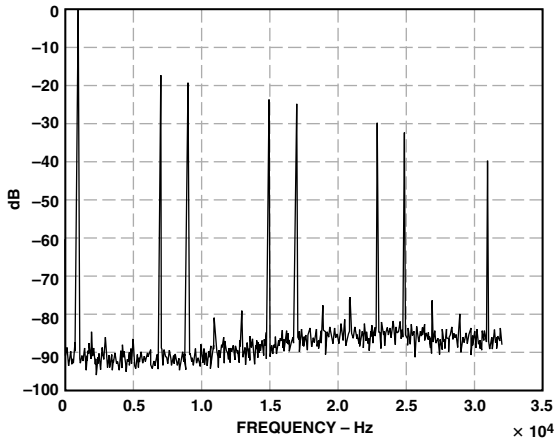


Figure 22. FFT (DAC 8 kHz Sampling—Interpolator Bypassed)

Decoder Group Delay

The interpolator roll-off is mainly due to its sinc-cubed function characteristic, which has an inherent group delay given by the equation:

$$Group\ Delay\ (Interpolator) = Order \times (L - 1)/2) \times T_{INT}$$

where:

Order is the interpolator order (= 3),

L is the interpolation factor (= 32 @ 64 kHz, = 64 @ 32 kHz, = 128 @ 16 kHz, = 256 @ 8 kHz) and

T_{INT} is the interpolation sample interval (= 1/2.048e6)

=> Group Delay (Interpolator @ 64 kHz)

= 3 × (32 – 1)/2 × (1/2.048e6)

= 22.7 μs

The analog section has a group delay of approximately 25 μs.

On-Chip Filtering

The primary function of the system filtering's sinc-cubed (Sinc3) response is to eliminate aliases or images of the ADCs or DAC's resampling, respectively. Both modulators are sampled at a nominal rate of DMCLK/8 (which is 2.048 MHz for a DMCLK of 16.384 MHz) and the simple, external RC antialias filter is sufficient to provide the required stopband rejection above the Nyquist frequency for this sample rate. In the case of the ADC section, the decimating filter is required to both decrease sample rate and increase sample resolution. The process of changing sample rate (resampling) leads to aliases of the original sampled waveform appearing at integer multiples of the new sample rate. These aliases would get mapped into the required signal passband without the application of some further antialias filtering. In the AD73311L, the sinc-cubed response of the decimating filter creates spectral nulls at integer multiples of the new sample rate. These nulls coincide with the aliases of the original waveform which were created by the down-sampling process, therefore reducing or eliminating the aliasing due to sample rate reduction.

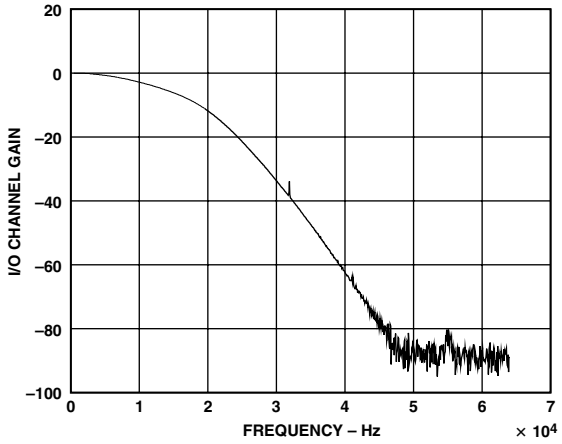


Figure 23. Codec Uncompensated Input-to-Output Frequency Response (f_{SAMP} = 64 kHz)

In the DAC section, increasing the sampling rate by interpolation creates images of the original waveform at intervals of the original sampling frequency. These images may be sufficiently rejected by external circuitry, but the sinc-cubed filter in the interpolator again nulls the output spectrum at integer intervals of the original sampling rate which corresponds with the images due to the interpolation process.

The spectral response of a sinc-cubed filter shows the characteristic nulls at integer intervals of the sampling frequency. Its passband characteristic (up to Nyquist frequency) features a roll-off that continues up to the sampling frequency, where the first null occurs. In many applications this smooth response will not give sufficient attenuation of frequencies outside the band of interest, therefore, it may be necessary to implement a final filter in the DSP which will equalize the passband rolloff and provide a sharper transition band and greater stopband attenuation.

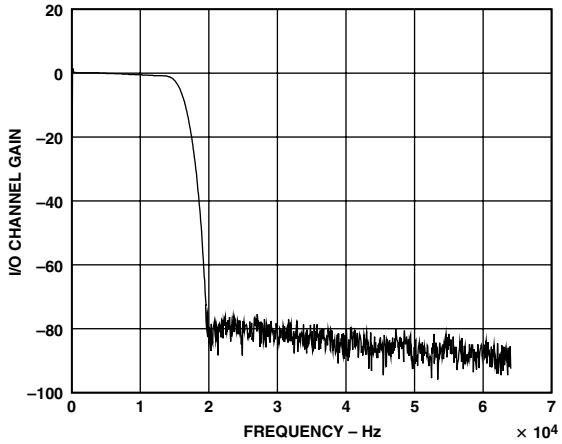


Figure 24. Codec Compensated Input-to-Output Frequency Response (f_{SAMP} = 64 kHz)

DESIGN CONSIDERATIONS

The AD73311L features both differential inputs and outputs on each channel to provide optimal performance and avoid common-mode noise. It is also possible to interface either inputs or outputs in single-ended mode. This section details the choice of input and output configurations and also gives some tips towards successful configuration of the analog interface sections.

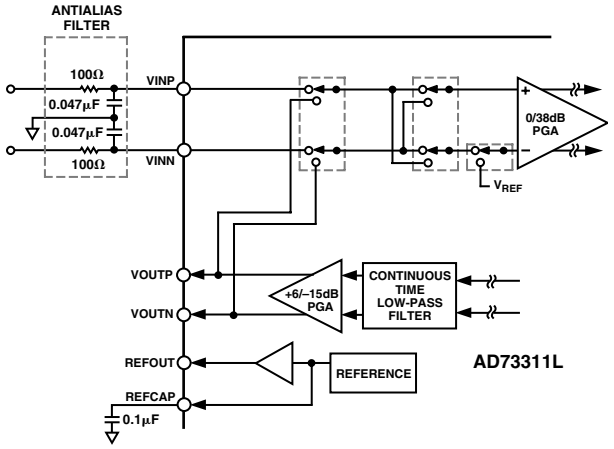


Figure 25. Analog Input (DC-Coupled)

Analog Inputs

The analog input (encoder) section of the AD73311L can be interfaced to external circuitry in either ac-coupled or dc-coupled modes.

It is also possible to drive the ADCs in either differential or single-ended modes. If the single-ended mode is chosen it is possible, using software control, to multiplex between two single-ended inputs connected to the positive and negative input pins.

The primary concerns in interfacing to the ADC are firstly to provide adequate antialias filtering and to ensure that the signal source will drive the switched-capacitor input of the ADC correctly. The sigma-delta design of the ADC and its oversampling characteristics simplify the antialias requirements but it must be remembered that the single pole RC filter is primarily intended to eliminate aliasing of frequencies above the Nyquist frequency of the sigma-delta modulator's sampling rate (typically 2.048 MHz). It may still require a more specific digital filter implementation in the DSP to provide the final signal frequency response characteristics. It is recommended that for optimum performance the capacitors used for the antialiasing filter be of high quality dielectric (NPO). The second issue mentioned above is interfacing the signal source to the ADC's switched capacitor input load. The SC input presents a complex dynamic load to a signal source, therefore, it is important to understand that the slew rate characteristic is an important consideration when choosing external buffers for use with the AD73311L. The internal inverting op amps on the AD73311L are specifically designed to interface to the ADC's SC input stage.

The AD73311L's on-chip 38 dB preamplifier can be enabled when there is not enough gain in the input circuit; the preamplifier is configured by bits IGS0-2 of CRD. The total gain must be configured to ensure that a full-scale input signal produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed the maximum input range.

The dc biasing of the analog input signal is accomplished with an on-chip voltage reference. If the input signal is not biased at the internal reference level (via REFOUT), it must be ac-coupled with external coupling capacitors. C_{IN} should be 0.1 μF or larger. The dc biasing of the input can then be accomplished using resistors to REFOUT as in Figures 27 through 29.

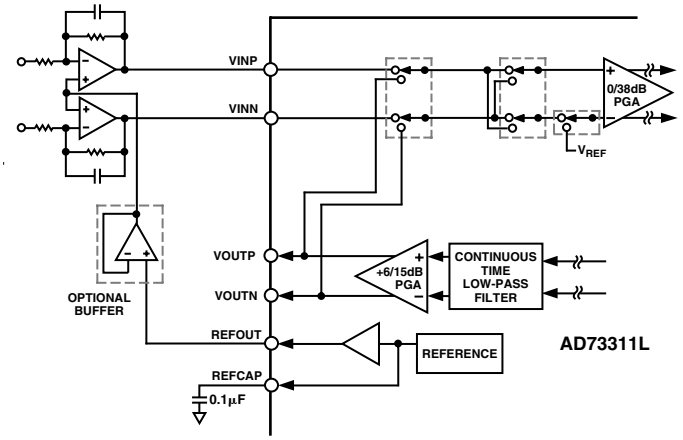


Figure 26. Analog Input (DC-Coupled) Using External Amplifiers

The AD73311L's ADC inputs are biased about the internal reference level (REFCAP level), therefore it may be necessary to bias external signals to this level using the buffered REFOUT level as the reference. This is applicable in either dc- or ac-coupled configurations. In the case of dc coupling, the signal (biased to REFOUT) may be applied directly to the inputs (using amplifier bypass), as shown in Figure 25, or it may be conditioned in an external op amp where it can also be biased to the reference level using the buffered REFOUT signal as shown in Figure 26.

In the case of ac-coupling, a capacitor is used to couple the signal to the input of the ADC. The ADC input must be biased to the internal reference (REFCAP) level which is done by connecting the input to the REFOUT pin through a 10 kΩ resistor as shown in Figure 27.

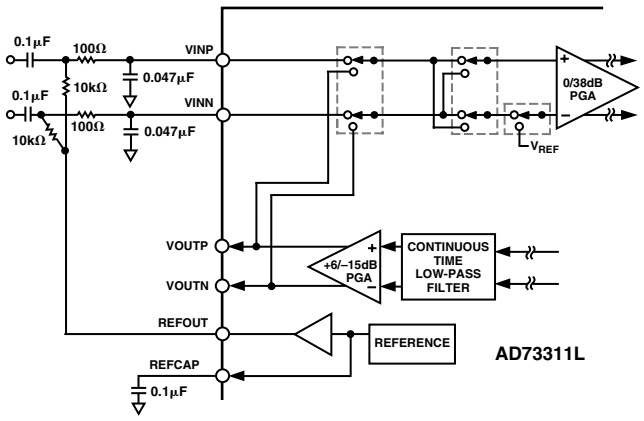


Figure 27. Analog Input (AC-Coupled) Differential

If the ADC is being connected in single-ended mode, the AD73311L should be programmed for single-ended mode using the SEEN and INV bits of CRF, and the inputs connected as shown in Figure 28. When operated in single-ended input mode, the AD73311L can multiplex one of the two inputs to the ADC input, as shown in Figures 28 and 29.

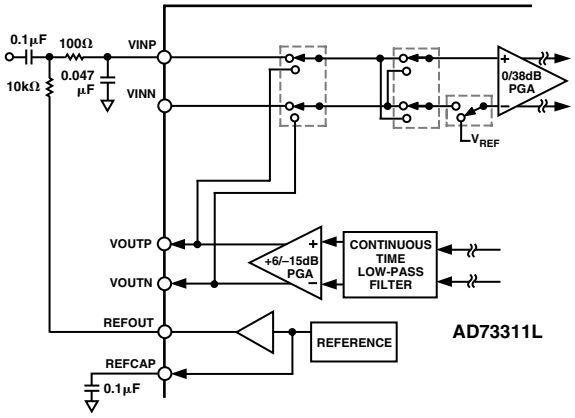


Figure 28. Analog Input (AC-Coupled) Single-Ended

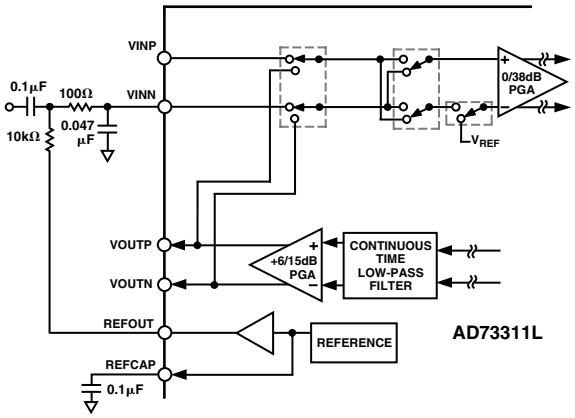


Figure 29. Analog Input (AC-Coupled) Single-Ended (Alternate Input)

Interfacing to an Electret Microphone

Figure 30 details an interface for an electret microphone which may be used in some voice applications. Electret microphones typically feature a FET amplifier whose output is accessed on the same lead that supplies power to the microphone; therefore, this output signal must be capacitively coupled to remove the power supply (dc) component. In this circuit the AD73311L input channel is being used in single-ended mode where the internal inverting amplifier provides suitable gain to scale the input signal relative to the ADC's full-scale input range. The buffered internal reference level at REFOUT is used via an external buffer to provide power to the electret microphone. This provides a quiet, stable supply for the microphone. If this is not a concern, the microphone can be powered from the system power supply.

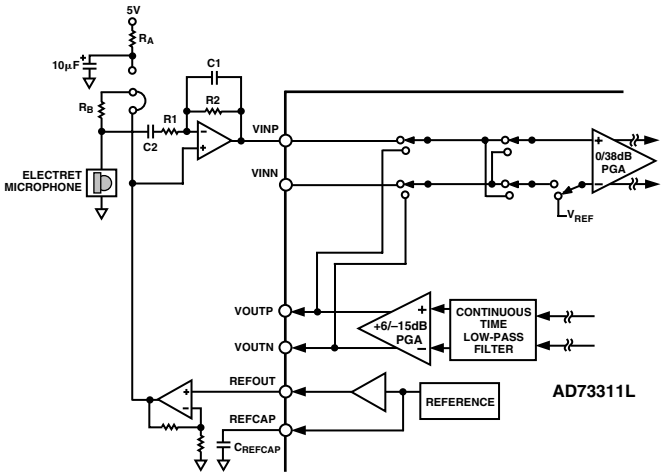


Figure 30. Electret Microphone Interface Circuit

Analog Output

The AD73311L's differential analog output (VOUT) is produced by an on-chip differential amplifier. The differential output can be ac-coupled or dc-coupled directly to a load that can be a headset or the input of an external amplifier (the specified minimum resistive load on the output section is 150 Ω). It is possible to connect the outputs in either a differential or a single-ended configuration but please note that the effective maximum output voltage swing (peak to peak) is halved in the case of single-ended connection. Figure 31 shows a simple circuit providing a differential output with ac coupling. The capacitors in this circuit (C_{OUT}) are optional; if used, their value can be chosen as follows:

$$C_{OUT} = \frac{1}{2\ \pi\ f_C\ R_{LOAD}}$$

where f_C = desired cutoff frequency.

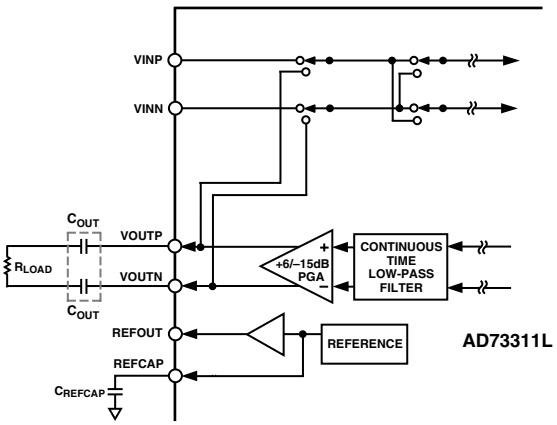


Figure 31. Example Circuit for Differential Output

Figure 32 shows an example circuit for providing a single-ended output with ac coupling. The capacitor of this circuit (C_{OUT}) is not optional if dc current drain is to be avoided.

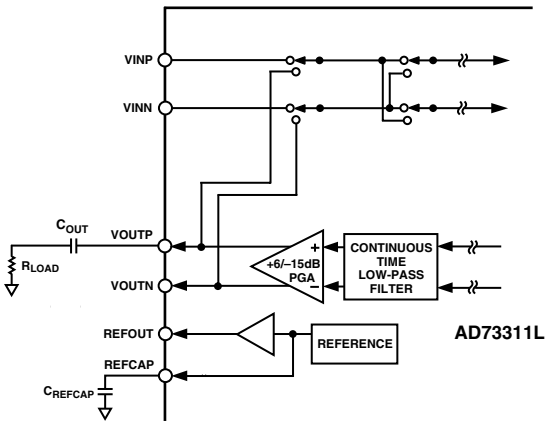


Figure 32. Example Circuit for Single-Ended Output

Differential-to-Single-Ended Output

In some applications it may be desirable to convert the full differential output of the decoder channel to a single-ended signal. The circuit of Figure 33 shows a scheme for doing this.

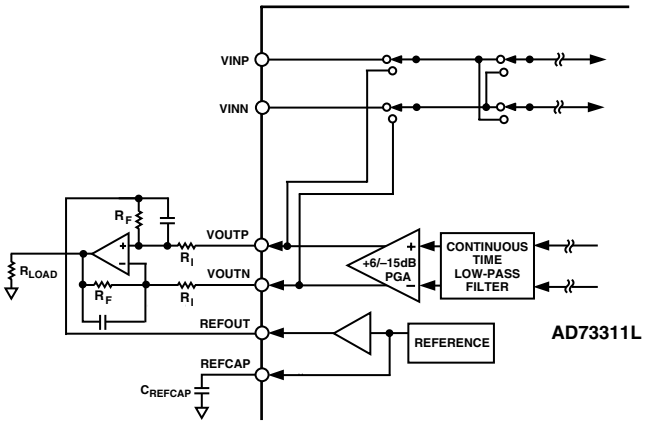


Figure 33. Example Circuit for Differential-to-Single-Ended Output Conversion

Digital Interfacing

The AD73311L is designed to easily interface to most common DSPs. The SCLK, SDO, SDOFS, SDI and SDIFS must be connected to the SCLK, DR, RFS, DT and TFS pins of the DSP respectively. The SE pin may be controlled from a parallel output pin or flag pin such as FL0–2 on the ADSP-218x (or XF on the TMS320C5x) or, where SPORT power-down is not required, it can be permanently strapped high using a suitable pull-up resistor. The $\overline{\text{RESET}}$ pin may be connected to the system hardware reset structure or it may also be controlled using a dedicated control line. In the event of tying it to the global system reset, it is necessary to operate the device in mixed mode, which allows a software reset, otherwise there is no convenient way of resetting the device. Figures 34 and 35 show typical connections to an ADSP-218x and TMS320C5x respectively.

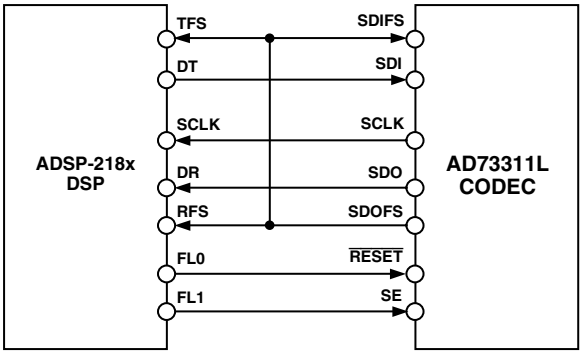


Figure 34. AD73311L Connected to ADSP-218x

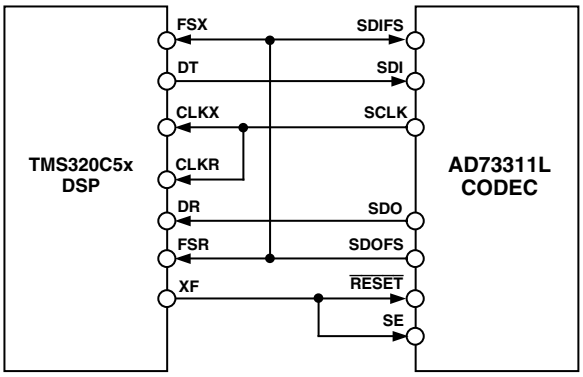


Figure 35. AD73311L Connected to TMS320C5x

Cascade Operation

Where it is required to configure a cascade of up to eight devices, it is necessary to ensure that the timing of the SE and $\overline{\text{RESET}}$ signals are synchronized at each device in the cascade. A simple D-type flip-flop is sufficient to sync each signal to the master clock MCLK, as in Figure 36.

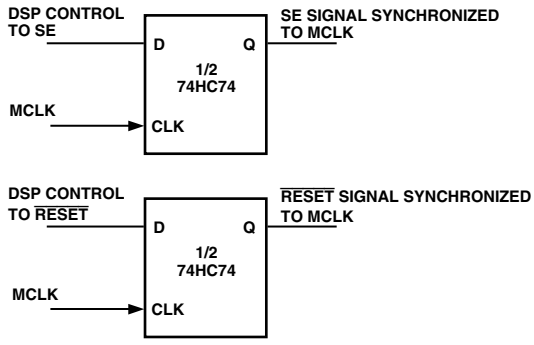


Figure 36. SE and $\overline{\text{RESET}}$ Sync Circuit for Cascaded Operation

Connection of a cascade of devices to a DSP, as shown in Figure 37, is no more complicated than connecting a single device. Instead of connecting the SDO and SDOFS to the DSP's Rx port, these are now daisy-chained to the SDI and SDIFS of the next device in the cascade. The SDO and SDOFS of the final device in the cascade are connected to the DSP's Rx port to complete the cascade. SE and $\overline{\text{RESET}}$ on all devices are fed from the signals that were synchronized with the MCLK using the circuit as described above. The SCLK from only one device need be connected to the DSP's SCLK input(s) as all devices will be running at the same SCLK frequency and phase.

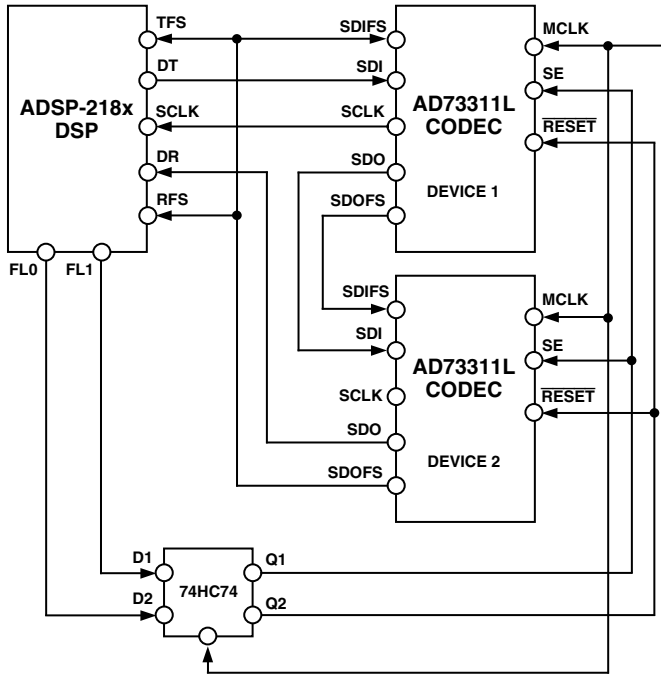


Figure 37. Connection of Two AD73311Ls Cascaded to ADSP-218x

Grounding and Layout

Since the analog inputs to the AD73311L are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the AD73311L are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters on the encoder section will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the AD73311's ADC is high, and the noise levels from the AD73311L are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD73311L should be designed so the analog and digital sections are separated and confined to certain sections of the board. The AD73311L pin configuration offers a major advantage in that its analog and digital interfaces are connected on opposite sides of the package. This facilitates the use of ground planes that can be easily separated, as shown in Figure 38. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place. If this connection is close to the device, it is recommended to use a ferrite bead inductor as shown in Figure 38.

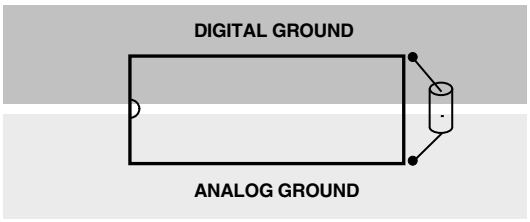


Figure 38. Ground Plane Layout

Avoid running digital lines under the device for they will couple noise onto the die. The analog ground plane should be allowed to run under the AD73311L to avoid noise coupling. The power supply lines to the AD73311L should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND and DGND respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against it. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD73311, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD73311L and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

DSP Programming Considerations

This section discusses some aspects of how the serial port of the DSP should be configured and the implications of whether Rx and Tx interrupts should be enabled.

DSP SPORT Configuration

Following are the key settings of the DSP SPORT required for the successful operation with the AD73311L:

- Configure for external SCLK.
- Serial Word Length = 16 bits.
- Transmit and Receive Frame Syncs required with every word.
- Receive Frame Sync is an input to the DSP.
- Transmit Frame Sync is an:
  Input—in Frame Sync Loop-Back Mode
  Output—in Nonframe Sync Loop-Back Mode.
- Frame Syncs occur one SCLK cycle before the MSB of the serial word.
- Frame Syncs are active high.

DSP SPORT Interrupts

If SPORT interrupts are enabled, it is important to note that the active signals on the frame sync pins do not necessarily correspond with the positions in time of where SPORT interrupts are generated.

On ADSP-218x processors, it is necessary to enable SPORT interrupts and use Interrupt Service Routines (ISRs) to handle Tx/Rx activity, while on the TMS320C5x processors it is possible to poll the status of the Rx and Tx registers, which means that Rx/Tx activity can be monitored using a single ISR that would ideally be the Tx ISR as the Tx interrupt will typically occur before the Rx ISR.

DSP SOFTWARE CONSIDERATIONS WHEN INTERFACING TO THE AD73311L

It is important when choosing the operating mode and hardware configuration of the AD73311L to be aware of their implications for DSP software operation. The user has the flexibility of choosing from either FSLB or nonFSLB when deciding on DSP to AFE connectivity. There is also a choice to be made between using autobuffering of input and output samples or simply choosing to accept them as individual interrupts. As most modern DSP engines support these modes, this appendix will attempt to discuss these topics in a generic DSP sense.

Operating Mode

The AD73311L supports two basic operating modes: Frame Sync Loop Back (FSLB) and nonFSLB (see Interfacing section). As described previously, FSLB has some limitations when used in Mixed Mode but is very suitable for use with the autobuffering feature that is offered on many modern DSPs. Autobuffering allows the user to specify the number of input or output words (samples) that are transferred before a specific Tx or Rx SPORT interrupt is generated. Given that the AD73311L outputs two sample words per sample period, it is possible using autobuffering to have the DSP's SPORT generate a single interrupt on receipt of the second of the two sample words. Additionally, both samples could be stored in a data buffer within the data memory store. This technique has the advantage of reducing the number of both Tx and Rx SPORT interrupts to a single one at each sample interval. The user also knows where each sample is stored. The alternative is to handle a larger number of SPORT interrupts (twice as many in the case of a single AD73311L) while also having some status flags to indicate where each new sample comes from (or is destined for).

Mixed-Mode Operation

To take full advantage of Mixed-Mode operation, it is necessary to configure the DSP/Codec interface in nonFSLB and to disable autobuffering. This allows a variable numbers of words to be sent to the AD73311L in each sample period—the extra words being control words which are typically used to update gain settings in adaptive control applications. The recommended sequence for updating control registers in mixed-mode is to send the control word(s) first before the DAC update word.

It is possible to use Mixed-Mode operation when configured in FSLB, but it is necessary to replace the DAC update with a control word write in each sample period which may cause some discontinuity in the output signal due to a sample point being missed and the previous sample being repeated. This however may be acceptable in some cases as the effect may be masked by gain changes, etc.

Interrupts

The AD73311L transfers and receives information over the serial connection from the DSP's SPORT. This occurs following reset—during the initialization phase—and in both Data-Mode and Mixed-Mode. Each transfer of data to or from the DSP can cause a SPORT interrupt to occur. However, even in FSLB configuration where serial transfers in and out of the DSP are synchronous, it is important to note that Tx and Rx interrupts do not occur at the same time due to the way that Tx and Rx interrupts are generated internally within the DSP's SPORT. This is especially important in time-critical control loop applications where it may be necessary to use Rx interrupts only, as the relative positioning of the Tx interrupts relative to the Rx interrupts in a single sample interval are not suitable for quick update of new DAC positions.

Initialization

Following reset, the AD73311L is in its default condition, which ensures that the device is in Control Mode and must be programmed or initialized from the DSP to start conversions. As communications between AD73311L and the DSP are interrupt driven, it is usually not practical to embed the initialization codes into the body of the initialization routine. It is more practical to put the sequence of initialization codes in a data (or program) memory buffer and to access this buffer with a pointer that is updated on each interrupt. If a circular buffer is used, it allows the interrupt routine to check when the circular buffer pointer has wrapped around—at which point the initialization sequence is complete.

In FSLB configurations, a single control word per codec per sample period is sent to the AD73311L whereas in nonFSLB, it is possible to initialize the device in a single sample period provided the SCLK rate is programmed to a high rate. It is also possible to use autobuffering, in which case an interrupt is generated when the entire initialization sequence has been sent to the AD73311L.

Running the AD73311L with ADCs or DACs in Power-Down

The programmability of the AD73311L allows the user flexibility in choosing which sections of the AD73311L need be powered up. This allows better matching of the power consumption to the application requirements as the AD73311L offers an ADC and a DAC in any combination. The AD73311L always interfaces to the DSP in a standard way regardless of whether the ADC or DAC sections are enabled or disabled. Therefore, the DSP will expect to receive an ADC samples per sample period and to transmit two DAC samples per sample period. If the ADC is disabled (in power-down), its sample value will be invalid. Likewise, a sample sent to a DAC that is disabled will have no effect.

There are two distinct phases of operation of the AD73311L: initialization of the device via the control registers, and operation of the converter sections of each codec. The initialization phase involves programming the control registers of the AD73311L to ensure the required operating characteristics such as sampling rate, serial clock rate, I/O gain, etc. There are several ways in which the DSP can be programmed to initialize the AD73311L. These range from hard-coding a sequence of DSP SPORT Tx register writes with constants used for the initialization words, to putting the initialization sequence in a circular data buffer and using an autobuffered transmit sequence.

Hard-coding involves creating a sequence of writes to the DSP's SPORT Tx buffer which are separated by loops or instructions that idle and wait for the next Tx interrupt to occur as shown in the code below.

```
ax0     = b#1000000100000100;
tx0     = ax0;
idle; {wait for tx register to send current word}
```

The circular buffer approach can be useful if a long initialization sequence is required. The list of initialization words is put into the buffer in the required order.

```
.VAR/DM/RAM/CIRC   init_cmds[8];   {Codec init sequence}
.VAR/DM/RAM  stat_flag;
.INIT   init_cmds:
  b # 1 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 ,
  b # 1 0 0 0 0 0 1 0 1 1 1 1 1 0 0 1 ,
  b # 1 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 ,
  b # 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 ,
  b # 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 ,
  b # 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 ,
  b # 1 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 ,
  b # 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 ,
```

and the DSP program initializes pointers to the top of the buffer

```
i3 = ^init_cmds;          l3 = %init_cmds;
```

and puts the first entry in the DSP's transmit buffer so it is available at the first SDOFS pulse.

```
ax0 = dm(i3,m1);
tx0 = ax0;
```

The DSP's transmit interrupt is enabled.

```
imask = b#0001000000;
```

At each occurrence of an SDOFS pulse, the DSP's transmit buffer contents are sent to the SDI pin of the AD73311L. This also causes a subsequent DSP Tx interrupt which transfers the initialization word, pointed to by the circular buffer pointer, to the Tx buffer. The buffer pointer is updated to point to the next unsent initialization word. When the circular buffer pointer wraps around, which happens after the last word has been accessed, it indicates that the initialization phase is complete. This can be done "manually" in the DSP using a simple address check or autobuffered mode can be used to the complete transfer automatically.

```
txcdat: ar = dm(stat_flag);
  ar = pass ar;
  if eq rti;
  ena sec_reg;
  ax0 = dm (i3, m1);
  tx0 = ax0;
  ax0 = i3;
  ay0 = ^init_cmds;
  ar = ax0 - ay0;
  if gt rti;
  ax0 = 0x00;
  dm (stat_flag) = ax0;
  rti;
```

In the main body of the program, the code loops waiting for the initialization sequence to be completed.

```
check_init:
   ax0 = dm (stat_flag);
   af = pass ax0;
   if ne jump check_init;
```

If the AD73311L is used in a cascade of two or more codec units, it is important to observe some restrictions in the sequence of sending initialization words to the two codecs. It is preferable to send groups of control words for the corresponding control registers in each codec and it is essential to send the control words in descending order—last device first . . . first device last. Control Registers A and B contain settings, such as sampling rate, serial clock rate etc., which critically require synchronous update in each codec.

Once the device has been initialized, Control Register A on each codecs is written with a control word which changes the Operating Mode from Program Mode to either Data Mode or Mixed Control Data Mode. The device count field, which defaults to 000b, will have to be programmed to the required setting—depending on the number of devices in cascade. In Data Mode or Mixed Mode, the main function of the device is to return ADC samples from each codec and to accept DAC words for each codecs. During each sample interval, ADC samples will be returned from the device equal to the number of devices in cascade, while in the same interval DAC update samples will be sent to the device again the number of DAC words being equal to the number of devices in the cascade.

In order to reduce the number of interrupts and to reduce complexity, autobuffering can be used to ensure that only one interrupt is generated during each sampling interval.

APPENDIX A

Configuring an AD73311L to Operate in Data Mode

This section describes the typical sequence of control words that are required to be sent to an AD73311L to set it up for data mode operation. In this sequence, Registers B, C and A are programmed before the device enters data mode. This description panel refers to Table XIX.

At each sampling event, an SDOFS pulse will be observed that will cause a control (programming) word to be sent to the device from the DSP.

Step 1: The first output sample event following device reset. The SDOFS signal is raised, which prepares the DSP Rx Register to accept the ADC word from the AD73311L. As the AD73311L's SDOFS is coupled to the DSP's TFS and RFS, and to the SDIFS of the AD73311L, this event also forces a new control word to be output from the DSP Tx Register to the AD73311L.

Step 2: We observe the status of the channel following the transmission of the control word. The DSP has received the ADC word (invalid because the ADC is not yet powered up) from the AD73311L and the AD73311L has received the control word destined for Control Register B. At this stage, the eight LSBs of the control word are loaded to Control Register B, which sets the internal MCLK divider ratio to 1, SCLK rate to DMCLK/8.

Step 3: The next ADC sample event that occurs raises the SDOFS line of the AD73311L. The DSP Tx Register contains the control word to be written to the AD73311L.

Step 4: Following transmission of the control word, the DSP Rx Register contains the ADC word that during Program Mode is a copy of the control word written at the previous sampling interval where the device address field (Bits 13–11) have been decremented from 000b to 111b. The AD73311L has received a control word that is addressed to Control Register C, which turns on power to the ADC, DAC, REFCAP and buffered REFOUT.

Steps 5 and 6: The programming phase is completed by sending a control word addressed to Control Register A, which sets the device in Data Mode.

Step 7: The AD73311L provides its first valid ADC sample as the ADC has been powered up and data mode is enabled. In data mode all words sent *to* the device are interpreted as DAC words. Likewise, all words received *from* the device are interpreted as ADC words.

Step 8: The first DAC word has been transmitted to the device and is loaded to the internal DAC register.

Steps 9 and 10: Another ADC read and DAC write cycle.

Table XIX.

Step	DSP Tx	AD73311L	DSP Rx
1	1000000100001011	0000000000000000	xxxxxxxxxxxxxxxx
2	1000001011111001	1000000100001011	0000000000000000
3	1000001011111001	1000000100001011	xxxxxxxxxxxxxxxx
4	1000000000000001	1000001001111001	1011100100001011
5	1000000000000001	1000001011111001	xxxxxxxxxxxxxxxx
6	DAC WORD N	1000000000000001	1011101011111001
7	DAC WORD N	ADC RESULT N	xxxxxxxxxxxxxxxx
8	DAC WORD N+1	DAC WORD N	ADC RESULT N
9	DAC WORD N+1	ADC RESULT N+1	xxxxxxxxxxxxxxxx
10	DAC WORD N+2	DAC WORD N+1	ADC RESULT N+1

APPENDIX B

Configuring an AD73311L to Operate in Mixed Mode

This section describes a typical sequence of control words that would be sent to an AD73311L to configure it for operation in mixed mode. It is not intended to be a definitive initialization sequence, but will show users the typical input/output events that occur in the programming and Operation Phases[1]. This description panel refers to Table XX.

Steps 1–3 detail the transfer of the control words to Control Register A, which programs the device for Mixed-Mode operation. In Step 1, we have the first output sample event following device reset. The SDOFS signal is raised which prepares the DSP Rx register to accept the ADC word from the AD73311L. The device is configured as nonFSLB, which means that the DSP has control over what is transmitted to the device and in this case we will not transmit to the device until the output word has been received from the AD73311L.

In Step 2 the DSP has now received the ADC word. Typically, an interrupt will be generated following reception of the output words by the DSP. The transmit register of the DSP is loaded with the control word destined for the AD73311L. This generates a transmit frame-sync (TFS) that is input to the SDIFS input of the AD73311L to indicate the start of transmission.

In Step 3 the device has received a control word that addresses Control Register A and programs the channels into Mixed Mode-MM and $\overline{\text{PGM}}$/DATA set to one. Following Step 3, the device has been programmed into mixed-mode although none of the analog sections have been powered up (controlled by Control Register C). Steps 4–6 detail update of Control Register B in mixed-mode. In Steps 4, 5 the ADC sample, which is invalid as the ADC section is not yet powered up, is transferred to the DSP's Rx section. In the subsequent interrupt service routine the Tx register is loaded with the control word setting for Control Register B which programs DMCLK = MCLK, the sampling rate to DMCLK/256, SCLK = DMCLK/2.

Steps 7–10 are similar to Steps 4–6 except that Control Register C is programmed to power up all analog sections (ADC, DAC, Reference = 1.2 V, REFOUT). In Step 10, a DAC word is sent to the device. As the channels are in mixed mode, the serial port interrogates the MSB of the 16-bit word sent to determine whether it contains DAC data or control information.

Steps 7–10 illustrate the implementation of Control Register update and DAC update in a single sample period. Note that this combination is not possible in the FSLB configuration[2]. Steps 11–15 illustrate a Control Register readback cycle. In Step 13, the device has received a Control Word that addresses Control Register C for readback (Bit 14 of the Control Word = 1). When the device receives the readback request, the register contents are loaded to the serial register as shown in Step 14. SDOFS is raised in the device, which causes the readback word to be shifted out toward the DSP. In Step 15, the DSP has received the readback word (note that the address field in the readback word has been decremented to 111b). Steps 16–18 detail an ADC and DAC update cycle using the nonFSLB configuration. In this case no Control Register update is required.

NOTES

[1]This sequence assumes that the DSP SPORT's Rx and Tx interrupts are enabled. It is important to ensure there is no latency (separation) between control words in a cascade configuration. This is especially the case when programming Control Registers A and B.

[2]Mixed mode operation with the FSLB configuration is more restricted in that only a single word can be sent per sample period.

Table XX. Mixed Mode Operation

Step	DSP Tx	AD73311L	DSP Rx
1	DON'T CARE xxxxxxxxxxxxxxxx	OUTPUT CH1 0000000000000000	DON'T CARE xxxxxxxxxxxxxxxx
2	CRA-CH1 1000101011111001	DON'T CARE xxxxxxxxxxxxxxxx	OUTPUT CH1 0000000000000000
3	DON'T CARE xxxxxxxxxxxxxxxx	CRA-CH1 1000000000010011	DON'T CARE xxxxxxxxxxxxxxxx
4	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000	DON'T CARE xxxxxxxxxxxxxxxx
5	CRB-CH1 1000100100001001	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000
6	DON'T CARE xxxxxxxxxxxxxxxx	CRB-CH1 1000000100001011	DON'T CARE xxxxxxxxxxxxxxxx
7	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000	DON'T CARE xxxxxxxxxxxxxxxx
8	CRC-CH1 1000101011111001	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000
9	DAC WORD 0111111111111111	CRC-CH1 1000001011111001	DON'T CARE xxxxxxxxxxxxxxxx
10	DAC WORD 1000000000000000	DAC WORD 0111111111111111	DON'T CARE xxxxxxxxxxxxxxxx
11	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000	DON'T CARE xxxxxxxxxxxxxxxx
12	CRC-CH1 10000010xxxxxxxx	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 0000000000000000
13	DON'T CARE xxxxxxxxxxxxxxxx	CRC-CH1 10000010xxxxxxxx	DON'T CARE xxxxxxxxxxxxxxxx
14	DON'T CARE xxxxxxxxxxxxxxxx	READBACK CH 1 1100001011111001	DON'T CARE xxxxxxxxxxxxxxxx
15	DON'T CARE xxxxxxxxxxxxxxxx	DON'T CARE xxxxxxxxxxxxxxxx	READBACK CH 1 1111001011111001
16	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 ????????????????	DON'T CARE xxxxxxxxxxxxxxxx
17	DAC WORD CH 1 0111111111111111	DON'T CARE xxxxxxxxxxxxxxxx	ADC RESULT CH1 ????????????????
18	DAC WORD CH 1 1000000000000000	DAC WORD CH 1 0111111111111111	DON'T CARE xxxxxxxxxxxxxxxx

APPENDIX C

Configuring a Cascade of Two AD73311Ls to Operate in Data Mode[1]

This section describes the typical sequence of control words that are required to be sent to a cascade of two AD73311Ls to set them up for data mode operation. In this sequence Registers B, C and A are programmed before the device enters data mode. This description panel refers to Table XXI.

At each sampling event, a pair of SDOFS pulses will be observed which will cause a pair of control (programming) words to be sent to the device from the DSP. It is advisable that each pair of control words should program a single register in each device. The sequence to be followed is Device 2 followed by Device 1.

In Step 1, we have the first output sample event following device reset. The SDOFS signal is raised on both devices simultaneously, which prepares the DSP Rx register to accept the ADC word from Device 2, while SDOFS from Device 1 becomes an SDIFS to Device 2. As the SDOFS of Device 2 is coupled to the DSP's TFS and RFS, and to the SDIFS of Device 1, this event also forces a new control word to be output from the DSP Tx register to Device 1.

In Step 2, we observe the status of the devices following the transmission of the first control word. The DSP has received the output word from Device 2, while Device 2 has received the output word from Device 1. Device 1 has received the Control word destined for Device 2. At this stage, the SDOFS of both devices are again raised because Device 2 has received Device 1's output word, and as it is not a valid control word addressed to Device 2, it is passed on to the DSP. Likewise, Device 1 has received a control word destined for Device 2-address field is not zero-and it decrements the address field of the control word and passes it on.

Step 3 shows completion of the first series of control word writes. The DSP has now received both output words and each device has received a control word that addresses control register B and sets the internal MCLK divider ratio to 1, SCLK rate to DMCLK/2 and sampling rate to DMCLK/256. Note that both devices are updated simultaneously as both receive the addressed control word at the same time. This is an important factor in cascaded operation as any latency between updating the SCLK or DMCLK of devices can result in corrupted operation. This will not happen in the case of an FSLB configuration as shown here, but must be taken into account in a nonFSLB configuration. One other important observation of this sequence is that the data words are received and transmitted in reverse order, i.e., the ADC words are received by the DSP, Device 2 first, then Device 1 and, similarly, the transmit words from the DSP are sent to Device 2 first, then to Channel 1. This ensures that all devices are updated at the same time. Steps 4–6 are similar to Steps 1–3 but, instead, program Control Register C to power-up the analog sections of the device (ADCs, DACs and reference). Steps 7–9 are similar to Steps 1–3 but, instead, program Control Register A, with a device count field equal to two devices in cascade and sets the $\overline{\text{PGM}}$/DATA bit to one to put the device in data mode.

In Step 10, the programming phase is complete and we now begin actual device data read and write. The words loaded into the serial registers of the two devices at the ADC sampling event now contain valid ADC data and the words written to the devices from the DSP's Tx register will now be interpreted as DAC words. The DSP Tx register contains the DAC word for Device 2.

In Step 11, the first DAC word has been transmitted into the cascade and the ADC word from Device 2 has been read from the cascade. The DSP Tx register now contains the DAC word for Device 1. As the words being sent to the cascade are now being interpreted as 16-bit DAC words, the addressing scheme now changes from one where the address was embedded in the transmitted word, to one where the serial port now counts the SDIFS pulses. When the number of SDIFS pulses received equals the value in the Device count field of Control Register A, the length of the cascade-each device updates its DAC register with the present word in its serial register. In Step 11 each device has received only one SDIFS pulse; Device 2 received one SDIFS from the SDOFS of Device 1 when it sent its ADC word, and Device 1 received one SDIFS pulse when it received the DAC word for Device 2 from the DSP's Tx register. Therefore, each device raises its SDOFS line to pass on the current word in its serial register, and each device now receives another SDIFS pulse.

Step 12 shows the completion of an ADC read and DAC write cycle. Following Step 11, each device has received two SDIFS pulses that equal the setting of the device count field in Control Register A. The DAC register in each device is now updated with the contents of the word that accompanied the SDIFS pulse that satisfied the device count requirement. The internal frame sync counter is now reset to zero and will begin counting for the next DAC update cycle. Steps 10–12 are repeated on each sampling event.

NOTE

[1]This sequence assumes that the DSP SPORT's Rx and Tx interrupts are enabled. It is important to ensure that there is no latency (separation) between control words in a cascade configuration. This is especially the case when programming Control Registers A and B, as they must be updated synchronously in each channel.

Table XXI. Data Mode Operation

Step	DSP Tx	AD733111L Device 1	AD73311L Device 2	DSP Rx
1	CRB-CH2	OUTPUT CH1	OUTPUT CH2	DON'T CARE
	1000100100001011	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
2	CRB-CH1	CRB-CH2	OUTPUT CH1	OUTPUT CH2
	1000000100001011	1000100100001011	0000000000000000	0000000000000000
3	CRC-CH2	CRB-CH1	CRB-CH2	OUTPUT CH1
	1000101011111001	1000000100001011	1000000100001011	0000000000000000
4	CRC-CH2	OUTPUT CH1	OUTPUT CH2	DON'T CARE
	1000101011111001	1000000100001011	1000000100001011	xxxxxxxxxxxxxxxx
5	CRC-CH1	CRC-CH2	OUTPUT CH2	OUTPUT CH2
	1000001011111001	1000101011111001	1011100100001011	1011100100001011
6	CRA-CH2	CRC-CH1	CRC-CH2	OUTPUT CH1
	1000100000010001	1000001011111001	1000001011111001	1011000100001011
7	CRA-CH2	OUTPUT CH1	OUTPUT CH2	DON'T CARE
	1000100000010001	1000001011111001	1000001011111001	xxxxxxxxxxxxxxxx
8	CRA-CH1	CRA-CH2	OUTPUT CH2	OUTPUT CH2
	1000000000010001	1000100000010001	1011101011111001	1011101011111001
9	CRB-CH2	CRA-CH1	CRA-CH2	OUTPUT CH1
	0111111111111111	1000000000010001	1000000000010001	1011001011111001
10	DAC WORD CH 2	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
	0111111111111111	????????????????	????????????????	xxxxxxxxxxxxxxxx
11	DAC WORD CH 1	DAC WORD CH 2	ADC RESULT CH1	ADC RESULT CH2
	1000000000000000	0111111111111111	????????????????	????????????????
12	DON'T CARE	DAC WORD CH 1	DAC WORD CH 2	ADC RESULT CH1
	xxxxxxxxxxxxxxxx	1000000000000000	0111111111111111	????????????????

APPENDIX D

Configuring a cascade of two AD73311Ls to Operate in Mixed Mode

This section describes a typical sequence of control words that would be sent to a cascade of two AD73311Ls to configure them for operation in mixed mode. It is not intended to be a definitive initialization sequence, but will show users the typical input/output events that occur in the programming and operation phases.[1] This description panel refers to Table XXII.

Steps 1–5 detail the transfer of the control words to Control Register A, which programs the devices for Mixed-Mode operation. In Step 1, we have the first output sample event following device reset. The SDOFS signal is simultaneously raised on both devices, which prepares the DSP Rx register to accept the ADC word from Device 2 while SDOFS from Device 1 becomes an SDIFS to Device 2. The cascade is configured as nonFSLB, which means that the DSP has control over what is transmitted to the cascade[2] and in this case we will not transmit to the devices until both output words have been received from the AD73311Ls.

In Step 2, we observe the status of the devices following the reception of the Device 2 output word. The DSP has received the ADC word from Device 2, while Device 2 has received the output word from Device 1. At this stage, the SDOFS of Device 2 is again raised because Device 2 has received Channel 1's output word and, as it is not addressed to Device 2, it is passed on to the DSP.

In Step 3 the DSP has now received both ADC words. Typically, an interrupt will be generated following reception of the two output words by the DSP (this involves programming the DSP to use autobuffered transfers of two words). The transmit register of the DSP is loaded with the control word destined for Device 2. This generates a transmit frame-sync (TFS) that is input to the SDIFS input of the AD73311L (Device 1) to indicate the start of transmission.

In Step 4, Device 1 now contains the Control Word destined for Device 2. The address field is decremented, SDOFS1 is raised (internally) and the Control word is passed on to Channel 2. The Tx register of the DSP has now been updated with the Control Word destined for Device 1 (this can be done using autobuffering of transmit or by handling transmit interrupts following each word sent).

In Step 5 each device has received a control word that addresses Control Register A and sets the device count field equal to two devices and programs the devices into Mixed Mode—MM and $\overline{\text{PGM}}$/DATA set to one. Following Step 5, the device has been programmed into mixed-mode although none of the analog sections have been powered up (controlled by Control Register C). Steps 6–10 detail update of Control Register B in mixed-mode. In Steps 6–8 the ADC samples, which are invalid as the ADC section is not yet powered up, are transferred to the DSP's Rx section. In the subsequent interrupt service routine the Tx Register is loaded with the control word for Device 2. In Steps 9–10, Devices 1 and 2 are loaded with a control word setting for Control Register B which programs DMCLK = MCLK, the sampling rate to DMCLK/256, SCLK = DMCLK/2.

Steps 11–17 are similar to Steps 6–12 except that Control Register C is programmed to power up all analog sections (ADC, DAC, Reference = 2.4 V, REFOUT). In Steps 16–17, DAC words are sent to the device—both DAC words are necessary as each device will only update its DAC when the device has counted a number of SDIFS pulses, accompanied by DAC words (in mixed-mode, the MSB = 0), that is equal to the device count field of Control Register A[3]. As the devices are in mixed mode, the serial port interrogates the MSB of the 16-bit word sent to determine whether it contains DAC data or control information. DAC words should be sent in the sequence Channel 2 followed by Device 1.

Steps 11–17 illustrate the implementation of Control Register update and DAC update in a single sample period. Note that this combination is not possible in the FSLB configuration.[2]

Steps 18–25 illustrate a Control Register readback cycle. In Step 22, both devices have received a Control Word that addresses Control Register C for readback (Bit 14 of the Control Word = 1). When the devices receive the readback request, the register contents are loaded to the serial registers as shown in Step 23. SDOFS is raised in both devices, which causes these readback words to be shifted out toward the DSP. In Step 24, the DSP has received the Device 2 readback word while Device 2 has received the Device 1 readback word (note that the address field in both words has been decremented to 111b). In Step 25, the DSP has received the Device 1 readback word (its address field has been further decremented to 110b).

Steps 26–30 detail an ADC and DAC update cycle using the nonFSLB configuration. In this case no Control Register update is required.

NOTES

[1]This sequence assumes that the DSP SPORT's Rx and Tx interrupts are enabled. It is important to ensure there is no latency (separation) between control words in a cascade configuration. This is especially the case when programming Control Registers A and B.

[2]Mixed mode operation with the FSLB configuration is more restricted in that the number of words sent to the cascade equals the number of devices in the cascade, which means that DAC updates may need to be substituted with a register write or read.

[3]In mixed mode, DAC update is done using the same SDIFS counting scheme as in normal data mode with the exception that only DAC words (MSB set to zero) are recognized as being able to increment the frame sync counters.

Table XXII. Mixed Mode Operation

Step	DSP Tx	AD73311L Device 1	AD73311L Device 2	DSP Rx
	DON'T CARE	OUTPUT CH1	OUTPUT CH2	DON'T CARE
1	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	OUTPUT CH1	OUTPUT CH2
2	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRA-CH2	DON'T CARE	DON'T CARE	OUTPUT CH1
3	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRA-CH1	CRA-CH2	DON'T CARE	DON'T CARE
4	1000000000010011	1000100000010011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRA-CH1	CRA-CH2	DON'T CARE
5	xxxxxxxxxxxxxxxx	1000000000010011	1000000000010011	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
6	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
7	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRB-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
8	1000100100001011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRB-CH1	CRB-CH2	DON'T CARE	DON'T CARE
9	1000000100001011	1000100100001011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRB-CH1	CRB-CH2	DON'T CARE
10	xxxxxxxxxxxxxxxx	1000000100001011	1000000100001011	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
11	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
12	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRC-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
13	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRC-CH1	CRC-CH2	DON'T CARE	DON'T CARE
14	1000001011111001	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DAC WORD CH 2	CRC-CH1	CRC-CH2	DON'T CARE
15	0111111111111111	1000001011111001	1000001011111001	xxxxxxxxxxxxxxxx
	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE	DON'T CARE
16	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE
17	xxxxxxxxxxxxxxxx	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
18	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
19	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRC-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
20	11001010xxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRC-CH1	CRC-CH2	DON'T CARE	DON'T CARE
21	10000010xxxxxxxx	11001010xxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRC-CH1	CRC-CH2	DON'T CARE
22	xxxxxxxxxxxxxxxx	10000010xxxxxxxx	10000010xxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	READBACK CH 1	READBACK CH 2	DON'T CARE
23	xxxxxxxxxxxxxxxx	1100001011111001	1100001011111001	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	READBACK CH 1	READBACK CH 2
24	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	1111101011111001	1111101011111001
	DON'T CARE	DON'T CARE	DON'T CARE	READBACK CH 1
25	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	1111001011111001
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
26	xxxxxxxxxxxxxxxx	????????????????	????????????????	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
27	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	????????????????	????????????????
	DAC WORD CH 2	DON'T CARE	DON'T CARE	ADC RESULT CH1
28	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	????????????????
	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE	DON'T CARE
29	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE
30	xxxxxxxxxxxxxxxx	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx

APPENDIX E

DAC Timing Control Example

The AD73311's DAC is loaded from the DAC register contents just before the ADC register contents are loaded to the serial register (SDOFS going high). This default DAC load position can be advanced in time to occur earlier with respect to the SDOFS going high. Figure 39 shows an example of the ADC unload and DAC load sequence. At time t_1 the SDOFS is raised to indicate that a new ADC word is ready. Following the SDOFS pulse, 16 bits of ADC data are clocked out on SDO in the subsequent 16 SCLK cycles finishing at time t_2 where the DSP's SPORT will have received the 16-bit word. The DSP may process this information and generate a DAC word to be sent to the AD73311. Time t_3 marks the beginning of the sequence of sending the DAC word to the AD73311. This sequence ends at time t_4 where the DAC register will be updated from the 16 bits in the AD73311's serial register. However, the DAC will not be updated from the DAC register until time t_5, which may not be acceptable in certain applications. In order to reduce this delay and load the DAC at time t_6, the DAC advance register can be programmed with a suitable setting corresponding to the required time advance (refer to Table VIII for details of DAC Timing Control settings).

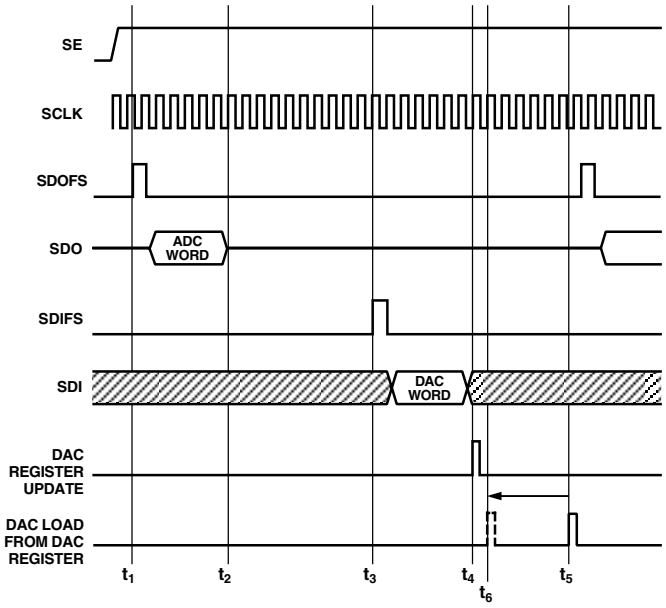


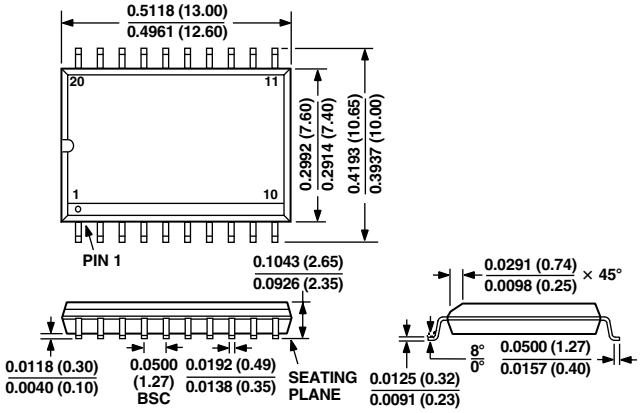
Figure 39. DAC Timing Control

C00689a–2.5–8/00 (rev. A)

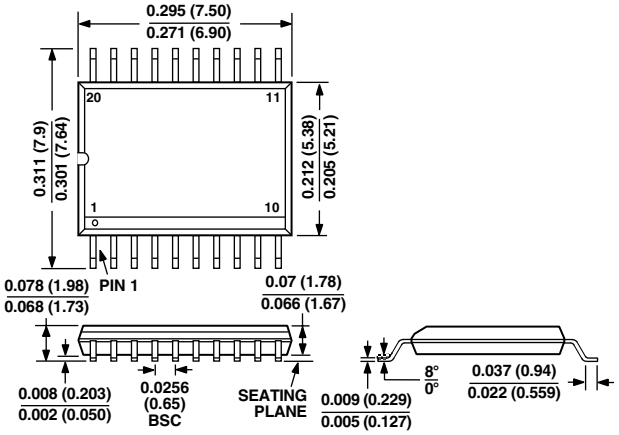
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

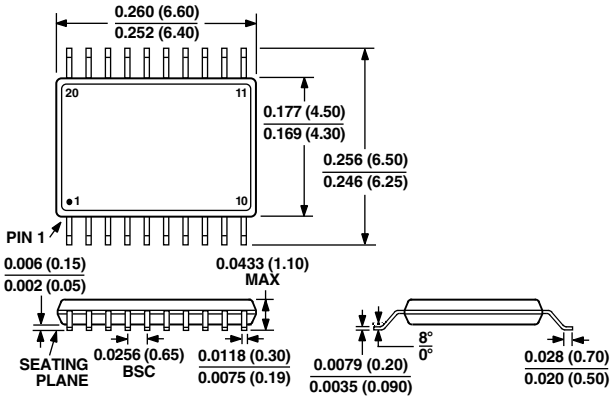
20-Lead Small Outline IC (R-20)



20-Lead Shrink Small Outline IC (RS-20)



20-Lead Thin Shrink Small Outline IC (RU-20)



PRINTED IN U.S.A.