3 V/5 V, 2 MSPS, 8-Bit, 1-/4-/8-Channel Sampling ADCs

AD7822/AD7825/AD7829

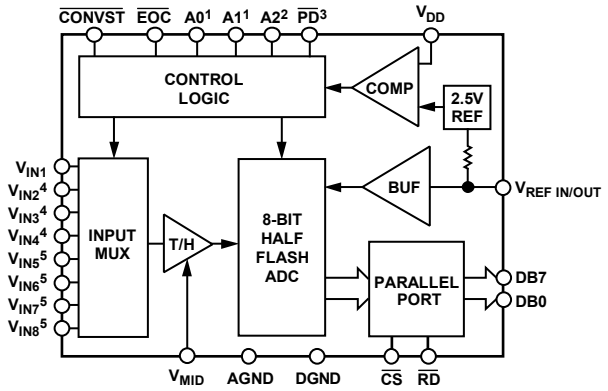
FEATURES

- 8-bit half-flash ADC with 420 ns conversion time
- One, four, and eight single-ended analog input channels
  - Available with input offset adjust
- On-chip track-and-hold
- SNR performance given for input frequencies up to 10 MHz
- On-chip reference (2.5 V)
- Automatic power-down at the end of conversion
- Wide operating supply range
  - 3 V ± 10% and 5 V ± 10%
- Input ranges
  - 0 V to 2 V p-p, V_{DD} = 3 V ± 10%
  - 0 V to 2.5 V p-p, V_{DD} = 5 V ± 10%
- Flexible parallel interface with $\overline{EOC}$ pulse to allow standalone operation

APPLICATIONS

- Data acquisition systems, DSP front ends
- Disk drives
- Mobile communication systems, subsampling applications

FUNCTIONAL BLOCK DIAGRAM



[1] A0, A1 AD7825/AD7829
[2] A2 AD7829
[3] PD AD7822/AD7825
[4] V_{IN2} TO V_{IN4} AD7825/AD7829
[5] V_{IN5} TO V_{IN8} AD7829

01321-001

Figure 1.

GENERAL DESCRIPTION

The AD7822/AD7825/AD7829 are high speed, 1-, 4-, and 8-channel, microprocessor-compatible, 8-bit analog-to-digital converters with a maximum throughput of 2 MSPS. The AD7822/AD7825/AD7829 contain an on-chip reference of 2.5 V (2% tolerance); a track-and-hold amplifier; a 420 ns, 8-bit half-flash ADC; and a high speed parallel interface. The converters can operate from a single 3 V ± 10% and 5 V ± 10% supply.

The AD7822/AD7825/AD7829 combine the convert start and power-down functions at one pin, that is, the $\overline{CONVST}$ pin. This allows a unique automatic power-down at the end of a conversion to be implemented. The logic level on the $\overline{CONVST}$ pin is sampled after the end of a conversion when an $\overline{EOC}$ (end of conversion) signal goes high. If it is logic low at that point, the ADC is powered down. The AD7822 and AD7825 also have a separate power-down pin (see the Operating Modes section).

The parallel interface is designed to allow easy interfacing to microprocessors and DSPs. Using only address decoding logic, the parts are easily mapped into the microprocessor address space. The $\overline{EOC}$ pulse allows the ADCs to be used in a stand-alone manner (see the Parallel Interface section.)

The AD7822 and AD7825 are available in 20-lead and 24-lead, 0.3" wide, plastic dual in-line packages (PDIP); 20-lead and 24-lead standard small outline packages (SOIC); and 20-lead and 24-lead thin shrink small outline packages (TSSOP). The AD7829 is available in a 28-lead, 0.6" wide PDIP; a 28-lead SOIC; and a 28-lead TSSOP.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time. The AD7822/AD7825/AD7829 have a conversion time of 420 ns. Faster conversion times maximize the DSP processing time in a real-time system.
2. Analog Input Span Adjustment. The V_{MID} pin allows the user to offset the input span. This feature can reduce the requirements of single-supply op amps and take into account any system offsets.
3. FPBW (Full Power Bandwidth) of Track-and-Hold. The track-and-hold amplifier has an excellent high frequency performance. The AD7822/AD7825/AD7829 are capable of converting full-scale input signals up to a frequency of 10 MHz. This makes the parts ideally suited to subsampling applications.
4. Channel Selection. Channel selection is made without the necessity of writing to the part.

Rev. C
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REVISION HISTORY

8/06—Rev. B to Rev. C

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12/99—**Rev. 0 to Rev. A**

SPECIFICATIONS

V_{DD} = 3 V ± 10%, V_{DD} = 5 V ± 10%, GND = 0 V, $V_{REF\ IN/OUT}$ = 2.5 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Version B	Unit	Test Condition/Comment
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz, f_{SAMPLE} = 2 MHz
Signal to (Noise + Distortion) Ratio[1]	48	dB min	
Total Harmonic Distortion[1]	−55	dB max	
Peak Harmonic or Spurious Noise[1]	−55	dB max	
Intermodulation Distortion[1]			fa = 27.3 kHz, fb = 28.3 kHz
Second-Order Terms	−65	dB typ	
Third-Order Terms	−65	dB typ	
Channel-to-Channel Isolation[1]	−70	dB typ	f_{IN} = 20 kHz
DC ACCURACY			
Resolution	8	Bits	
Minimum Resolution for Which			
No Missing Codes Are Guaranteed	8	Bits	
Integral Nonlinearity (INL)[1]	±0.75	LSB max	
Differential Nonlinearity (DNL)[1]	±0.75	LSB max	
Gain Error[1]	±2	LSB max	
Gain Error Match[1]	±0.1	LSB typ	
Offset Error[1]	±1	LSB max	
Offset Error Match[1]	±0.1	LSB typ	
ANALOG INPUTS[2]			See Analog Input section
V_{DD} = 5 V ± 10%			Input voltage span = 2.5 V
V_{IN1} to V_{IN8} Input Voltage	V_{DD}	V max	
	0	V min	
V_{MID} Input Voltage	V_{DD} − 1.25	V max	Default V_{MID} = 1.25 V
	1.25	V min	
V_{DD} = 3 V ± 10%			Input voltage span = 2 V
V_{IN1} to V_{IN8} Input Voltage	V_{DD}	V max	
	0	V min	
V_{MID} Input Voltage	V_{DD} − 1	V max	Default V_{MID} = 1 V
	1	V min	
V_{IN} Input Leakage Current	±1	µA max	
V_{IN} Input Capacitance	15	pF max	
V_{MID} Input Impedance	6	kΩ typ	
REFERENCE INPUT			
$V_{REF\ IN/OUT}$ Input Voltage Range	2.55	V max	2.5 V + 2%
	2.45	V min	2.5 V − 2%
Input Current	1	µA typ	
	100	µA max	
ON-CHIP REFERENCE			Nominal 2.5 V
Reference Error	±50	mV max	
Temperature Coefficient	50	ppm/°C typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 10%
Input High Voltage, V_{INH}	2	V min	V_{DD} = 3 V ± 10%
Input Low Voltage, V_{INL}	0.4	V max	V_{DD} = 3 V ± 10%
Input Current, I_{IN}	±1	µA max	10 nA typical, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF max	

Parameter	Version B	Unit	Test Condition/Comment
LOGIC OUTPUTS			
Output High Voltage, V_{OH}			I_{SOURCE} = 200 µA
	4	V min	V_{DD} = 5 V ± 10%
	2.4	V min	V_{DD} = 3 V ± 10%
Output Low Voltage, V_{OL}			I_{SINK} = 200 µA
	0.4	V max	V_{DD} = 5 V ± 10%
	0.2	V max	V_{DD} = 3 V ± 10%
High Impedance Leakage Current	±1	µA max	
High Impedance Capacitance	10	pF max	
CONVERSION RATE			
Track-and-Hold Acquisition Time	200	ns max	See Circuit Description section
Conversion Time	420	ns max	
POWER SUPPLY REJECTION			
V_{DD} ± 10%	±1	LSB max	
POWER REQUIREMENTS			
V_{DD}	4.5	V min	5 V ± 10%; for specified performance
	5.5	V max	
V_{DD}	2.7	V min	3 V ± 10%; for specified performance
	3.3	V max	
I_{DD}			
Normal Operation	12	mA max	8 mA typical
Power-Down	5	µA max	Logic inputs = 0 V or V_{DD}
	0.2	µA typ	
Power Dissipation			V_{DD} = 3 V
Normal Operation	36	mW max	24 mW typical
Power-Down			
200 kSPS	9.58	mW typ	
500 kSPS	23.94	mW typ	

[1] See the Terminology section of this data sheet.
[2] Refer to the Analog Input section for an explanation of the analog input(s).

TIMING CHARACTERISTICS

$V_{REF\ IN/OUT}$ = 2.5 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	5 V ± 10%	3 V ± 10%	Unit	Conditions/Comments
t_1	420	420	ns max	Conversion time
t_2	20	20	ns min	Minimum $\overline{CONVST}$ pulse width
t_3	30	30	ns min	Minimum time between the rising edge of $\overline{RD}$ and the next falling edge of convert star
t_4	110	110	ns max	$\overline{EOC}$ pulse width
	70	70	ns min	
t_5	10	10	ns max	$\overline{RD}$ rising edge to $\overline{EOC}$ pulse high
t_6	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_7	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_8	30	30	ns min	Minimum $\overline{RD}$ pulse width
t_9[3]	10	20	ns max	Data access time after $\overline{RD}$ low
t_{10}[4]	5	5	ns min	Bus relinquish time after $\overline{RD}$ high
	20	20	ns max	
t_{11}	10	10	ns min	Address setup time before falling edge of $\overline{RD}$
t_{12}	15	15	ns min	Address hold time after falling edge of $\overline{RD}$
t_{13}	200	200	ns min	Minimum time between new channel selection and convert start
$t_{POWER\ UP}$	25	25	µs typ	Power-up time from rising edge of $\overline{CONVST}$ using on-chip reference
$t_{POWER\ UP}$	1	1	µs max	Power-up time from rising edge of $\overline{CONVST}$ using external 2.5 V reference

[1] Sample tested to ensure compliance.
[2] See Figure 24, Figure 25, and Figure 26.
[3] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V with V_{DD} = 5 V ± 10%, and time required for an output to cross 0.4 V or 2.0 V with V_{DD} = 3 V ± 10%.
[4] Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{10}, quoted in the timing characteristics is the true bus relinquish time of the part and, as such, is independent of external bus loading capacitances.

TIMING DIAGRAM

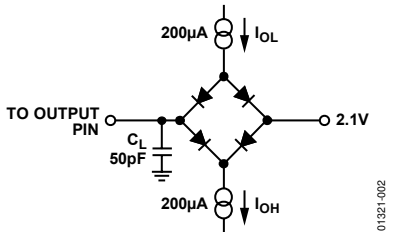


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
V_{IN1} to V_{IN8}	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
V_{MID} Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
PDIP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	105°C/W
Lead Temperature, (Soldering, 10 sec)	260°C
SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	128°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

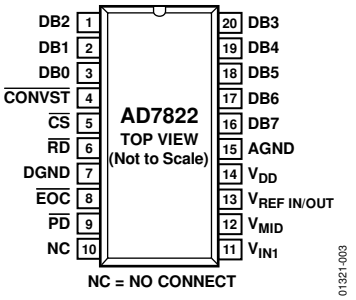


Figure 3. Pin Configuration

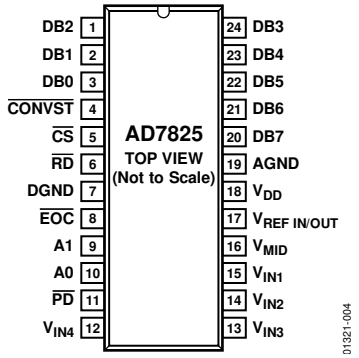


Figure 4. Pin Configuration

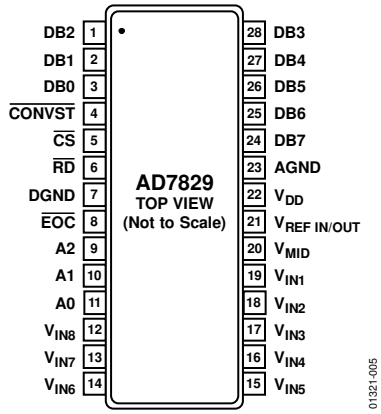


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Mnemonic	Description
V_{IN1} to V_{IN8}	Analog Input Channels. The AD7822 has a single input channel; the AD7825 and AD7829 have four and eight analog input channels, respectively. The inputs have an input span of 2.5 V and 2 V depending on the supply voltage (V_{DD}). This span can be centered anywhere in the range AGND to V_{DD} using the V_{MID} pin. The default input range (V_{MID} unconnected) is AGND to 2 V (V_{DD} = 3 V ± 10%) or AGND to 2.5 V (V_{DD} = 5 V ± 10%). See the Analog Input section of the data sheet for more information.
V_{DD}	Positive Supply Voltage, 3 V ± 10% and 5 V ± 10%.
AGND	Analog Ground. Ground reference for track-and-hold, comparators, reference circuit, and multiplexer.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{\text{CONVST}}$	Logic Input Signal. The convert start signal initiates an 8-bit analog-to-digital conversion on the falling edge of this signal. The falling edge of this signal places the track-and-hold in hold mode. The track-and-hold goes into track mode again 120 ns after the start of a conversion. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of a conversion. If it is logic low, the AD7822/AD7825/AD7829 powers down (see the Operating Modes section of the data sheet).
$\overline{\text{EOC}}$	Logic Output. The end-of-conversion signal indicates when a conversion has finished. The signal can be used to interrupt a microcontroller when a conversion has finished or latch data into a gate array (see the Parallel Interface section).
$\overline{\text{CS}}$	Logic Input Signal. The chip select signal is used to enable the parallel port of the AD7822/AD7825/AD7829. This is necessary if the ADC is sharing a common data bus with another device.
$\overline{\text{PD}}$	Logic Input. The power-down pin is present on the AD7822 and AD7825 only. Bringing the $\overline{\text{PD}}$ pin low places the AD7822 and AD7825 in power-down mode. The ADCs power up when $\overline{\text{PD}}$ is brought logic high again.
$\overline{\text{RD}}$	Logic Input Signal. The read signal is used to take the output buffers out of their high impedance state and drive data onto the data bus. The signal is internally gated with the $\overline{\text{CS}}$ signal. Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ must be logic low to enable the data bus.
A0 to A2	Channel Address Inputs. The address of the next multiplexer channel must be present on these inputs when the $\overline{\text{RD}}$ signal goes low.
DB0 to DB7	Data Output Lines. They are normally held in a high impedance state. Data is driven onto the data bus when both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ go active low.
$V_{REF\ IN/OUT}$	Analog Input and Output. An external reference can be connected to the AD7822/AD7825/AD7829 at this pin. The on-chip reference is also available at this pin. When using the internal reference, this pin can be left unconnected or, in some cases, it can be decoupled to AGND with a 0.1 µF capacitor.
V_{MID}	The V_{MID} pin, if connected, is used to center the analog input span anywhere in the range of AGND to V_{DD} (see the Analog Input section).

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
The measured ratio of signal-to-(noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(*Noise* + *Distortion*) = (6.02 *N* + 1.76) dB

Thus, for an 8-bit converter, this is 50 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7822/AD7825/AD7829, it is defined as

$$THD\ (\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, … . Intermodulation terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7822/AD7825/AD7829 are tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second- and third-order terms are of different significance. The second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in decibels (dB).

Channel-to-Channel Isolation
A measure of the level of crosstalk between channels. It is measured by applying a full-scale 20 kHz sine wave signal to one input channel and determining how much that signal is attenuated in each of the other channels. The figure given is the worst case across all four or eight channels of the AD7825 and AD7829, respectively.

Relative Accuracy or Endpoint Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
The difference between the measured and the ideal one LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the 128th code transition (01111111) to (10000000) from the ideal, that is, V_{MID}.

Offset Error Match
The difference in offset error between any two channels.

Zero-Scale Error
The deviation of the first code transition (00000000) to (00000001) from the ideal; that is, V_{MID} − 1.25 V + 1 LSB (V_{DD} = 5 V ± 10%), or V_{MID} − 1.0 V + 1 LSB (V_{DD} = 3 V ± 10%).

Full-Scale Error
The deviation of the last code transition (11111110) to (11111111) from the ideal; that is, V_{MID} + 1.25 V − 1 LSB (V_{DD} = 5 V ± 10%), or V_{MID} + 1.0 V − 1 LSB (V_{DD} = 3 V ± 10%).

Gain Error
The deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal, that is, V_{REF} − 1 LSB, after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

Track-and-Hold Acquisition Time
The time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the point at which the track-and-hold returns to track mode. This happens approximately 120 ns after the falling edge of $\overline{\text{CONVST}}$.

It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7822/AD7825/AD7829. It means that the user must wait for the duration of the track-and-hold acquisition time after a channel change/step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

PSR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the converter linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

CIRCUIT INFORMATION

CIRCUIT DESCRIPTION

The AD7822/AD7825/AD7829 consist of a track-and-hold amplifier followed by a half-flash analog-to-digital converter. These devices use a half-flash conversion technique where one 4-bit flash ADC is used to achieve an 8-bit result. The 4-bit flash ADC contains a sampling capacitor followed by 15 comparators that compare the unknown input to a reference ladder to achieve a 4-bit result. This first flash (that is, coarse conversion) provides the four MSBs. For a full 8-bit reading to be realized, a second flash (that is, fine conversion) must be performed to provide the four LSBs. The 8-bit word is then placed on the data output bus.

Figure 6 and Figure 7 show simplified schematics of the ADC. When the ADC starts a conversion, the track-and-hold goes into hold mode and holds the analog input for 120 ns. This is the acquisition phase, as shown in Figure 6, when Switch 2 is in Position A. At the point when the track-and-hold returns to its track mode, this signal is sampled by the sampling capacitor, as Switch 2 moves into Position B. The first flash occurs at this instant and is then followed by the second flash. Typically, the first flash is complete after 100 ns, that is, at 220 ns; and the end of the second flash and, hence, the 8-bit conversion result is available at 330 ns (minimum). The maximum conversion time is 420 ns. As shown in Figure 8, the track-and-hold returns to track mode after 120 ns and starts the next acquisition before the end of the current conversion. Figure 10 shows the ADC transfer function.

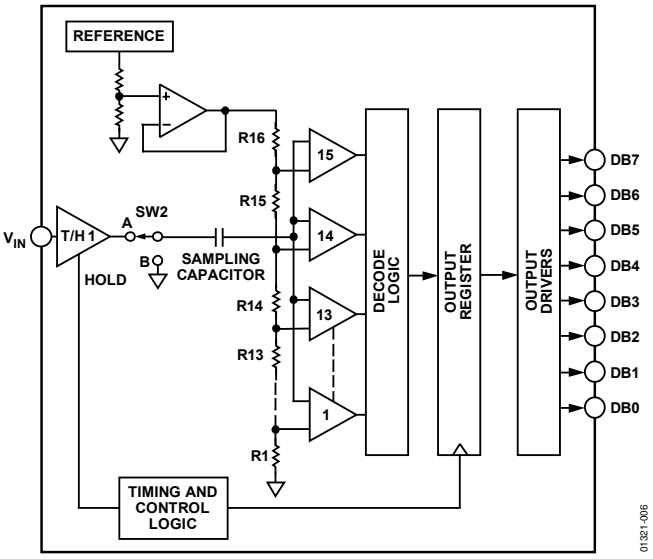


Figure 6. ADC Acquisition Phase

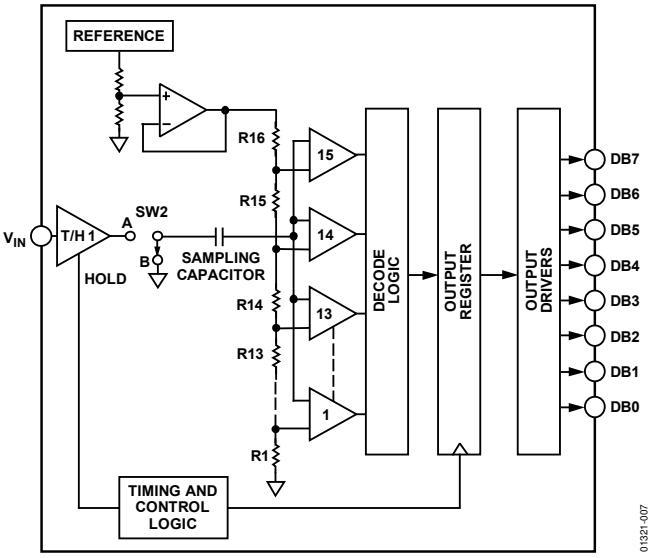


Figure 7. ADC Conversion Phase

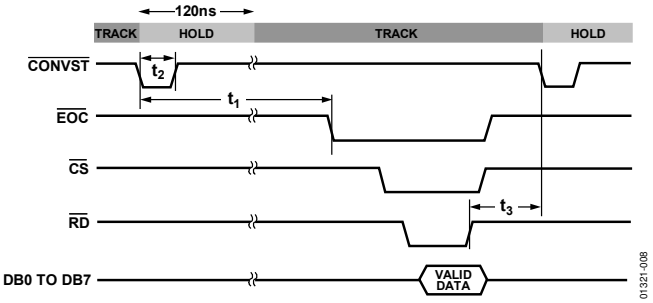
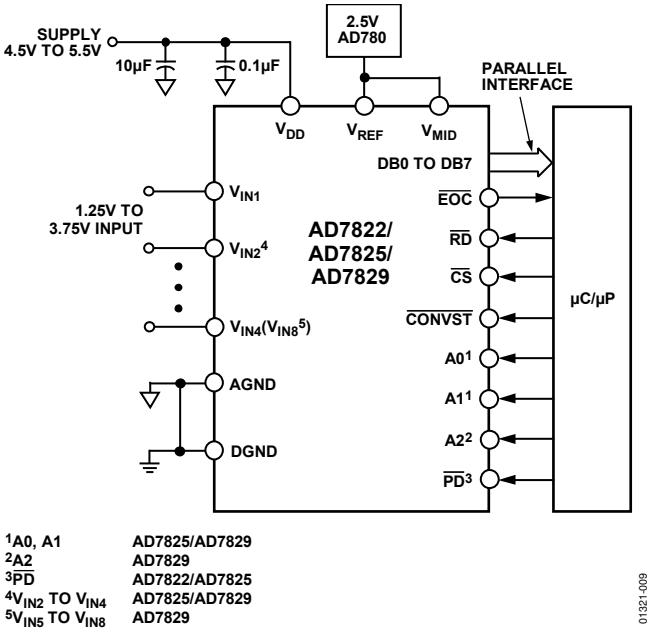


Figure 8. Track-and-Hold Timing

TYPICAL CONNECTION DIAGRAM

Figure 9 shows a typical connection diagram for the AD7822/AD7825/AD7829. The AGND and DGND are connected together at the device for good noise suppression. The parallel interface is implemented using an 8-bit data bus. The end of conversion signal ($\overline{EOC}$) idles high, the falling edge of $\overline{CONVST}$ initiates a conversion, and at the end of conversion the falling edge of $\overline{EOC}$ is used to initiate an interrupt service routine (ISR) on a microprocessor (see the Parallel Interface section for more details.) V_{REF} and V_{MID} are connected to a voltage source such as the AD780, and V_{DD} is connected to a voltage source that can vary from 4.5 V to 5.5 V (see Table 5 in the Analog Input section). When V_{DD} is first connected, the AD7822/AD7825/AD7829 power up in a low current mode, that is, power-down mode, with the default logic level on the $\overline{EOC}$ pin on the AD7822 and AD7825 equal to a low. Ensure the $\overline{CONVST}$ line is not floating when V_{DD} is applied, because this can put the AD7822/AD7825/AD7829 into an unknown state.

A suggestion is to tie $\overline{\text{CONVST}}$ to V_{DD} or DGND through a pull-up or pull-down resistor. A rising edge on the $\overline{\text{CONVST}}$ pin causes the AD7829 to fully power up, while a rising edge on the $\overline{\text{PD}}$ pin causes the AD7822 and AD7825 to fully power up. For applications where power consumption is of concern, the automatic power-down at the end of a conversion should be used to improve power performance (see the Power vs. Throughput section).



[1]A0, A1 AD7825/AD7829
[2]A2 AD7829
[3]$\overline{\text{PD}}$ AD7822/AD7825
[4]V_{IN2} TO V_{IN4} AD7825/AD7829
[5]V_{IN5} TO V_{IN8} AD7829

Figure 9. Typical Connection Diagram

ADC TRANSFER FUNCTION

The output coding of the AD7822/AD7825/AD7829 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size = $V_{REF}/256$ (V_{DD} = 5 V) or the LSB size = (0.8 V_{REF})/256 (V_{DD} = 3 V). The ideal transfer characteristic for the AD7822/AD7825/AD7829 is shown in Figure 10.

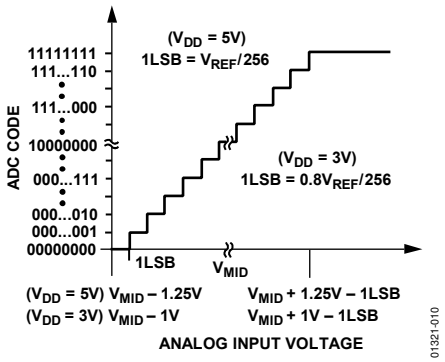


Figure 10. Transfer Characteristic

ANALOG INPUT

The AD7822 has a single input channel, and the AD7825 and AD7829 have four and eight input channels, respectively. Each input channel has an input span of 2.5 V or 2.0 V, depending on the supply voltage (V_{DD}). This input span is automatically set up by an on-chip V_{DD} detector circuit. A 5 V operation of the ADCs is detected when V_{DD} exceeds 4.1 V, and a 3 V operation is detected when V_{DD} falls below 3.8 V. This circuit also possesses a degree of glitch rejection; for example, a glitch from 5.5 V to 2.7 V up to 60 ns wide does not trip the V_{DD} detector.

The V_{MID} pin is used to center this input span anywhere in the range of AGND to V_{DD}. If no input voltage is applied to V_{MID}, the default input range is AGND to 2.0 V (V_{DD} = 3 V ± 10%), that is, centered about 1.0 V; or AGND to 2.5 V (V_{DD} = 5 V ± 10%), that is, centered about 1.25 V. When using the default input range, the V_{MID} pin can be left unconnected, or in some cases, it can be decoupled to AGND with a 0.1 µF capacitor.

If, however, an external V_{MID} is applied, the analog input range is from V_{MID} − 1.0 V to V_{MID} + 1.0 V (V_{DD} = 3 V ± 10%), or from V_{MID} − 1.25 V to V_{MID} + 1.25 V (V_{DD} = 5 V ± 10%).

The range of values of V_{MID} that can be applied depends on the value of V_{DD}. For V_{DD} = 3 V ± 10%, the range of values that can be applied to V_{MID} is from 1.0 V to V_{DD} − 1.0 V and from 1.25 V to V_{DD} − 1.25 V when V_{DD} = 5 V ± 10%. Table 5 shows the relevant ranges of V_{MID} and the input span for various values of V_{DD}. Figure 11 illustrates the input signal range available with various values of V_{MID}.

Table 5.

V_{DD}	V_{MID} Internal	V_{MID} Ext Max	V_{IN} Span	V_{MID} Ext Min	V_{IN} Span	Unit
5.5	1.25	4.25	3.0 to 5.5	1.25	0 to 2.5	V
5.0	1.25	3.75	2.5 to 5.0	1.25	0 to 2.5	V
4.5	1.25	3.25	2.0 to 4.5	1.25	0 to 2.5	V
3.3	1.00	2.3	1.3 to 3.3	1.00	0 to 2.0	V
3.0	1.00	2.0	1.0 to 3.0	1.00	0 to 2.0	V
2.7	1.00	1.7	0.7 to 2.7	1.00	0 to 2.0	V

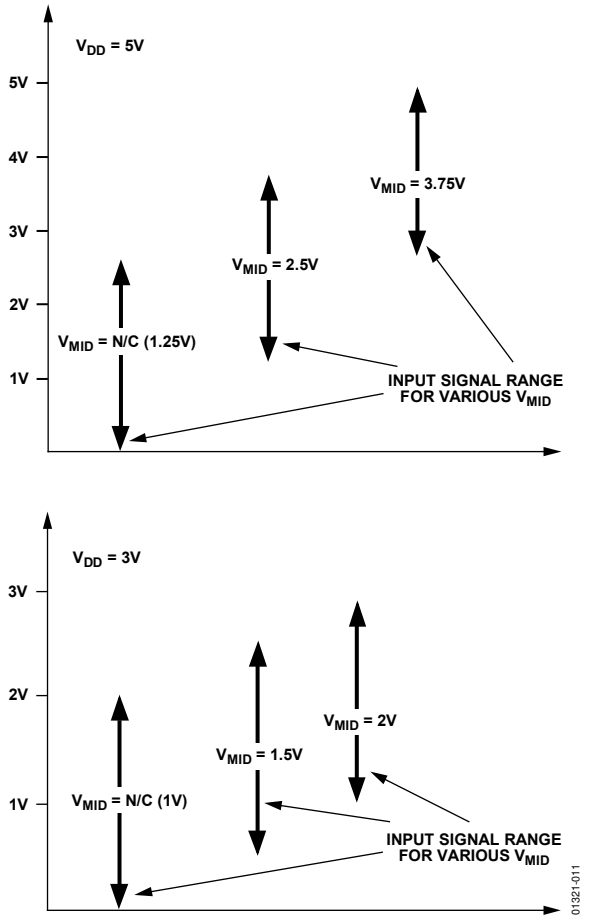


Figure 11. Analog Input Span Variation with V_{MID}

V_{MID} can be used to remove offsets in a system by applying the offset to the V_{MID} pin as shown in Figure 12, or it can be used to accommodate bipolar signals by applying V_{MID} to a level-shifting circuit before V_{IN}, as shown in Figure 13. When V_{MID} is being driven by an external source, the source can be directly tied to the level-shifting circuitry (see Figure 13). However, if the internal V_{MID}, that is, the default value, is being used as an output, it must be buffered before applying it to the level-shifting circuitry because the V_{MID} pin has an impedance of approximately 6 kΩ (see Figure 14).

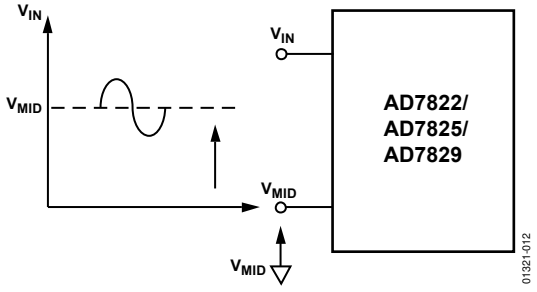


Figure 12. Removing Offsets Using V_{MID}

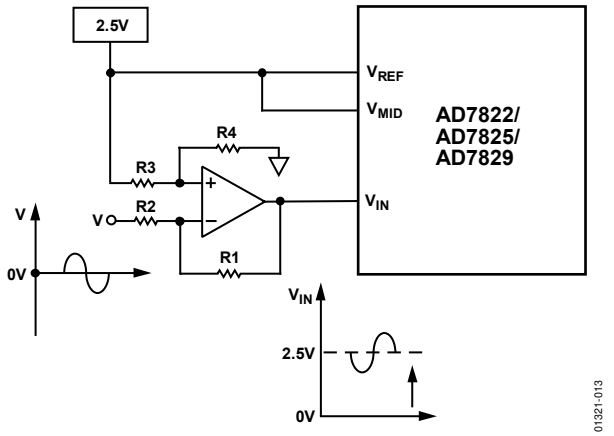


Figure 13. Accommodating Bipolar Signals Using External V_{MID}

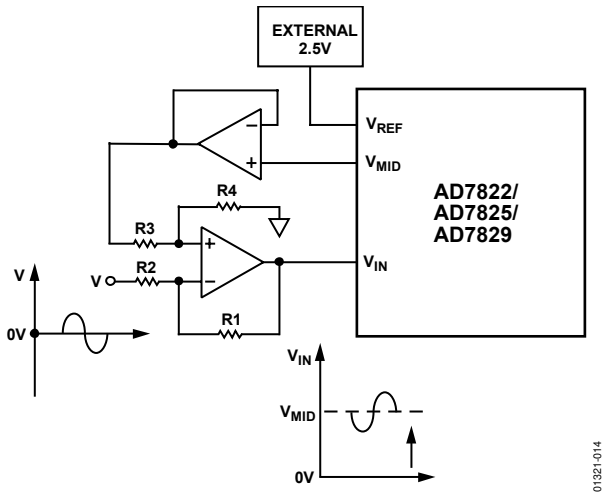


Figure 14. Accommodating Bipolar Signals Using Internal V_{MID}

NOTE: Although there is a V_{REF} pin from which a voltage reference of 2.5 V can be sourced, or to which an external reference can be applied, this does not provide an option of varying the value of the voltage reference. As stated in the specifications for the AD7822/AD7825/AD7829, the input voltage range at this pin is 2.5 V ± 2%.

Analog Input Structure

Figure 15 shows an equivalent circuit of the analog input structure of the AD7822/AD7825/AD7829. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. Doing so causes these diodes to become forward biased and start conducting current into the substrate. A maximum current of 20 mA can be conducted by these diodes without causing irreversible damage to the part. However, it is worth noting that a small amount of current (1 mA) being conducted into the substrate, due to an overvoltage on an unselected channel, can cause inaccurate conversions on a selected channel.

Capacitor C2 in Figure 15 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor, R1, is a lumped component made up of the on resistance of several components, including that of the multiplexer and the track-and-hold. This resistor is typically about 310 Ω. Capacitor C1 is the track-and-hold capacitor and has a capacitance of 0.5 pF. Switch 1 is the track-and-hold switch, and Switch 2 is that of the sampling capacitor, as shown in Figure 6 and Figure 7.

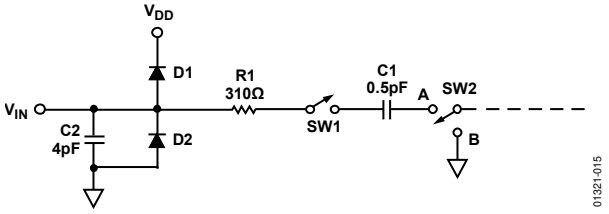


Figure 15. Equivalent Analog Input Circuit

When in track phase, Switch 1 is closed and Switch 2 is in Position A. When in hold mode, Switch 1 opens and Switch 2 remains in Position A. The track-and-hold remains in hold mode for 120 ns (see the Circuit Description section), after which it returns to track mode and the ADC enters its conversion phase. At this point, Switch 1 opens and Switch 2 moves to Position B. At the end of the conversion, Switch 2 moves back to Position A.

Analog Input Selection

On power-up, the default V_{IN} selection is V_{IN1}. When returning to normal operation from power-down, the V_{IN} selected is the same one that was selected prior to initiation of power-down. Table 6 shows the multiplexer address corresponding to each analog input from V_{IN1} to $V_{IN4(8)}$ for the AD7825 or AD7829.

Table 6.

A2	A1	A0	Analog Input Selected
0	0	0	V_{IN1}
0	0	1	V_{IN2}
0	1	0	V_{IN3}
0	1	1	V_{IN4}
1	0	0	V_{IN5}
1	0	1	V_{IN6}
1	1	0	V_{IN7}
1	1	1	V_{IN8}

Channel selection on the AD7825 and AD7829 is made without the necessity of a write operation. The address of the next channel to be converted is latched at the start of the current read operation, that is, on the falling edge of $\overline{RD}$ while $\overline{CS}$ is low, as shown in Figure 16. This allows for improved throughput rates in "channel hopping" applications.

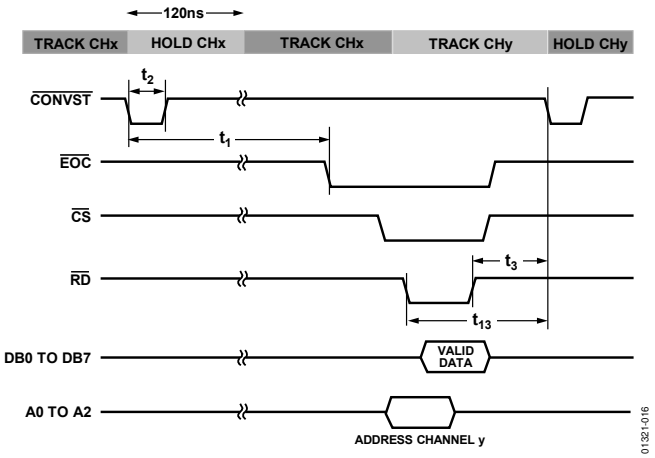


Figure 16. Channel Hopping Timing

There is a minimum time delay between the falling edge of $\overline{RD}$ and the next falling edge of the $\overline{CONVST}$ signal, t_{13}. This is the minimum acquisition time required of the track-and-hold to maintain 8-bit performance. Figure 17 shows the typical performance of the AD7825 when channel hopping for various acquisition times. These results are obtained using an external reference and internal V_{MID} while channel hopping between V_{IN1} and V_{IN4} with 0 V on Channel 4 and 0.5 V on Channel 1.

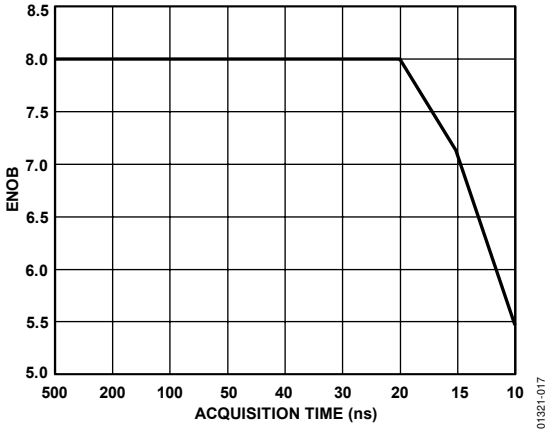


Figure 17. Effective Number of Bits vs. Acquisition Time for the AD7825

The on-chip track-and-hold can accommodate input frequencies to 10 MHz, making the AD7822/AD7825/AD7829 ideal for subsampling applications. When the AD7825 is converting a 10 MHz input signal at a sampling rate of 2 MSPS, the effective number of bits typically remains above seven, corresponding to a signal-to-noise ratio of 42 dBs, as shown in Figure 18.

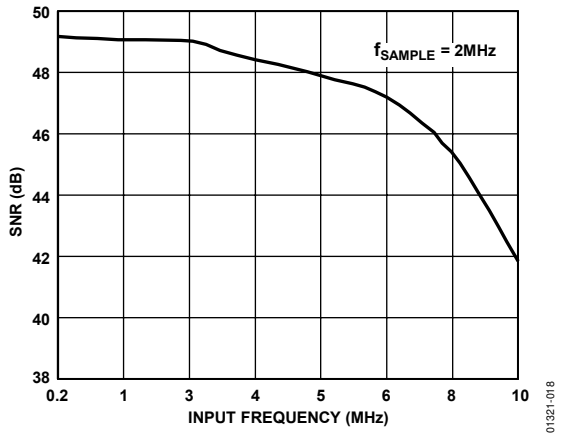


Figure 18. SNR vs. Input Frequency on the AD7825

POWER-UP TIMES

The AD7822/AD7825/AD7829 have a 1 µs power-up time when using an external reference and a 25 µs power-up time when using the on-chip reference. When V_{DD} is first connected, the AD7822/AD7825/AD7829 are in a low current mode of operation. Ensure that the $\overline{CONVST}$ line is not floating when V_{DD} is applied. If there is a glitch on $\overline{CONVST}$ while V_{DD} is rising, the part attempts to power up before V_{DD} has fully settled and can enter an unknown state. To carry out a conversion, the AD7822/AD7825/AD7829 must first be powered up. The AD7829 is powered up by a rising edge on the $\overline{CONVST}$ pin, and a conversion is initiated on the falling edge of $\overline{CONVST}$. Figure 19 shows how to power up the AD7829 when V_{DD} is first connected or after the AD7829 has been powered down using the $\overline{CONVST}$ pin when using either the on-chip reference or an external reference. When using an external reference, the falling edge of $\overline{CONVST}$ may occur before the required power-up time has elapsed; however, the conversion is not initiated on the falling edge of $\overline{CONVST}$ but rather at the moment when the part has completely powered up, that is, after 1 µs. If the falling edge of $\overline{CONVST}$ occurs after the required power-up time has elapsed, then it is upon this falling edge that a conversion is initiated. When using the on-chip reference, it is necessary to wait the required power-up time of approximately 25 µs before initiating a conversion; that is, a falling edge on $\overline{CONVST}$ must not occur before the required power-up time has elapsed, when V_{DD} is first connected or after the AD7829 has been powered down using the $\overline{CONVST}$ pin, as shown in Figure 19.

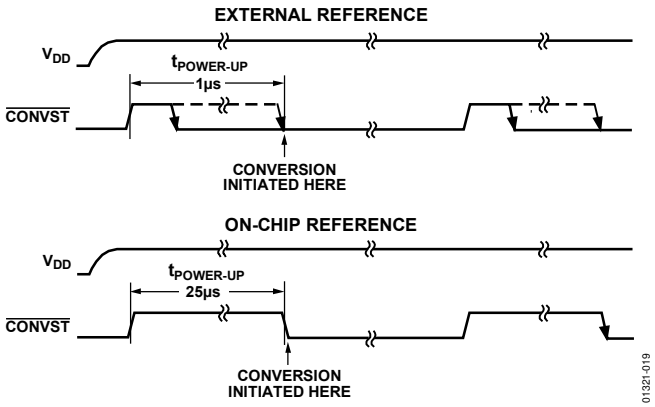


Figure 19. AD7829 Power-Up Time

Figure 20 shows how to power up the AD7822 or AD7825 when V_{DD} is first connected or after the ADCs have been powered down, using the $\overline{PD}$ pin or the $\overline{CONVST}$ pin, with either the on-chip reference or an external reference. When the supplies are first connected or after the part has been powered down by the $\overline{PD}$ pin, only a rising edge on the $\overline{PD}$ pin causes the part to power up. When the part has been powered down using the $\overline{CONVST}$ pin, a rising edge on either the $\overline{PD}$ pin or the $\overline{CONVST}$ pin powers the part up again.

As with the AD7829, when using an external reference with the AD7822 or AD7825, the falling edge of $\overline{CONVST}$ may occur before the required power-up time has elapsed. If this is the case, the conversion is not initiated on the falling edge of $\overline{CONVST}$, but rather at the moment when the part has powered up completely, that is, after 1 µs. If the falling edge of $\overline{CONVST}$ occurs after the required power-up time has elapsed, it is upon this falling edge that a conversion is initiated. When using the on-chip reference, it is necessary to wait the required power-up time of approximately 25 µs before initiating a conversion; that is, a falling edge on $\overline{CONVST}$ must not occur before the required power-up time has elapsed, when supplies are first connected to the AD7822 or AD7825, or when the ADCs have been powered down using the $\overline{PD}$ pin or the $\overline{CONVST}$ pin, as shown in Figure 20.

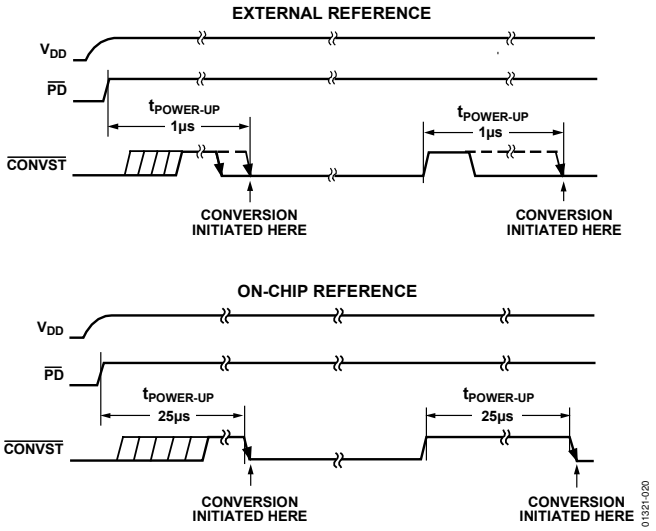


Figure 20. AD7822/AD7825 Power-Up Time

POWER VS. THROUGHPUT

Superior power performance can be achieved by using the automatic power-down (Mode 2) at the end of a conversion (see the Operating Modes section).

Figure 21 shows how the automatic power-down is implemented using the $\overline{\text{CONVST}}$ signal to achieve the optimum power performance for the AD7822/AD7825/AD7829. The duration of the $\overline{\text{CONVST}}$ pulse is set to be equal to or less than the power-up time of the devices (see the Operating Modes section). As the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

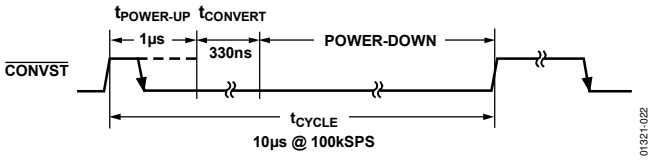


Figure 21. Automatic Power-Down

For example, if the AD7822 is operated in a continuous sampling mode, with a throughput rate of 100 kSPS and using an external reference, the power consumption is calculated as follows. The power dissipation during normal operation is 36 mW, V_{DD} = 3 V. If the power-up time is 1 µs and the conversion time is 330 ns (@ +25°C), the AD7822 can be said to dissipate 36 mW (maximum) for 1.33 µs during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (1.33/10) × (36 mW) = 4.79 mW. This calculation uses the minimum conversion time, thus giving the best-case power dissipation at this throughput rate. However, the actual power dissipated during each conversion cycle could increase, depending on the actual conversion time (up to a maximum of 420 ns).

Figure 22 shows the power vs. throughput rate for automatic full power-down.

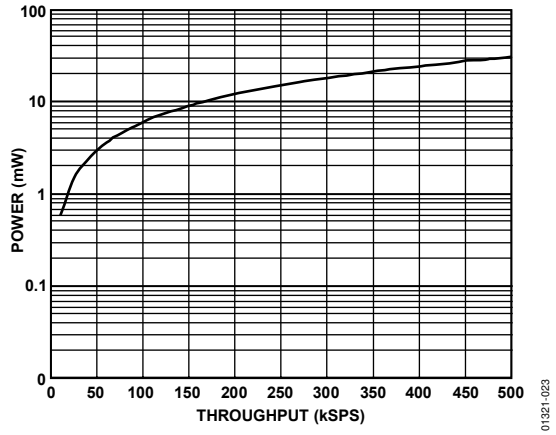


Figure 22. AD7822/AD7825/AD7829 Power vs. Throughput

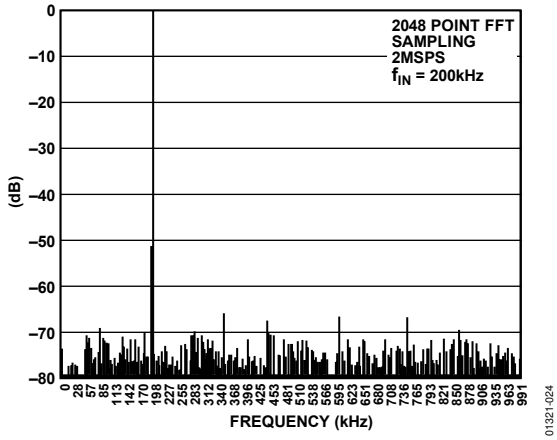


Figure 23. AD7822/AD7825/AD7829 SNR

OPERATING MODES

The AD7822/AD7825/AD7829 have two possible modes of operation, depending on the state of the $\overline{\text{CONVST}}$ pulse approximately 100 ns after the end of a conversion, that is, upon the rising edge of the $\overline{\text{EOC}}$ pulse.

Mode 1 Operation (High Speed Sampling)

When the AD7822/AD7825/AD7829 are operated in Mode 1, they are not powered down between conversions. This mode of operation allows high throughput rates to be achieved.

Figure 24 shows how this optimum throughput rate is achieved by bringing $\overline{\text{CONVST}}$ high before the end of a conversion, that is, before the $\overline{\text{EOC}}$ pulses low. When operating in this mode, a new conversion should not be initiated until 30 ns after the end of a read operation. This allows the track-and-hold to acquire the analog signal to 0.5 LSB accuracy.

Mode 2 Operation (Automatic Power-Down)

When the AD7822/AD7825/AD7829 are operated in Mode 2 (see Figure 25), they automatically power down at the end of a conversion. The $\overline{\text{CONVST}}$ signal is brought low to initiate a conversion and is left logic low until after the $\overline{\text{EOC}}$ goes high, that is, approximately 100 ns after the end of the conversion. The state of the $\overline{\text{CONVST}}$ signal is sampled at this point (that is, 530 ns maximum after $\overline{\text{CONVST}}$ falling edge), and the AD7822/AD7825/AD7829 power down as long as $\overline{\text{CONVST}}$ is low.

The ADC is powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. Superior power performance can be achieved in this mode of operation by powering up the AD7822/AD7825/AD7829 only to carry out a conversion. The parallel interface of the AD7822/AD7825/AD7829 remains fully operational while the ADCs are powered down. A read may occur while the part is powered down, and, therefore, it does not necessarily need to be placed within the $\overline{\text{EOC}}$ pulse, as shown in Figure 25.

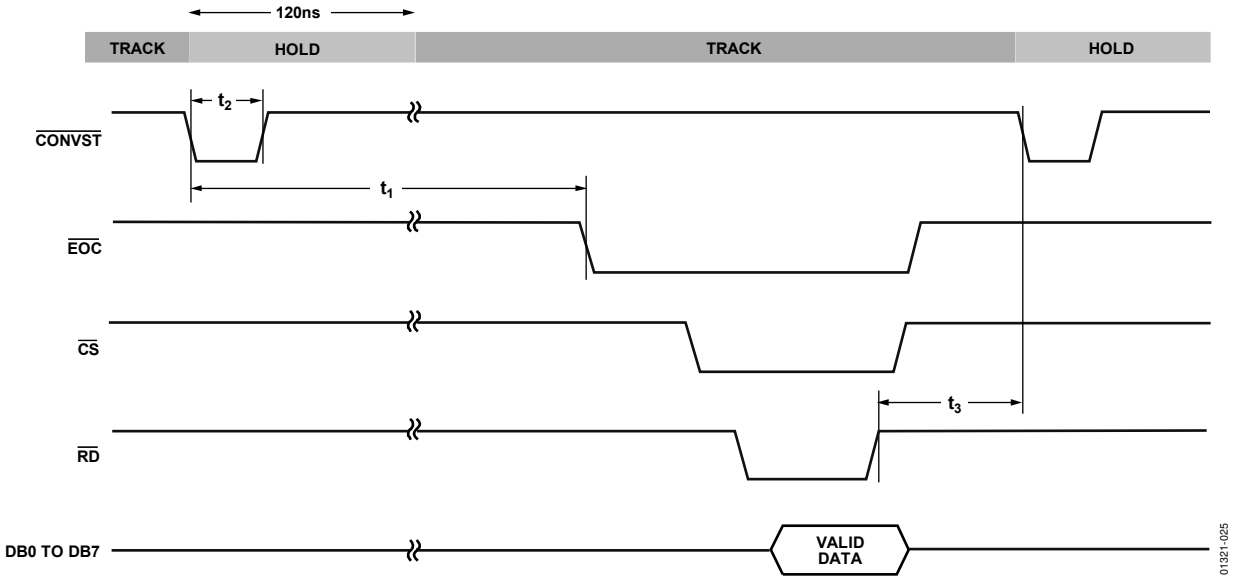


Figure 24. Mode 1 Operation

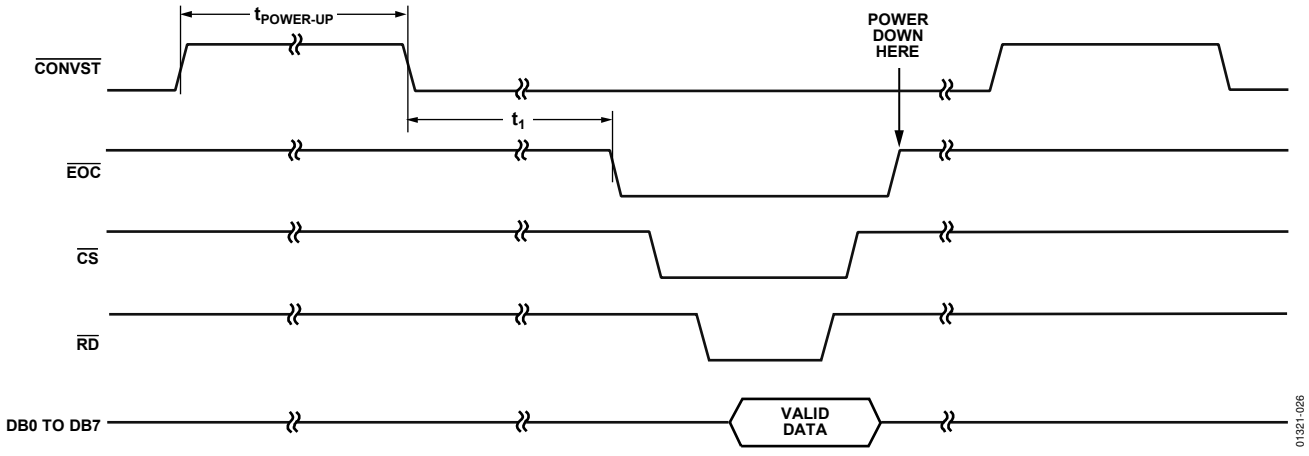


Figure 25. Mode 2 Operation

PARALLEL INTERFACE

The parallel interface of the AD7822/AD7825/AD7829 is eight bits wide. Figure 26 shows a timing diagram illustrating the operational sequence of the AD7822/AD7825/AD7829 parallel interface. The multiplexer address is latched into the AD7822/AD7825/AD7829 on the falling edge of the $\overline{RD}$ input. The on-chip track-and-hold goes into hold mode on the falling edge of $\overline{CONVST}$, and a conversion is also initiated at this point. When the conversion is complete, the end of conversion line ($\overline{EOC}$) pulses low to indicate that new data is available in the output register of the AD7822/AD7825/AD7829. The $\overline{EOC}$ pulse stays logic low for a maximum time of 110 ns.

However, the $\overline{EOC}$ pulse can be reset high by a rising edge of $\overline{RD}$. This $\overline{EOC}$ line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{CS}$ and $\overline{RD}$ going low accesses the 8-bit conversion result. It is possible to tie $\overline{CS}$ permanently low and use only $\overline{RD}$ to access the data. In systems where the part is interfaced to a gate array or ASIC, this $\overline{EOC}$ pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7822/AD7825/AD7829 and into the gate array or ASIC. This means that the gate array or ASIC does not need any conversion status recognition logic, and it also eliminates the logic required in the gate array or ASIC to generate the read signal for the AD7822/AD7825/AD7829.

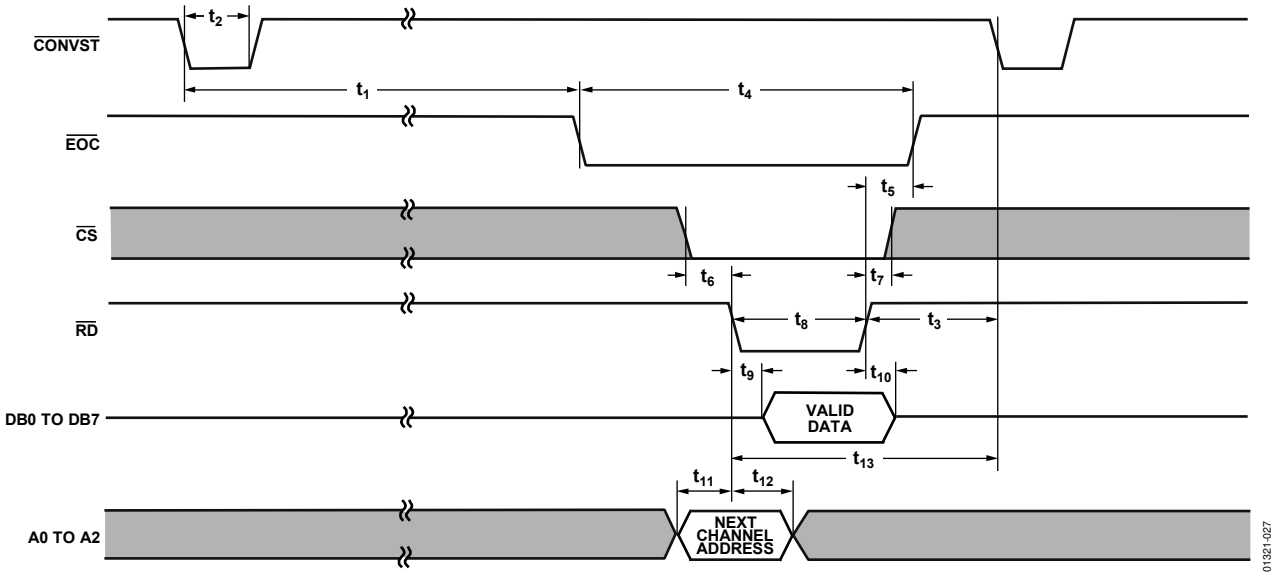


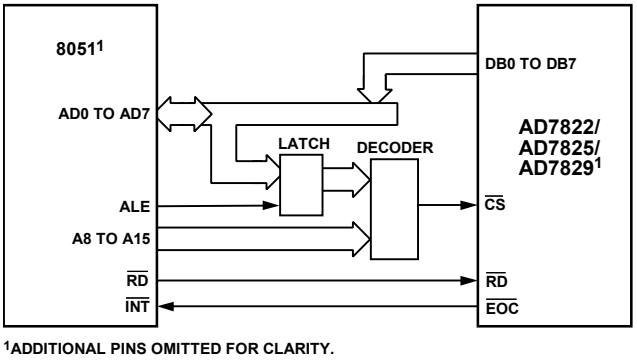
Figure 26. AD7822/AD7825/AD7829 Parallel Port Timing

MICROPROCESSOR INTERFACING

The parallel port on the AD7822/AD7825/AD7829 allows the ADCs to be interfaced to a range of many different microcontrollers. This section explains how to interface the AD7822/AD7825/AD7829 with some of the more common microcontroller parallel interface protocols.

AD7822/AD7825/AD7829 TO 8051

Figure 27 shows a parallel interface between the AD7822/AD7825/AD7829 and the 8051 microcontroller. The $\overline{EOC}$ signal on the AD7822/AD7825/AD7829 provides an interrupt request to the 8051 when a conversion ends and data is ready. Port 0 of the 8051 can serve as an input or output port; or, as in this case when used together with the address latch enable (ALE) of the 8051, can be used as a bidirectional low order address and data bus. The ALE output of the 8051 is used to latch the low byte of the address during accesses to the device, while the high order address byte is supplied from Port 2. Port 2 latches remain stable when the AD7822/AD7825/ AD7829 are addressed because they do not have to be turned around (set to 1) for data input, as is the case for Port 0.

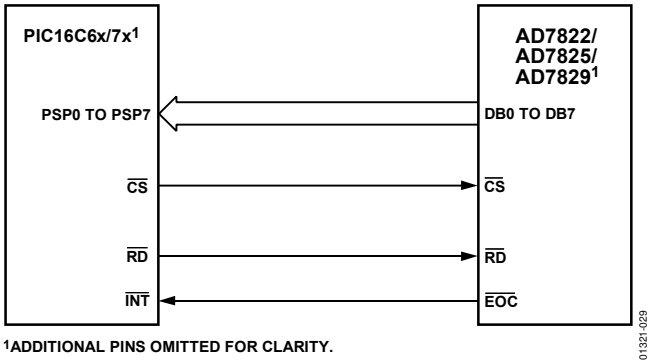


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 27. Interfacing to the 8051

AD7822/AD7825/AD7829 TO PIC16C6x/PIC16C7x

Figure 28 shows a parallel interface between the AD7822/AD7825/AD7829 and the PIC16C64/PIC16C65/PIC16C74. The $\overline{EOC}$ signal on the AD7822/AD7825/AD7829 provides an interrupt request to the microcontroller when a conversion begins. Of the PIC16C6x/PIC16C7x range of microcontrollers, only the PIC16C64/PIC16C65/PIC16C74 can provide the option of a parallel slave port. Port D of the microcontroller operates as an 8-bit wide parallel slave port when Control Bit PSPMODE in the TRISE register is set. Setting PSPMODE enables Port Pin RE0 to be the $\overline{RD}$ output and RE2 to be the $\overline{CS}$ (chip select) output. For this functionality, the corresponding data direction bits of the TRISE register must be configured as outputs (reset to 0). See the PIC16C6x/PIC16C7x microcontroller user manual.

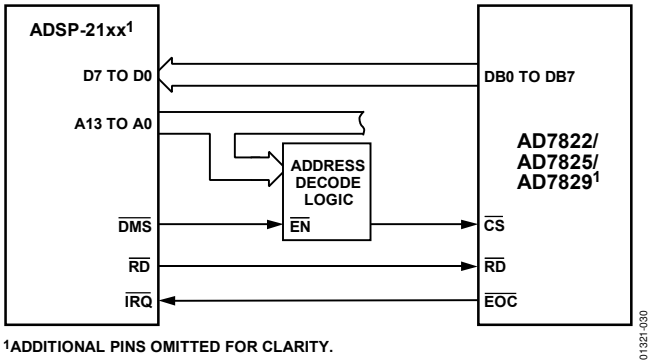


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 28. Interfacing to the PIC16C6x/ PIC16C7x

AD7822/AD7825/AD7829 TO ADSP-21xx

Figure 29 shows a parallel interface between the AD7822/AD7825/AD7829 and the ADSP-21xx series of DSPs. As before, the $\overline{EOC}$ signal on the AD7822/AD7825/AD7829 provides an interrupt request to the DSP when a conversion ends.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 29. Interfacing to the ADSP-21xx

INTERFACING MULTIPLEXER ADDRESS INPUTS

Figure 30 shows a simplified interfacing scheme between the AD7825/AD7829 and any microprocessor or microcontroller, which facilitates easy channel selection on the ADCs. The multiplexer address is latched on the falling edge of the $\overline{RD}$ signal, as outlined in the Parallel Interface section, allowing the use of the three LSBs of the address bus to select the channel address. As shown in Figure 30, only Address Bit A3 to Address Bit A15 are address decoded, allowing A0 to A2 to be changed according to desired channel selection without affecting chip selection.

AD7822 STANDALONE OPERATION

The AD7822, being the single channel device, does not have any multiplexer addressing associated with it and can be controlled with just one signal, that is, the $\overline{\text{CONVST}}$ signal. As shown in Figure 31, the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are both tied to the $\overline{\text{EOC}}$ pin.

The resulting signal can be used as an interrupt request signal (IRQ) on a DSP, as a $\overline{\text{WR}}$ signal to memory, or as a CLK to a latch or ASIC. The timing for this interface, as shown in Figure 31, demonstrates how, with the $\overline{\text{CONVST}}$ signal alone, a conversion can be initiated, data is latched out, and the operating mode of the AD7822 can be selected.

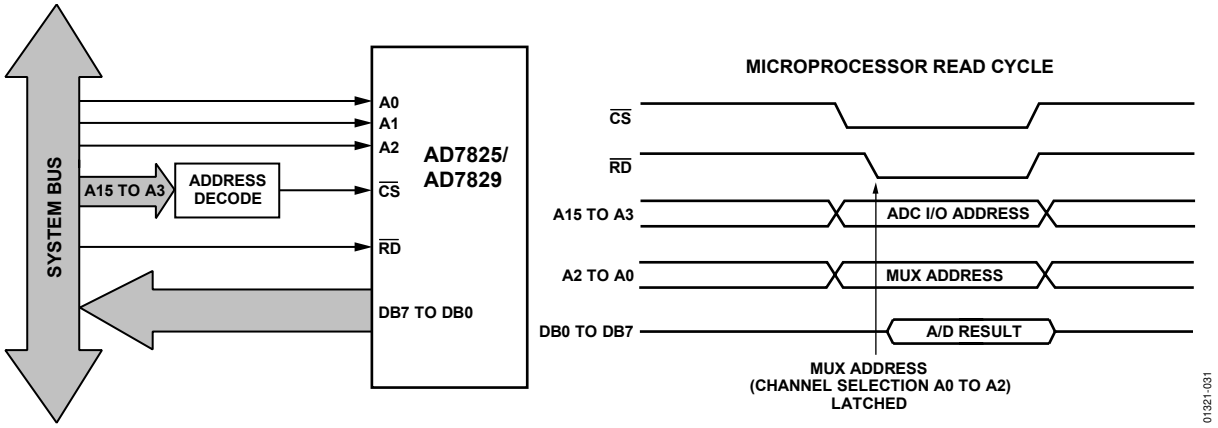


Figure 30. AD7825/AD7829 Simplified Microinterfacing Scheme

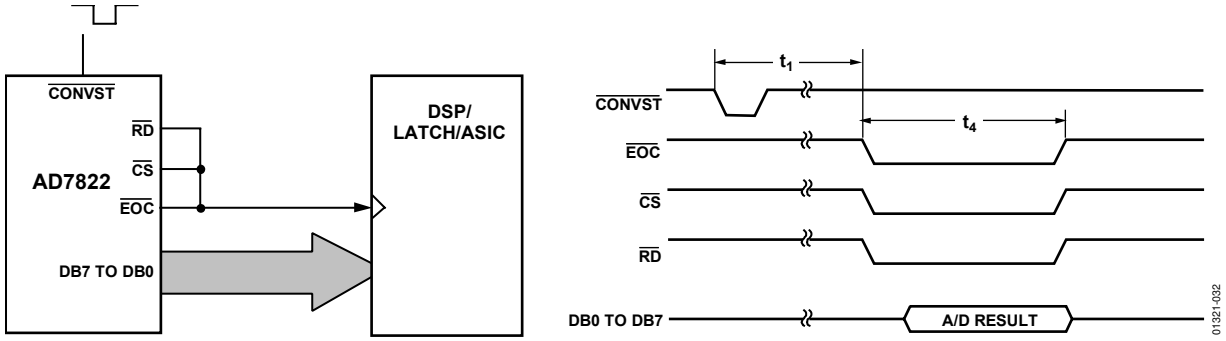
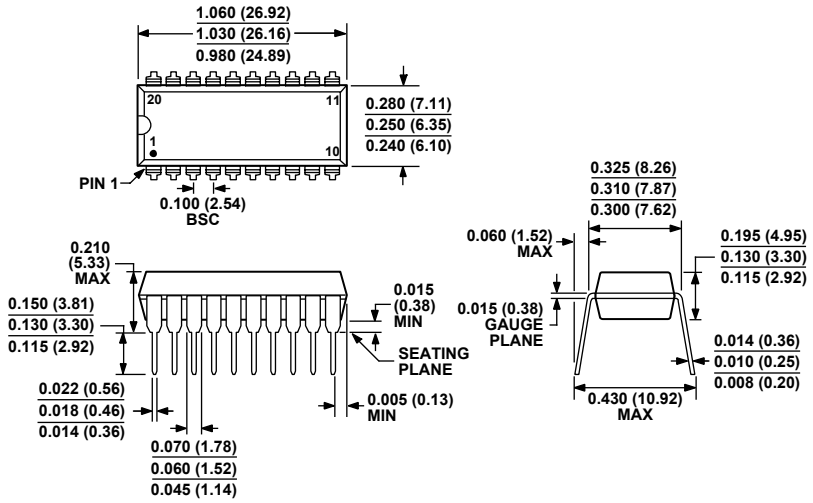


Figure 31. AD7822 Standalone Operation

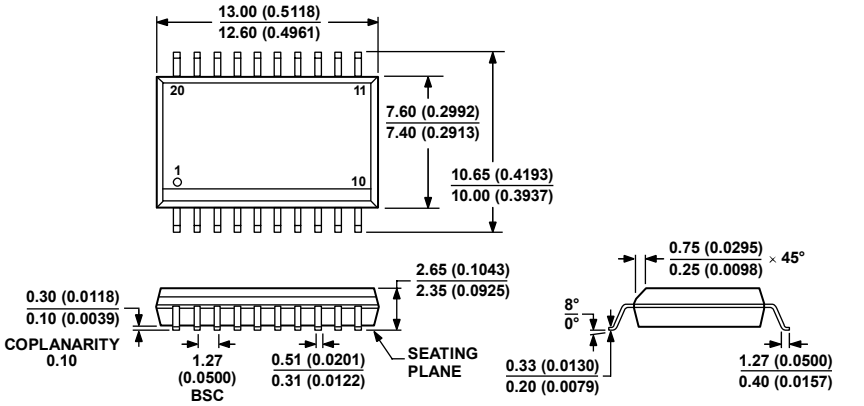
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AD

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 32. 20-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-20)
Dimensions shown in inches and (millimeters)

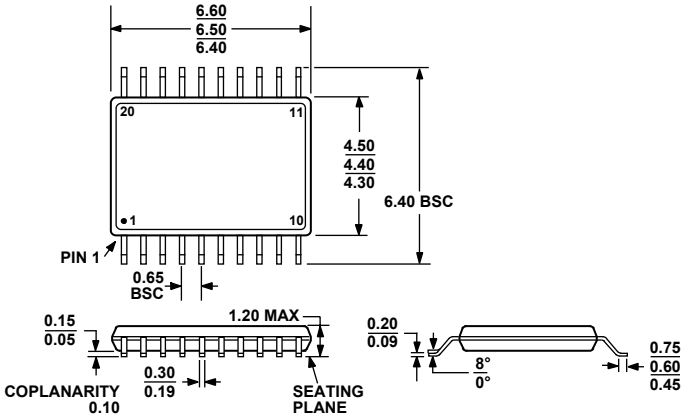


COMPLIANT TO JEDEC STANDARDS MS-013-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

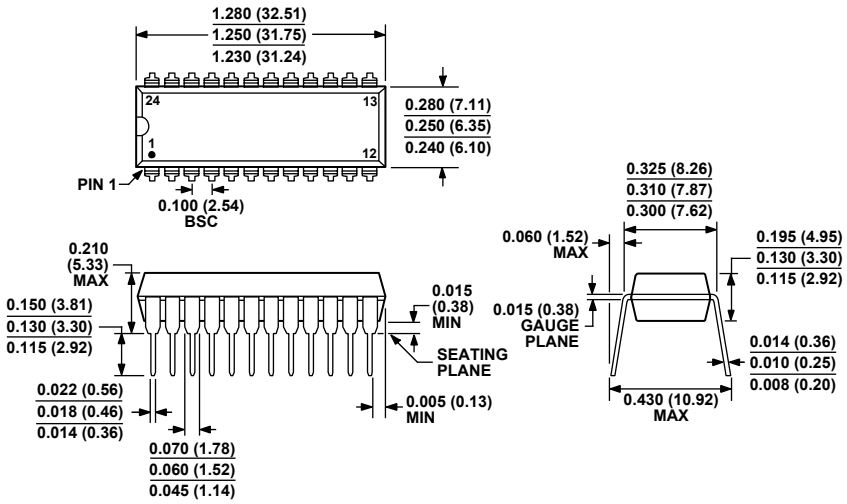
060706-A

Figure 33. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AC

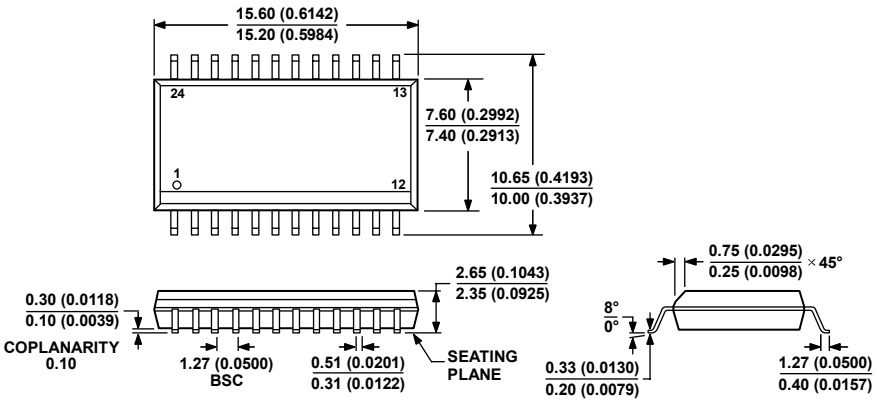
Figure 34. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-001-AF

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

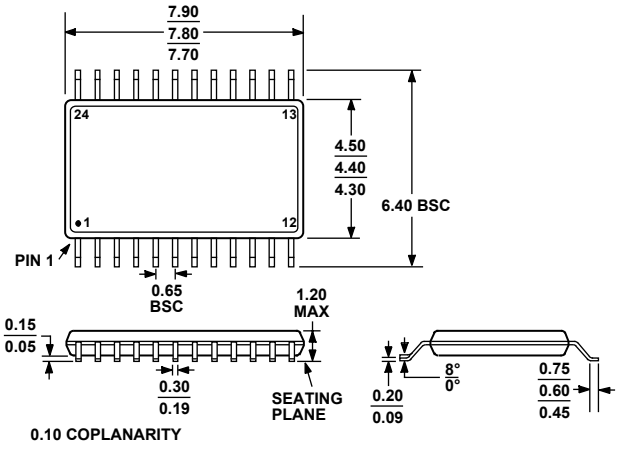
Figure 35. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

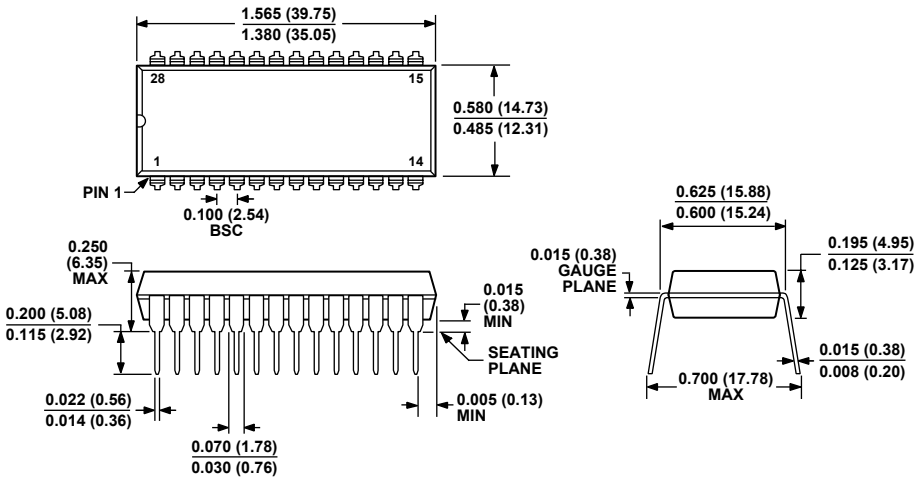
060706-A

Figure 36. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)



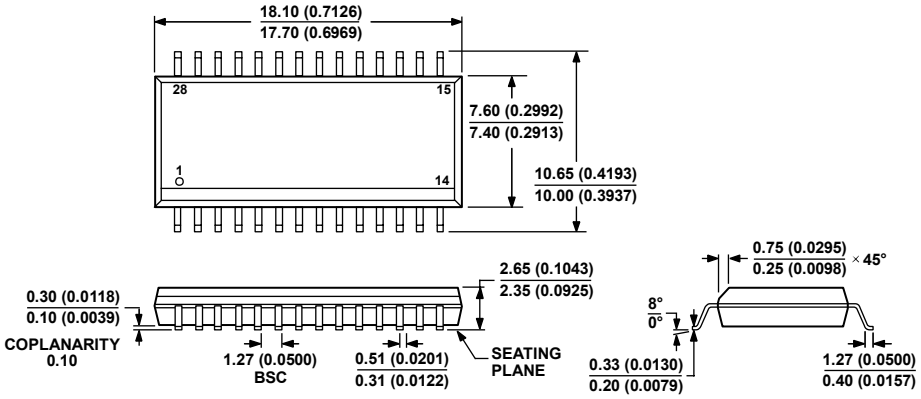
COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 37. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-011-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 38. 28-Lead Plastic Dual In-Line Package [PDIP]
Wide Body
(N-28-2)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 39. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

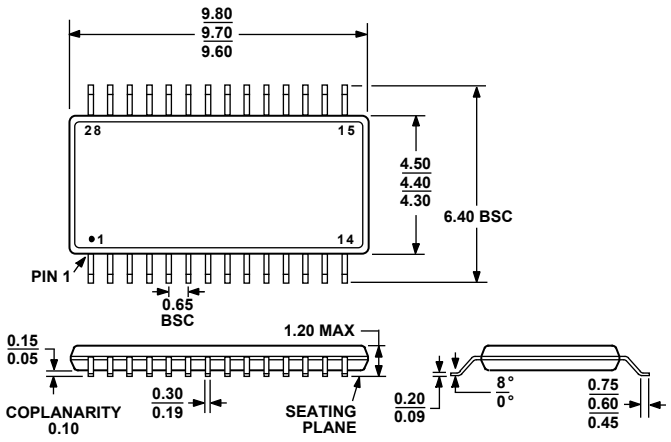


Figure 40. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Linearity Error
AD7822BN	−40°C to +85°C	20-Lead PDIP	N-20	±0.75 LSB
AD7822BNZ[1]	−40°C to +85°C	20-Lead PDIP	N-20	±0.75 LSB
AD7822BR	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BR-REEL	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BR-REEL7	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BRZ[1]	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BRZ-REEL[1]	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BRZ-REEL7[1]	−40°C to +85°C	20-Lead SOIC_W	RW-20	±0.75 LSB
AD7822BRU	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7822BRU-REEL	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7822BRU-REEL7	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7822BRUZ[1]	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7822BRUZ-REEL[1]	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7822BRUZ-REEL7[1]	−40°C to +85°C	20-Lead TSSOP	RU-20	±0.75 LSB
AD7825BN	−40°C to +85°C	24-Lead PDIP	N-24-1	±0.75 LSB
AD7825BNZ[1]	−40°C to +85°C	24-Lead PDIP	N-24-1	±0.75 LSB
AD7825BR	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BR-REEL	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BR-REEL7	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BRZ[1]	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BRZ-REEL[1]	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BRZ-REEL7[1]	−40°C to +85°C	24-Lead SOIC_W	RW-24	±0.75 LSB
AD7825BRU	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7825BRU-REEL	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7825BRU-REEL7	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7825BRUZ[1]	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7825BRUZ-REEL[1]	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7825BRUZ-REEL7[1]	−40°C to +85°C	24-Lead TSSOP	RU-24	±0.75 LSB
AD7829BN	−40°C to +85°C	28-Lead PDIP	N-28-2	±0.75 LSB
AD7829BNZ[1]	−40°C to +85°C	28-Lead PDIP	N-28-2	±0.75 LSB
AD7829BR	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BR-REEL	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BR-REEL7	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BRZ[1]	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BRZ-REEL[1]	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BRZ-REEL7[1]	−40°C to +85°C	28-Lead SOIC_W	RW-28	±0.75 LSB
AD7829BRU	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB
AD7829BRU-REEL	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB
AD7829BRU-REEL7	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB
AD7829BRUZ[1]	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB
AD7829BRUZ-REEL[1]	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB
AD7829BRUZ-REEL7[1]	−40°C to +85°C	28-Lead TSSOP	RU-28	±0.75 LSB

[1] Z = Pb-free part.

NOTES

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