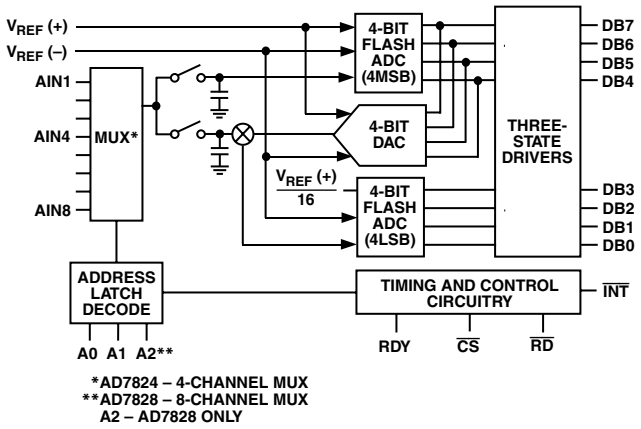
LC²MOS High Speed 4- and 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES
4 or 8 Analog Input Channels
Built-In Track-and-Hold Function
10 kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single 5 V Supply
Low Power: 50 mW
Fast Conversion Rate: 2.5 μs/Channel
Tight Error Specification: 1/2 LSB

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7824 and AD7828 are high speed, multichannel, 8-bit ADCs with a choice of four (AD7824) or eight (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5 μs per channel, and the parts have a built-in track-and-hold function capable of digitizing full-scale signals of 10 kHz (157 mV/μs slew rate) on all channels. The AD7824 and AD7828 operate from a single 5 V supply and have an analog input range of 0 V to 5 V, using an external 5 V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to initiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, linear compatible CMOS process (LC²MOS) and have low power dissipation of 40 mW (typ). The AD7824 is available in a 0.3" wide, 24-lead "skinny" DIP, while the AD7828 is available in a 0.6" wide, 28-lead DIP and in 28-terminal surface-mount packages.

PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost effective, space-saving multichannel ADC system.
2. Fast conversion rate of 2.5 μs/channel features a per-channel sampling frequency of 100 kHz for the AD7824 or 50 kHz for the AD7828.
3. Built-in track-and-hold function allows handling of four or eight channels up to 10 kHz bandwidth (157 mV/μs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single 5 V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

REV. F

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AD7824/AD7828–SPECIFICATIONS (V_{DD} = 5 V, V_{REF} (+) = 5 V, V_{REF} (–) = GND = 0 V, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Specifications apply to Mode 0.)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Unit	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which						
No Missing Codes Are Guaranteed	8	8	8	8	Bits	
Channel-to-Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF} (+) Input Voltage Range	V_{REF} (–)/ V_{DD}	V_{REF} (–)/ V_{DD}	V_{REF} (–)/ V_{DD}	V_{REF} (–)/ V_{DD}	V min/V max	
V_{REF} (–) Input Voltage Range	GND/ V_{REF} (+)	GND/ V_{REF} (+)	GND/ V_{REF} (+)	GND/ V_{REF} (+)	V min/V max	
ANALOG INPUT						
Input Voltage Range	V_{REF} (–)/ V_{REF} (+)	V_{REF} (–)/ V_{REF} (+)	V_{REF} (–)/ V_{REF} (+)	V_{REF} (–)/ V_{REF} (+)	V min/V max	
Input Leakage Current	±3	±3	±3	±3	µA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 V to 5 V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1, and A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	µA max	
I_{INL}	–1	–1	–1	–1	µA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS						
DB0–DB7 and $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360 µA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	µA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5 pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	±3	±3	µA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5 pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/µs typ	
	0.157	0.157	0.157	0.157	V/µs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	V	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4 V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16 LSB typ
						V_{DD} = 5 V ± 5%

NOTES

[1]Temperature ranges are as follows: K, L Versions: 0°C to 70°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C

[2]Total Unadjusted Error includes offset, full-scale and linearity errors.

[3]Sample tested at 25°C by Product Assurance to ensure compliance.

[4]RDY is an open-drain output.

[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

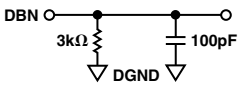
TIMING CHARACTERISTICS[1] (V_{DD} = 5 V; V_{REF}(+) = 5 V; V_{REF}(–) = GND = 0 V, unless otherwise noted.)

Parameter	Limit at 25°C (All Grades)	Limit at T_{MIN}, T_{MAX} (K, L, B, C Grades)	Limit at T_{MIN}, T_{MAX} (T, U Grades)	Unit	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}[2]	40	60	60	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5 kΩ.
t_{CRD}	2.0	2.4	2.8	μs max	Conversion Time, Mode 0
t_{ACC1}[3]	85	110	120	ns max	Data Access Time after $\overline{RD}$
t_{ACC2}[3]	50	60	70	ns max	Data Access Time after $\overline{INT}$, Mode 0
t_{INTH}[2]	40	65	70	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay
	75	100	100	ns max	
t_{DH}[4]	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulsewidth, Mode 1
	600	500	400	ns max	

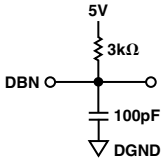
NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with t_{RISE} = t_{FALL} = 20 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]C_L = 50 pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

Test Circuits

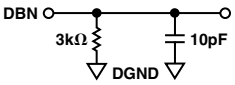


a. High-Z to V_{OH}

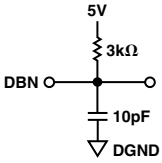


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C, unless otherwise noted.)

V_{DD} . . . . . 0 V, 7 V
Digital Input Voltage to GND
($\overline{RD}$, $\overline{CS}$, A0, A1, and A2) . . . . . –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
(DB0, DB7, RDY, and $\overline{INT}$) . . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} (+) to GND . . . . . V_{REF} (–), V_{DD} + 0.3 V
V_{REF} (–) to GND . . . . . 0 V, V_{REF} (+)
Analog Input (Any Channel) . . . . . –0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Commercial (K, L Versions) . . . . . 0°C to 70°C
Industrial (B, C Versions) . . . . . –40°C to +85°C
Extended (T, U Versions) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . 300°C
Power Dissipation (Any Package) to 75°C . . . . . 450 mW
Derates above 75°C by . . . . . 6 mW/°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

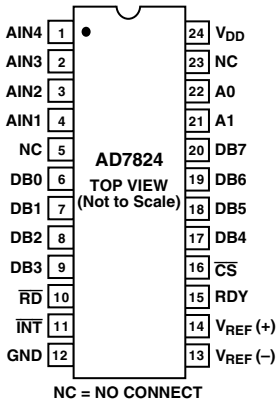
CAUTION

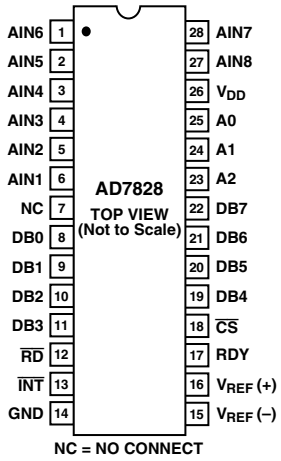
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although AD7824/AD7828 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



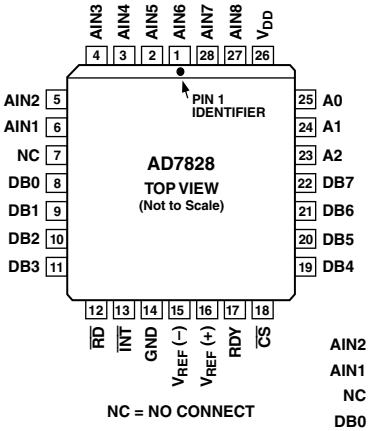
PIN CONFIGURATIONS

DIP/SOIC/SSOP

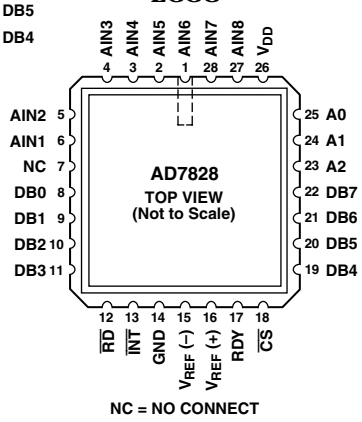




PLCC



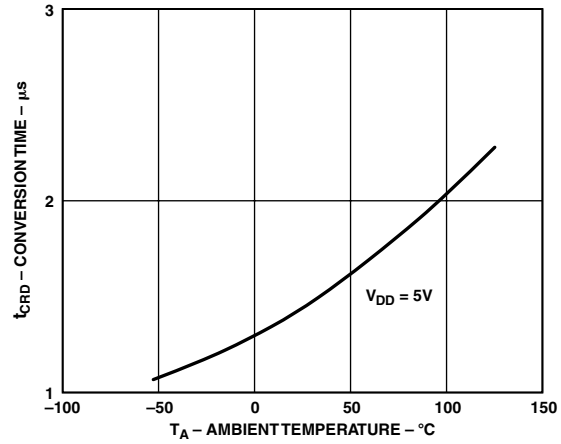
LCCC



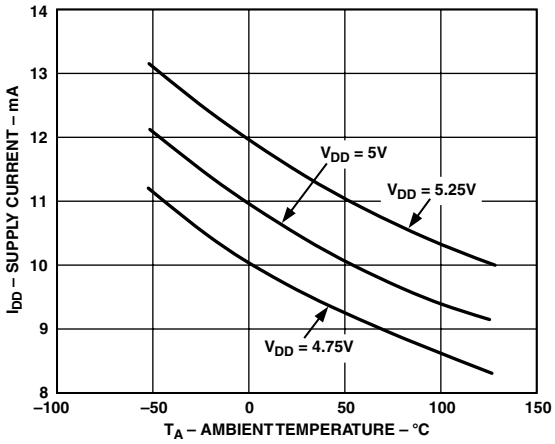
ORDERING GUIDE

Model	Temperature Range	Total Unadjusted Error (LSBs)	Package Option
AD7824KN	0°C to 70°C	±1	N-24
AD7824LN	0°C to 70°C	±1/2	N-24
AD7824KR	0°C to 70°C	±1	R-24
AD7824BQ	–40°C to +85°C	±1	Q-24
AD7824CQ	–40°C to +85°C	±1/2	Q-24
AD7824TQ*	–55°C to +125°C	±1	Q-24
AD7824UQ*	–55°C to +125°C	±1/2	Q-24
AD7828KN	0°C to 70°C	±1	N-28
AD7828LN	0°C to 70°C	±1/2	N-28
AD7828KP	0°C to 70°C	±1	P-28A
AD7828LP	0°C to 70°C	±1/2	P-28A
AD7828BQ	–40°C to +85°C	±1	Q-28
AD7828CQ	–40°C to +85°C	±1/2	Q-28
AD7828BR	–40°C to +85°C	+1	R-28
AD7828LRS	0°C to 70°C	±1/2	RS-28
AD7828TQ*	–55°C to +125°C	±1	Q-28
AD7828UQ*	–55°C to +125°C	±1/2	Q-28
AD7828TE*	–55°C to +125°C	±1	E-28A
AD7828UE*	–55°C to +125°C	±1/2	E-28A

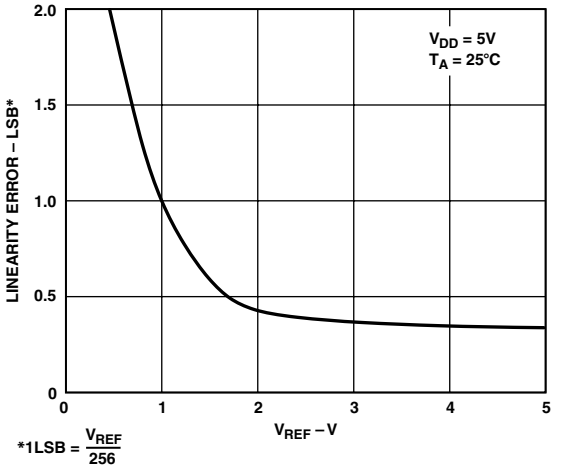
*Available to /883B processing only. Contact our local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5692-88764.



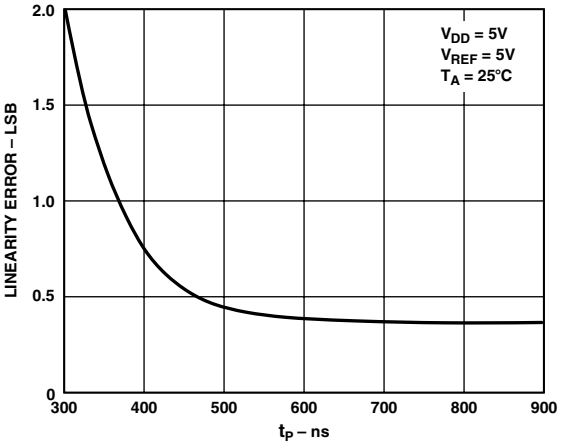
TPC 1. Conversion Time vs. Temperature



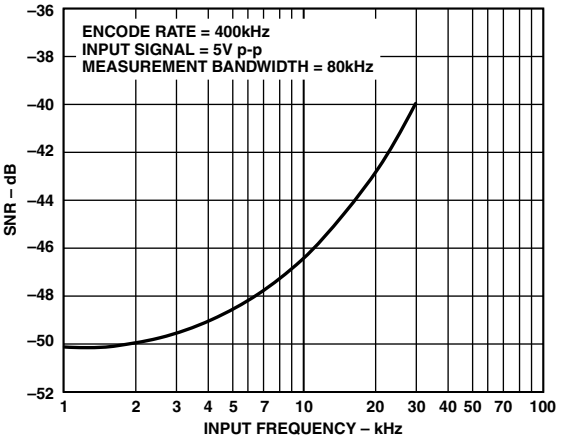
TPC 4. Power Supply Current vs. Temperature (Not Including Reference Ladder)



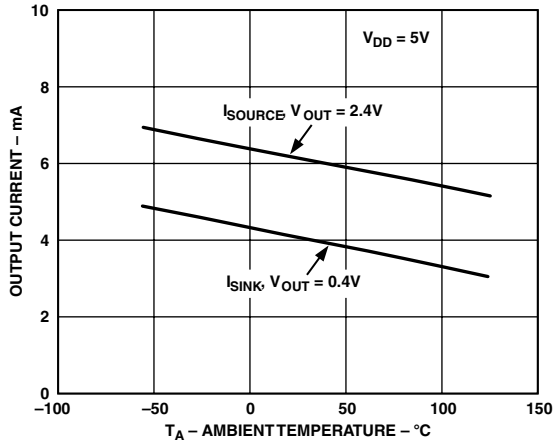
TPC 2. Accuracy vs. V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



TPC 5. Accuracy vs. t_P



TPC 3. Signal Noise Ratio vs. Input Frequency



TPC 6. Output Current vs. Temperature

OPERATIONAL DIAGRAM

The AD7824 is a 4-channel 8-bit ADC and the AD7828 is an 8-channel 8-bit ADC. Operational diagrams for both of these devices are shown in Figures 3 and 4. The addition of just a 5 V reference allows the devices to perform the analog-to-digital function.

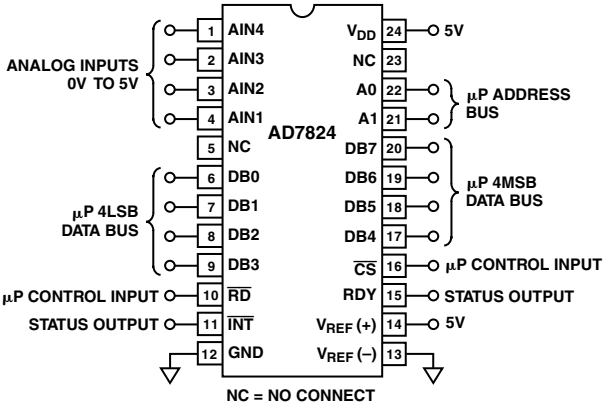


Figure 3. AD7824 Operational Diagram

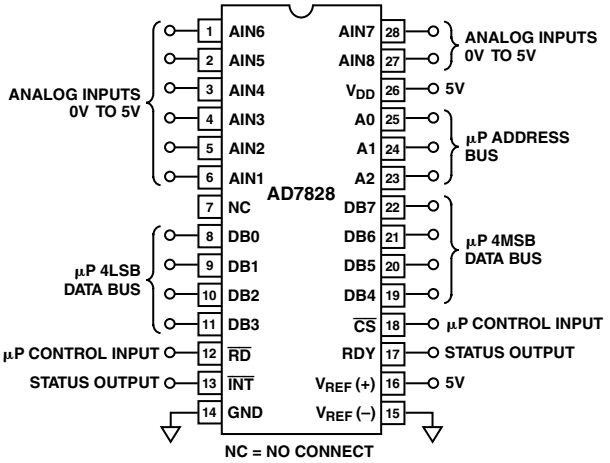


Figure 4. AD7828 Operational Diagram

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7824/AD7828 uses a half-flash conversion technique whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators that compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the four most significant data bits. An internal DAC, driven by the four MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the four least significant bits of the output data. The most significant flash ADC also has one additional comparator to detect overrange on the analog input.

APPLYING THE AD7824/AD7828

REFERENCE AND INPUT

The two reference inputs on the AD7824/AD7828 are fully differential and define the zero to full-scale input range of the ADC. As a result, the span of the analog input voltage for all channels can easily be varied. By reducing the reference span, V_{REF} (+) to V_{REF} (–), to less than 5 V, the sensitivity of the converter can be increased (e.g., if V_{REF} = 2 V then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input channel voltage span to be offset from zero. The voltage at V_{REF} (–) sets the input level for all channels, which produces a digital output of all zeroes. Therefore, although the analog inputs are not themselves differential, they have nearly differential input capability in most measurement applications because of the reference design. Figures 5 to 7 show some of the configurations that are possible.

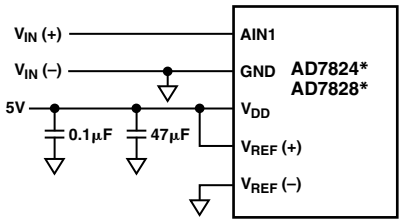


Figure 5. Power Supply as Reference

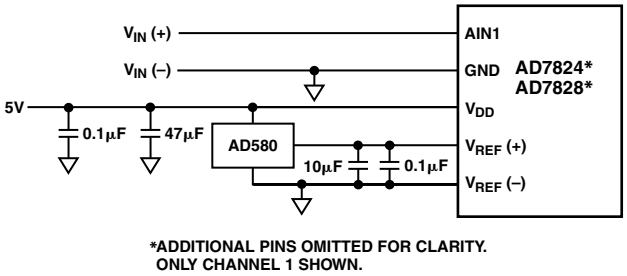


Figure 6. External Reference Using the AD580, Full-Scale Input is 2.5 V

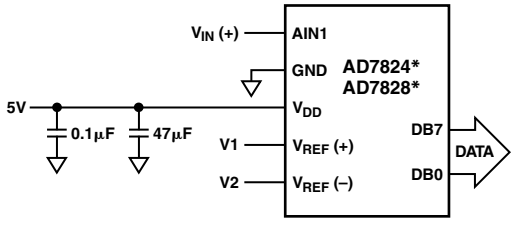


Figure 7. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7824/AD7828, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7824/AD7828 is shown in Figure 8. When a conversion starts ($\overline{CS}$ and $\overline{RD}$ going low), all input switches close, and the selected input channel is connected to the most significant and least significant comparators. Therefore, the analog input is simultaneously connected to 31 input capacitors of 1 pF each.

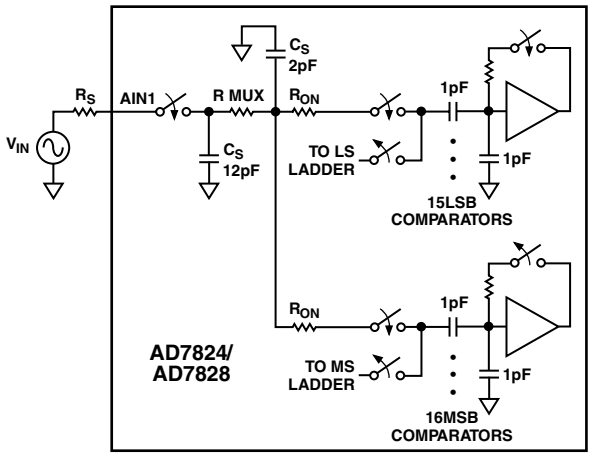


Figure 8. AD7824/AD7828 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 3 kΩ to 6 kΩ). In addition, about 14 pF of input stray capacitance must be charged. The analog input for any channel can be modelled as an RC network, as shown in Figure 9. As R_S increases, it takes longer for the input capacitance to charge.

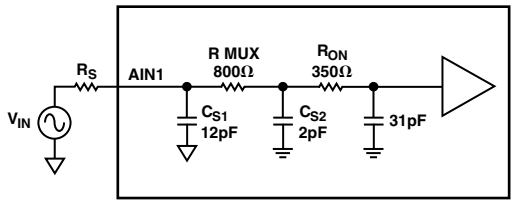


Figure 9. RC Network Model

The time for which the input comparators track the analog input is approximately 1 µs at the start of conversion. Because of input transients on the analog inputs, it is recommended that a source impedance no greater than 100 Ω be connected to the analog inputs. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest. It is important that the amplifier driving the AD7824/AD7828 analog inputs have sufficient loop gain at the input signal frequency as to make the output impedance low.

Suitable op amps for driving the AD7824/AD7828 are the AD544 or AD644.

INHERENT SAMPLE-HOLD

A major benefit of the AD7824's and AD7828's analog input structure is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least 1/2 LSB throughout the conversion process if rated accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7824/AD7828 input comparators, by nature of their input switching, inherently accomplish this sample-and-hold function. Although the conversion time for AD7824/AD7828 is 2 µs, the time for which any selected analog input must be 1/2 LSB stable is much smaller. The AD7824/AD7828 tracks the selected input channel for approximately 1 µs after conversion start. The value of the analog input at that instant (1 µs from conversion start) is the measured value. This value is then used in the least significant flash to generate the lower four bits of data.

SINUSOIDAL INPUTS

The AD7824/AD7828 can measure input signals with slew rates as high as 157 mV/µs to the rated specifications. This means that the analog input frequency can be up to 10 kHz without the aid of an external sample-and-hold. Furthermore, the AD7828 can measure eight 10 kHz signals without a sample-and-hold. The Nyquist criterion requires that the sampling rate be twice the input frequency (i.e., 2 × 10 kHz). This requires an ideal antialiasing filter with an infinite roll-off. To ease the problem of antialiasing filter design, the sampling rate is usually much greater than the Nyquist criterion. The maximum sampling rate (F_{MAX}) for the AD7824/AD7828 can be calculated as follows:

$$F_{MAX} = \frac{1}{t_{CRD} + t_P}$$

$$F_{MAX} = \frac{1}{2E-6+0.5E-6} = 400\ kHz$$

t_{CRD} = AD7824/AD7828 Conversion Time
t_P = Minimum Delay Between Conversion

This permits a maximum sampling rate of 50 kHz for each of the eight channels when using the AD7828 and 100 kHz for each of the four channels when using the AD7824.

UNIPOLAR OPERATION

The analog input range for any channel of the AD7824/AD7828 is 0 V to 5 V as shown in the unipolar operational diagram of Figure 10. Figure 11 shows the designed code transitions that occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, 5/2 LSB, FS 3/2 LSBs). The output code is natural binary with 1 LSB = FS/256 = (5/256) V = 19.5 mV.

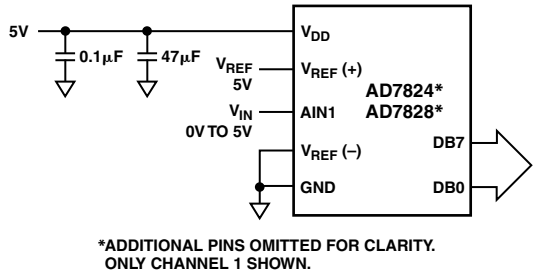


Figure 10. AD7824/AD7828 Unipolar 0 V to 5 V Operation

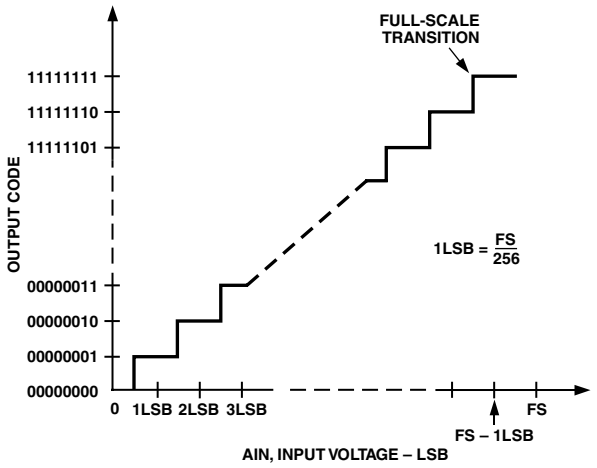


Figure 11. Ideal Input/Output Transfer Characteristic for Unipolar 0 V to 5 V Operation

BIPOLAR OPERATION

The circuit of Figure 12 is designed for bipolar operation. An AD544 op amp conditions the signal input (V_{IN}) so that only positive voltages appear at AIN1. The closed loop transfer function of the op amp for the resistor values shown is given below:

$$AIN1 = \left(2.5 - 0.625 V_{IN}\right) Volts$$

The analog input range is ±4 V and the LSB size is 31.25 mV. The output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 13.

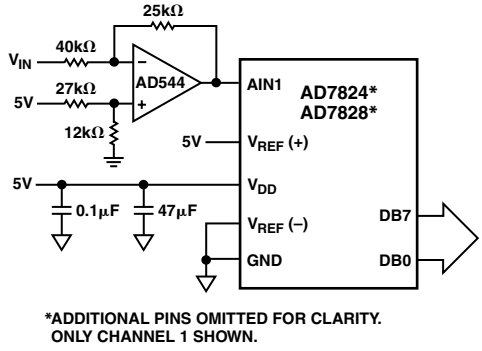


Figure 12. AD7824/AD7828 Bipolar ±4 V Operation

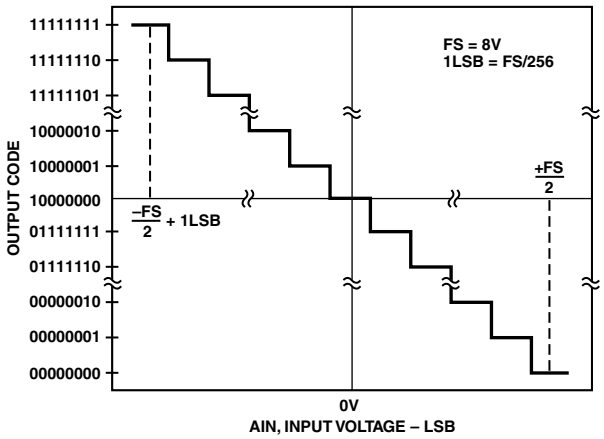


Figure 13. Ideal Input/Output Transfer Characteristic for ±4 V Operation

TIMING AND CONTROL

The AD7824/AD7828 has two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which starts a conversion on the channel selected by the multiplexer address inputs (see Table I). There are two modes of operation as outlined by the timing diagrams of Figures 14 and 15. Mode 0 is designed for microprocessors that can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode l does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

Table I. Truth Table for Input Channel Selection

AD7824		AD7828			
A1	A0	A2	A1	A0	Channel
0	0	0	0	0	AIN1
0	1	0	0	1	AIN2
1	0	0	1	0	AIN3
1	1	0	1	1	AIN4
		1	0	0	AIN5
		1	0	1	AIN6
		1	1	0	AIN7
		1	1	1	AIN8

MODE 0

Figure 14 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors that have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which starts a conversion. The analog multiplexer address inputs must remain valid while $\overline{CS}$ and $\overline{RD}$ are low. The data bus (DB7–DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY), which can be used to drive the microprocessor READY/WAIT input. The RDY is an open-drain output (no internal pull-up device) that goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion when the 8-bit conversion result appears on the data outputs. If the RDY status is not required, the external pull-up resistor can be omitted and the RDY output tied to GND. The $\overline{INT}$ goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

MODE 1

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low, which triggers a conversion (see Figure 15). The multiplexer address inputs are latched on the rising edge of $\overline{RD}$. Data from the previous conversion is read from the three-state data outputs (DB7–DB0). This data may be disregarded if not required. Note that the RDY output (open drain output) does not provide any status information in this mode and must be connected to GND. At the end of conversion, $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ or $\overline{RD}$ returns high. A delay of 2.5 μs must be allowed between READ operations.

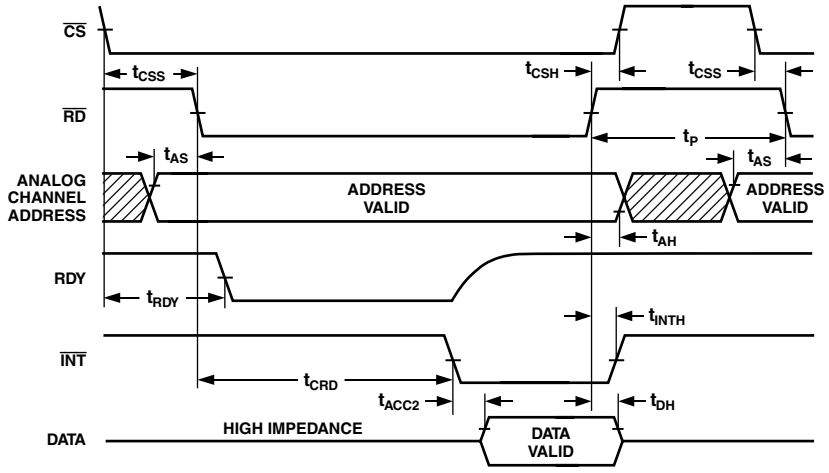


Figure 14. Mode 0 Timing Diagram

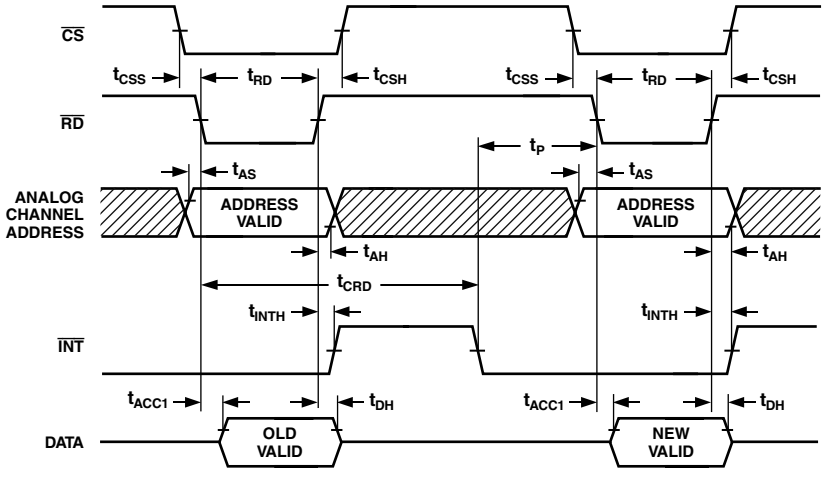


Figure 15. Mode 1 Timing Diagram

MICROPROCESSOR INTERFACING

The AD7824/AD7828 is designed to interface to microprocessors as Read Only Memory (ROM). Analog channel selection, conversion start, and data read operations are controlled by $\overline{CS}$, $\overline{RD}$, and the channel address inputs. These signals are common to all memory peripheral devices.

Z80 MICROPROCESSOR

Figure 16 shows a typical AD7824/AD7828–Z80 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is assigned a memory block starting at address C000. The following LOAD instruction to any of the addresses listed in Table II will start a conversion of the selected channel and read the conversion result.

LD B, (C000)

At the beginning of the instruction cycle when the ADC address is selected, RDY asserts the WAIT input so that the Z80 is forced into a WAIT state. At the end of conversion, RDY returns high and the conversion result is placed in the B register of the microprocessor.

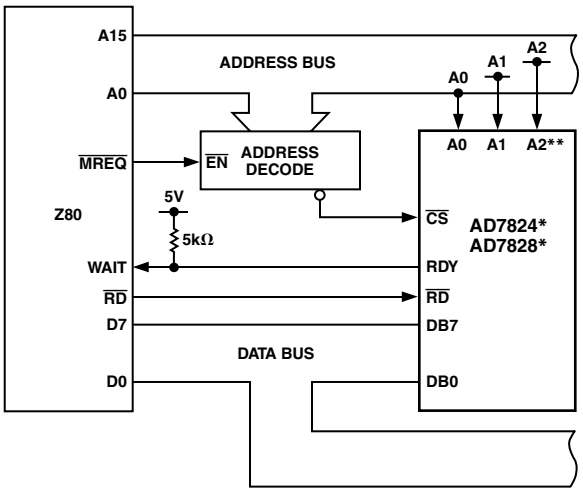


Figure 16. AD7824/AD7828–Z80 Interface

Table II. Address Channel Selection

Address	AD7824 Channel	AD7828 Channel
C000	1	1
C001	2	2
C002	3	3
C003	4	4
C004		5
C005		6
C006		7
C007		8

MC68000 MICROPROCESSOR

Figure 17 shows an MC68000 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is again assigned a memory block starting at address C000. A MOVE instruction to any of the addresses in Table II starts a conversion and reads the conversion result.

MOVE × B $C000, D0

Once conversion has begun, the MC68000 inserts WAIT states until INT goes low, asserting DTACK at the end of conversion. The microprocessor then places the conversion results into the D0 register.

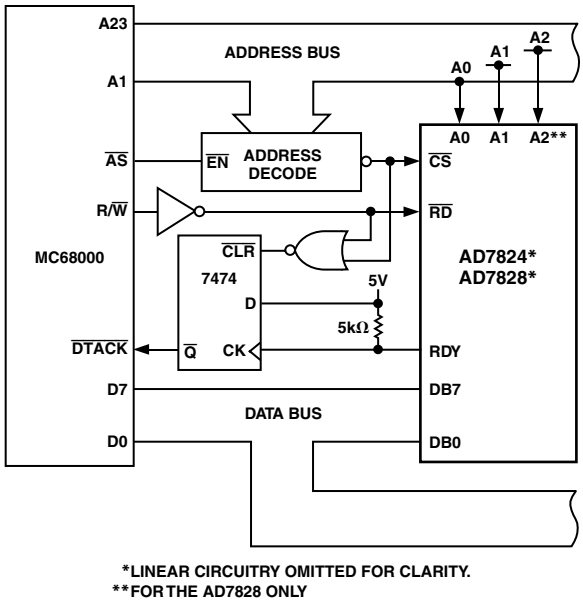


Figure 17. AD7824/AD7828–MC68000 Interface

TMS32010 MICROCOMPUTER

A TMS32010 interface is shown in Figure 18. The AD7824/AD7828 is operating in Mode 1 (i.e., no µP WAIT states). The ADC is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into the accumulator.

IN, A PA (PA = PORT ADDRESS)

The port address (000 to 111) selects the analog channel to be converted. When conversion is complete, a second I/O instruction (IN, A PA) reads the up-to-date data into the accumulator and starts another conversion. A delay of 2.5 µs must be allowed between conversions.

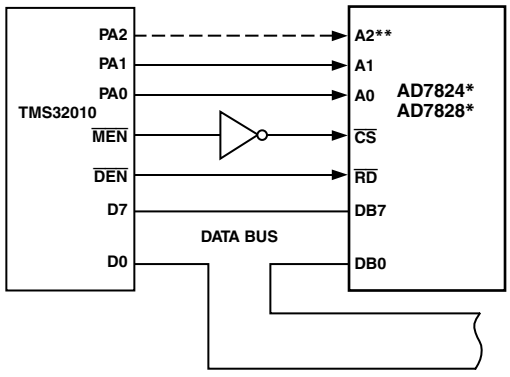


Figure 18. AD7824/AD7828–TMS32010 Interface

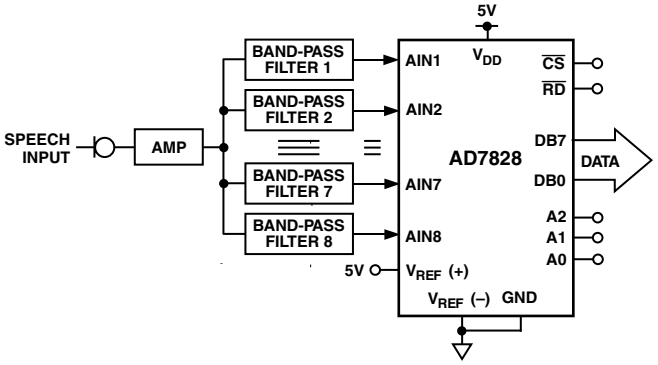


Figure 19. Speech Analysis Using Real-Time Filtering

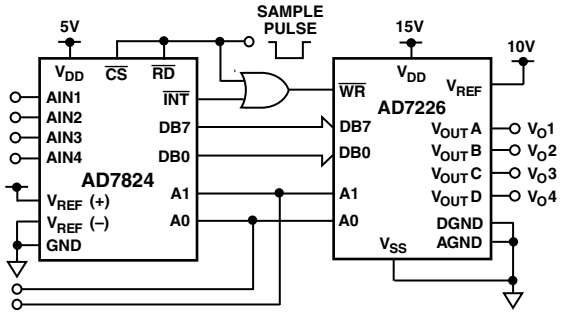
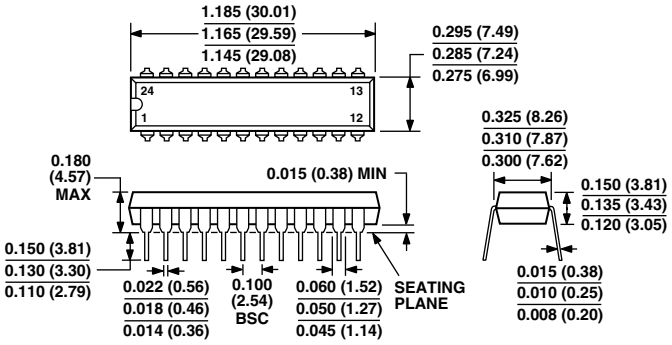


Figure 20. 4-Channel Fast Infinite Sample-and-Hold

OUTLINE DIMENSIONS

24-Lead Plastic Dual-in-Line Package [PDIP]
(N-24)

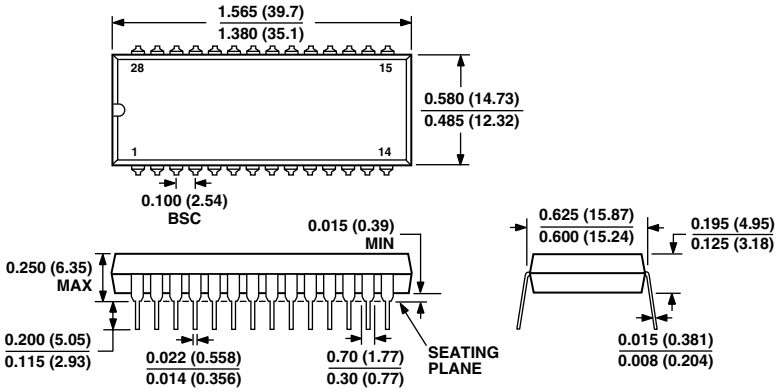
Dimensions shown in inches and (millimeters)



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28-Lead Plastic Dual-in-Line Package [PDIP]
(N-28)

Dimensions shown in inches and (millimeters)

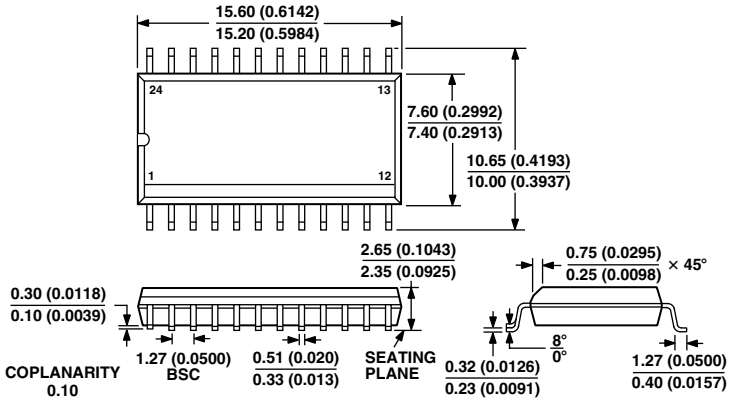


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OUTLINE DIMENSIONS

24-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-24)

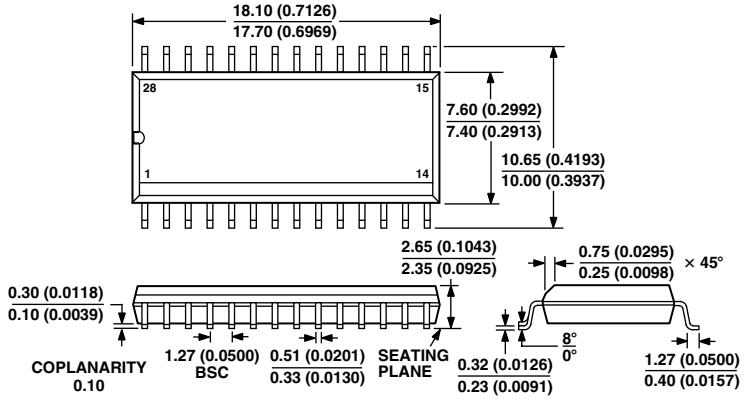
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28-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-28)

Dimensions shown in millimeters and (inches)

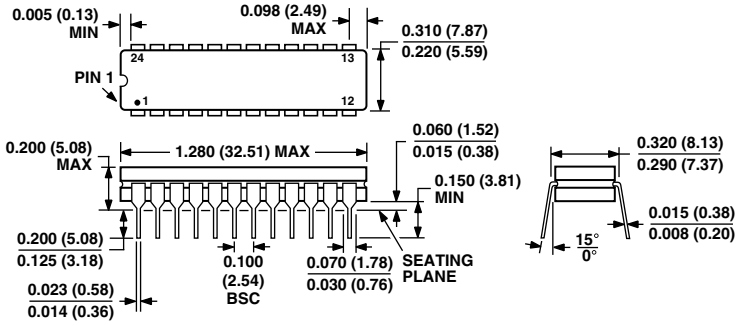


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OUTLINE DIMENSIONS

24-Lead Ceramic DIP - Glass Hermetic Seal [CERDIP]
(Q-24)

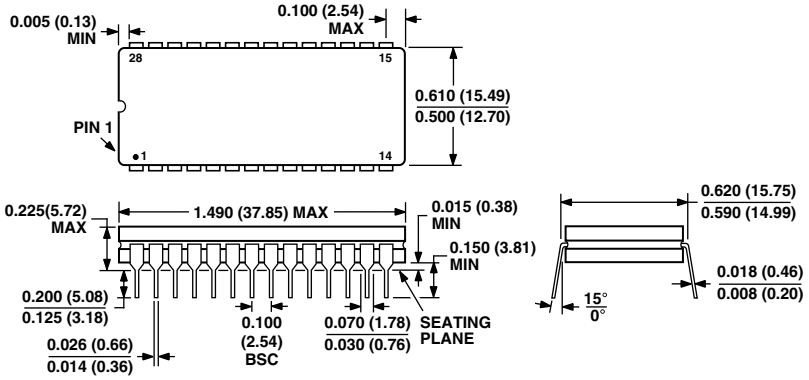
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28-Lead Ceramic DIP - Glass Hermetic Seal [CERDIP]
(Q-28)

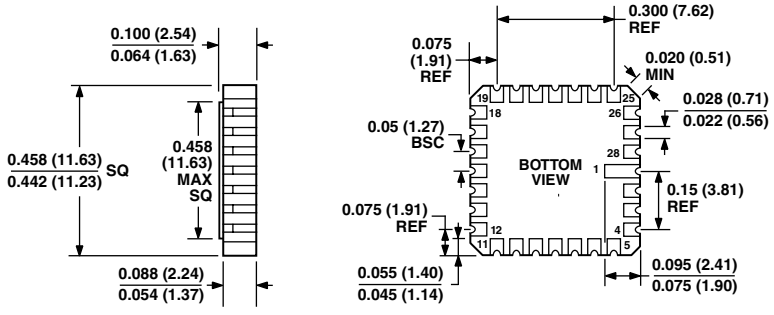
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28-Terminal Ceramic Leaded Chip Carrier [LCC]
(E-28A)

Dimensions shown in inches and (millimeters)

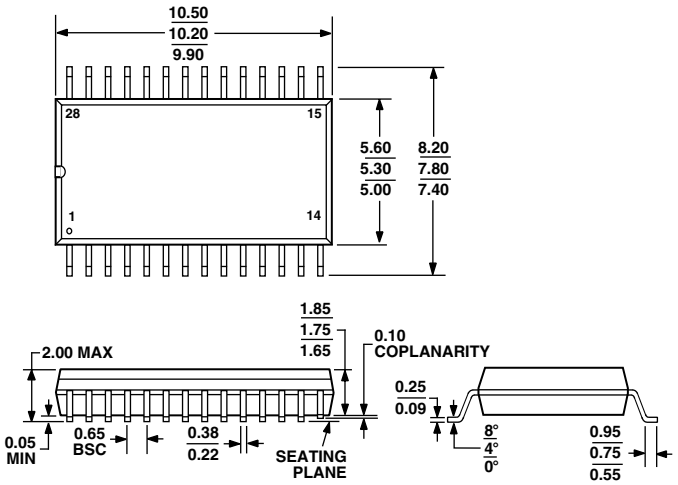


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OUTLINE DIMENSIONS

28-Lead Shrink Small Outline Package [SSOP]
(RS-28)

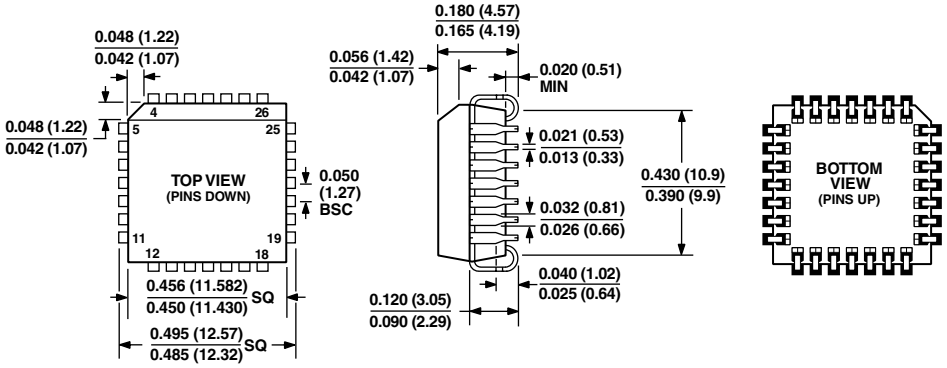
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AH

28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28A)

Dimensions shown in inches and (millimeters)



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Revision History

Location	Page
1/03—Data Sheet changed from REV. E to REV. F.	
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to DIP/SOIC/SSOP, LCCC, AND PLCC Pin Configurations	4
Edit to Figure 3	6
Edits to Circuit Information Basic Description section	6
Edits to Input Current section	7
Edit to Figure 8	7
Edit to Figure 9	7
Updated OUTLINE DIMENSIONS	11
4/02—Data Sheet changed from REV. D to REV. E.	
Edits to ORDERING GUIDE	4

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