LC²MOS 16-Bit Voltage Output DAC

AD7846

FEATURES

16-bit monotonicity over temperature
±2 LSBs integral linearity error
Microprocessor compatible with readback capability
Unipolar or bipolar output
Multiplying capability
Low power (100 mW typical)

FUNCTIONAL BLOCK DIAGRAM

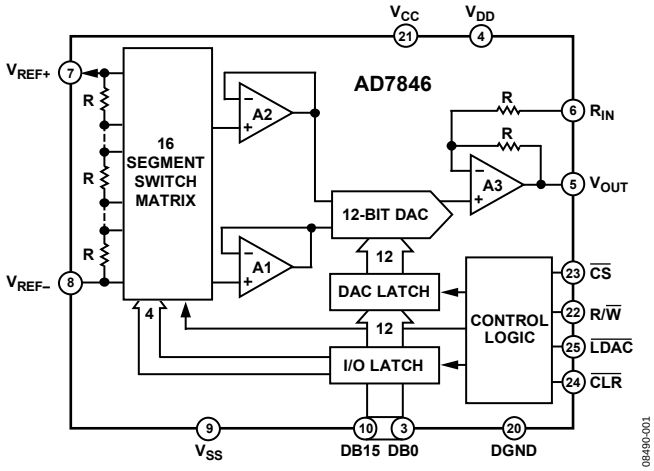


Figure 1.

GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with the Analog Devices, Inc., LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipolar output range (0 V to +5 V, 0 V to +10 V) or bipolar output ranges (±5 V, ±10 V).

The DAC uses a segmented architecture. The four MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function, which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents of the DAC latch to 00…000 or 10…000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0 V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-lead plastic, ceramic, and PLCC packages.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100 mW makes the AD7846 the lowest power, high accuracy DAC on the market.

Rev. G
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Comparable Parts

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Documentation

Data Sheet

- AD7846: LC2MOS16-Bit Voltage Output DAC Data Sheet
- AD7846: Military Data Sheet

Reference Materials

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Design Resources

- AD7846 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

4/10—Rev. F to Rev. G

Change to Figure 1 ... 1

12/09—Rev. E to Rev. F

Updated Format ... Universal
Changes to Table 4 ... 6
Deleted Other Output Voltage Ranges Section ... 9
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SPECIFICATIONS

V_{DD} = +14.25 V to +15.75 V; V_{SS} = −14.25 V to −15.75 V; V_{CC} = +4.75 V to +5.25 V. V_{OUT} loaded with 2 kΩ, 1000 pF to 0 V; V_{REF+} = +5 V; R_{IN} connected to 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	J, A Versions	K, B Versions	Unit	Test Conditions/Comments
RESOLUTION	16	16	Bits	
UNIPOLAR OUTPUT				V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy at +25°C	±12	±4	LSB typ	1 LSB = 153 μV
T_{MIN} to T_{MAX}	±16	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	LSB max	All grades guaranteed monotonic
Gain Error at +25°C	±12	±6	LSB typ	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±16	LSB max	
Offset Error at +25°C	±12	±6	LSB typ	
T_{MIN} to T_{MAX}	±16	±16	LSB max	
Gain TC[2]	±1	±1	ppm FSR/°C typ	
Offset TC[2]	±1	±1	ppm FSR/°C typ	
BIPOLAR OUTPUT				V_{REF-} = −5 V, V_{OUT} = −10 V to +10 V
Relative Accuracy at +25°C	±6	±2	LSB typ	1 LSB = 305 μV
T_{MIN} to T_{MAX}	±8	±4	LSB max	
Differential Nonlinearity Error	±1	±0.5	LSB max	All grades guaranteed monotonic
Gain Error at +25°C	±6	±4	LSB typ	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±16	LSB max	
Offset Error at +25°C	±6	±4	LSB typ	V_{OUT} load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±12	LSB max	
Bipolar Zero Error at +25°C	±6	±4	LSB typ	
T_{MIN} to T_{MAX}	±12	±8	LSB max	
Gain TC[2]	±1	±1	ppm FSR/°Ctyp	
Offset TC[2]	±1	±1	ppm FSR/°Ctyp	
Bipolar Zero TC[2]	±1	±1	ppm FSR/°Ctyp	
REFERENCE INPUT				
Input Resistance	20	20	kΩ min	Resistance from V_{REF+} to V_{REF-}
	40	40	kΩ max	Typically 30 kΩ
V_{REF+} Range	V_{SS} + 6 to	V_{SS} + 6 to	V min to	
	V_{DD} − 6	V_{DD} − 6	V max	
V_{REF-} Range	V_{SS} + 6 to	V_{SS} + 6 to	V min to	
	V_{DD} − 6	V_{DD} − 6	V max	
OUTPUT CHARACTERISTICS				
Output Voltage Swing	V_{SS} + 4 to	V_{SS} + 4 to	V max	
	V_{DD} − 3	V_{DD} − 3		
Resistive Load	2	2	kΩ min	To 0 V
Capacitive Load	1000	1000	pF max	To 0 V
Output Resistance	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	mA typ	To 0 V or any power supply
DIGITAL INPUTS				
V_{IH} (Input High Voltage)	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	pF max	

Parameter[1]	J, A Versions	K, B Versions	Unit	Test Conditions/Comments
DIGITAL OUTPUTS				
V_{OL} (Output Low Voltage)	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH} (Output High Voltage)	4.0	4.0	V min	I_{SOURCE} = 400 μA
Floating State Leakage Current	±10	±10	μA max	DB0 to DB15 = 0 to V_{CC}
Floating State Output Capacitance[2]	10	10	pF max	
POWER REQUIREMENTS[3]				
V_{DD}	+11.4/+15.75	+11.4/+15.75	V min/V max	
V_{SS}	−11.4/−15.75	−11.4/−15.75	V min/V max	
V_{CC}	+4.75/+5.25	+4.75/+5.25	V min/V max	
I_{DD}	5	5	mA max	V_{OUT} unloaded
I_{SS}	5	5	mA max	V_{OUT} unloaded
I_{CC}	1	1	mA max	
Power Supply Sensitivity[4]	1.5	1.5	LSB/V max	
Power Dissipation	100	100	mW typ	V_{OUT} unloaded

[1] Temperature ranges as follows: J, K versions: 0°C to +70°C; A, B versions: −40°C to +85°C.
[2] Guaranteed by design and characterization, not production tested.
[3] The AD7846 is functional with power supplies of ±12 V. See the Typical Performance Characteristics section.
[4] Sensitivity of gain error, offset error, and bipolar zero error to V_{DD}, V_{SS} variations.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance and are not subject to test. V_{REF+} = +5 V; V_{DD} = +14.25 V to +15.75 V; V_{SS} = −14.25 V to −15.75 V; V_{CC} = +4.75 V to +5.25 V; R_{IN} connected to 0 V, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (All Versions)	Unit	Test Conditions/Comments
Output Settling Time[1]	6	μs max	To 0.006% FSR, V_{OUT} loaded, V_{REF-} = 0 V, typically 3.5 μs
	9	μs max	To 0.003% FSR, V_{OUT} loaded, V_{REF-} = −5 V, typically 6.5 μs
Slew Rate	7	V/μs typ	
Digital-to-Analog Glitch Impulse	70	nV-sec typ	DAC alternately loaded with 10…0000 and 01…1111, V_{OUT} unloaded
AC Feedthrough	0.5	mV p-p typ	V_{REF-} = 0 V, V_{REF+} = 1 V rms, 10 kHz sine wave, DAC loaded with all 0s
Digital Feedthrough	10	nV-sec typ	DAC alternately loaded with all 1s and all 0s. $\overline{CS}$ high
Output Noise Voltage Density, 1 kHz to 100 kHz	50	nV/√Hz typ	Measured at V_{OUT}, DAC loaded with 0111011…11, V_{REF+} = V_{REF-} = 0 V

[1] $\overline{LDAC}$ = 0. Settling time does not include deglitching time of 2.5 μs (typ).

TIMING CHARACTERISTICS

V_{DD} = +14.25 V to +15.75 V, V_{SS} = −14.25 V to −15.75 V, V_{CC} = +4.75 V to +5.25 V, unless otherwise noted.

Table 3.

Parameter[1]	Limit at T_{MIN} to T_{MAX} (All Versions)	Unit	Test Conditions/Comments
t_1	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	60	ns min	$\overline{CS}$ pulse width (write cycle)
t_3	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_4	60	ns min	Data setup time
t_5	0	ns min	Data hold time
t_6[2]	120	ns max	Data access time
t_7[3]	10	ns min	Bus relinquish time
	60	ns max	
t_8	0	ns min	$\overline{CLR}$ setup time
t_9	70	ns min	$\overline{CLR}$ pulse width
t_{10}	0	ns min	$\overline{CLR}$ hold time
t_{11}	70	ns min	$\overline{LDAC}$ pulse width
t_{12}	130	ns min	$\overline{CS}$ pulse width (read cycle)

[1] Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2] t_6 is measured with the load circuits of Figure 3 and Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3] t_7 is defined as the time required for an output to change 0.5 V when loaded with the circuits of Figure 5 and Figure 6.

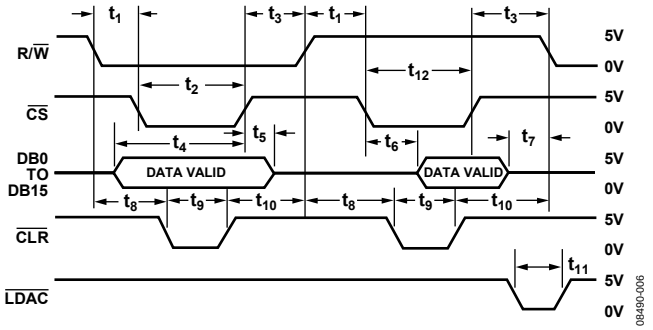


Figure 2. Timing Diagram



Figure 3. Load Circuit for Access Time (t_6)—High Z to V_{OH}

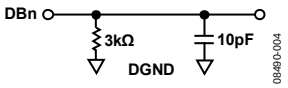


Figure 5. Load Circuit for Access Time (t_7)—High Z to V_{OH}

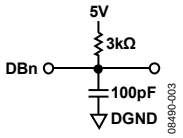


Figure 4. Load Circuits for Bus Relinquish Time (t_6)—High Z to V_{OL}

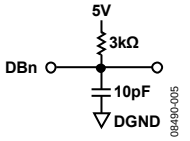


Figure 6. Load Circuits for Bus Relinquish Time (t_7)—High Z to V_{OL}

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to DGND	−0.4 V to +17 V
V_{CC} to DGND	−0.4 V, V_{DD} + 0.4 V, or +7 V (whichever is lower)
V_{SS} to DGND	+0.4 V to −17 V
V_{REF+} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
V_{REF-} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
V_{OUT} to DGND[1]	V_{DD} + 0.4 V, V_{SS} − 0.4 V, or ±10 V (whichever is lower)
R_{IN} to DGND	V_{DD} + 0.4 V, V_{SS} − 0.4 V
Digital Input Voltage to DGND	−0.4 V to V_{CC} + 0.4 V
Digital Output Voltage to DGND	−0.4 V to V_{CC} + 0.4 V
Power Dissipation (Any Package)	
To +75°C	1000 mW
Derates above +75°C	10 mW/°C
Operating Temperature Range	
J, K Versions	0°C to +70°C
A, B Versions	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering)	+300°C

[1] V_{OUT} can be shorted to DGND, V_{DD}, V_{SS}, or V_{CC} provided that the power dissipation of the package is not exceeded.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

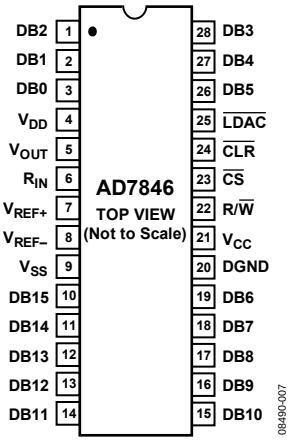


Figure 7. PDIP Pin Configuration

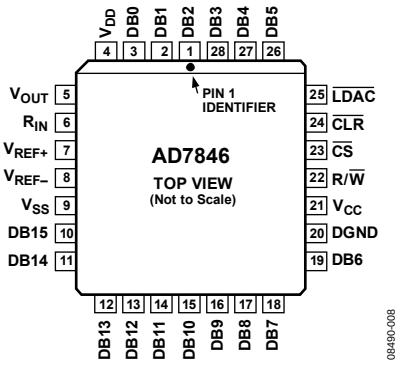


Figure 8. CERDIP Pin Configuration

Table 5. Pin Function Descriptions

Pin	Mnemonic	Description
1 to 3	DB2 to DB0	Data I/Os. DB0 is LSB.
4	V_{DD}	Positive Supply for Analog Circuitry. This is +15 V nominal.
5	V_{OUT}	DAC Output Voltage.
6	R_{IN}	Input to Summing Resistor of DAC Output Amplifier. This is used to select output voltage ranges. See Table 6.
7	V_{REF+}	V_{REF+} Input. The DAC is specified for V_{REF+} = +5 V.
8	V_{REF-}	V_{REF-} Input. For unipolar operation connect V_{REF-} to 0 V, and for bipolar operation connect it to −5 V. The device is specified for both conditions.
9	V_{SS}	Negative Supply for the Analog Circuitry. This is −15 V nominal.
10 to 19	DB15 to DB6	Data I/Os. DB15 is MSB.
20	DGND	Ground for Digital Circuitry.
21	V_{CC}	Positive Supply for Digital Circuitry. This is +5 V nominal.
22	R/$\overline{W}$	R/$\overline{W}$ Input. This pin can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Chip Select Input. This pin selects the device.
24	$\overline{CLR}$	Clear Input. The DAC can be cleared to 000…000 or 100…000. See Table 7.
25	$\overline{LDAC}$	Asynchronous Load Input to DAC.
26 to 28	DB5 to DB3	Data I/Os.

Table 6. Output Voltage Ranges

Output Range	V_{REF+}	V_{REF-}	R_{IN}
0 V to +5 V	+5 V	0 V	V_{OUT}
0 V to +10 V	+5 V	0 V	0 V
+5 V to −5 V	+5 V	−5 V	V_{OUT}
+5 V to −5 V	+5 V	0 V	+5 V
+10 V to −10 V	+5 V	−5 V	0 V

TYPICAL PERFORMANCE CHARACTERISTICS

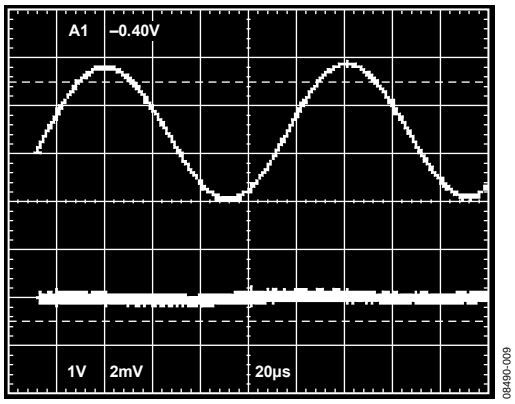


Figure 9. AC Feedthrough, V_{REF+} = 1 V rms, 10 kHz Sine Wave

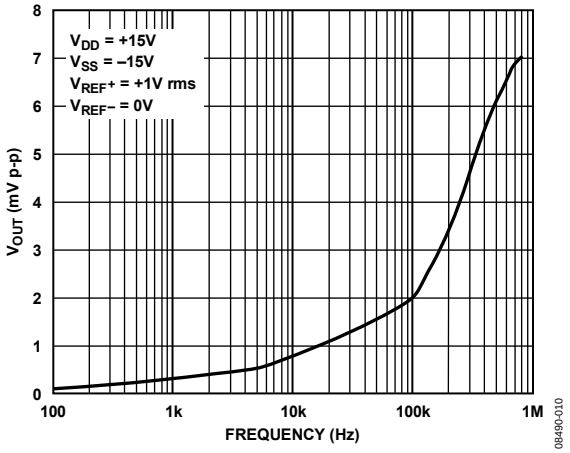


Figure 10. AC Feedthrough to V_{OUT} vs. Frequency

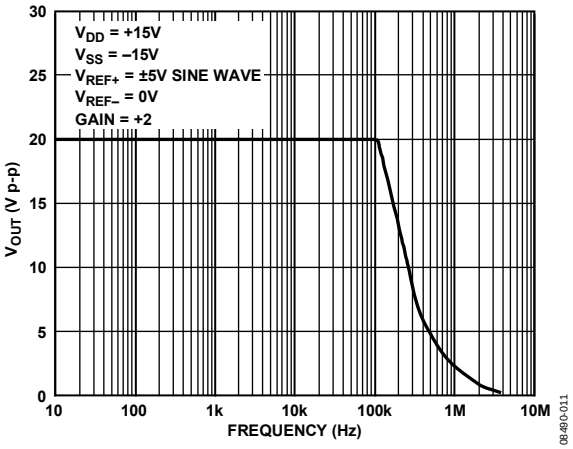


Figure 11. Large Signal Frequency Response

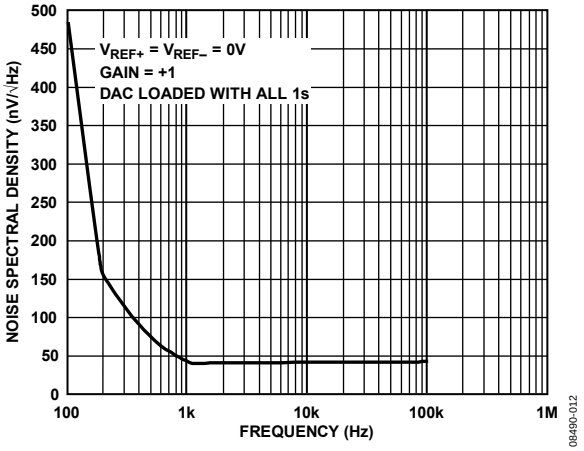


Figure 12. Noise Spectral Density

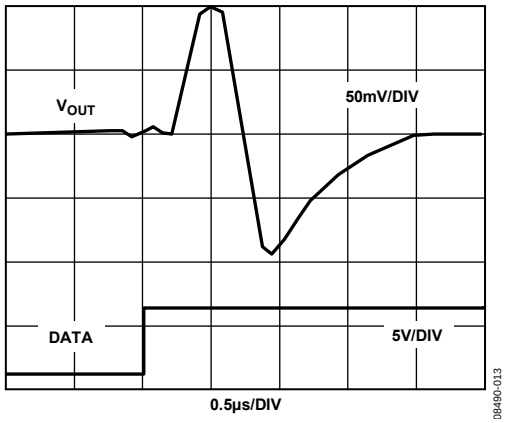


Figure 13. Digital-to-Analog Glitch Impulse Without Internal Deglitcher (10…000 to 011…111 Transition)

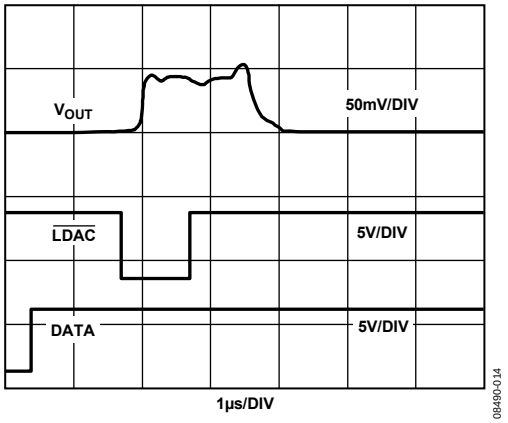


Figure 14. Digital-to-Analog Glitch Impulse with Internal Deglitcher (10…000 to 011…111 Transition)

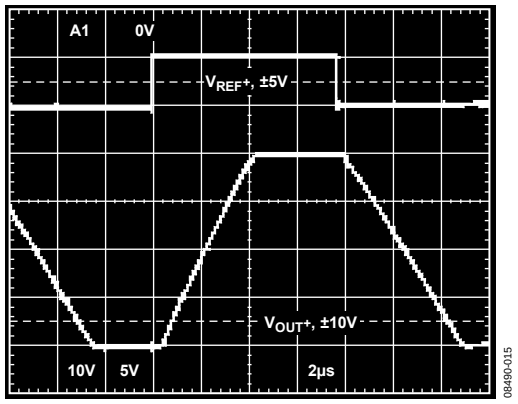


Figure 15. Pulse Response (Large Signal)

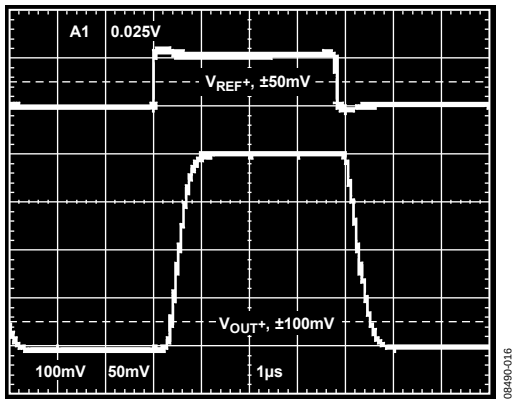


Figure 16. Pulse Response (Small Signal)

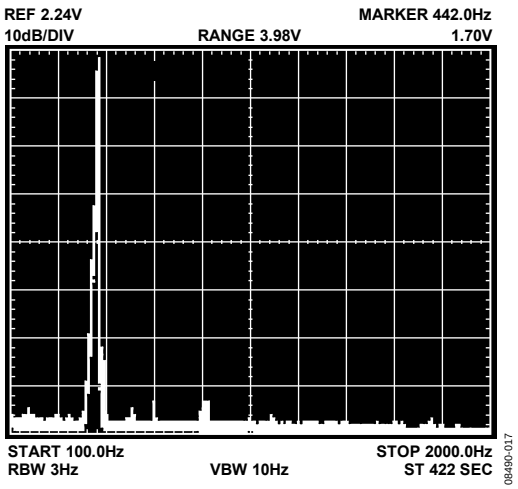


Figure 17. Spectral Response of Digitally Constructed Sine Wave

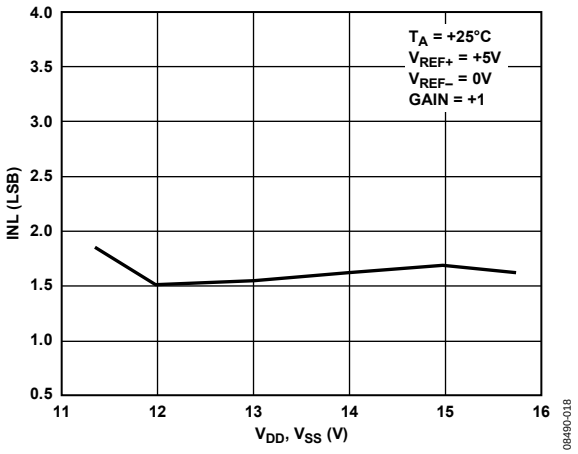


Figure 18. Typical Integral Nonlinearity vs. V_{DD}/V_{SS}

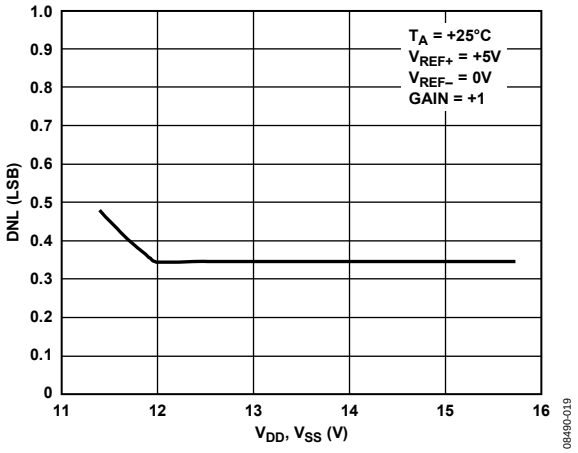


Figure 19. Typical Differential Nonlinearity vs. V_{DD}/V_{SS}

TERMINOLOGY

Least Significant Bit
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7846, 1 LSB = $(V_{REF+} - V_{REF-})/2^{16}$.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (that is, offset and gain errors are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB over the operating temperature range ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

Offset Error
This is the error present at the device output with all 0s loaded in the DAC. It is due to op amp input offset voltage and bias current and the DAC leakage current.

Bipolar Zero Error
When the AD7846 is connected for bipolar output and 10…000 is loaded to the DAC, the deviation of the analog output from the ideal midscale of 0 V is called the bipolar zero error.

Digital-to-Analog Glitch Impulse
This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-sec or nV-sec depending upon whether the glitch is measured as a current or a voltage.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from either of the V_{REF} terminals to V_{OUT} when the DAC is loaded with all 0s.

Digital Feedthrough
When the DAC is not selected (that is, $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

CIRCUIT DESCRIPTION

DIGITAL SECTION

Figure 20 shows the digital control logic and on-chip data latches in the AD7846. Table 7 is the associated truth table. The digital-to-analog converter (DAC) has two latches that are controlled by four signals: $\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$, and $\overline{CLR}$. The input latch is connected to the data bus (DB15 to DB0). A word is written to the input latch by bringing $\overline{CS}$ low and R/$\overline{W}$ low. The contents of the input latch can be read back by bringing $\overline{CS}$ low and R/$\overline{W}$ high. This feature is called readback and is used in system diagnostic and calibration routines.

Data is transferred from the input latch to the DAC latch with the $\overline{LDAC}$ strobe. The equivalent analog value of the DAC latch contents appears at the DAC output. The $\overline{CLR}$ pin resets the DAC latch contents to 000…000 or 100…000, depending on the state of R/$\overline{W}$. Writing a $\overline{CLR}$ loads 000…000 and reading a $\overline{CLR}$ loads 100…000. To reset a DAC to 0 V in a unipolar system, the user should assert $\overline{CLR}$ while R/$\overline{W}$ is low; to reset to 0 V in a bipolar system, assert the $\overline{CLR}$ while R/$\overline{W}$ is high.

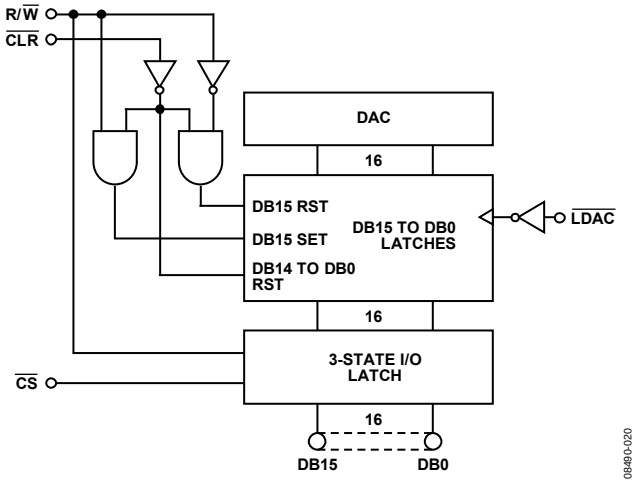


Figure 20. Input Control Logic

Table 7. Control Logic Truth Table

$\overline{CS}$	R/$\overline{W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-state DAC I/O latch in high-Z state
0	0	X	X	DAC I/O latch loaded with DB15 to DB0
0	1	X	X	Contents of DAC I/O latch available on DB15 to DB0
X	X	0	1	Contents of DAC I/O latch transferred to DAC latch
X	0	X	0	DAC latch loaded with 000…000
X	1	X	0	DAC latch loaded with 100…000

DIGITAL-TO-ANALOG CONVERSION

Figure 21 shows the digital-to-analog section of the AD7846. There are three DACs, each of which has its own buffer amplifiers. DAC1 and DAC2 are 4-bit DACs. They share a 16-resistor string but have their own analog multiplexers. The voltage reference is applied to the resistor string. DAC3 is a 12-bit voltage mode DAC with its own output stage.

The four MSBs of the 16-bit digital code drive DAC1 and DAC2, and the 12 LSBs control DAC3. Using DAC1 and DAC2, the MSBs select a pair of adjacent nodes on the resistor string and present that voltage to the positive and negative inputs of DAC3. This DAC interpolates between these two voltages to produce the analog output voltage.

To prevent nonmonotonicity in the DAC due to amplifier offset voltages, DAC1 and DAC2 leap along the resistor string. For example, when switching from Segment 1 to Segment 2, DAC1 switches from the bottom of Segment 1 to the top of Segment 2 while DAC2 stays connected to the top of Segment 1. The code driving DAC3 is automatically complemented to compensate for the inversion of its inputs. This means that any linearity effects due to amplifier offset voltages remain unchanged when switching from one segment to the next and 16-bit monotonicity is ensured if DAC3 is monotonic. Thus, 12-bit resistor matching in DAC3 guarantees overall 16-bit monotonicity. This is much more achievable than 16-bit matching, which a conventional R-2R structure needs.

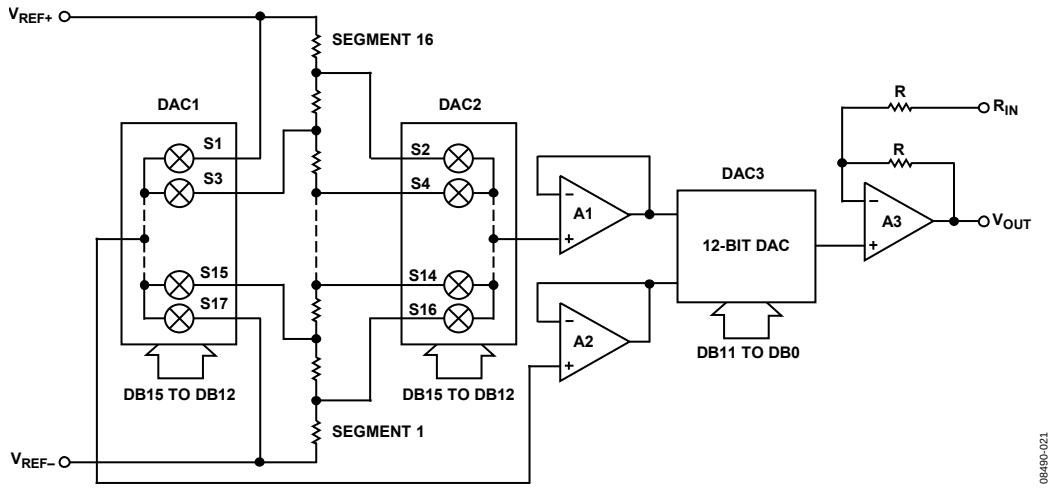


Figure 21. Digital-to-Analog Conversion

OUTPUT STAGE

The output stage of the AD7846 is shown in Figure 22. It is capable of driving a 2 kΩ/1000 pF load. It also has a resistor feedback network that allows the user to configure it for gains of 1 or 2. Table 6 shows the different output ranges that are possible.

An additional feature is that the output buffer is configured as a track-and-hold amplifier. Although normally tracking its input, this amplifier is placed in a hold mode for approximately 2.5 µs after the leading edge of $\overline{\text{LDAC}}$. This short state keeps the DAC output at its previous voltage while the AD7846 is internally changing to its new value. Thus, any glitches that occur in the transition are not seen at the output. In systems where the $\overline{\text{LDAC}}$ is tied permanently low, the deglitching is not in operation. Figure 13 and Figure 14 show the outputs of the AD7846 without and with the deglitcher.

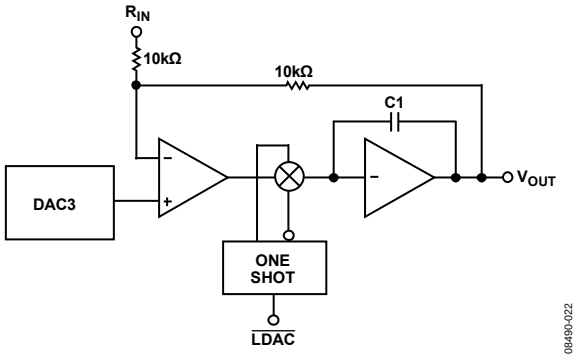


Figure 22. Output Stage

UNIPOLAR BINARY OPERATION

Figure 23 shows the AD7846 in the unipolar binary circuit configuration. The DAC is driven by the AD586 +5 V reference. Because R_{IN} is tied to 0 V, the output amplifier has a gain of 2 and the output range is 0 V to +10 V. If a 0 V to +5 V range is required, R_{IN} should be tied to V_{OUT}, configuring the output stage for a gain of 1. Table 8 gives the code table for the circuit of Figure 23.

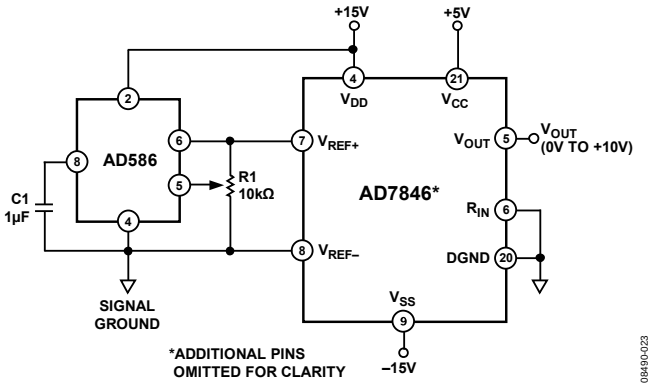


Figure 23. Unipolar Binary Operation

Table 8. Code Table for Figure 23

Binary Number in DAC Latch		
MSB	**LSB[1]**	**Analog Output (V_{OUT})**
1111 1111 1111 1111		+10 (65,535/65,536) V
1000 0000 0000 0000		+10 (32,768/65,536) V
0000 0000 0000 0001		+10 (1/65,536) V
0000 0000 0000 0000		0 V

[1] LSB = 10 V/2^{16} = 10 V/65,536 = 152 µV.

Offset and gain can be adjusted in Figure 23 as follows:

- To adjust offset, disconnect the V_{REF-} input from 0 V, load the DAC with all 0s, and adjust the V_{REF-} voltage until V_{OUT} = 0 V.
- For gain adjustment, the AD7846 should be loaded with all 1s and R1 adjusted until V_{OUT} = 10 (65,535)/(65,536) = 9.999847 V. If a simple resistor divider is used to vary the V_{REF-} voltage, it is important that the temperature coefficients of these resistors match that of the DAC input resistance (−300 ppm/°C). Otherwise, extra offset errors are introduced over temperature. Many circuits do not require these offset and gain adjustments. In these circuits, R1 can be omitted. Pin 5 of the AD586 can be left open circuit and Pin 8 (V_{REF-}) of the AD7846 tied to 0 V.

BIPOLAR OPERATION

Figure 24 shows the AD7846 set up for ±10 V bipolar operation. The AD588 provides precision ±5 V tracking outputs that are fed to the V_{REF+} and V_{REF-} inputs of the AD7846. The code table for Figure 24 is shown in Table 9.

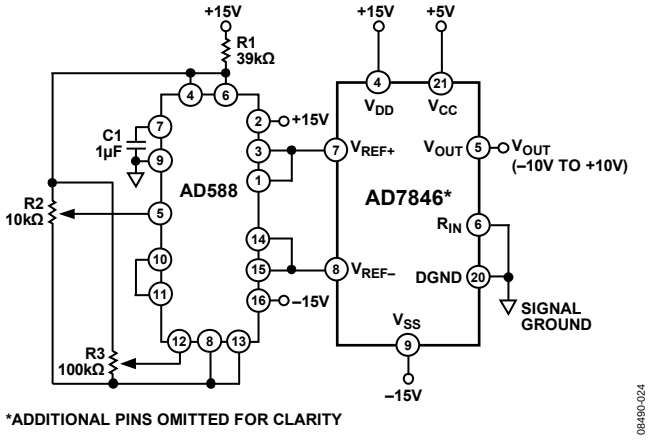


Figure 24. Bipolar ±10 V Operation

Table 9. Offset Binary Code Table for Figure 24

Binary Number in DAC Latch		
MSB	LSB[1]	Analog Output (V_{OUT})
1111 1111 1111 1111		+10 (32,767/32,768) V
1000 0000 0000 0001		+10 (1/32,768) V
1000 0000 0000 0000		0 V
0111 1111 1111 1111		−10 (1/32,768) V
0000 0000 0000 0000		−10 (32,768/32,768) V

[1] LSB = 10 V/2^{15} = 10 V/32,768 = 305 μV.

Full-scale and bipolar zero adjustment are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the +5 V and −5 V outputs together with respect to ground.

For bipolar zero adjustment on the AD7846, load the DAC with 100…000 and adjust R3 until V_{OUT} = 0 V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 9.999694 V.

When bipolar zero and full-scale adjustment are not needed, R2 and R3 can be omitted, Pin 12 on the AD588 should be connected to Pin 11, and Pin 5 should be left floating. If a user wants a 5 V output range, there are two choices. By tying Pin 6 (R_{IN}) of the AD7846 to V_{OUT} (Pin 5), the output stage gain is reduced to unity and the output range is ±5 V. If only a positive 5 V reference is available, bipolar ±5 V operation is still possible. Tie V_{REF-} to 0 V and connect R_{IN} to V_{REF+}. This also gives a ±5 V output range. However, the linearity, gain, and offset error specifications are the same as the unipolar 0 V to 5 V range.

MULTIPLYING OPERATION

The AD7846 is a full multiplying DAC. To obtain four-quadrant multiplication, tie V_{REF-} to 0 V, apply the ac input to V_{REF+}, and tie R_{IN} to V_{REF+}. Figure 11 shows the large signal frequency response when the DAC is used in this fashion.

POSITION MEASUREMENT APPLICATION

Figure 25 shows the AD7846 in a position measurement application using an linear variable displacement transducer (LVDT), an AD630 synchronous demodulator and a comparator to make a 16-bit LVDT-to-digital converter. The LVDT is excited with a fixed frequency and fixed amplitude sine wave (usually 2.5 kHz, 2 V p-p). The outputs of the secondary coil are in antiphase and their relative amplitudes depend on the position of the core in the LVDT. The AD7846 output interpolates between these two inputs in response to the DAC input code. The AD630 is set up so that it rectifies the DAC output signal. Thus, if the output of the DAC is in phase with the V_{REF+} input, the inverting input to the comparator is positive, and if it is in phase with V_{REF-}, the output is negative. By turning on each bit of the DAC in succession starting with the MSB and deciding to leave it on or turn it off based on the comparator output, a 16-bit measurement of the core position is obtained.

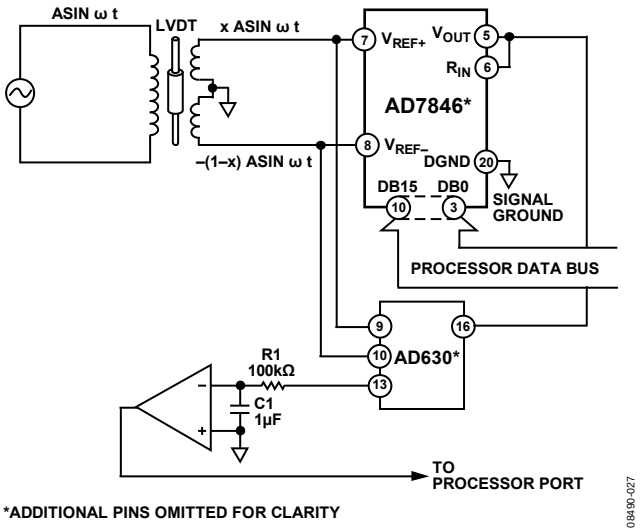


Figure 25. AD7846 in Position Measurement Application

MICROPROCESSOR INTERFACING

AD7846-TO-8086 INTERFACE

Figure 26 shows the 8086 16-bit processor interfacing to the AD7846. The double buffering feature of the DAC is not used in this circuit because $\overline{\text{LDAC}}$ is permanently tied to 0 V. AD0 to AD15 (the 16-bit data bus) are connected to the DAC data bus (DB0 to DB15). The 16-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example, the DAC address is 0xD000.

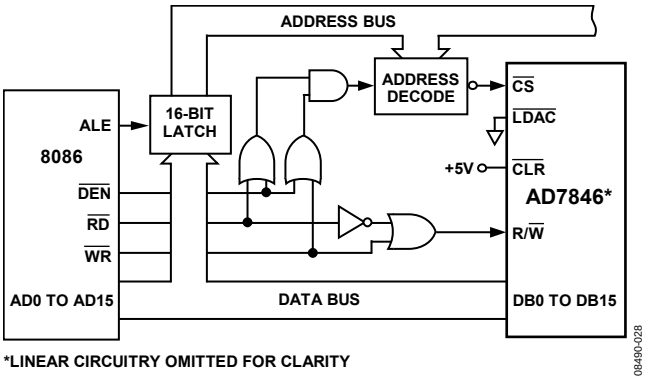


Figure 26. AD7846-to-8086 Interface Circuit

In a multiple DAC system, the double buffering of the AD7846 allows the user to simultaneously update all DACs. In Figure 27, a 16-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{\text{CS}}$4 (that is, $\overline{\text{LDAC}}$) is brought low, updating all the DACs simultaneously.

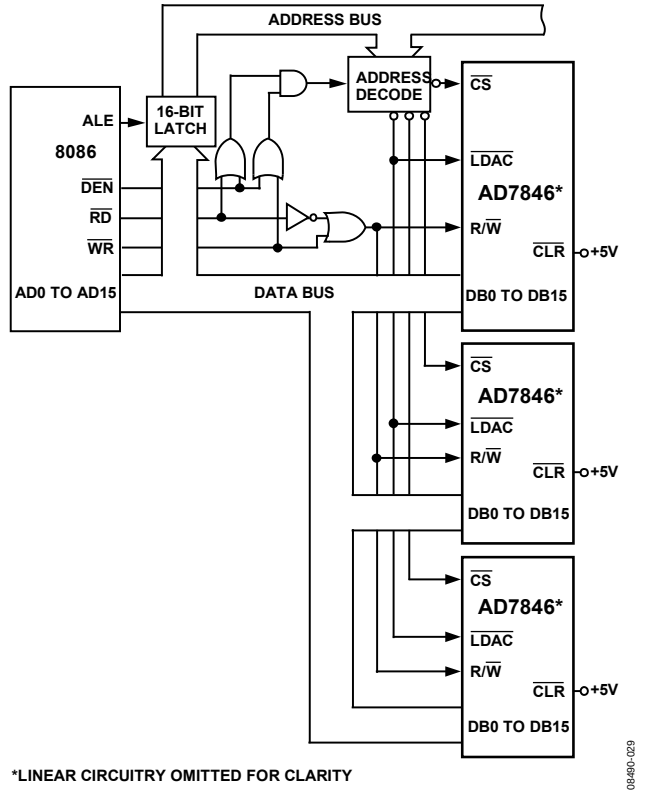


Figure 27. AD7846-to-8086 Interface: Multiple DAC System

AD7846-TO-MC68000 INTERFACE

Interfacing between the AD7846 and MC68000 is accomplished using the circuit of Figure 28. The following routine writes data to the DAC latches and then outputs the data via the DAC latch.

```
1000  MOVE.W   #W,      The desired DAC data,
               D0       W, is loaded into
                        Data Register 0. W
                        may be any value
                        between 0 and 65535
                        (decimal) or 0 and
                        FFFF (hexadecimal).

      MOVE.W   D0,      The data, W, is
               $E000    transferred between
                        D0 and the DAC
                        register.

      MOVE.W   #228,    Control is returned
      TRAP     D7       to the System Monitor
               #14      using these two
                        instructions.
```

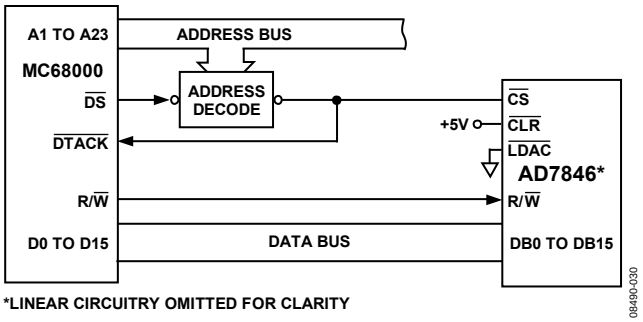


Figure 28. AD7846-to-MC68000 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7846 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs are constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough, isolate the DAC from the noise source. Figure 29 shows an interface circuit that isolates the DAC from the bus.

Note that to make use of the AD7846 readback feature using the isolation technique of Figure 29, the latch needs to be bidirectional.

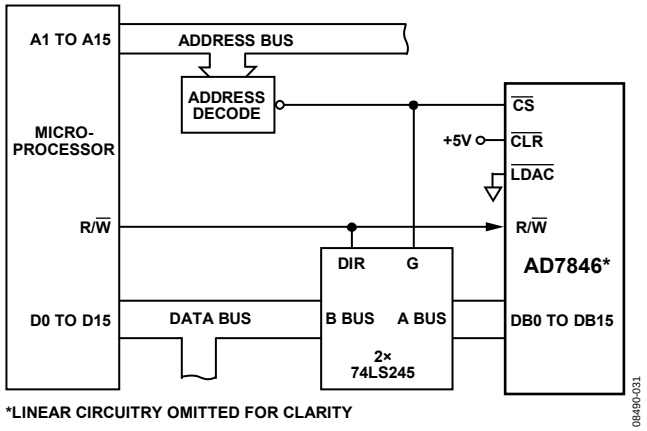


Figure 29. AD7846 Interface Circuit Using Latches to Minimize Digital Feedthrough

APPLICATION HINTS

NOISE

In high resolution systems, noise is often the limiting factor. With a 10 V span, a 16-bit LSB is 152 µV (–96 dB). Thus, the noise floor must stay below –96 dB in the frequency range of interest. Figure 12 shows the noise spectral density for the AD7846.

GROUNDING

As well as noise, the other prime consideration in high resolution DAC systems is grounding. With an LSB size of 152 µV and a load current of 5 mA, 1 LSB of error can be introduced by series resistance of only 0.03 Ω.

Figure 30 shows recommended grounding for the AD7846 in a typical application.

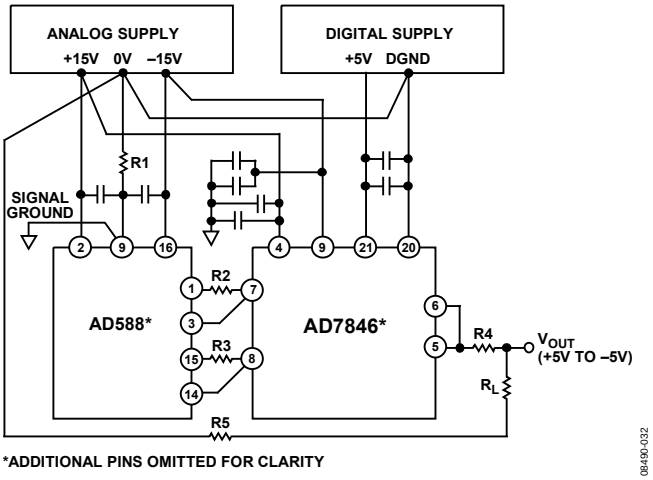


Figure 30. AD7846 Grounding

R1 to R5 represent lead and track resistances on the printed circuit board. R1 is the resistance between the analog power supply ground and the signal ground. Because current flowing in R1 is very low (bias current of AD588 sense amplifier), the effect of R1 is negligible. R2 and R3 represent track resistance between the AD588 outputs and the AD7846 reference inputs. Because of the force and sense outputs on the AD588, these resistances will also have a negligible effect on accuracy.

R4 is the resistance between the DAC output and the load. If R_L is constant, then R4 introduces a gain error only that can be trimmed out in the calibration cycle. R5 is the resistance between the load and the analog common. If the output voltage is sensed across the load, R5 introduces a further gain error, which can be trimmed out. If, on the other hand, the output voltage is sensed at the analog supply common, R5 appears as part of the load and therefore introduces no errors.

PRINTED CIRCUIT BOARD LAYOUT

Figure 31 shows the AD7846 in a typical application with the AD588 reference, producing an output analog voltage in the ±10 V range. Full-scale and bipolar zero adjustment are provided by Potentiometer R2 and Potentiometer R3. Latches (2 × 74LS245) isolate the DAC digital inputs from the active microprocessor bus and minimize digital feedthrough.

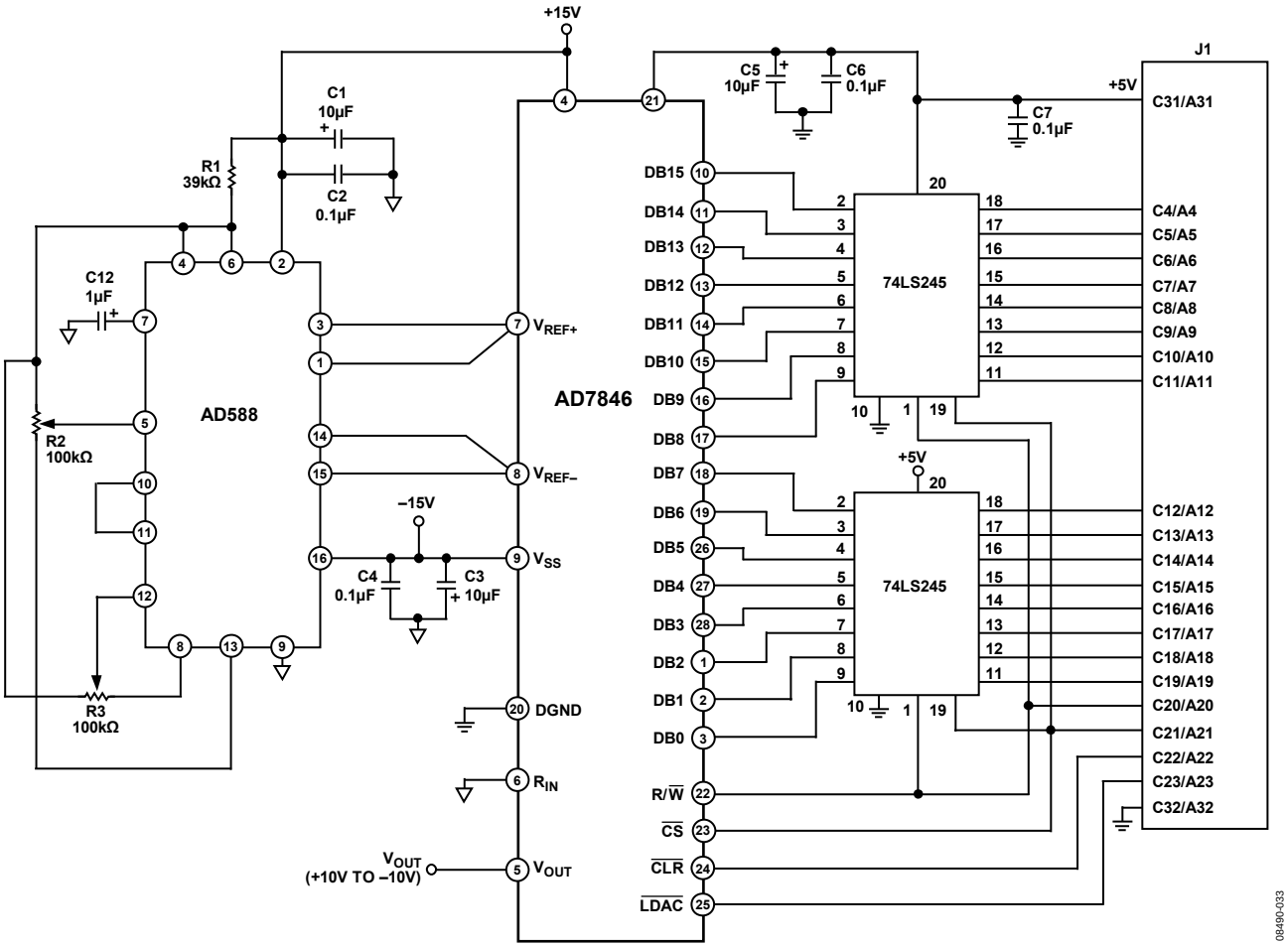
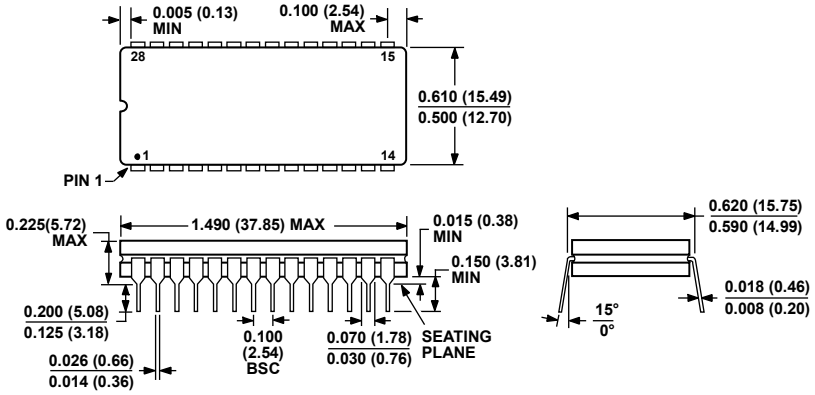


Figure 31. Schematic for AD7846 Board

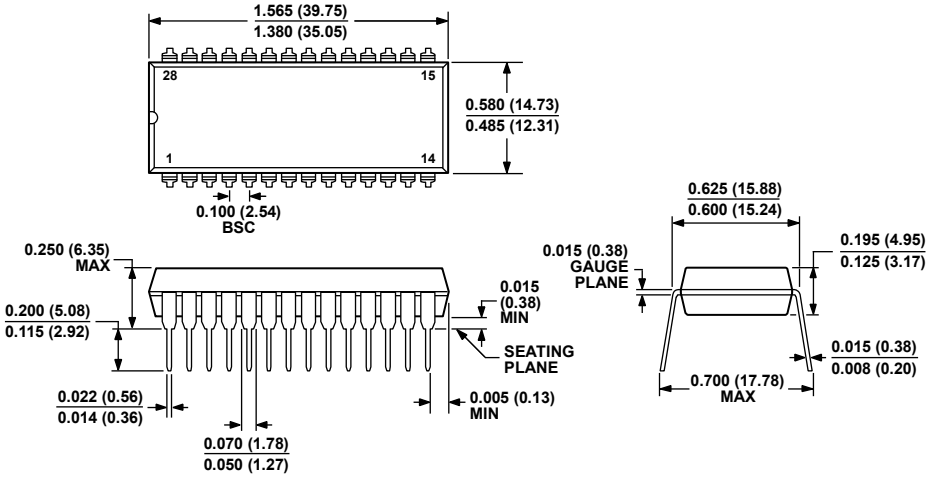
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

030106-A

Figure 32. 28-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-28-2)
Dimensions shown in inches and (millimeters)

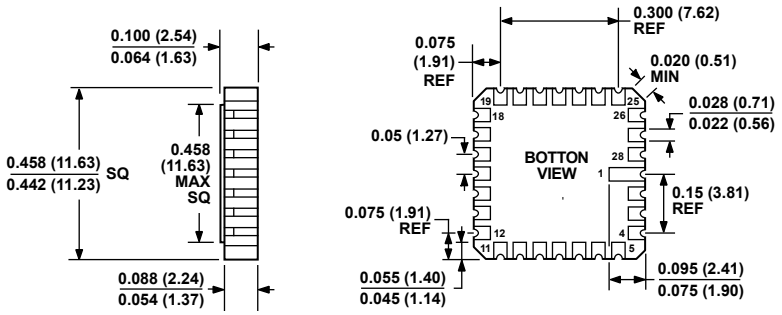


COMPLIANT TO JEDEC STANDARDS MS-011

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REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

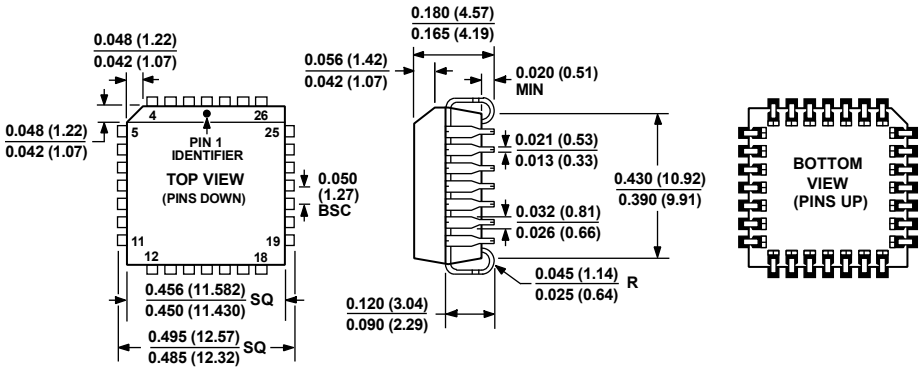
Figure 33. 28-Lead Plastic Dual In-Line Package [PDIP]
Wide Body
(N-28-2)
Dimensions shown in inches and (millimeters)



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022106-A

Figure 34. 28-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-28-1)
Dimensions shown in inches and (millimeters)



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042508-A

Figure 35. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Description	Package Option
5962-89697013A	−55°C to +125°C	±16 LSB	28-Terminal Ceramic Leadless Chip Carrier [LCC]	E-28-1
5962-8969701XA	−55°C to +125°C	±16 LSB	28-Lead Ceramic Dual In-Line Package [CERDIP]	Q-28-2
AD7846JN	0°C to +70°C	±16 LSB	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD7846JNZ	0°C to +70°C	±16 LSB	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD7846KN	0°C to +70°C	±8 LSB	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD7846KNZ	0°C to +70°C	±8 LSB	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD7846JP	0°C to +70°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846JP-REEL	0°C to +70°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846JPZ	0°C to +70°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846JPZ-REEL	0°C to +70°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846KP	0°C to +70°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846KP-REEL	0°C to +70°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846KPZ	0°C to +70°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846KPZ-REEL	0°C to +70°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846AP	−40°C to +85°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846APZ	−40°C to +85°C	±16 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846AQ	−40°C to +85°C	±16 LSB	28-Lead Ceramic Dual In-Line Package [CERDIP]	Q-28-2
AD7846BP	−40°C to +85°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846BPZ	−40°C to +85°C	±8 LSB	28-Lead Plastic Leaded Chip Carrier [PLCC]	P-28
AD7846ACHIPS	−40°C to +85°C	±16 LSB		DIE

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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