5 V Single Supply, 8-Channel 14-Bit 285 kSPS Sampling ADC

AD7856

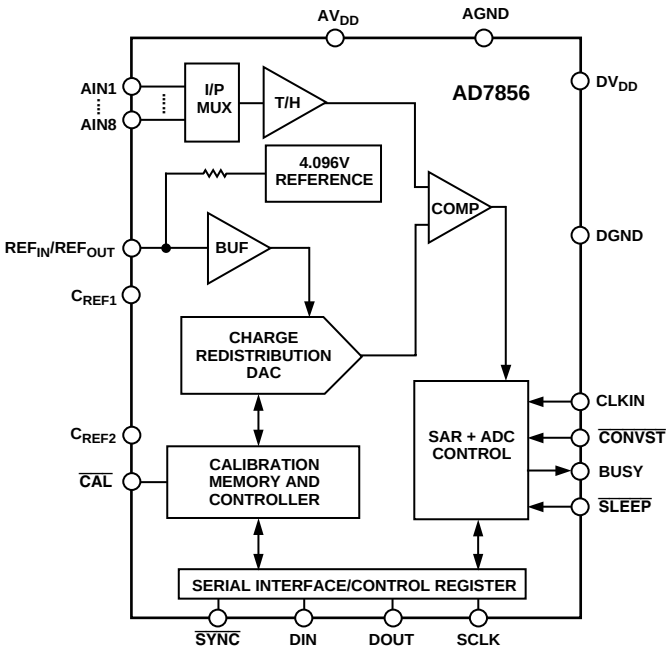
FEATURES

Single 5 V Supply
285 kSPS Throughput Rate
Self- and System Calibration with Autocalibration on Power-Up
Eight Single-Ended or Four Pseudo-Differential Inputs
Low Power: 60 mW Typ
Automatic Power-Down After Conversion (2.5 μW Typ)
Flexible Serial Interface: 8051/SPI™/QSPI™/μP Compatible
24-Lead DIP, SOIC and SSOP Packages

APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Pen Computers
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7856 is a high speed, low power, 14-bit ADC that operates from a single 5 V power supply. The ADC powers up with a set of default conditions at which time it can be operated as a read only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and it has a number of power-down options for low power applications.

The AD7856 is capable of 285 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7856 voltage range is 0 to V_{REF} with straight binary output coding. Input signal range is to the supply and the part is capable of converting full power signals to 10 MHz.

CMOS construction ensures low power dissipation of typically 60 mW for normal operation and 5.1 mW in power-down mode at 10 kSPS throughput rate. The part is available in 24-lead, 0.3 inch-wide dual in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.
Please see page 31 for data sheet index.

PRODUCT HIGHLIGHTS

1. Single 5 V supply.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic power-down after conversion.
4. Operates with reference voltages from 1.2 V to V_{DD}.
5. Analog input range from 0 V to V_{DD}.
6. Eight single-ended or four pseudo-differential input channels.
7. Self- and system calibration.
8. Versatile serial I/O port (SPI/QSPI/8051/μP).

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AD7856–SPECIFICATIONS[1, 2]

A Grade: f_{CLKIN} = 6 MHz, (–40°C to +105°C), f_{SAMPLE} = 285 kHz; K Grade: f_{CLKIN} = 4 MHz, (0°C to +105°C), f_{SAMPLE} = 102 kHz; (AV_{DD} = DV_{DD} = +5.0 V ± 5%, REF_{IN}/REF_{OUT} = 4.096 V External Reference unless otherwise noted, $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) Specifications apply for Mode 2 operation, standard 3-wire SPI interface; refer to Detailed Timing section for Mode 1 Specifications.

Parameter	A Version[1]	K Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 10 kHz
Signal to Noise + Distortion Ratio[3] (SNR)	78	78	dB min	79.5 dB typ
Total Harmonic Distortion (THD)	–86	–86	dB max	–95 dB typ
Peak Harmonic or Spurious Noise	–87	–87	dB max	–95 dB typ
Intermodulation Distortion (IMD)				
Second Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb = 10.05 kHz
Third Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb = 10.05 kHz
Channel-to-Channel Isolation	–90	–90	dB typ	V_{IN} = 25 kHz
DC ACCURACY				Any Channel
Resolution	14	14	Bits	
Integral Nonlinearity		±2	LSB max	4.096 V External Reference, V_{DD} = 5 V
	±2		LSB typ	
Differential Nonlinearity		±2	LSB max	Guaranteed No Missed Codes to 13 Bits.
	±2		LSB typ	
Offset Error		±10	LSB max	
	±10	±5	LSB typ	
Offset Error Match		±3	LSB max	
Positive Full-Scale Error		±10	LSB max	
	±10		LSB typ	
Positive Full-Scale Error Match		±2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) Can Be Biased Up, but AIN(+) Cannot Go Below AIN(–)
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	4.096/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	Resistor Connected to Internal Reference Node
REF_{OUT} Output Voltage	3.696/4.496	3.696/4.496	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	V_{DD} – 1.0	V_{DD} – 1.0	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} – 0.4	V_{DD} – 0.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±1	±1	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	3.5	5.25	µs max	21 CLKIN Cycles
Track/Hold Acquisition Time	0.33	0.5	µs min	

Parameter	A Version[1]	K Version[1]	Units	Test Conditions/Comments
POWER PERFORMANCE				
AV_{DD}, DV_{DD}	+4.75/+5.25	+4.75/+5.25	V min/max	
I_{DD}				
Normal Mode[5]	17	17	mA max	$AV_{DD} = DV_{DD}$ = 4.75 V to 5.25 V. Typically 12 mA
Sleep Mode[6]				
With External Clock On	30	10	μA typ	Full Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0
	400	500	μA typ	Partial Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1
With External Clock Off	5	5	μA max	Typically 0.5 μA. Full Power-Down. Power Management. Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0
	200	200	μA typ	Partial Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1
Normal Mode Power Dissipation	89.25	89.25	mW max	V_{DD} = 5.25 V. Typically 60 mW; $\overline{SLEEP} = V_{DD}$
Sleep Mode Power Dissipation				
With External Clock On	52.5	52.5	μW typ	V_{DD} = 5.25 V. $\overline{SLEEP}$ = 0 V
With External Clock Off	26.25	26.25	μW max	V_{DD} = 5.25 V. Typically 5.25 μW; $\overline{SLEEP}$ = 0 V
SYSTEM CALIBRATION				
Offset Calibration Span[7]	$+0.0375 \times V_{REF}/-0.0375 \times V_{REF}$		V max/min	Allowable Offset Voltage Span for Calibration
Gain Calibration Span[7]	$+1.01875 \times V_{REF}/-0.98125 \times V_{REF}$		V max/min	Allowable Full-Scale Voltage Span for Calibration

NOTES

[1]Temperature ranges as follows: A Version: –40°C to +105°C. K Version: 0°C to +105°C.

[2]Specifications apply after calibration.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @ +25°C to ensure compliance.

[5]All digital inputs @ DGND except for $\overline{CONVST}$, $\overline{SLEEP}$, $\overline{CAL}$ and $\overline{SYNC}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.

[6]CLKIN @ DGND when external clock off. All digital inputs @ DGND except for $\overline{CONVST}$, $\overline{SLEEP}$, $\overline{CAL}$, and $\overline{SYNC}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.

[7]The Offset and Gain Calibration Spans are defined as the range of offset and gain errors that the AD7856 can calibrate. Note also that these are voltage spans and are not absolute voltages (i.e., the allowable system offset voltage presented at AIN(+) for the system offset error to be adjusted out will be AIN(–) $\pm 0.0375 \times V_{REF}$, and the allowable system full-scale voltage applied between AIN(+) and AIN(–) for the system full-scale voltage error to be adjusted out will be $V_{REF} \pm 0.01875 \times V_{REF}$). This is explained in more detail in the Calibration section of the data sheet.

Specifications subject to change without notice.

AD7856

TIMING SPECIFICATIONS[1] (V_{DD} = 5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. A Grade: f_{CLKIN} = 6 MHz; K Grade: f_{CLKIN} = 4 MHz.)

Parameter	Limit at T_{MIN}, T_{MAX} A Version	K Version	Units	Description
f_{CLKIN}[2]	500	500	kHz min	Master Clock Frequency
	6	4	MHz max	
f_{SCLK}	6	4	MHz max	
t_1[3]	100	100	ns min	$\overline{CONVST}$ Pulsewidth
t_2	50	50	ns max	$\overline{CONVST}\downarrow$ to BUSY$\uparrow$ Propagation Delay
$t_{CONVERT}$	3.5	5.25	µs max	Conversion Time = 20 t_{CLKIN}
t_3	–0.4 t_{SCLK}	–0.4 t_{SCLK}	ns min	$\overline{SYNC}\downarrow$ to SCLK$\downarrow$ Setup Time (Noncontinuous SCLK Input)
	±0.4 t_{SCLK}	±0.4 t_{SCLK}	ns min/max	$\overline{SYNC}\downarrow$ to SCLK$\downarrow$ Setup Time (Continuous SCLK Input)
t_4[4]	30	50	ns max	Delay from $\overline{SYNC}\downarrow$ Until DOUT 3-State Disabled
t_5[4]	30	50	ns max	Delay from $\overline{SYNC}\downarrow$ Until DIN 3-State Disabled
t_6[4]	45	75	ns max	Data Access Time After SCLK$\downarrow$
t_7	30	40	ns min	Data Setup Time Prior to SCLK$\uparrow$
t_8	20	20	ns min	Data Valid to SCLK Hold Time
t_9	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_{10}	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_{11}	30	30	ns min	SCLK$\uparrow$ to $\overline{SYNC}\uparrow$ Hold Time (Noncontinuous SCLK)
	30/0.4 t_{SCLK}	30/0.4 t_{SCLK}	ns min/max	(Continuous SCLK)
t_{12}[5]	50	50	ns max	Delay from $\overline{SYNC}\uparrow$ Until DOUT 3-State Enabled
t_{13}	90	90	ns max	Delay from SCLK$\uparrow$ to DIN Being Configured as Output
t_{14}[6]	50	50	ns max	Delay from SCLK$\uparrow$ to DIN Being Configured as Input
t_{15}	2.5 t_{CLKIN}	2.5 t_{CLKIN}	ns max	$\overline{CAL}\uparrow$ to BUSY$\uparrow$ Delay
t_{16}	2.5 t_{CLKIN}	2.5 t_{CLKIN}	ns max	$\overline{CONVST}\downarrow$ to BUSY$\uparrow$ Delay in Calibration Sequence
t_{CAL}	41.7	62.5	ms typ	Full Self-Calibration Time, Master Clock Dependent (250026 t_{CLKIN})
t_{CAL1}	37.04	55.5	ms typ	Internal DAC Plus System Full-Scale Cal Time, Master Clock Dependent (222228 t_{CLKIN})
t_{CAL2}	4.63	6.94	ms typ	System Offset Calibration Time, Master Clock Dependent (27798 t_{CLKIN})

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Table X and timing diagrams for different interface modes and calibration.

[2]Mark/Space ratio for the master clock input is 40/60 to 60/40.

[3]The $\overline{CONVST}$ pulsewidth here only applies for normal operation. When the part is in power-down mode, a different $\overline{CONVST}$ pulsewidth will apply (see Power-Down section).

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[5]t_{12} is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_{12}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[6]t_{14} is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_{14}, quoted in the Timing Characteristics is the true delay of the part in turning off the output drivers and configuring the DIN line as an input. Once this time has elapsed the user can drive the DIN line knowing that a bus conflict will not occur.

Specifications subject to change without notice.

TYPICAL TIMING DIAGRAMS

Figures 2 and 3 show typical read and write timing diagrams for serial Interface Mode 2. The reading and writing occurs after conversion in Figure 2, and during conversion in Figure 3. To attain the maximum sample rate of 285 kHz, reading and writing must be performed during conversion as in Figure 3. At least 330 ns acquisition time must be allowed (the time from the falling edge of BUSY to the next rising edge of $\overline{\text{CONVST}}$) before the next conversion begins to ensure that the part is settled to the 14-bit level. If the user does not want to provide the $\overline{\text{CONVST}}$ signal, the conversion can be initiated in software by writing to the control register.

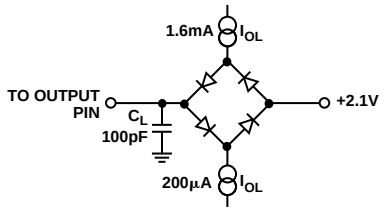


Figure 1. Load Circuit for Digital Output Timing Specifications

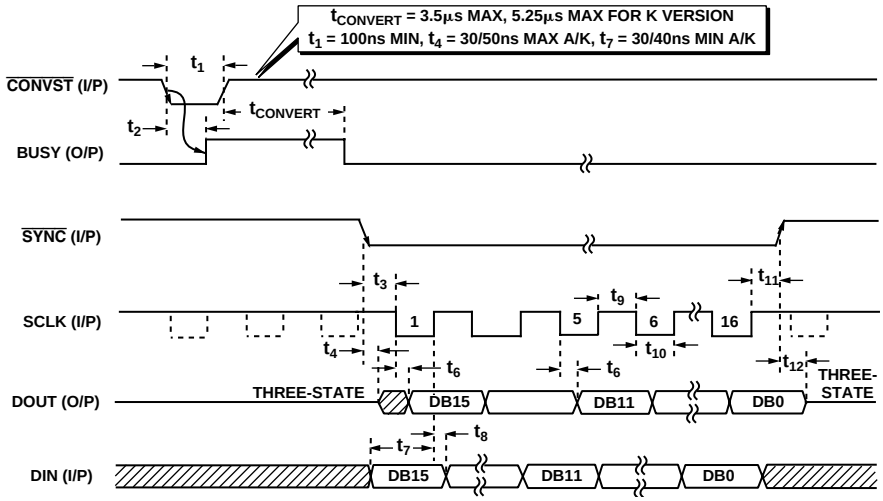


Figure 2. Timing Diagram for Interface Mode 2 (Reading/Writing After Conversion)

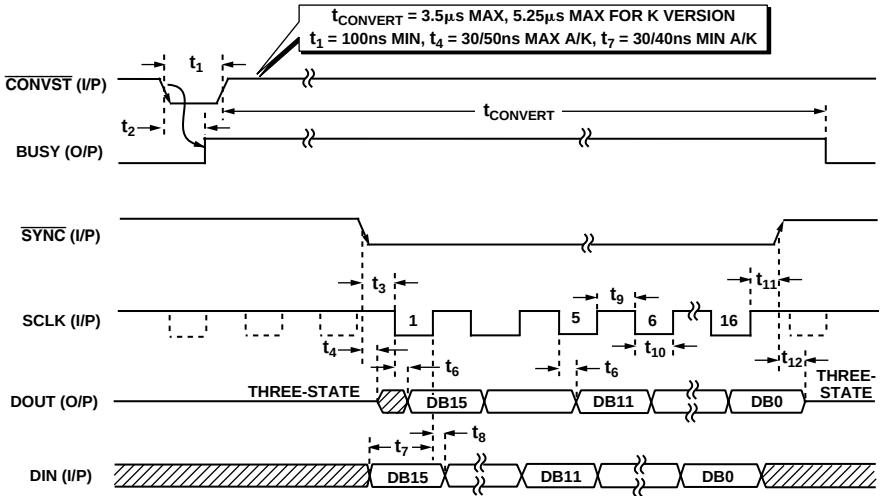


Figure 3. Timing Diagram for Interface Mode 2 (Reading/Writing During Conversion)

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range Commercial
A Version ..... –40°C to +105°C
K Version ..... 0°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
θ_{JC} Thermal Impedance ..... 34.7°C/W
Lead Temperature, (Soldering, 10 secs) ..... +260°C
SOIC, SSOP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance . 75°C/W (SOIC) 115°C/W (SSOP)
θ_{JC} Thermal Impedance .. 25°C/W (SOIC) 35°C/W (SSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infrared (15 secs) ..... +220°C
ESD ..... >1 kV

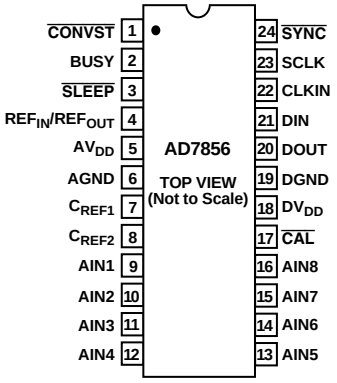
NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Package Options[2]
AD7856AN	±2 typ	N-24
AD7856AR	±2 typ	R-24
AD7856KR	±2	R-24
AD7856ARS	±2 typ	RS-24
EVAL-AD7856CB[3]		
EVAL-CONTROL BOARD[4]		

NOTES
[1]Linearity error here refers to integral linearity error.
[2]N = Plastic DIP; R = SOIC; RS = SSOP.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

PIN CONFIGURATIONS (DIP, SOIC AND SSOP)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7856 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. When this input is not used, it should be tied to DV_{DD}.
2	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ or rising edge of $\overline{\text{CAL}}$, and remains high until conversion is completed. BUSY is also used to indicate when the AD7856 has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep Input/Low Power Mode. A Logic 0 initiates a sleep, and all circuitry is powered down, including the internal voltage reference, provided there is no conversion or calibration being performed. Calibration data is retained. A Logic 1 results in normal operation. See Power-Down section for more details.
4	REF_{IN}/REF_{OUT}	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal reference voltage is 4.096 V and this appears at the pin. This pin can be overdriven by an external reference or can be taken as high as AV_{DD}. When this pin is tied to AV_{DD}, or when an externally applied reference approaches AV_{DD}, the C_{REF1} pin should also be tied to AV_{DD}.
5	AV_{DD}	Analog Positive Supply Voltage, +5.0 V ± 5%.
6	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
7	C_{REF1}	Reference Capacitor (0.1 μF Multilayer Ceramic in parallel with a 470 nF NPO type). This external capacitor is used as a charge source for the internal DAC. The capacitor should be tied between the pin and AGND.
8	C_{REF2}	Reference Capacitor (0.01 μF Multilayer Ceramic). This external capacitor is used in conjunction with the on-chip reference. The capacitor should be tied between the pin and AGND.
9–16	AIN1–AIN8	Analog Inputs. Eight analog inputs that can be used as eight single-ended inputs (referenced to AGND) or four pseudo-differential inputs. Channel configuration is selected by writing to the control register. Both the positive and negative inputs cannot go below AGND or above AV_{DD} at any time. Also the positive input cannot go below the negative input. See Table III for channel selection.
17	$\overline{\text{CAL}}$	Calibration Input. This pin has an internal pull-up current source of 0.15 μA. A falling edge on this pin resets all calibration control logic and initiates a calibration on its rising edge. There is the option of connecting a 10 nF capacitor from this pin to DGND to allow for an automatic self-calibration on power-up. This input overrides all other internal operations. If the autocalibration is not required, this pin should be tied to a logic high.
18	DV_{DD}	Digital Supply Voltage, +5.0 V ± 5%.
19	DGND	Digital Ground. Ground reference point for digital circuitry.
20	DOUT	Serial Data Output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial Data Input. The data to be written is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the serial interface mode the part is in (see Table X).
22	CLKIN	Master clock signal for the device (A Grade: 6 MHz; K Grade: 4 MHz). Sets the conversion and calibration times.
23	SCLK	Serial Port Clock. Logic Input. The user must provide a serial clock on this input.
24	$\overline{\text{SYNC}}$	Frame Sync. Logic Input. This pin is level triggered active low and frames the serial clock for the read and write operations (see Table IX).

TERMINOLOGY[1]

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Total Unadjusted Error
This is the deviation of the actual code from the ideal code taking all errors into account (*Gain, Offset, Integral Nonlinearity and other errors*) at any point along the transfer function.

Unipolar Offset Error
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(–) + 1/2 LSB).

Positive Full-Scale Error
This is the deviation of the last code transition from the ideal AIN(+) voltage (AIN(–) + Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of crosstalk between the channels. It is measured by applying a full-scale 25 kHz signal to the other seven channels and determining how much that signal is attenuated in the channel of interest. The figure given is the worst case for all channels.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

Thus for a 14-bit converter, this is 86 dB.

NOTE
[1]AIN(+) refers to the positive input of the pseudo-differential pair, and AIN(–) refers to the negative analog input of the pseudo-differential pair or to AGND depending on the channel configuration.

Total Harmonic Distortion
Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7856, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Full Power Bandwidth
The Full Power Bandwidth (FPBW) of the AD7856 is that frequency at which the amplitude of the reconstructed (using FFTs) fundamental (neglecting harmonics and SNR) is reduced by 3 dB for a full-scale input.

ON-CHIP REGISTERS

The AD7856 powers up with a set of default conditions. The only writing that is required is to select the channel configuration. Without performing any other write operations the AD7856 still retains the flexibility for performing a full power-down, and a full self-calibration.

Extra features and flexibility such as performing different power-down options, different types of calibrations including system calibration, and software conversion start can be selected by further writing to the part.

The AD7856 contains a **Control Register, ADC Output Data Register, Status Register, Test Register** and ten **Calibration Registers**. The control register is write only, the ADC output data register and the status register are read only, and the test and calibration registers are both read/write registers. The Test Register is used for testing the part and should not be written to.

Addressing the On-Chip Registers

Writing

A write operation to the AD7856 consists of 16 bits. The two MSBs, ADDR0 and ADDR1, are decoded to determine which register is addressed, and the subsequent 14 bits of data are written to the addressed register. It is not until all 16 bits are written that the data is latched into the addressed registers. Table I shows the decoding of the address bits while Figure 4 shows the overall write register hierarchy.

Table I. Write Register Addressing

ADDR1	ADDR0	Comment
0	0	This combination does not address any register so the subsequent 14 data bits are ignored.
0	1	This combination addresses the TEST REGISTER. The subsequent 14 data bits are written to the test register.
1	0	This combination addresses the CALIBRATION REGISTERS. The subsequent 14 data bits are written to the selected calibration register.
1	1	This combination addresses the CONTROL REGISTER. The subsequent 14 data bits are written to the control register.

Reading

To read from the various registers the user must first write to Bits 6 and 7 in the Control Register, RDSLT0 and RDSLT1. These bits are decoded to determine which register is addressed during a read operation. Table II shows the decoding of the read address bits while Figure 5 shows the overall read register hierarchy. The power-up status of these bits is 00 so that the default read will be from the ADC output data register.

Once the read selection bits are set in the Control Register, all subsequent read operations that follow will be from the selected register until the read selection bits are changed in the Control Register.

Table II. Read Register Addressing

RDSLT1	RDSLT0	Comment
0	0	All successive read operations will be from ADC OUTPUT DATA REGISTER. This is the power-up default setting. There will always be two leading zeros when reading from the ADC Output Data Register.
0	1	All successive read operations will be from TEST REGISTER.
1	0	All successive read operations will be from CALIBRATION REGISTERS.
1	1	All successive read operations will be from STATUS REGISTER.

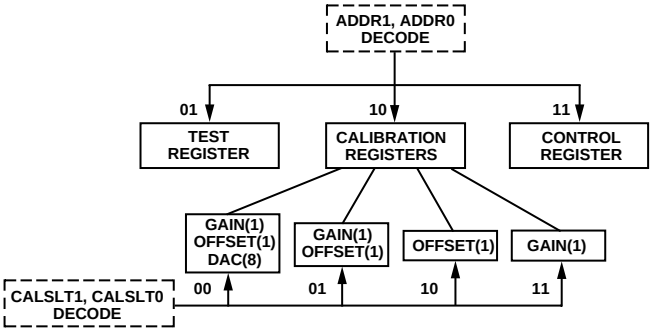


Figure 4. Write Register Hierarchy/Address Decoding

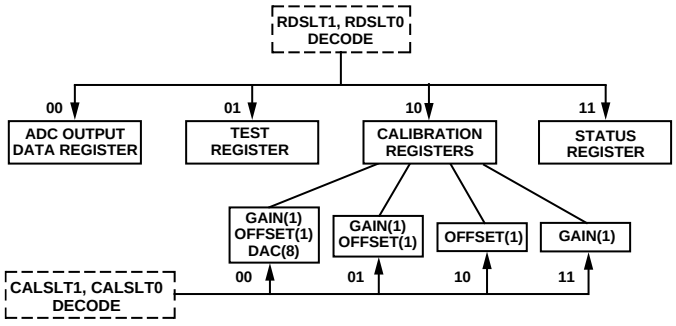


Figure 5. Read Register Hierarchy/Address Decoding

CONTROL REGISTER

The arrangement of the Control Register is shown below. The control register is a write only register and contains 14 bits of data. The control register is selected by putting two 1s in ADDR1 and ADDR0. The function of the bits in the control register are described below. The power-up status of all bits is 0.

MSB

SGL/$\overline{\text{DIFF}}$	**CH2**	**CH1**	**CH0**	**PMGT1**	**PMGT0**	**RDSLT1**
RDSLT0	**2/$\overline{3}$ MODE**	**CONVST**	**CALMD**	**CALSLT1**	**CALSLT0**	**STCAL**

LSB

CONTROL REGISTER BIT FUNCTION DESCRIPTION

Bit	Mnemonic	Comment
13	SGL/$\overline{\text{DIFF}}$	A 0 in this bit position configures the input channels in pseudo-differential mode. A 1 in this bit position configures the input channels in single-ended mode (see Table III).
12 11 10	CH2 CH1 CH0	These three bits are used to select the channel on which the conversion is performed. The channels can be configured as eight single-ended channels or four pseudo-differential channels. The default selection is AIN1 for the positive input and AIN2 for the negative input (see Table III for channel selection).
9 8	PMGT1 PMGT0	Power Management Bits. These two bits are used with the $\overline{\text{SLEEP}}$ pin for putting the part into various power-down modes (see Power-Down section for more details).
7 6	RDSLT1 RDSLT0	These two bits determine which register is addressed for the read operations (see Table II).
5	2/$\overline{3}$ MODE	Interface Mode Select Bit. With this bit set to 0, Interface Mode 2 is enabled. With this bit set to 1, Interface Mode 1 is enabled where DIN is used as an output as well as an input. This bit is set to 0 by default after every read cycle; thus when using the Two-Wire Interface Mode, this bit needs to be set to 1 in every write cycle.
4	CONVST	Conversion Start Bit. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of conversion. This bit may also used in conjunction with system calibration (see Calibration section.)
3	CALMD	Calibration Mode Bit. A 0 here selects self-calibration, and a 1 selects a system calibration (see Table IV).
2 1 0	CALSLT1 CALSLT0 STCAL	Calibration Selection Bits and Start Calibration Bit. These bits have two functions. With the STCAL bit set to 1 the CALSLT1 and CALSLT0 bits determine the type of calibration performed by the part (see Table IV). The STCAL bit is automatically reset to 0 at the end of calibration. With the STCAL bit set to 0 the CALSLT1 and CALSLT0 bits are decoded to address the calibration register for read/write of calibration coefficients (see section on the Calibration Registers for more details).

Table III. Channel Selection

SGL/$\overline{\text{DIFF}}$	CH2	CH1	CH0	AIN(+)*	AIN(–)*
0	0	0	0	AIN_1	AIN_2
0	0	0	1	AIN_3	AIN_4
0	0	1	0	AIN_5	AIN_6
0	0	1	1	AIN_7	AIN_8
0	1	0	0	AIN_2	AIN_1
0	1	0	1	AIN_4	AIN_3
0	1	1	0	AIN_6	AIN_5
0	1	1	1	AIN_8	AIN_7
1	0	0	0	AIN_1	AGND
1	0	0	1	AIN_3	AGND
1	0	1	0	AIN_5	AGND
1	0	1	1	AIN_7	AGND
1	1	0	0	AIN_2	AGND
1	1	0	1	AIN_4	AGND
1	1	1	0	AIN_6	AGND
1	1	1	1	AIN_8	AGND

*AIN(+) refers to the positive input seen by the AD7856 sample and hold circuit.
AIN(–) refers to the negative input seen by the AD7856 sample and hold circuit.

Table IV. Calibration Selection

CALMD	CALSLT1	CALSLT0	Calibration Type
0	0	0	A Full Internal Calibration is initiated where the Internal DAC is calibrated followed by the Internal Gain Error, and finally the Internal Offset Error is calibrated out. This is the default setting.
0	0	1	Here the Internal Gain Error is calibrated out followed by the Internal Offset Error calibrated out.
0	1	0	This calibrates out the Internal Offset Error only.
0	1	1	This calibrates out the Internal Gain Error only.
1	0	0	A Full System Calibration is initiated here where first the Internal DAC is calibrated followed by the System Gain Error, and finally the System Offset Error is calibrated out.
1	0	1	Here the System Gain Error is calibrated out followed by the System Offset Error.
1	1	0	This calibrates out the System Offset Error only.
1	1	1	This calibrates out the System Gain Error only.

STATUS REGISTER

The arrangement of the Status Register is shown below. The status register is a read only register and contains 16 bits of data. The status register is selected by first writing to the control register and putting two 1s in RDSLT1 and RDSLT0. The function of the bits in the status register are described below. The power-up status of all bits is 0.

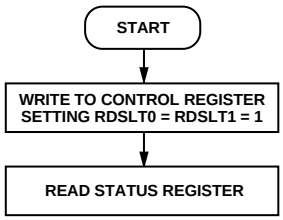


Figure 6. Flowchart for Reading the Status Register

MSB

ZERO	**BUSY**	**SGL/$\overline{\text{DIFF}}$**	**CH2**	**CH1**	**CH0**	**PMGT1**	**PMGT0**
RDSLT1	**RDSLT0**	**2/$\overline{3}$ MODE**	**X**	**CALMD**	**CALSLT1**	**CALSLT0**	**STCAL**

LSB

STATUS REGISTER BIT FUNCTION DESCRIPTION

Bit	Mnemonic	Comment
15	ZERO	This bit is always 0.
14	BUSY	Conversion/Calibration Busy Bit. When this bit is 1 it indicates that there is a conversion or calibration in progress. When this bit is 0, there is no conversion or calibration in progress.
13	SGL/$\overline{\text{DIFF}}$	These four bits indicate the channel which is selected for conversion (see Table III).
12	CH2	
11	CH1	
10	CH0	
9	PMGT1	Power management bits. These bits, along with the $\overline{\text{SLEEP}}$ pin, will indicate if the part is in a power-down mode or not. See Table VI for description.
8	PMGT0	
7	RDSLT1	Both of these bits are always 1, indicating it is the status register which is being read (see Table II).
6	RDSLT0	
5	2/$\overline{3}$ MODE	Interface Mode Select Bit. With this bit at 0, the device is in Interface Mode 2. With this bit at 1, the device is in Interface Mode 1. This bit is reset to 0 after every read cycle.
4	X	Don't care bit.
3	CALMD	Calibration Mode Bit. A 0 in this bit indicates a self calibration is selected, and a 1 in this bit indicates a system calibration is selected (see Table IV).
2	CALSLT1	Calibration Selection Bits and Start Calibration Bit. The STCAL bit is read as a 1 if a calibration is in progress and as a 0 if there is no calibration in progress. The CALSLT1 and CALSLT0 bits indicate which of the calibration registers are addressed for reading and writing (see section on the Calibration Registers for more details).
1	CALSLT0	
0	STCAL	

CALIBRATION REGISTERS

The AD7856 has ten calibration registers in all, eight for the DAC, one for the offset and one for gain. Data can be written to or read from all ten calibration registers. In self- and system calibration the part automatically modifies the calibration registers; only if the user needs to modify the calibration registers should an attempt be made to read from and write to the calibration registers.

Addressing the Calibration Registers

The calibration selection bits in the control register CALSLT1 and CALSLT0 determine which of the calibration registers are addressed (see Table V). The addressing applies to both the read and write operations for the calibration registers. The user should not attempt to read from and write to the calibration registers at the same time.

Table V. Calibration Register Addressing

CALSLT1	CALSLT0	Comment
0	0	This combination addresses the Gain (1), Offset (1) and DAC Registers (8). Ten registers in total.
0	1	This combination addresses the Gain (1) and Offset (1) Registers. Two registers in total.
1	0	This combination addresses the Offset Register. One register in total.
1	1	This combination addresses the Gain Register. One register in total.

Writing to/Reading from the Calibration Registers

For writing to the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits. For reading from the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits, but also to set the RDSLT1 and RDSLT0 bits to 10 (this addresses the calibration registers for reading). The calibration register pointer is reset upon writing to the control register setting the CALSLT1 and CALSLT0 bits, or upon completion of all the calibration register write/read operations. When reset, it points to the first calibration register in the selected write/read sequence. The calibration register pointer will point to the gain calibration register upon reset in all but one case, this case being where the offset calibration register is selected on its own (CALSLT1 = 1, CALSLT0 = 0). Where more than one calibration register is being accessed the calibration register pointer will be automatically incremented after each calibration register write/read operation. The order in which the ten calibration registers are arranged is shown in Figure 7. The user may abort at any time before all the calibration register write/read operations are completed, and the next control register write operation will reset the calibration register pointer. The flowchart in Figure 8 shows the sequence for writing to the calibration registers and Figure 9 for reading.

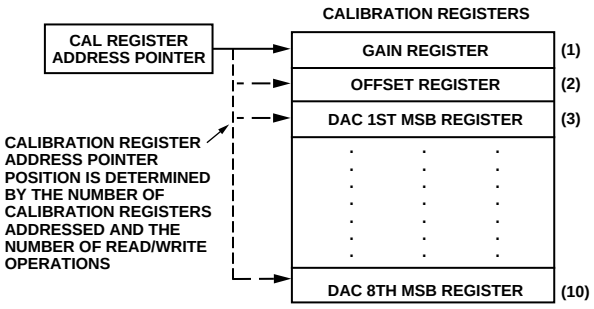


Figure 7. Calibration Register Arrangements

When reading from the calibration registers there will always be two leading zeros for each of the registers. When operating in Serial Interface Mode 1 the read operations to the calibration registers cannot be aborted. The full number of read operations must be completed (see section on Serial Interface Mode 1 Timing for more detail).

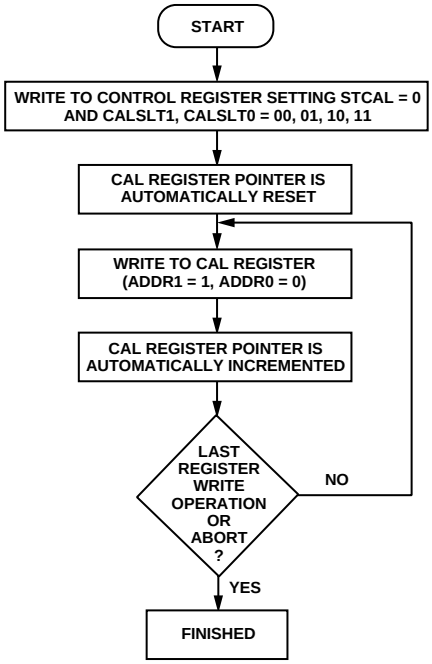


Figure 8. Flowchart for Writing to the Calibration Registers

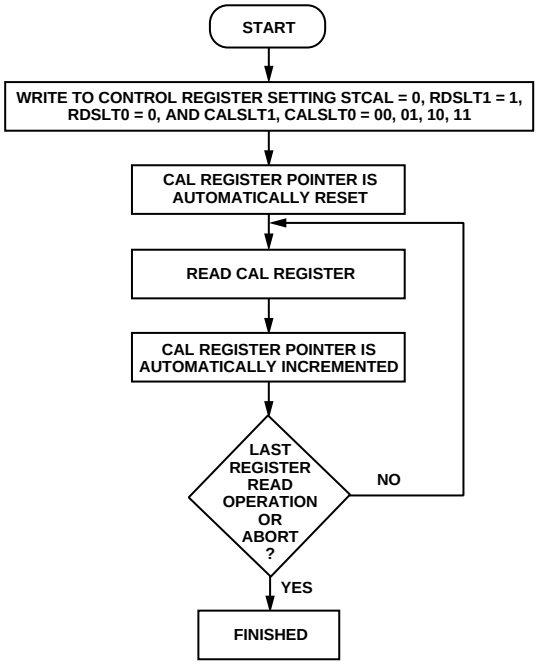


Figure 9. Flowchart for Reading from the Calibration Registers

Adjusting the Offset Calibration Register

The offset calibration register contains 16 bits, two leading zeros and 14 data bits. By changing the contents of the offset register different amounts of offset on the analog input signal can be compensated for. Increasing the number in the offset calibration register compensates for negative offset on the analog input signal, and decreasing the number in the offset calibration register compensates for positive offset on the analog input signal. The default value of the offset calibration register is approximately 0010 0000 0000 0000. This is not an exact value, but the value in the offset register should be close to this value. Each of the 14 data bits in the offset register is binary weighted: the MSB has a weighting of 5% of the reference voltage, the MSB-1 has a weighting of 2.5%, the MSB-2 has a weighting of 1.25%, and so on down to the LSB, which has a weighting of 0.0006%. This gives a resolution of approximately ±0.0006% of V_{REF}. More accurately the resolution is $\pm(0.05 \times V_{REF})/2^{13}$ volts = ±0.015 mV, with a 2.5 V reference. The maximum specified offset that can be compensated for is ±3.75% of the reference voltage but is typically ±5%, which equates to ±125 mV with a 2.5 V reference and ±250 mV with a 5 V reference.

Q. If a +20 mV offset is present in the analog input signal and the reference voltage is 2.5 V, what code needs to be written to the offset register to compensate for the offset?

A. 2.5 V reference implies that the resolution in the offset register is $5\% \times 2.5\ V/2^{13}$ = 0.015 mV. +20 mV/0.015 mV = 1310.72; rounding to the nearest number gives 1311. In binary terms this is 0101 0001 1111. Therefore, decrease the offset register by 0101 0001 1111.

This method of compensating for offset in the analog input signal allows for fine tuning the offset compensation. If the offset on the analog input signal is known, there will be no need to apply the offset voltage to the analog input pins and do a system calibration. The offset compensation can take place in software.

Adjusting the Gain Calibration Register

The gain calibration register contains 16 bits, two leading 0s and 14 data bits. The data bits are binary weighted as in the offset calibration register. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register compensates for a smaller analog input range and decreasing the gain register compensates for a larger input range. The maximum analog input range for which the gain register can compensate is 1.01875 times the reference voltage; the minimum input range is 0.98125 times the reference voltage.

CIRCUIT INFORMATION

The AD7856 is a fast, 14-bit single supply A/D converter. The part requires an external 6 MHz/4 MHz master clock (CLKIN), two C_{REF} capacitors, a $\overline{\text{CONVST}}$ signal to start conversion and power supply decoupling capacitors. The part provides the user with track/hold, on-chip reference, calibration features, A/D converter and serial interface logic functions on a single chip. The A/D converter section of the AD7856 consists of a conventional successive-approximation converter based around a capacitor DAC. The AD7856 accepts an analog input range of 0 to $+V_{DD}$ where the reference can be tied to V_{DD}. The reference input to the part is buffered on-chip.

A major advantage of the AD7856 is that a conversion can be initiated in software as well as applying a signal to the $\overline{\text{CONVST}}$ pin. Another innovative feature of the AD7856 is self-calibration on power-up, which is initiated having a 0.01 μF capacitor from the $\overline{\text{CAL}}$ pin to DGND, to give superior dc accuracy. The part should be allowed 150 ms after power up to perform this automatic calibration before any reading or writing takes place. The part is available in a 24-pin SSOP package and this offers the user considerable spacing saving advantages over alternative solutions.

CONVERTER DETAILS

The master clock for the part must be applied to the CLKIN pin. Conversion is initiated on the AD7856 by pulsing the $\overline{\text{CONVST}}$ input or by writing to the control register and setting the CONVST bit to 1. On the rising edge of $\overline{\text{CONVST}}$ (or at the end of the control register write operation), the on-chip track/hold goes from track to hold mode. The falling edge of the CLKIN signal that follows the rising edge of the $\overline{\text{CONVST}}$ signal initiates the conversion, provided the rising edge of $\overline{\text{CONVST}}$ occurs at least 10 ns typically before this CLKIN edge. The conversion cycle will take 20 CLKIN periods from this CLKIN falling edge. If the 10 ns setup time is not met, the conversion will take 21 CLKIN periods. The maximum specified conversion time is 3.5 μs (6 MHz) 5.25 μs (4 MHz) for the AD7856. When a conversion is completed, the BUSY output goes low, and then the result of the conversion can be read by accessing the data through the serial interface. To obtain optimum performance from the part, the read operation should not occur during the conversion or 500 ns prior to the next $\overline{\text{CONVST}}$ rising edge. However, the maximum throughput rates are achieved by reading/writing during conversion, and reading/writing during conversion is likely to degrade the Signal to (Noise + Distortion) by only 0.5 dBs. The AD7856 can operate at throughput rates up to 285 kHz. For the AD7856 a conversion takes 21 CLKIN periods; two CLKIN periods are needed for the acquisition time, giving a full cycle time of 3.66 μs (= 260 kHz, CLKIN = 6 MHz). When using the software conversion start for maximum throughput the user must ensure the control register write operation extends beyond the falling edge of BUSY. The falling edge of BUSY resets the $\overline{\text{CONVST}}$ bit to 0 and allows it to be reprogrammed to 1 to start the next conversion.

TYPICAL CONNECTION DIAGRAM

Figure 10 shows a typical connection diagram for the AD7856. The AGND and DGND pins are connected together at the device for good noise suppression. The $\overline{\text{CAL}}$ pin has a 0.01 μF capacitor to enable an automatic self-calibration on power-up. The conversion result is output in a 16-bit word with two leading zeros followed by the MSB of the 14-bit result. Note that after the AV_{DD} and DV_{DD} power-up the part will require 150 ms for the internal reference to settle and for the automatic calibration on power-up to be completed.

For applications where power consumption is a major concern the $\overline{\text{SLEEP}}$ pin can be connected to DGND. See Power-Down section for more detail on low power applications.

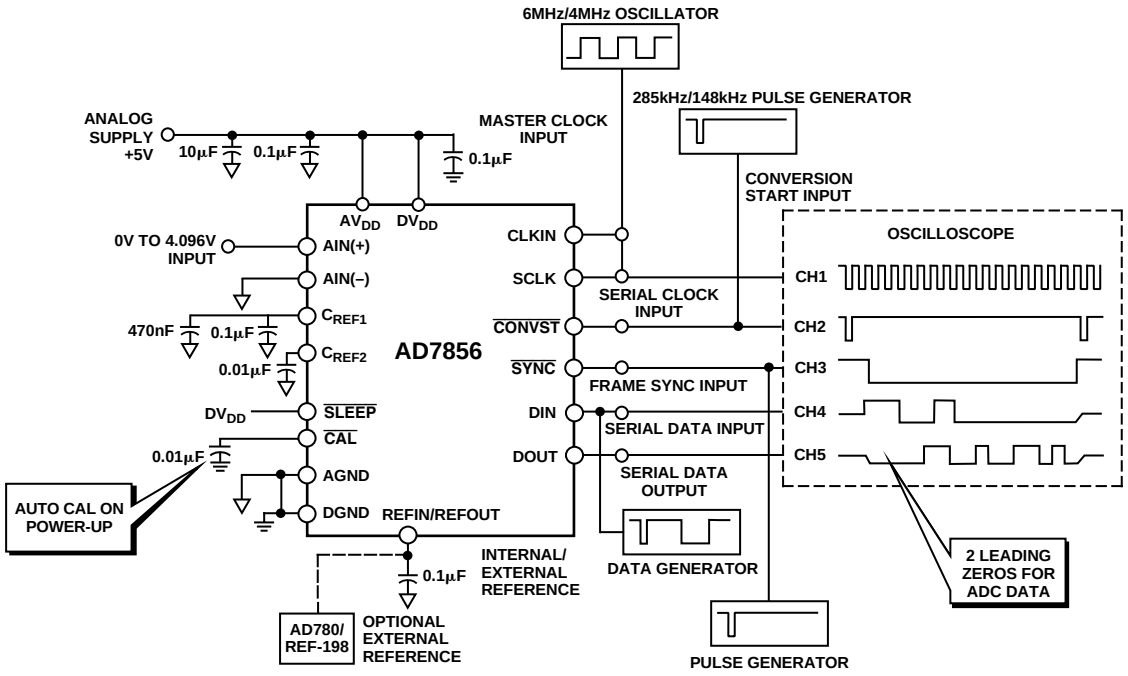


Figure 10. Typical Circuit

ANALOG INPUT

The equivalent circuit of the analog input section is shown in Figure 11. During the acquisition interval the switches are both in the track position and the AIN(+) charges the 20 pF capacitor through the 125 Ω resistance. On the rising edge of $\overline{\text{CONVST}}$ switches SW1 and SW2 go into the hold position retaining charge on the 20 pF capacitor as a sample of the signal on AIN(+). The AIN(–) is connected to the 20 pF capacitor, and this unbalances the voltage at node A at the input of the comparator. The capacitor DAC adjusts during the remainder of the conversion cycle to restore the voltage at node A to the correct value. This action transfers a charge, representing the analog input signal, to the capacitor DAC which in turn forms a digital representation of the analog input signal. The voltage on the AIN(–) pin directly influences the charge transferred to the capacitor DAC at the hold instant. If this voltage changes during the conversion period, the DAC representation of the analog input voltage will be altered. Therefore it is most important that the voltage on the AIN(–) pin remains constant during the conversion period. Furthermore, it is recommended that the AIN(–) pin is always connected to AGND or to a fixed dc voltage.

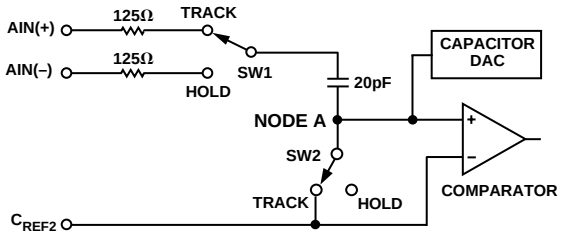


Figure 11. Analog Input Equivalent Circuit

Acquisition Time

The track and hold amplifier enters its tracking mode on the falling edge of the BUSY signal. The time required for the track and hold amplifier to acquire an input signal will depend on how quickly the 20 pF input capacitance is charged. The acquisition time is calculated using the formula:

$$t_{ACQ} = 10 \times (R_{IN} + 125\ \Omega) \times 20\ pF$$

where R_{IN} is the source impedance of the input signal, and 125 Ω, 20 pF is the input RC.

DC/AC Applications

For dc applications high source impedances are acceptable provided there is enough acquisition time between conversions to charge the 20 pF capacitor. The acquisition time can be calculated from the above formula for different source impedances. For example, with R_{IN} = 5 kΩ the required acquisition time will be 1025 ns.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the AIN(+) pin as shown in Figure 13. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 12 shows a graph of the total harmonic distortion versus analog input signal frequency for different source impedances. With the setup as in Figure 13, the THD is at the –90 dB level. With a source impedance of 1 kΩ and no capacitor on the AIN(+) pin, the THD increases with frequency.

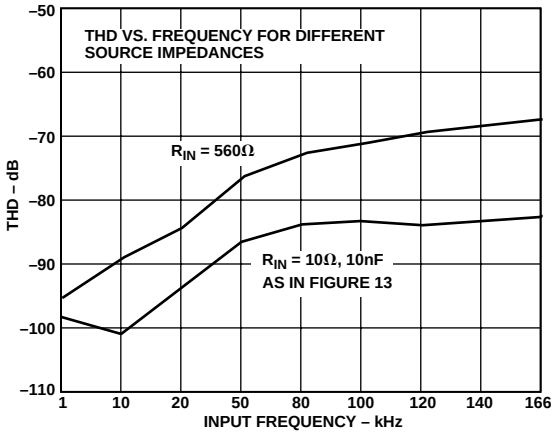


Figure 12. THD vs. Analog Input Frequency

In a single supply application (5 V), the V+ and V– of the op amp can be taken directly from the supplies to the AD7856 which eliminates the need for extra external power supplies. When operating with rail-to-rail inputs and outputs, at frequencies greater than 10 kHz care must be taken in selecting the particular op amp for the application. In particular for single supply applications the input amplifiers should be connected in a gain of –1 arrangement to get the optimum performance. Figure 13 shows the arrangement for a single supply application with a 50 Ω and 10 nF low-pass filter (cutoff frequency 320 kHz) on the AIN(+) pin. Note that the 10 nF is a capacitor with good linearity to ensure good ac performance. Recommended single supply op amp is the AD820.

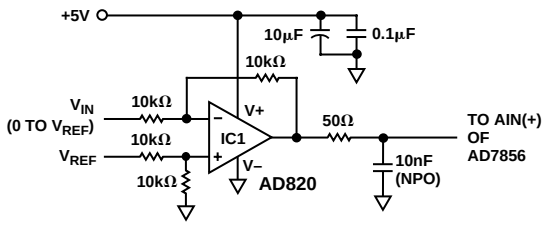


Figure 13. Analog Input Buffering

Input Range

The analog input range for the AD7856 is 0 V to V_{REF}. The AIN(–) pin on the AD7856 can be biased up above AGND, if required. The advantage of biasing the lower end of the analog input range away from AGND is that the user does not need to have the analog input swing all the way down to AGND. This has the advantage in true single supply applications that the input amplifier does not need to swing all the way down to AGND. The upper end of the analog input range is shifted up by the same amount. Care must be taken so that the bias applied does not shift the upper end of the analog input above the AV_{DD} supply. In the case where the reference is the supply, AV_{DD}, the AIN(–) must be tied to AGND.

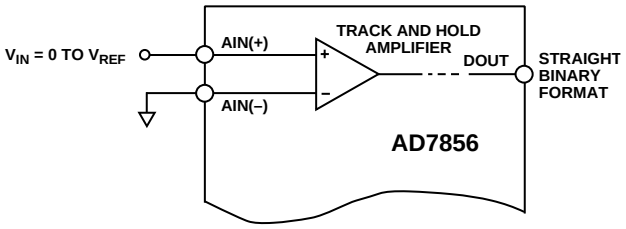


Figure 14. 0 to V_{REF} Input Configuration

Transfer Function

For the AD7856 input range the designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS – 3/2 LSBs). The output coding is straight binary, with 1 LSB = FS/16384 = 4.096 V/16384 = 0.25 mV when V_{REF} = 4.096 V. The ideal input/output transfer characteristic is shown in Figure 15.

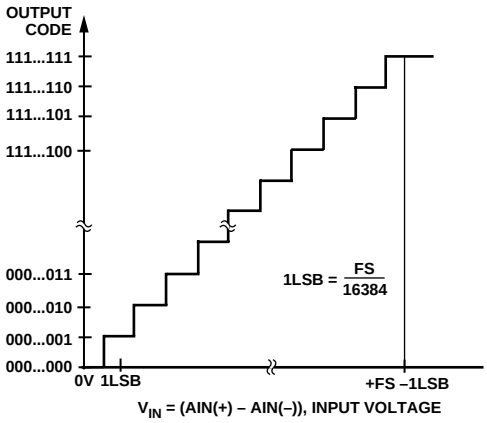


Figure 15. Transfer Characteristic

REFERENCE SECTION

For specified performance, it is recommended that when using an external reference this reference should be between 4 V and the analog supply AV_{DD}. The connections for the relevant reference pins are shown in the typical connection diagrams. If the internal reference is being used, the REF_{IN}/REF_{OUT} pin should have a 100 nF capacitor connected to AGND very close to the REF_{IN}/REF_{OUT} pin. These connections are shown in Figure 16.

If the internal reference is required for use external to the ADC, it should be buffered at the REF_{IN}/REF_{OUT} pin and a 100 nF capacitor connected from this pin to AGND. The typical noise performance for the internal reference, with 5 V supplies is 150 nV/$\sqrt{\text{Hz}}$ @ 1 kHz and dc noise is 100 μV p-p.

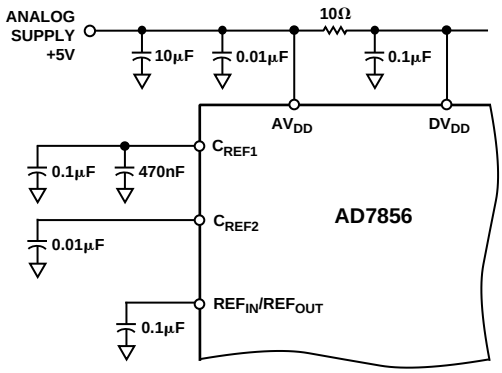


Figure 16. Relevant Connections When Using Internal Reference

The other option is that the REF_{IN}/REF_{OUT} pin be overdriven by connecting it to an external reference. This is possible due to the series resistance from the REF_{IN}/REF_{OUT} pin to the internal reference. This external reference can have a range that includes AV_{DD}. When using AV_{DD} as the reference source or when an externally applied reference approaches AV_{DD}, the 100 nF capacitor from the REF_{IN}/REF_{OUT} pin to AGND should be as close as possible to the REF_{IN}/REF_{OUT} pin, and also the C_{REF1} pin should be connected to AV_{DD} to keep this pin at the same level as the reference. The connections for this arrangement are shown in Figure 17. When using AV_{DD} it may be necessary to add a resistor in series with the AV_{DD} supply. This will have the effect of filtering the noise associated with the AV_{DD} supply.

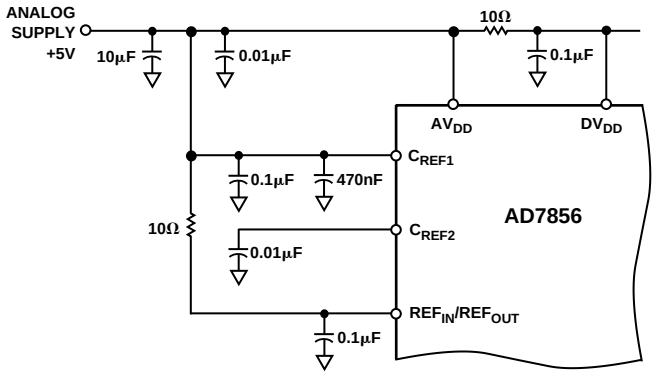


Figure 17. Relevant Connections When Using AV_{DD} as the Reference

PERFORMANCE CURVES

The following performance curves apply to Mode 2 operation only. If a conversion is initiated in software, then a slight degradation in SNR can be expected when in Mode 2 operation. As the sampling instant cannot be guaranteed internally, nonequidistant sampling will occur, resulting in a rise in the noise floor. Initiating conversions in software is not recommended for Mode 1 operation.

Figure 18 shows a typical FFT plot for the AD7856 at 190 kHz sample rate and 10 kHz input frequency.

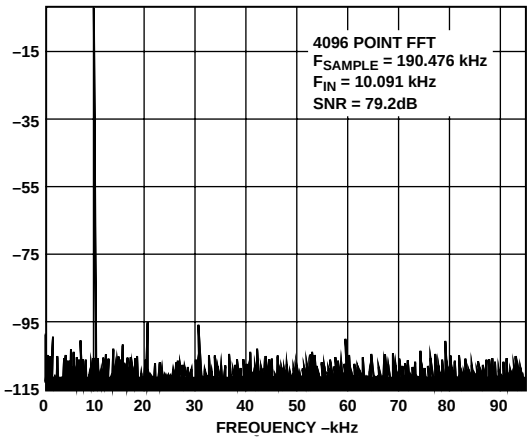


Figure 18. FFT Plot

Figure 19 shows the SNR vs. Frequency for 5 V supply and a 4.096 external reference (5 V reference is typically 1 dB better performance).

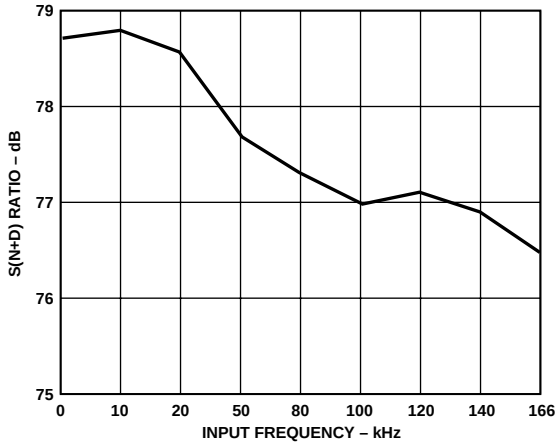


Figure 19. SNR vs. Frequency

Figure 20 shows the Power Supply Rejection Ratio versus Frequency for the part. The Power Supply Rejection Ratio is defined as the ratio of the power in ADC output at frequency f to the power of a full-scale sine wave.

$$PSRR\ (dB) = 10 \log (Pf/Pfs)$$

Pf = Power at frequency f in ADC output, *Pfs* = power of a full-scale sine wave. Here a 100 mV peak-to-peak sine wave is coupled onto the AV_{DD} supply while the digital supply is left unaltered.

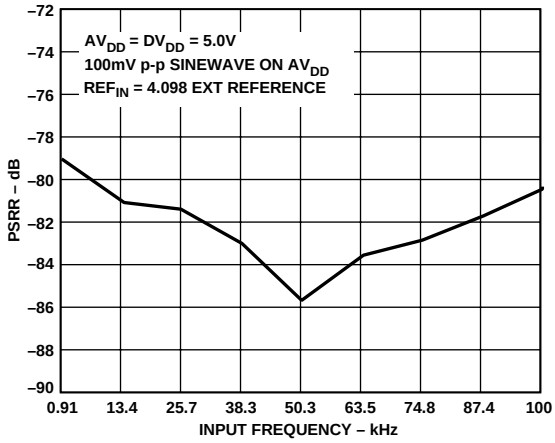


Figure 20. PSRR vs. Frequency

POWER-DOWN OPTIONS

The AD7856 provides flexible power management to allow the user to achieve the best power performance for a given throughput rate. The power management options are selected by programming the power management bits, PMGT1 and PMGT0, in the control register and by use of the $\overline{SLEEP}$ pin. Table VI summarizes the power-down options that are available and how they can be selected by using either software, hardware or a combination of both. The AD7856 can be fully or partially powered down. When fully powered down, all the on-chip circuitry is powered down and I_{DD} is 1 μA typ. If a partial power-down is selected, then all the on-chip circuitry except the reference is powered down and I_{DD} is 400 μA typ. The choice of full or partial power-down does not give any significant improvement in throughput with a power-down between conversions. This is discussed in the next section–Power-Up Times. However, a partial power-down does allow the on-chip reference to be used externally even though the rest of the AD7856 circuitry is powered down. It also allows the AD7856 to be powered up faster after a long power-down period when using the on-chip reference (See Power-Up Times–Using On-Chip Reference).

When using the $\overline{SLEEP}$ pin, the power management bits PMGT1 and PMGT0 should be set to zero (default status on power-up). Bringing the $\overline{SLEEP}$ pin logic high ensures normal operation, and the part does not power down at any stage. This may be necessary if the part is being used at high throughput rates when it is not possible to power down between conversions. If the user wishes to power down between conversions at lower throughput rates (i.e. <100 kSPS for the AD7856) to achieve better power performances, then the $\overline{SLEEP}$ pin should be tied logic low.

If the power-down options are to be selected in software only, then the $\overline{SLEEP}$ pin should be tied logic high. By setting the power management bits PMGT1 and PMGT0 as shown in Table VI, a Full Power-Down, Full Power-Up, Full Power-Down Between Conversions, and a Partial Power-Down Between Conversions can be selected.

A combination of hardware and software selection can also be used to achieve the desired effect.

Table VI. Power Management Options

PMGT1 Bit	PMGT0 Bit	$\overline{\text{SLEEP}}$ Pin	Comment
0	0	0	Full Power-Down Between Conversions (HW/SW)
0	0	1	Full Power-Up (HW/SW)
0	1	X	Normal Operation (Independent of the $\overline{\text{SLEEP}}$ Pin)
1	0	X	Full Power-Down (SW)
1	1	X	Partial Power-Down Between Conversions

NOTE
HW = Hardware Selection; SW = Software Selection.

POWER-UP TIMES

Using an External Reference

When the AD7856 is powered up, the part is powered up from one of two conditions. First, when the power supplies are initially powered up and, secondly, when the part is powered up from either a hardware or software power-down (see last section).

When AV_{DD} and DV_{DD} are powered up, the AD7856 should be left idle for approximately 42 ms (6 MHz CLK) to allow for the autocalibration if a 10 nF cap is placed on the $\overline{\text{CAL}}$ pin, (see Calibration section). During power-up the functionality of the $\overline{\text{SLEEP}}$ pin is disabled, i.e., the part will not power down until the end of the calibration if $\overline{\text{SLEEP}}$ is tied logic low. The autocalibration on power-up can be disabled if the $\overline{\text{CAL}}$ pin is tied to a logic high. If the autocalibration is disabled, then the user must take into account the time required by the AD7856 to power-up before a self-calibration is carried out. This power-up time is the time taken for the AD7856 to power up when power is first applied (300 μs) typ) or the time it takes the external reference to settle to the 14-bit level–whichever is the longer.

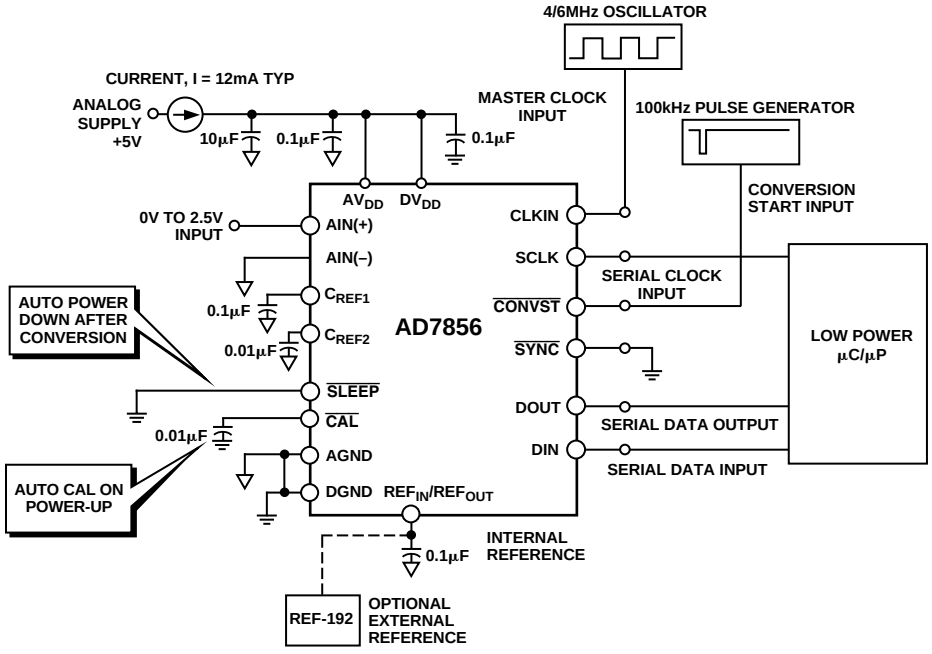


Figure 21. Typical Low Power Circuit

The AD7856 powers up from a full hardware or software power-down in 5 µs typ. This limits the throughput which the part is capable of to 93 kSPS for the K grade and 113 kSPS for the A grade when powering down between conversions. Figure 22 shows how power-down between conversions is implemented using the $\overline{\text{CONVST}}$ pin. The user first selects the power-down between conversions option by using the $\overline{\text{SLEEP}}$ pin and the power management bits, PMGT1 and PMGT0, in the control register, (see last section). In this mode the AD7856 automatically enters a full power-down at the end of a conversion, i.e., when BUSY goes low. The falling edge of the next $\overline{\text{CONVST}}$ pulse causes the part to power up. Assuming the external reference is left powered up, the AD7856 should be ready for normal operation 5 µs after this falling edge. The rising edge of $\overline{\text{CONVST}}$ initiates a conversion so the $\overline{\text{CONVST}}$ pulse should be at least 5 µs wide. The part automatically powers down on completion of the conversion.

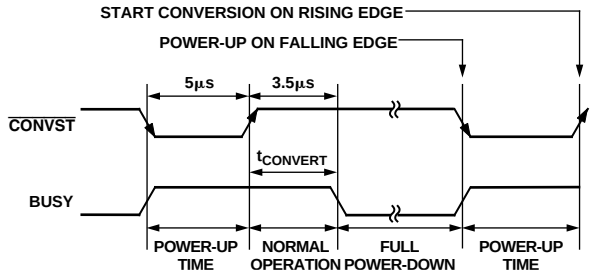


Figure 22. Power-Up Timing When Using $\overline{\text{CONVST}}$ Pin

NOTE: Where the software $\overline{\text{CONVST}}$ is used, the part must be powered up in software with an extra write setting PMGT1 = 0 and PMGT0 = 1 before a conversion is initiated in the next write. Automatic partial power-down after a calibration is not possible; the part must be powered down manually. If software calibrations are to be used when operating in the partial power-down mode, then three separate writes are required. The first initiates the type of calibration required, the second write powers the part down into partial power-down mode, while the third write powers the part up again before the next calibration command is issued.

Using the Internal (On-Chip) Reference

As in the case of an external reference, the AD7856 can power-up from one of two conditions, power-up after the supplies are connected or power-up from hardware/software power-down. When using the on-chip reference and powering up when AV_{DD} and DV_{DD} are first connected, it is recommended that the power-up calibration mode be disabled as explained above. When using the on-chip reference, the power-up time is effectively the time it takes to charge up the external capacitor on the REF_{IN}/REF_{OUT} pin. This time is given by the equation:

$$t_{UP} = 10 \times R \times C$$

where $R \cong 150\ k\Omega$ and C = external capacitor.

The recommended value of the external capacitor is 100 nF; this gives a power-up time of approximately 150 ms before a calibration is initiated and normal operation should commence.

When C_{REF} is fully charged, the power-up time from a hardware or software power-down reduces to 5 µs. This is because an internal switch opens to provide a high impedance discharge path for the reference capacitor during power-down—see Figure 23. An added advantage of the low charge leakage from the reference capacitor during power-down is that even though the reference is being powered down between conversions, the reference capacitor holds the reference voltage to within 0.5 LSBs with throughput rates of 100 samples/second and over with a full power-down between conversions. A high input impedance op amp like the AD707 should be used to buffer this reference capacitor if it is being used externally. Note, if the AD7856 is left in its power-down state for more than 100 ms, the charge on C_{REF} will start to leak away and the power-up time will increase. If this long power-up time is a problem, the user can use a partial power-down for the last conversion so the reference remains powered up.

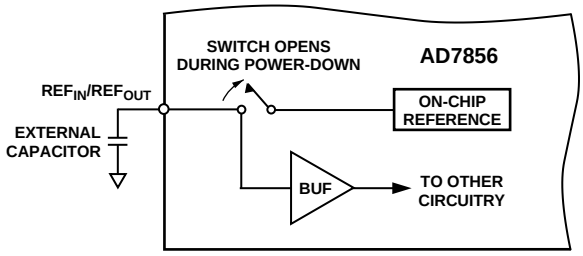


Figure 23. On-Chip Reference During Power-Down

POWER VS. THROUGHPUT RATE

The main advantage of a full power-down after a conversion is that it significantly reduces the power consumption of the part at lower throughput rates. When using this mode of operation the AD7856 is only powered up for the duration of the conversion. If the power-up time of the AD7856 is taken to be 5 µs and it is assumed that the current during power up is 12 mA typ, then power consumption as a function of throughput can easily be calculated. The AD7856 has a conversion time of 3.5 µs with a 6 MHz external clock. This means the AD7856 consumes 12 mA typ, (or 60 mW typ V_{DD} = 5 V) for 8.5 µs in every conversion cycle if the device is powered down at the end of a conversion. If the throughput rate is 1 kSPS, the cycle time is 1000 µs and the average power dissipated during each cycle is (8.5/1000) × (60 mW) = 510 µW. The graph, Figure 24, shows the power consumption of the AD7856 as a function of throughput. Table VII lists the power consumption for various throughput rates.

Table VII. Power Consumption vs. Throughput

Throughput Rate	Power
1 kSPS	510 µW
10 kSPS	5.1 mW

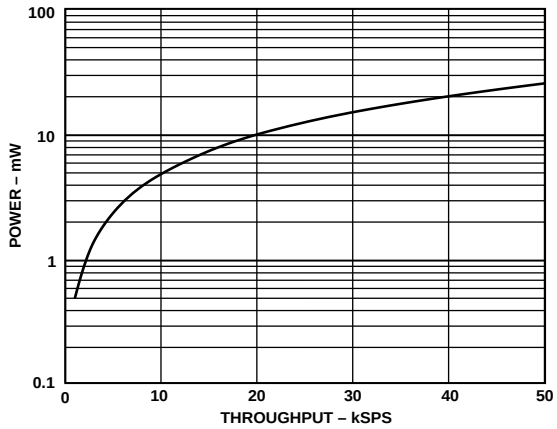


Figure 24. Power vs. Throughput Rate (6 MHz CLK)

CALIBRATION SECTION

Calibration Overview

The automatic calibration that is performed on power up ensures that the calibration options covered in this section will not be required in a significant amount of applications. The user will not have to initiate a calibration unless the operating conditions change (CLKIN frequency, analog input mode, reference voltage, temperature, and supply voltages). The AD7856 has a number of calibration features that may be required in some applications and there are a number of advantages in performing these different types of calibration. First, the internal errors in the ADC can be reduced significantly to give superior dc performance, and secondly, system offset and gain errors can be removed. This allows the user to remove reference errors (whether it be internal or external reference) and to make use of the full dynamic range of the AD7856 by adjusting the analog input range of the part for a specific system.

There are two main calibration modes on the AD7856, self-calibration and system calibration. There are various options in both self-calibration and system calibration as outlined previously in Table IV. All the calibration functions can be initiated by pulsing the $\overline{\text{CAL}}$ pin or by writing to the control register and setting the STCAL bit to one. The timing diagrams that follow involve using the $\overline{\text{CAL}}$ pin.

The duration of each of the different types of calibrations is given in Table VIII for the AD7856 with a 6 MHz master clock. These calibration times are master clock dependent.

Table VIII. Calibration Times (AD7856 with 6 MHz CLKIN)

Type of Self- or System Calibration	Time
Full	41.7 ms
Offset + Gain	9.26 ms
Offset	4.63 ms
Gain	4.63 ms

Automatic Calibration on Power-On

The $\overline{\text{CAL}}$ pin has a 0.15 μA pull up current source connected to it internally to allow for an automatic full self-calibration on power-on. A full self-calibration will be initiated on power-on if a capacitor is connected from the $\overline{\text{CAL}}$ pin to DGND. The internal current source connected to the $\overline{\text{CAL}}$ pin charges up the external capacitor and the time required to charge the external capacitor will depend on the size of the capacitor itself. This time should be large enough to ensure that the internal reference is settled before the calibration is performed. A 33 nF capacitor is sufficient to ensure that the internal reference has settled (see Power-Up Times) before a calibration is initiated taking into account trigger level and current source variations on the $\overline{\text{CAL}}$ pin. However, if an external reference is being used, this reference must have stabilized before the automatic calibration is initiated (a larger capacitor on the $\overline{\text{CAL}}$ pin should be used if the external reference has not settled when the autocalibration is initiated). Once the capacitor on the $\overline{\text{CAL}}$ pin has charged, the calibration will be performed which will take 42 ms (6 MHz CLKIN). Therefore the autocalibration should be complete before operating the part. After calibration, the part is accurate to the 14-bit level and the specifications quoted on the data sheet apply. There will be no need to perform another calibration unless the operating conditions change or unless a system calibration is required.

Self-Calibration Description

There are four different calibration options within the self-calibration mode. First, there is a full self-calibration where the DAC, internal gain, and internal offset errors are calibrated out. Then, there is the (Gain + Offset) self-calibration which calibrates out the internal gain error and then the internal offset errors. The internal DAC is not calibrated here. Finally, there are the self-offset and self-gain calibrations which calibrate out the internal offset errors and the internal gain errors respectively.

The internal capacitor DAC is calibrated by trimming each of the capacitors in the DAC. It is the ratio of these capacitors to each other that is critical, and so the calibration algorithm ensures that this ratio is at a specific value by the end of the calibration routine. For the offset and gain there are two separate capacitors, one of which is trimmed when an offset or gain calibration is performed. Again, it is the ratio of these capacitors to the capacitors in the DAC that is critical and the calibration algorithm ensures that this ratio is at a specified value for both the offset and gain calibrations.

The zero-scale error is adjusted for an offset calibration, and the positive full-scale error is adjusted for a gain calibration.

Self-Calibration Timing

The diagram of Figure 25 shows the timing for a full self-calibration. Here the BUSY line stays high for the full length of the self-calibration. A self-calibration is initiated by bringing the $\overline{\text{CAL}}$ pin low (which initiates an internal reset) and then high again or by writing to the control register and setting the STCAL bit to 1 (*note that if the part is in a power-down mode the $\overline{CAL}$ pulse - width must take account of the power-up time*). The BUSY line is triggered high from the rising edge of $\overline{\text{CAL}}$ (or the end of the write to the control register if calibration is initiated in software), and BUSY will go low when the full-self calibration is complete after a time t_{CAL} as shown in Figure 25.

For the self- (gain + offset), self-offset and self-gain calibrations the BUSY line will be triggered high by the rising edge of the $\overline{\text{CAL}}$ signal (or the end of the write to the control register if calibration is initiated in software) and will stay high for the full duration of the self calibration. The length of time that the BUSY is high will depend on the type of self-calibration that

is initiated. Typical figures are given in Table VIII. The timing diagrams for the other self-calibration options will be similar to that outlined in Figure 25.

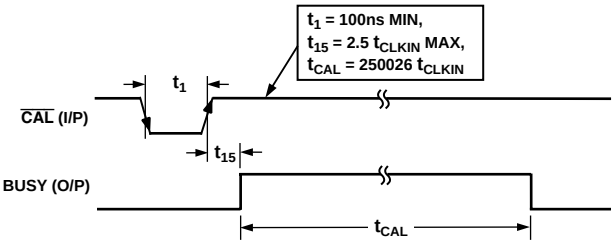


Figure 25. Timing Diagram for Full-Self Calibration

System Calibration Description

System calibration allows the user to take out system errors external to the AD7856 as well as calibrate the errors of the AD7856 itself. The maximum calibration range specified for the system offset errors is ±3.75% of V_{REF} but typically is ±5% and for the system gain errors is ±1.875% of V_{REF}. Therefore, under worst case conditions the maximum allowable system offset voltage applied between AIN(+) and AIN(–) would be ±0.0375 × V_{REF}, but under typical conditions this means that the maximum allowable system offset voltage applied between the AIN(+) and AIN(–) pins for the calibration to adjust out this error is ±0.05 × V_{REF} (*i.e., the AIN(+) can be 0.05 × V_{REF} above AIN(–) or 0.05 × V_{REF} below AIN(–)*). For the System gain error the maximum allowable system full-scale voltage that can be applied between AIN(+) and AIN(–) for the calibration to adjust out this error is V_{REF} ± *0.01875* × V_{REF} (*i.e., the AIN(+) can be V_{REF} + 0.01875 × V_{REF} above AIN(–) or V_{REF} – 0.01875 × V_{REF} above AIN(–)*). If the system offset or system gain errors are outside the ranges mentioned the system calibration algorithm will reduce the errors as much as the trim range allows.

Figures 26 through 28 illustrate why a specific type of system calibration might be used. Figure 26 shows a system offset calibration (assuming a positive offset) where the analog input range has been shifted upward by the system offset after the system offset calibration is completed. A negative offset may also be accounted for by a system offset calibration.

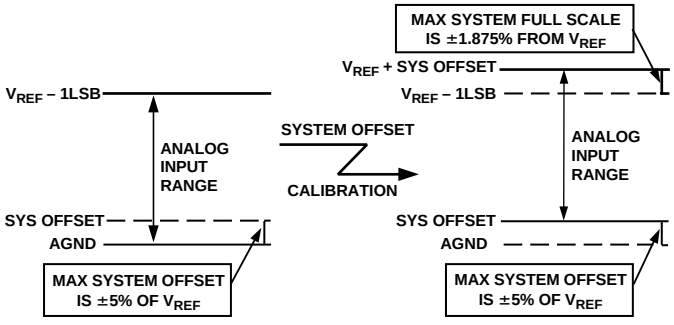


Figure 26. System Offset Calibration

Figure 27 shows a system gain calibration (assuming a system full scale greater than the reference voltage) where the analog input range has been increased after the system gain calibration is completed. A system full-scale voltage less than the reference voltage may also be accounted for by a system gain calibration.

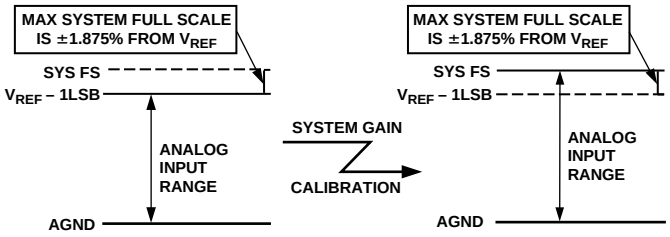


Figure 27. System Gain Calibration

Finally, in Figure 28 both the system offset and gain are accounted for by the system offset followed by a system gain calibration. First, the analog input range is shifted upward by the positive system offset and then the analog input range is adjusted at the top end to account for the system full scale.

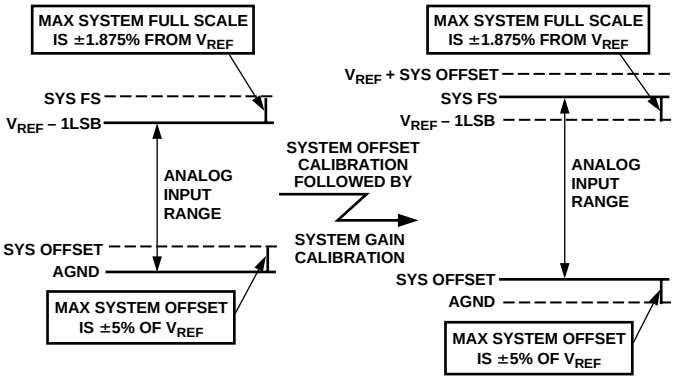


Figure 28. System (Gain + Offset) Calibration

System Gain and Offset Interaction

The inherent architecture of the AD7856 leads to an interaction between the system offset and gain errors when a system calibration is performed. Therefore, it is recommended to perform the cycle of a system offset calibration followed by a system gain calibration twice. Separate system offset and system gain calibrations reduce the offset and gain errors to at least the 14-bit level. By performing a system offset $\overline{\text{CAL}}$ first and a system gain calibration second, priority is given to reducing the gain error to zero before reducing the offset error to zero. If the system errors are small, a system offset calibration would be performed, followed by a system gain calibration. If the systems errors are large (close to the specified limits of the calibration range), this cycle would be repeated twice to ensure that the offset and gain errors were reduced to at least the 14-bit level. The advantage of doing separate system offset and system gain calibrations is that the user has more control over when the analog inputs need to be at the required levels, and the $\overline{\text{CONVST}}$ signal does not have to be used.

Alternatively, a system (gain + offset) calibration can be performed. It is recommended to perform three system (gain + offset) calibrations to reduce the offset and gain errors to the 14-bit level. For the system (gain + offset) calibration priority is given to reducing the offset error to zero before reducing the gain error to zero. Thus if the system errors are small then two system (gain + offset) calibrations will be sufficient. If the system errors are large (close to the specified limits of the calibration range) three system (gain + offset) calibrations may be

required to reduced the offset and gain errors to at least the 14-bit level. There will never be any need to perform more than three system (offset + gain) calibrations.

The zero scale error is adjusted for an offset calibration and the positive full-scale error is adjusted for a gain calibration.

System Calibration Timing

The calibration timing diagram in Figure 29 is for a full system calibration where the falling edge of $\overline{CAL}$ initiates an internal reset before starting a calibration (*note that if the part is in power-down mode, the* $\overline{CAL}$ *pulsewidth must take account of the power-up time*). For software calibrations with power-down modes, see note in Power-Up Times section. If a full system calibration is to be performed in software it is easier to perform separate gain and offset calibrations so that the CONVST bit in the control register does not have to be programmed in the middle of the system calibration sequence. The rising edge of $\overline{CAL}$ starts calibration of the internal DAC and causes the BUSY line to go high. If the control register is set for a full system calibration, the $\overline{CONVST}$ must be used also. The full-scale system voltage should be applied to the analog input pins from the start of calibration. The BUSY line will go low once the DAC and System Gain Calibration are complete. Next the system offset voltage is applied to the AIN pin for a minimum setup time (t_{SETUP}) of 100 ns before the rising edge of the $\overline{CONVST}$ and remains until the BUSY signal goes low. The rising edge of the $\overline{CONVST}$ starts the system offset calibration section of the full system calibration and also causes the BUSY signal to go high. The BUSY signal will go low after a time t_{CAL2} when the calibration sequence is complete. In some applications not all the input channels may be used. In this case it may be useful to dedicate two input channels for the system calibration, one which has the system offset voltage applied to it, and one which has the system full scale voltage applied to it. When a system offset or gain calibration is performed, the channel selected should correspond to the system offset or system full-scale voltage channel.

The timing for a system (gain + offset) calibration is very similar to that of Figure 29 the only difference being that the time t_{CAL1} will be replaced by a shorter time of the order of t_{CAL2} as the internal DAC will not be calibrated. The BUSY signal will signify when the gain calibration is finished and when the part is ready for the offset calibration.

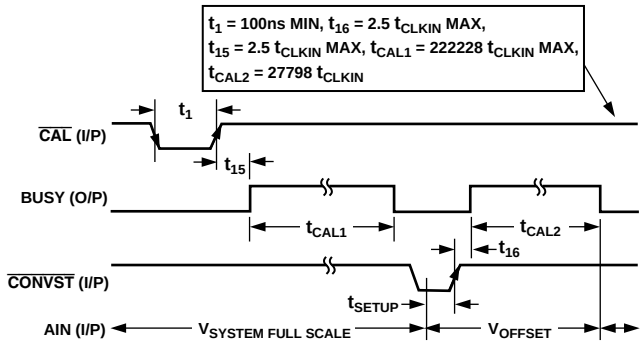


Figure 29. Timing Diagram for Full System Calibration

The timing diagram for a system offset or system gain calibration is shown in Figure 30. Here again the $\overline{CAL}$ is pulsed and the rising edge of the $\overline{CAL}$ initiates the calibration sequence (or the calibration can be initiated in software by writing to the control register). The rising edge of the $\overline{CAL}$ causes the BUSY line to go high and it will stay high until the calibration sequence is finished. The analog input should be set at the correct level for a minimum setup time (t_{SETUP}) of 100 ns before the rising edge of $\overline{CAL}$ and stay at the correct level until the BUSY signal goes low.

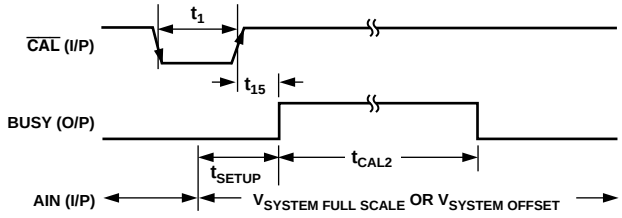


Figure 30. Timing Diagram for System Gain or System Offset Calibration

SERIAL INTERFACE SUMMARY

Table IX details the two interface modes and the serial clock edges from which the data is clocked out by the AD7856 (DOUT Edge) and that the data is latched in on (DIN Edge).

In both interface Modes 1, and 2 the $\overline{SYNC}$ is gated with the SCLK. Thus the falling edge of $\overline{SYNC}$ may clock out the MSB of data. Subsequent bits will be clocked out by the Serial Clock, SCLK. The condition for the falling edge of $\overline{SYNC}$ clocking out the MSB of data is as follows:

The falling edge of $\overline{SYNC}$ *will clock out the MSB if the serial clock is low when the* $\overline{SYNC}$ *goes low.*

If this condition is not the case, the SCLK will clock out the MSB. If a noncontinuous SCLK is used, it should idle high.

Table IX. SCLK Active Edges

Interface Mode	DOUT Edge	DIN Edge
1, 2	SCLK↓	SCLK↑

Resetting the Serial Interface

When writing to the part via the DIN line there is the possibility of writing data into the incorrect registers, such as the test register for instance, or writing the incorrect data and corrupting the serial interface. The $\overline{SYNC}$ pin acts as a reset. Bringing the $\overline{SYNC}$ pin high resets the internal shift register. The first data bit after the next $\overline{SYNC}$ falling edge will now be the first bit of a new 16-bit transfer. It is also possible that the test register contents were altered when the interface was lost. Therefore, once the serial interface is reset it may be necessary to write the 16-bit word 0100 0000 0000 0010 to restore the test register to its default value. Now the part and serial interface are completely reset. It is always useful to retain the ability to program the $\overline{SYNC}$ line from a port of the µController/DSP to have the ability to reset the serial interface.

Table X summarizes the interface modes provided by the AD7856. It also outlines the various µP/µC to which the particular interface is suited.

Interface Mode 1 may only be set by programming the control register (See section on Control Register).

Some of the more popular µProcessors, µControllers, and DSP machines that the AD7856 will interface to directly are mentioned here. This does not cover all µCs, µPs and DSPs. A more detailed timing description on each of the interface modes follows.

Table X. Interface Mode Description

Interface Mode	µProcessor/ µController	Comment
1	8XC51 8XL51 PIC17C42	(2-Wire) (DIN Is an Input/ Output Pin)
2	68HC11 68L11 68HC16 PIC16C64 ADSP-21xx DSP56000 DSP56001 DSP56002 DSP56L002	(3-Wire, SPI) (Default Mode)

DETAILED TIMING SECTION

Mode 1 (2-Wire 8051 Interface)

The read and write takes place on the DIN line and the conversion is initiated by pulsing the $\overline{\text{CONVST}}$ pin (note that in every write cycle the 2/$\overline{3}$ MODE bit must be set to 1). The conversion may be started by setting the CONVST bit in the control register to 1 instead of using the $\overline{\text{CONVST}}$ pin.

Figures 31 and 32 show the timing diagrams for Operating Mode 1 in Table X where the AD7856 is in the 2-wire interface mode. Here the DIN pin is used for both input and output as shown. The $\overline{\text{SYNC}}$ input is level-triggered active low and can be pulsed (Figure 31) or can be constantly low (Figure 32).

In Figure 31 the part samples the input data on the rising edge of SCLK. After the 16th rising edge of SCLK the DIN is configured as an output. When the $\overline{\text{SYNC}}$ is taken high the DIN is three-stated. Taking $\overline{\text{SYNC}}$ low disables the three-state on the DIN pin and the first SCLK falling edge clocks out the first data bit. Once the 16 clocks have been provided the DIN pin will automatically revert back to an input after a time, t_{14}. Note that a continuous SCLK shown by the dotted waveform in Figure 31 can be used provided that the $\overline{\text{SYNC}}$ is low for only 16 clock pulses in each of the read and write cycles.

In Figure 32 the $\overline{\text{SYNC}}$ line is permanently tied low and this results in a different timing arrangement. With $\overline{\text{SYNC}}$ permanently tied low the DIN pin will never be three-stated. The 16th rising edge of SCLK configures the DIN pin as an input or an output as shown in the diagram. Here no more than 16 SCLK pulses must occur for each of the read and write operations.

If reading from and writing to the calibration registers in this interface mode, all the selected calibration registers must be read from or written to. The read and write operations cannot be aborted. When reading from the calibration registers, the DIN pin will remain as an output for the full duration of all the calibration register read operations. When writing to the calibration registers, the DIN pin will remain as an input for the full duration of all the calibration register write operations.

NOTE: Initiating conversions in software is not recommended in Mode 1 operation.

A degradation of 0.3 LSB in linearity can be expected when operating in Mode 1; however, when hardware initiation of conversions is used, all other specifications that apply to Mode 2 operation also apply to Mode 1.

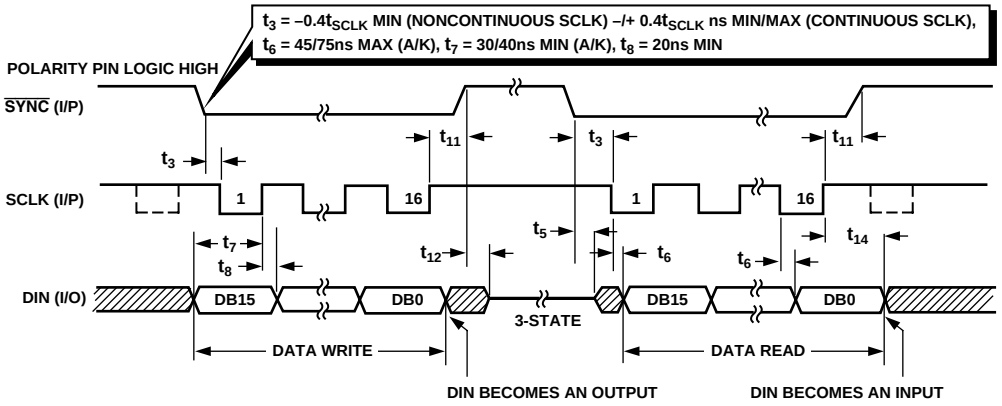


Figure 31. Timing Diagram for Read/Write Operation with DIN as an Input/Output (i.e., Mode 1)

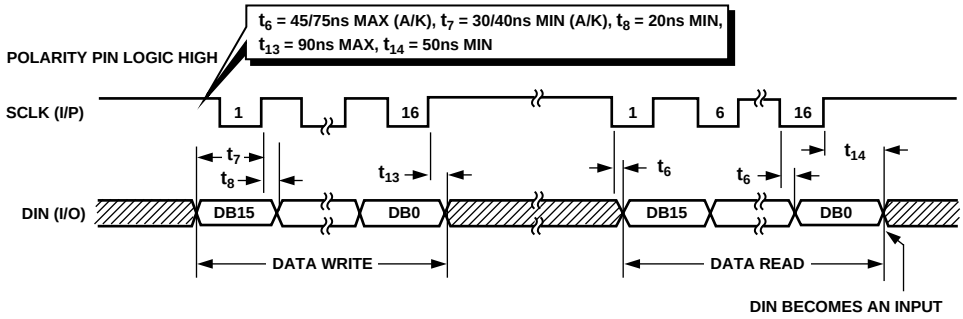


Figure 32. Timing Diagram for Read/Write Operation with DIN as an Input/Output and $\overline{\text{SYNC}}$ Input Tied Low (i.e., Interface Mode 1)

Mode 2 (3-Wire SPI/QSPI Interface Mode)
This is the DEFAULT INTERFACE MODE.

In Figure 33 below we have the timing diagram for interface Mode 2, which is the SPI/QSPI interface mode. Here the $\overline{\text{SYNC}}$ input is active low and may be pulsed or permanently tied low. If $\overline{\text{SYNC}}$ is permanently low, 16 clock pulses must be applied to the SCLK pin for the part to operate correctly otherwise, with a pulsed $\overline{\text{SYNC}}$ input, a continuous SCLK may be applied provided $\overline{\text{SYNC}}$ is low for only 16 SCLK cycles. In Figure 33 the $\overline{\text{SYNC}}$ going low disables the three-state on the DOUT pin. The first falling edge of the SCLK after the $\overline{\text{SYNC}}$ going low clocks out the first leading zero on the DOUT pin. The DOUT pin is three-stated again a time, t_{12}, after the $\overline{\text{SYNC}}$ goes high. With the DIN pin the data input has to be set up a time, t_7, before the SCLK rising edge as the part samples the input data on the SCLK rising edge in this case. If resetting the interface is required, the $\overline{\text{SYNC}}$ must be taken high and then low.

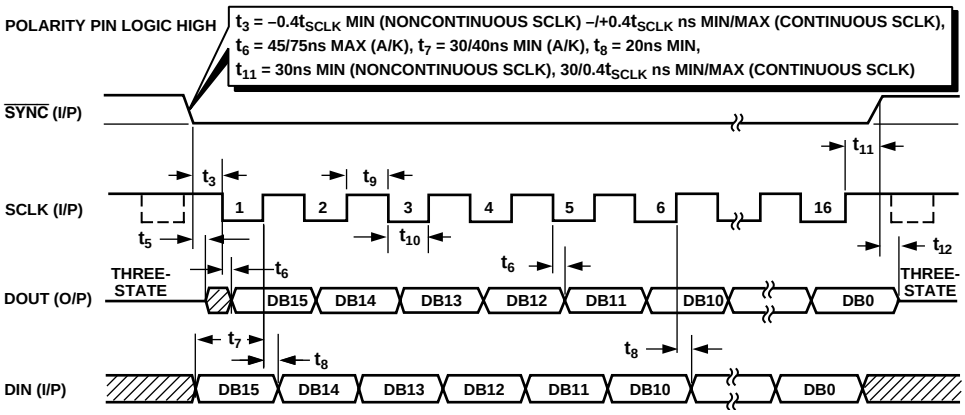


Figure 33. SPI/QSPI Mode 2 Timing Diagram for Read/Write Operation with DIN Input DOUT Output and $\overline{\text{SYNC}}$ Input

CONFIGURING THE AD7856

The AD7856 contains 14 on-chip registers that can be accessed via the serial interface. In the majority of applications it will not be necessary to access all of these registers. Here the CLKIN signal is applied directly after power-on, the CLKIN signal must be present to allow the part to perform a calibration. This automatic calibration will be completed approximately 150 ms after power-on.

Writing to the AD7856

For accessing the on-chip registers it is necessary to write to the part. To change the channel from the default channel setting the user will be required to write to the part. To enable Serial Interface Mode 1 the user must also write to the part. Figures 34 and 35 outline flowcharts of how to configure the AD7856 Serial Interface Modes 1 and 2 respectively. The continuous loops on all diagrams indicate the sequence for more than one conversion. The options of using a hardware (pulsing the $\overline{\text{CONVST}}$ pin) or software (setting the CONVST bit to 1) conversion start, and reading/writing during or after conversion are shown in Figures 34 and 35. If the $\overline{\text{CONVST}}$ pin is never used, it should be permanently tied to DV_{DD}. Where reference is made to the BUSY bit equal to a Logic 0, to indicate the end of conversion, the user in this case would poll the BUSY bit in the status register.

Interface Mode 1 Configuration

Figure 34 shows the flowchart for configuring the part in Interface Mode 1. This mode of operation can only be enabled by writing to the control register and setting the 2/$\overline{3}$ MODE bit. Reading and writing cannot take place simultaneously in this mode as the DIN pin is used for both reading and writing. Initiating conversions in software is not recommended in this mode, see Detailed Timing section.

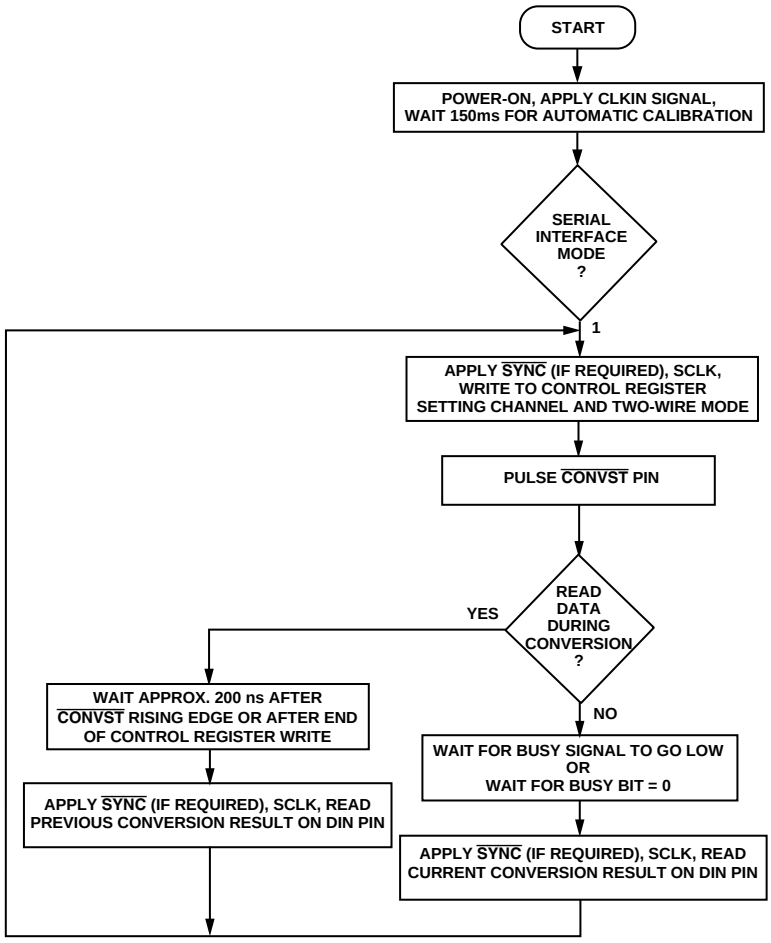


Figure 34. Flowchart for Setting Up, Reading and Writing in Interface Mode 1

Interface Mode 2 Configuration

Figure 35 shows the flowchart for configuring the part in Interface Mode 2. In this case the read and write operations take place simultaneously via the serial port. Writing all 0s ensures that no valid data is written to any of the registers. When using the software conversion start and transferring data during conversion, Note 1 must be obeyed.

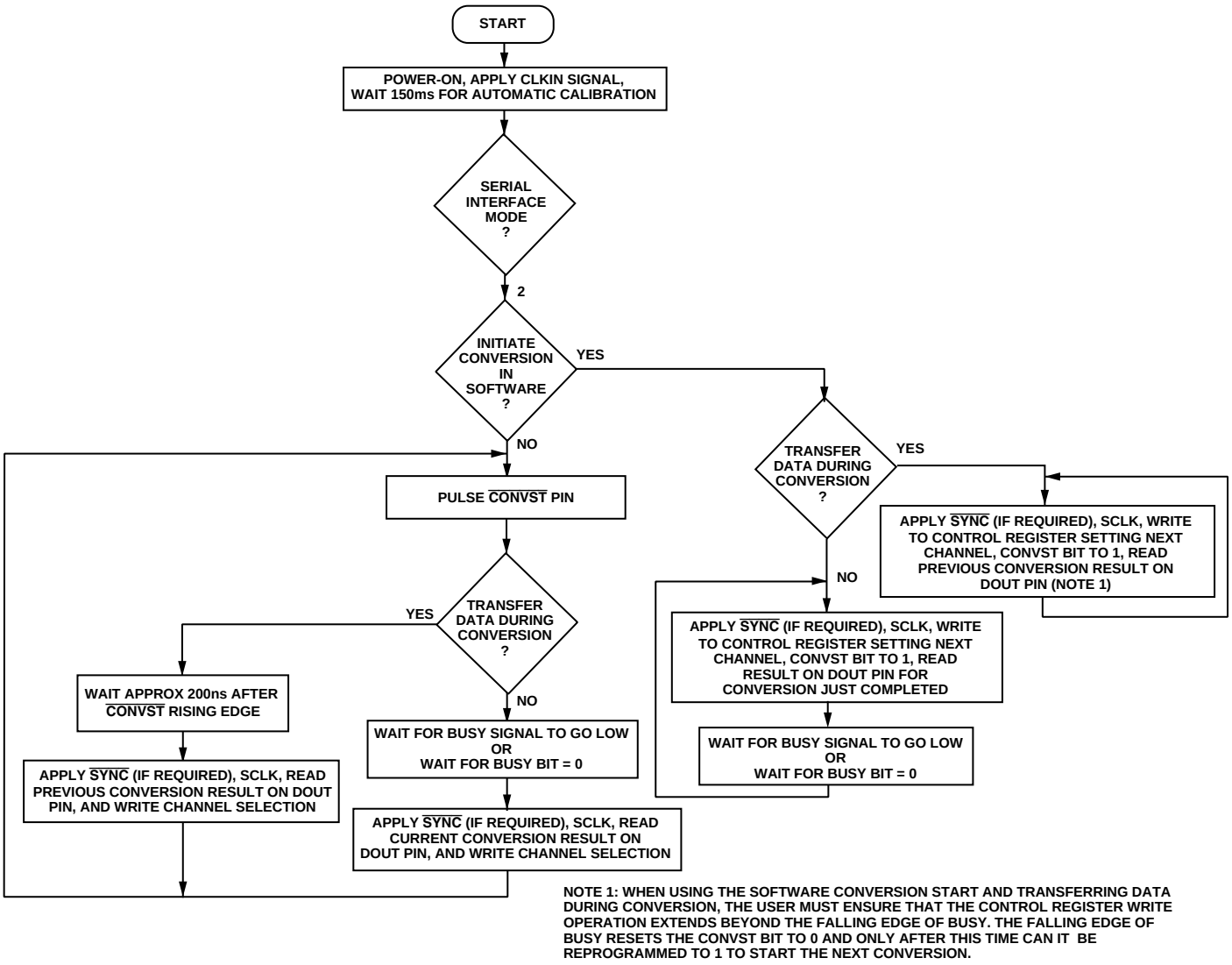


Figure 35. Flowchart for Setting Up, Reading and Writing in Interface Mode 2

MICROPROCESSOR INTERFACING

In many applications, the user may not require the facility of writing to most of the on-chip registers. The only writing necessary is to set the input channel configuration. After this the $\overline{\text{CONVST}}$ is applied, a conversion is performed and the result may be read using the SCLK to clock out the data from the output register onto the DOUT pin. At the same time, a write operation occurs and this may consist of all 0s where no data is written to the part or may set a different input channel configuration for the next conversion. The SCLK may be connected to the CLKIN pin if the user does not want to have to provide separate serial and master clocks. With this arrangement the $\overline{\text{SYNC}}$ signal must be low for 16 SCLK cycles for the read and write operations.

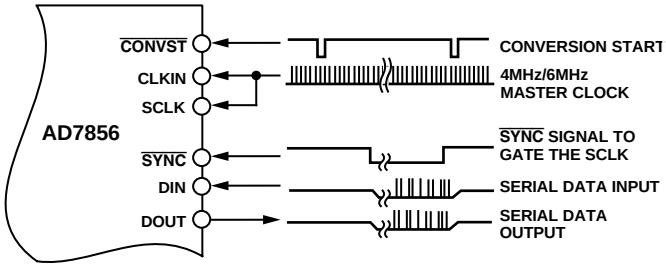


Figure 36. Simplified Interface Diagram

AD7856 to 8XC51 Interface

Figure 37 shows the AD7856 interface to the 8XC51. The 8XC51 only runs at 5 V. The 8XC51 is in Mode 0 operation. This is a two-wire interface consisting of the SCLK and the DIN which acts as a bidirectional line. The $\overline{\text{SYNC}}$ is tied low. The BUSY line can be used to give an interrupt driven system but this would not normally be the case with the 8XC51. For the 8XC51 12 MHz version the serial clock will run at a maximum of 1 MHz so the serial interface of the AD7856 will only be running at 1 MHz. The CLKIN signal must be provided separately to the AD7856 from a port line on the 8XC51 or from a source other than the 8XC51. Here the SCLK cannot be tied to the CLKIN as the $\overline{\text{SYNC}}$ is permanently tied low. The $\overline{\text{CONVST}}$ signal can be provided from an external timer or conversion can be started in software if required. The sequence of events would typically be writing to the control register via the DIN line setting a conversion start and the 2-wire interface mode (this would be performed in two 8-bit writes), wait for the conversion to be finished (3.5 μs with 6 MHz CLKIN), read the conversion result data on the DIN line (this would be performed in two 8-bit reads), and repeat the sequence. The maximum serial frequency will be determined by the data access and hold times of the 8XC51 and the AD7856.

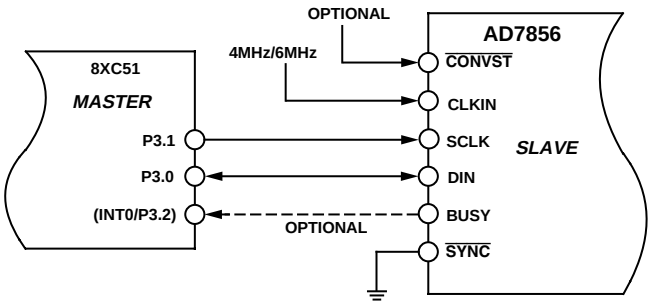


Figure 37. 8XC51/PIC16C42 Interface

AD7856 to 68HC11/16/L11/PIC16C42 Interface

Figure 38 shows the AD7856 SPI/QSPI interface to the 68HC11/16/L11/PIC16C42. The AD7856 is in Interface Mode 2. The $\overline{\text{SYNC}}$ line is not used and is tied to DGND. The μController is configured as the master, by setting the MSTR bit in the SPCR to 1, and provides the serial clock on the SCK pin. For all the μControllers the CPOL bit is set to 1 and for the 68HC11/16/L11 the CPHA bit is set to 1. The CLKIN and $\overline{\text{CONVST}}$ signals can be supplied from the μController or from separate sources. The BUSY signal can be used as an interrupt to tell the μController when the conversion is finished, then the reading and writing can take place. If required, the reading and writing can take place during conversion and there will be no need for the BUSY signal in this case.

For the 68HC16, the word length should be set to 16 bits and the $\overline{\text{SS}}$ line should be tied to the $\overline{\text{SYNC}}$ pin for the QSPI interface. The micro-sequencer and RAM associated with the 68HC16 QSPI port can be used to perform a number of read and write operations, and store the conversion results in memory, independent of the CPU. This is especially useful when reading the conversion results from all eight channels consecutively. The command section of the QSPI port RAM would be programmed to perform a conversion on one channel, read the conversion result, perform a conversion on the next channel, read the conversion result, and so on until all eight conversion results are stored into the QSPI RAM.

A typical sequence of events would be writing to the control register via the DIN line setting a conversion start and at the same time reading data from the previous conversion on the DOUT line (both the read and write operations would each be two 8-bit operations, one 16-bit operation for the 68HC16), wait for the conversion to be finished (= 3.5 μs for AD7856 with 6 MHz CLKIN), and then repeat the sequence. The maximum serial frequency will be determined by the data access and hold times of the μControllers and the AD7856.

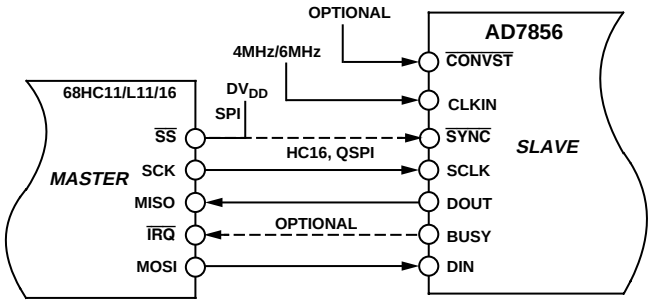


Figure 38. 68HC11 and 68HC16 Interface

AD7856 to ADSP-21xx Interface

Figure 39 shows the AD7856 interface to the ADSP-21xx. The ADSP-21xx is the master and the AD7856 is the slave. The AD7856 is in Interface Mode 2. For the ADSP-21xx the bits in the serial port control register should be set up as TFSR = RFSR = 1 (need a frame sync for every transfer), SLEN = 15 (16-bit word length), TFSW = RFSW = 1 (alternate framing mode for transmit and receive operations), INVRFS = INVTFS = 1 (active low RFS and TFS), IRFS = 0, ITFS = 1 (External RFS and internal TFS), and ISCLK = 1 (internal serial clock). The CLKIN and CONVST signals can be supplied from the ADSP-21xx or from an external source. The serial clock from the ADSP-21xx must be inverted before the SCLK pin of the AD7856. This SCLK could also be used to drive the CLKIN input of the AD7856. The BUSY signal indicates when the conversion is finished and may not be required. The data access and hold times of the ADSP-21xx and the AD7856 allow for a serial clock of 6 MHz at 5 V.

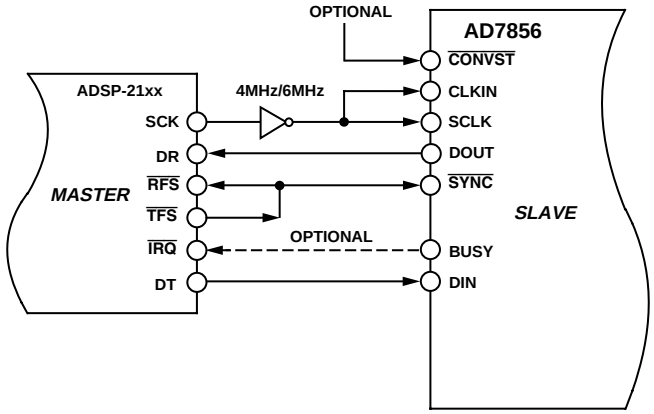


Figure 39. ADSP-21xx Interface

AD7856 to DSP56000/1/2/L002 Interface

Figure 40 shows the AD7856 to DSP56000/1/2/L002 interface. Here the DSP5600x is the master and the AD7856 is the slave. The AD7856 is in Interface Mode 2. The setting of the bits in the registers of the DSP5600x would be for synchronous operation (SYN = 1), internal frame sync (SCD2 = 1), gated internal clock (GCK = 1, SCKD = 1), 16-bit word length (WL1 = 1, WL0 = 0). Since a gated clock is used here the SCLK cannot be tied to the CLKIN of the AD7856. The SCLK from the DSP5600x must be inverted before it is applied to the AD7856. Again the data access and hold times of the DSP5600x and the AD7856 allows for a SCLK of 6 MHz, V_{DD} = 5 V.

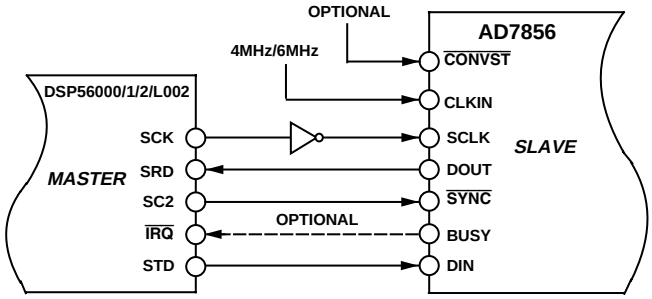


Figure 40. DSP56000/1/2/L002 Interface

APPLICATION HINTS

Grounding and Layout

The analog and digital supplies to the AD7856 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part has very good immunity to noise on the power supplies as can be seen by the PSRR vs. Frequency graph. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7856 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7856 is the only device requiring an AGND to DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD7856. If the AD7856 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7856.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7856 to avoid noise coupling. The power supply lines to the AD7856 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to AGND. All digital supplies should have a 0.1 μF disc ceramic capacitor to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the AV_{DD} and DV_{DD} of the AD7856, it is recommended that the system's AV_{DD} supply be used. In this case there should be a 10 Ω resistor between the AV_{DD} pin and DV_{DD} pin. This supply should have the recommended analog supply decoupling capacitors between the AV_{DD} pin of the AD7856 and AGND and the recommended digital supply decoupling capacitor between the DV_{DD} pin of the AD7856 and DGND.

Evaluating the AD7856 Performance

The recommended layout for the AD7856 is outlined in the evaluation board for the AD7856. The evaluation board package includes a fully assembled and tested evaluation board, documentation and software for controlling the board from the PC via the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7856 Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7856.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7856. It also gives full access to all the AD7856 on-chip registers allowing for various calibration and power-down options to be programmed.

AD785x Family

12 bits, 200 kSPS, 3.0 V to 5.5 V:
AD7853 – Single-Channel Serial
AD7854 – Single-Channel Parallel
AD7858 – 8-Channel Serial
AD7859 – 8-Channel Parallel

14 bits, 333 kSPS, 4.75 V to 5.25 V:
AD7851 – Single-Channel Serial

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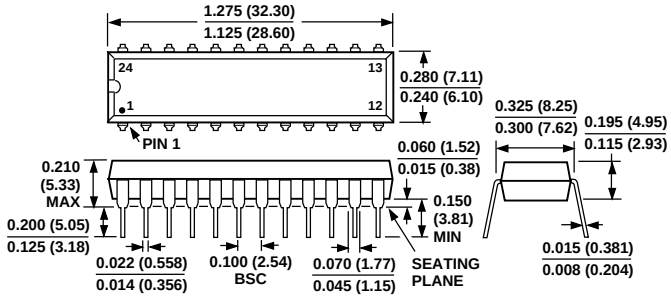
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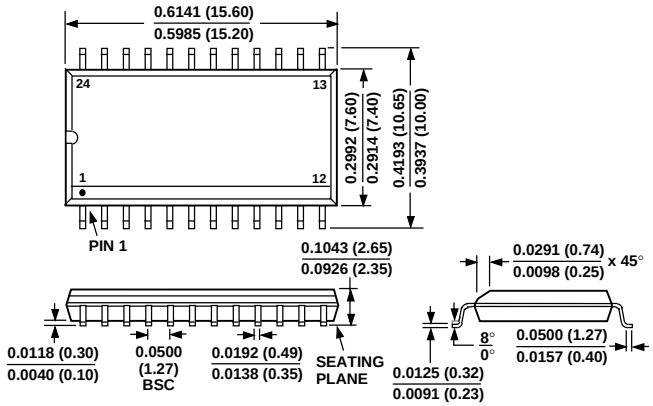
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

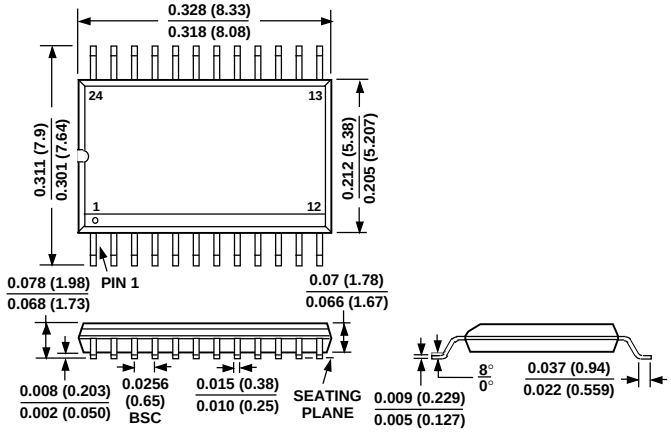
24-Lead Plastic DIP
(N-24)



24-Lead Small Outline Package
(R-24)



24-Lead Shrink Small Outline Package
(RS-24)



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PRINTED IN U.S.A.