Fiber Optic Receiver with Quantizer and Clock Recovery and Data Retiming

AD807

FEATURES

Meets CCITT G.958 Requirements for STM-1 Regenerator—Type A
Meets Bellcore TR-NWT-000253 Requirements for OC-3
Output Jitter: 2.0 Degrees RMS
155 Mbps Clock Recovery and Data Retiming
Accepts NRZ Data, No Preamble Required
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Quantizer Sensitivity: 2 mV
Level Detect Range: 2.0 mV to 30 mV
Single Supply Operation: +5 V or –5.2 V
Low Power: 170 mW
10 KH ECL/PECL Compatible Output
Package: 16-Lead Narrow 150 mil SOIC

PRODUCT DESCRIPTION

The AD807 provides the receiver functions of data quantization, signal level detect, clock recovery and data retiming for 155 Mbps NRZ data. The device, together with a PIN diode/preamplifier combination, can be used for a highly integrated, low cost, low power SONET OC-3 or SDH STM-1 fiber optic receiver.

The receiver front end signal level detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor. The signal level detect circuit 3 dB optical hysteresis prevents chatter at the signal level detect output.

The PLL has a factory-trimmed VCO center frequency and a frequency acquisition control loop that combine to guarantee frequency acquisition without false lock. This eliminates a reliance on external components such as a crystal or a SAW filter, to aid frequency acquisition.

The AD807 acquires frequency and phase lock on input data using two control loops that work without requiring external control. The frequency acquisition control loop initially acquires the frequency of the input data, acquiring frequency lock on random or scrambled data without the need for a preamble. At frequency lock, the frequency error is zero and the frequency detector has no further effect. The phase acquisition control loop then works to ensure that the output phase tracks the input phase. A patented phase detector has virtually eliminated pattern jitter throughout the AD807.

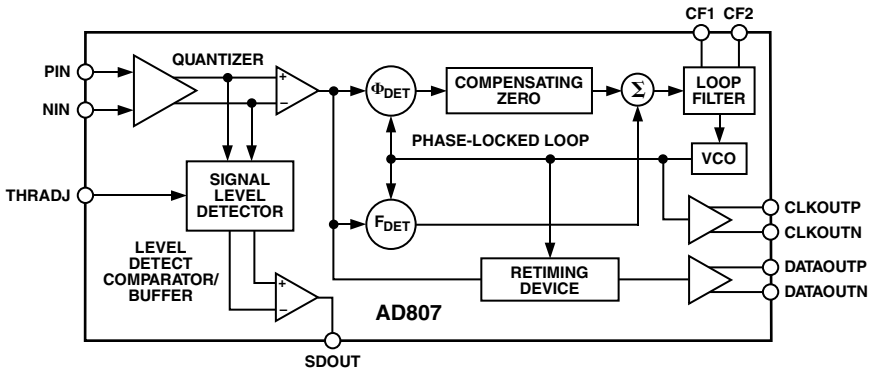
The device VCO uses a ring oscillator architecture and patented low noise design techniques. Jitter is 2.0 degrees rms. This low jitter results from using a fully differential signal architecture, Power Supply Rejection Ratio circuitry and a dielectrically isolated process that provides immunity from extraneous signals on the IC. The device can withstand hundreds of millivolts of power supply noise without an effect on jitter performance.

The user sets the jitter peaking and acquisition time of the PLL by choosing a damping factor capacitor whose value determines loop damping. CCITT G.958 Type A jitter transfer requirements can easily be met with a damping factor of 5 or greater.

Device design guarantees that the clock output frequency will drift by less than 20% in the absence of input data transitions. Shorting the damping factor capacitor, C_D, brings the clock output frequency to the VCO center frequency.

The AD807 consumes 170 mW and operates from a single power supply at either +5 V or –5.2 V.

FUNCTIONAL BLOCK DIAGRAM



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2000

AD807–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, C_D = 0.1 µF, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
QUANTIZER–DC CHARACTERISTICS					
Input Voltage Range	@ P_{IN} or N_{IN}	2.5		V_{CC}	V
Input Sensitivity, V_{SENSE}	P_{IN}–N_{IN}, Figure 1, BER = ≤ 1×10^{-10}	2			mV
Input Overdrive, V_{OD}	Figure 1, BER = ≤ 1×10^{-10}	0.001		2.5	V
Input Offset Voltage			50	500	µV
Input Current			5	10	µA
Input RMS Noise	BER = ≤ 1×10^{-10}		50		µV
Input Peak-to-Peak Noise	BER = ≤ 1×10^{-10}		650		µV
QUANTIZER–AC CHARACTERISTICS					
Upper –3 dB Bandwidth			180		MHz
Input Resistance			1		MΩ
Input Capacitance			2		pF
Pulsewidth Distortion			100		ps
LEVEL DETECT					
Level Detect Range	R_{THRESH} = INFINITE	0.8	2	4.0	mV
	R_{THRESH} = 49.9 kΩ	4	5	7.4	mV
	R_{THRESH} = 3.4 kΩ	14	20	25	mV
Response Time	DC-Coupled	0.1		1.5	µs
Hysteresis (Electrical)	R_{THRESH} = INFINITE	2.3	4.0	10.0	dB
	R_{THRESH} = 49.9 kΩ	3.0	5.0	9.0	dB
	R_{THRESH} = 3.4 kΩ	3.0	7.0	10.0	dB
SDOUT Output Logic High	Load = +4 mA	3.6			V
SDOUT Output Logic Low	Load = –1.2 mA			0.4	V
PHASE-LOCKED LOOP NOMINAL CENTER FREQUENCY			155.52		MHz
CAPTURE RANGE		155		156	MHz
TRACKING RANGE		155		156	MHz
STATIC PHASE ERROR	2^7–1 PRN Sequence		4	20	Degrees
SETUP TIME (t_{SU})	Figure 2	3.0	3.2	3.5	ns
HOLD TIME (t_H)	Figure 2	3.0	3.1	3.3	ns
PHASE DRIFT	240 Bits, No Transitions			40	Degrees
JITTER	2^7–1 PRN Sequence		2.0		Degrees RMS
	2^{23}–1 PRN Sequence		2.0	2.7	Degrees RMS
JITTER TOLERANCE	f = 10 Hz		3000		Unit Intervals
	f = 6.5 kHz	4.5	7.6		Unit Intervals
	f = 65 kHz	0.45	1.0		Unit Intervals
	f = 1.3 MHz	0.45	0.67		Unit Intervals
JITTER TRANSFER					
Peaking (Figure 11)	C_D = 0.15 µF		0.08		dB
	C_D = 0.33 µF		0.04		dB
Bandwidth		65	92	130	kHz
Acquisition Time					
C_D = 0.1 µF	2^{23}–1 PRN Sequence, T_A = 25°C		4×10^5	2×10^6	Bit Periods
C_D = 0.33 µF	V_{CC} = 5 V, V_{EE} = GND		2×10^6		Bit Periods
POWER SUPPLY VOLTAGE	V_{MIN} to V_{MAX}	4.5		5.5	Volts
POWER SUPPLY CURRENT	V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C	25	34.5	39.5	mA
PECL OUTPUT VOLTAGE LEVELS					
Output Logic High, V_{OH}	V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C	–1.2	–1.0	–0.7	Volts
Output Logic Low, V_{OL}	Referenced to V_{CC}	–2.0	–1.8	–1.7	Volts
SYMMETRY (Duty Cycle)	ρ = 1/2, T_A = 25°C,				
Recovered Clock Output, Pin 5	V_{CC} = 5 V, V_{EE} = GND	50.1		54.1	%
OUTPUT RISE / FALL TIMES					
Rise Time (t_R)	20%–80%		1.1	1.5	ns
Fall Time (t_F)	80%–20%		1.1	1.5	ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 12 V
Input Voltage (Pin 12 or Pin 13) . . . . . V_{CC} + 0.6 V
Maximum Junction Temperature . . . . . 165°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C
ESD Rating (Human Body Model) . . . . . 500 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics:
16-Lead Narrow Body SOIC Package: θ_{JA} = 110°C/W.

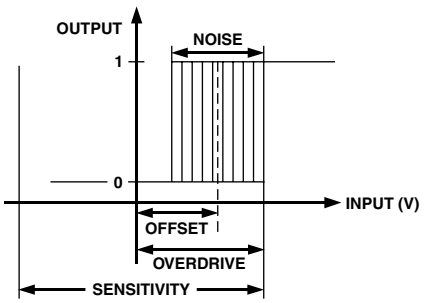


Figure 1. Input Sensitivity, Input Overdrive

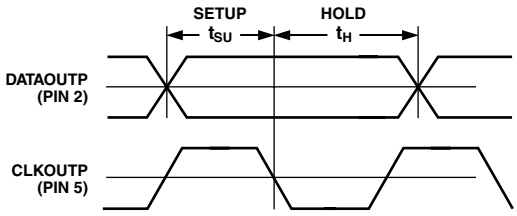
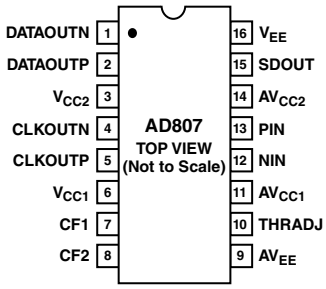


Figure 2. Setup and Hold Time

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DATAOUTN	Differential Retimed Data Output
2	DATAOUTP	Differential Retimed Data Output
3	V_{CC2}	Digital V_{CC} for ECL Outputs
4	CLKOUTN	Differential Recovered Clock Output
5	CLKOUTP	Differential Recovered Clock Output
6	V_{CC1}	Digital V_{CC} for Internal Logic
7	CF1	Loop Damping Capacitor
8	CF2	Loop Damping Capacitor
9	AV_{EE}	Analog V_{EE}
10	THRADJ	Level Detect Threshold Adjust
11	AV_{CC1}	Analog V_{CC} for PLL
12	NIN	Quantizer Differential Input
13	PIN	Quantizer Differential Input
14	AV_{CC2}	Analog V_{CC} for Quantizer
15	SDOUT	Signal Detect Output
16	V_{EE}	Digital V_{EE} for Internal Logic

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD807A-155BR	–40°C to +85°C	16-Lead Narrowbody SOIC	R-16A
AD807A-155BRRL7	–40°C to +85°C	750 Pieces, 7" Reel	R-16A
AD807A-155BRRL	–40°C to +85°C	2500 Pieces, 13" Reel	R-16A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD807 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



DEFINITION OF TERMS

Maximum, Minimum and Typical Specifications
Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations: if the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guardbanded to account for tester variation to thus guarantee that no device is shipped outside of data sheet specifications.

Input Sensitivity and Input Overdrive
Sensitivity and Overdrive specifications for the Quantizer involve offset voltage, gain and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 1.

For sufficiently large positive input voltage the output is always Logic 1 and similarly, for negative inputs, the output is always Logic 0. However, the transitions between output Logic Levels 1 and 0 are not at precisely defined input voltage levels, but occur over a range of input voltages. Within this Zone of Confusion, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer (650 μV at the 1×10^{-10} confidence level). The center of the Zone of Confusion is the quantizer input offset voltage (±500 μV maximum). Input Overdrive is the magnitude of signal required to guarantee correct logic level with 1×10^{-10} confidence level.

With a single-ended PIN-TIA (Figure 3), ac coupling is used and the inputs to the Quantizer are dc biased at some common-mode potential. Observing the Quantizer input with an oscilloscope probe at the point indicated shows a binary signal with average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the Quantizer Sensitivity. Referring to Figure 1, since both positive and negative offsets need to be accommodated, the Sensitivity is twice the Overdrive. The AD807 Quantizer has 2 mV Sensitivity.

With a differential TIA (Figure 3), Sensitivity seems to improve from observing the Quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 1 mV peak-to-peak signal appears to drive the AD807 Quantizer. However, the single-ended probe measures only half the signal. The true Quantizer input signal is twice this value since the other Quantizer input is a complementary signal to the signal being observed.

Response Time
Response time is the delay between removal of the input signal and indication of Loss of Signal (LOS) at SDOUT. The response time of the AD807 (1.5 μs maximum) is much faster than the SONET/SDH requirement (3 μs ≤ response time ≤ 100 μs). In practice, the time constant of the ac coupling at the Quantizer input determines the LOS response time.

Nominal Center Frequency
This is the frequency at which the VCO will oscillate with the loop damping capacitor, C_D, shorted.

Tracking Range
This is the range of input data rates over which the AD807 will remain in lock.

Capture Range
This is the range of input data rates over which the AD807 will acquire lock.

Static Phase Error
This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error, and IC input and output signals prohibit direct measurement of static phase error.

Data Transition Density, ρ
This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to bit periods.

Jitter
This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms or Unit Intervals (UI). Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

Output Jitter
This is the jitter on the retimed data, in degrees rms, due to a specific pattern or some pseudorandom input data sequence (PRN Sequence).

Jitter Tolerance
Jitter Tolerance is a measure of the AD807's ability to track a jittery input data signal. Jitter on the input data is best thought of as phase modulation, and is usually specified in unit intervals.

The PLL must provide a clock signal that tracks the phase modulation in order to accurately retime jittered data. In order for the VCO output to have a phase modulation that tracks the input jitter, some modulation signal must be generated at the output of the phase detector. The modulation output from the phase detector can only be produced by a phase error between its data input and its clock input. Hence, the PLL can never perfectly track jittered data. However, the magnitude of the phase error depends on the gain around the loop. At low frequencies, the integrator of the AD807 PLL provides very high gain, and thus very large jitter can be tracked with small phase errors between input data and recovered clock. At frequencies closer to the loop bandwidth, the gain of the integrator is much smaller, and thus less input jitter can be tolerated. The AD807 output will have a bit error rate less than 1×10^{-10} when in lock and retiming input data that has the CCITT G.958 specified jitter applied to it.

Jitter Transfer (Refer to Figure 11)
The AD807 exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth
This describes the frequency at which the AD807 attenuates sinusoidal input jitter by 3 dB.

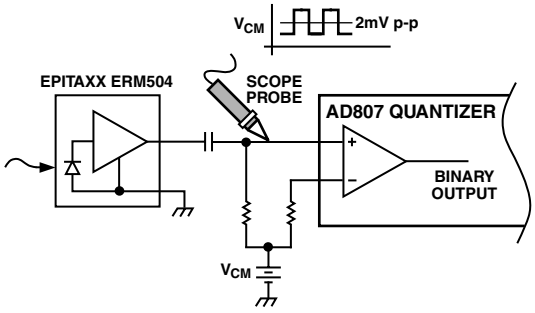
Peaking
This describes the maximum jitter gain of the AD807 in dB.

Damping Factor, ζ
Damping factor, ζ describes the compensation of the second order PLL. A larger value of ζ corresponds to more damping and less peaking in the jitter transfer function.

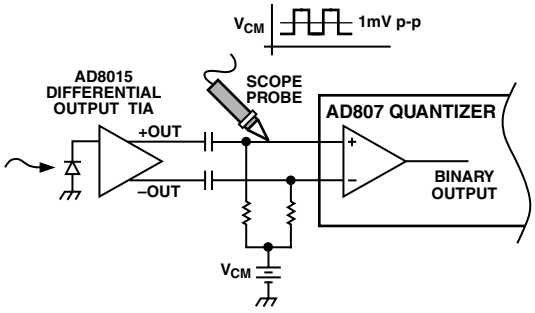
Acquisition Time
This is the transient time, measured in bit periods, required for the AD807 to lock onto input data from its free-running state.

Symmetry—Recovered Clock Duty Cycle
Symmetry is calculated as (100 × on time)/period, where on time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.

Bit Error Rate vs. Signal-to-Noise Ratio
AD807 Bit Error Rate vs. Signal-to-Noise Ratio performance is shown in TPC 6. Wideband amplitude noise is summed with the input data signal as shown in Figure 4. Performance is shown for input data levels of 5 mV and 10 mV.



a. Single-Ended Input Application



b. Differential Input Application

Figure 3. (a–b) Single-Ended and Differential Input Applications

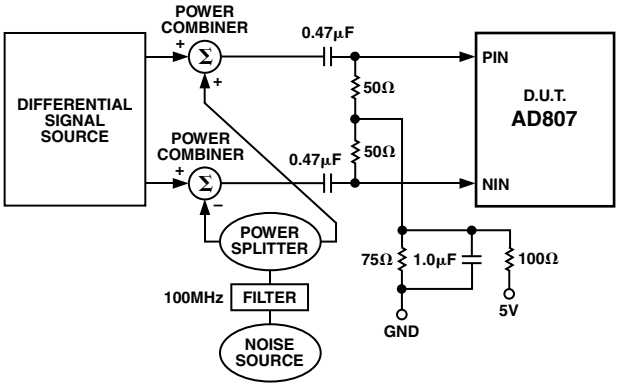
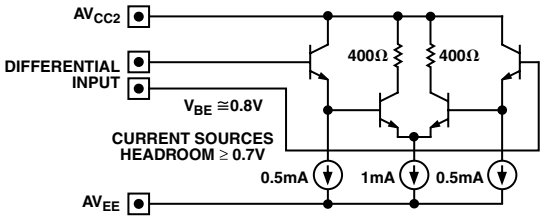
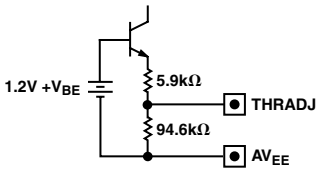


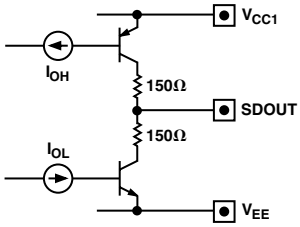
Figure 4. Bit Error Rate vs. Signal-to-Noise Ratio Test: Block Diagram



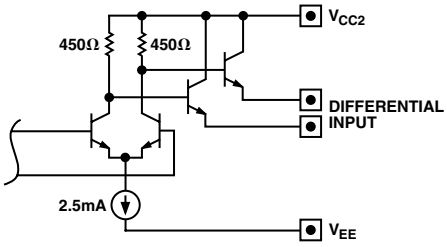
a. Quantizer Differential Input Stage



b. Threshold Adjust



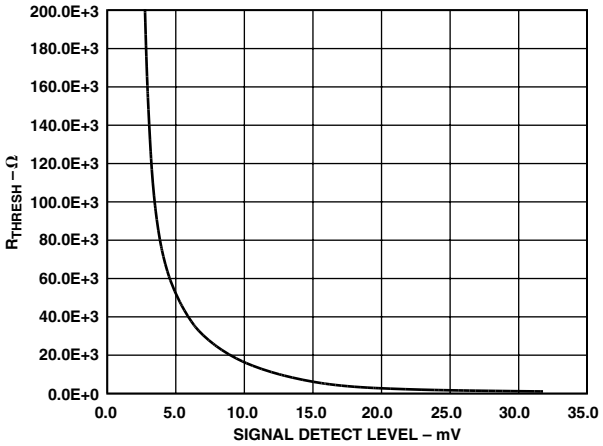
c. Signal Detect Output (SDOUT)



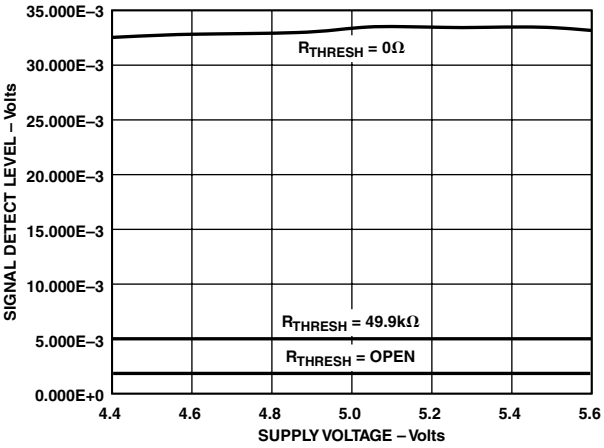
d. PLL Differential Output Stage—DATAOUT(N), CLKOUT(N)

Figure 5. (a–d) Simplified Schematics

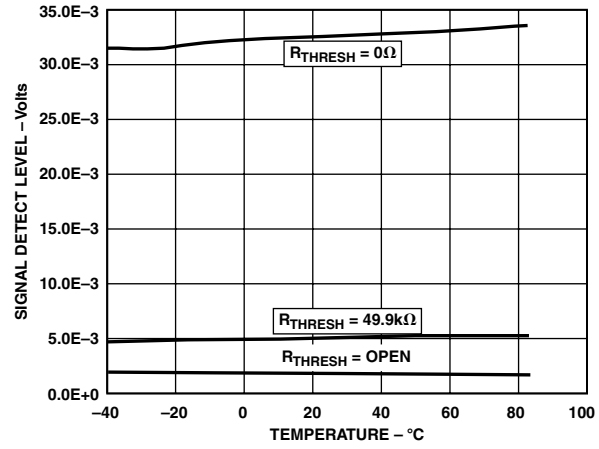
AD807–Typical Performance Characteristics



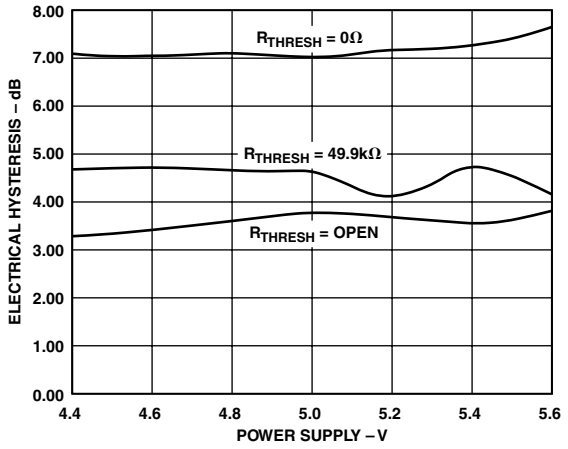
TPC 1. Signal Detect Level vs. R_{THRESH}



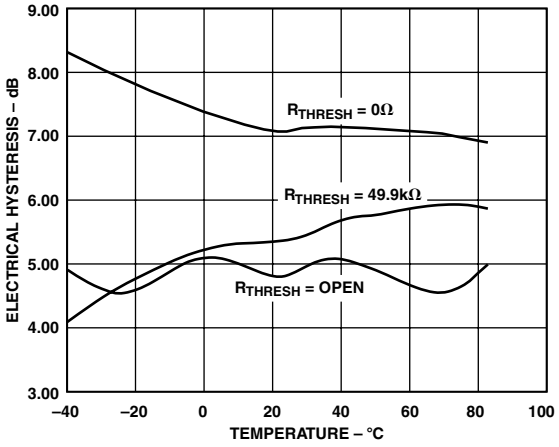
TPC 4. Signal Detect Level vs. Supply Voltage



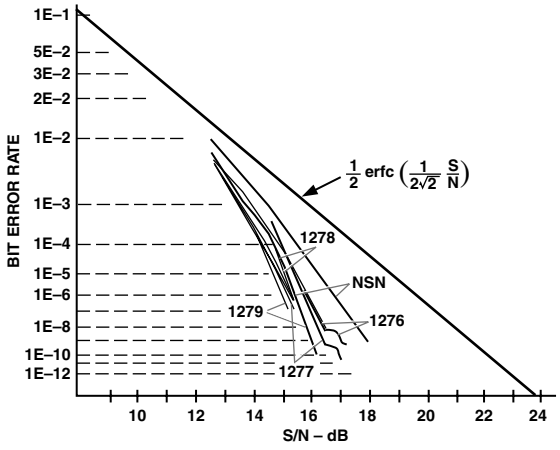
TPC 2. Signal Detect Level vs. Temperature



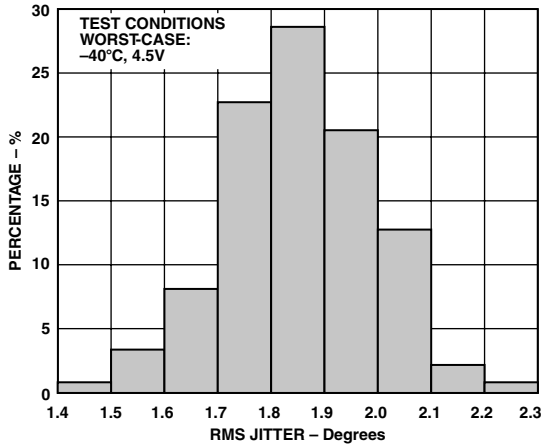
TPC 5. Signal Detect Hysteresis vs. Power Supply



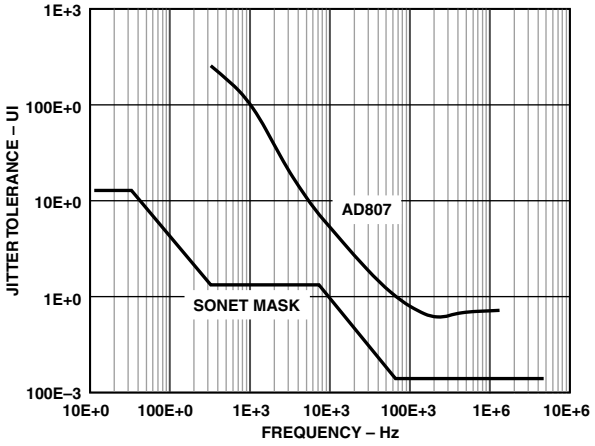
TPC 3. Signal Detect Hysteresis vs. Temperature



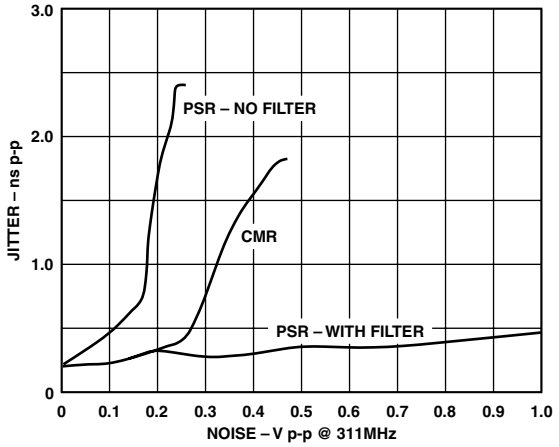
TPC 6. Bit Error Rate vs. Signal-to-Noise Ratio



TPC 7. Output Jitter Histogram



TPC 8. Jitter Tolerance



TPC 9. Output Jitter vs. Supply Noise and Output Jitter vs. Common Mode Noise

THEORY OF OPERATION

Quantizer

The quantizer (comparator) has three gain stages, providing a net gain of 350. The quantizer takes full advantage of the Extra Fast Complementary Bipolar (XFCB) process. The input stage uses a folded cascode architecture to virtually eliminate pulse width distortion, and to handle input signals with common-mode voltage as high as the positive supply. The input offset voltage is factory trimmed and guaranteed to be less than 500 µV. XFCB's dielectric isolation allows the different blocks within this mixed-signal IC to be isolated from each other, hence the 2 mV Sensitivity is achieved. Traditionally, high speed comparators are plagued by crosstalk between outputs and inputs, often resulting in oscillations when the input signal approaches 10 mV. The AD807 quantizer toggles at ±650 µV (1.3 mV sensitivity) at the input without making bit errors. When the input signal is lowered below ±650 µV, circuit performance is dominated by input noise, and not crosstalk.

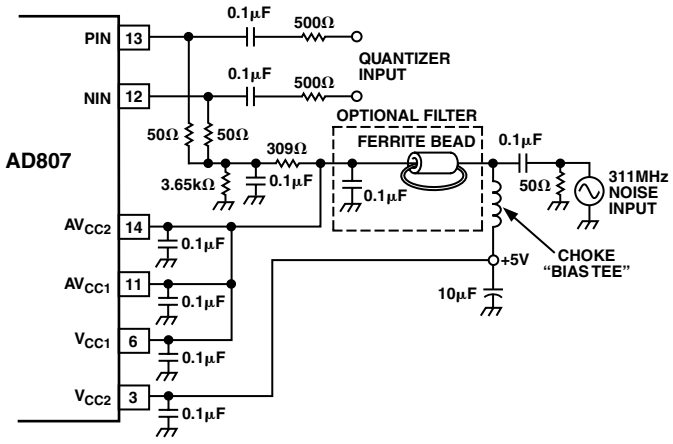


Figure 6. Power Supply Noise Sensitivity Test Circuit

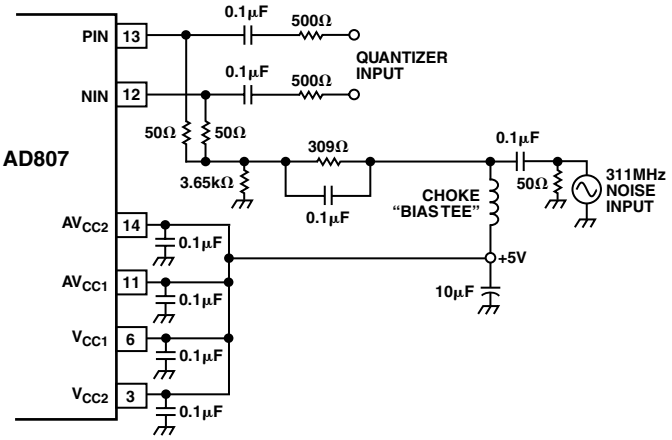


Figure 7. Common-Mode Rejection Test Circuit

Signal Detect

The input to the signal detect circuit is taken from the first stage of the quantizer. The input signal is first processed through a gain stage. The output from the gain stage is fed to both a positive and a negative peak detector. The threshold value is subtracted from the positive peak signal and added to the negative peak signal. The positive and negative peak signals are then compared. If the positive peak, POS, is more positive than the negative peak, NEG, the signal amplitude is greater than the threshold, and the output, SDOUT, will indicate the presence of signal by remaining low. When POS becomes more negative than NEG, the signal amplitude has fallen below the threshold, and SDOUT will indicate a loss of signal (LOS) by going high. The circuit provides hysteresis by adjusting the threshold level higher by a factor of two when the low signal level is detected. This means that the input data amplitude needs to reach twice the set LOS threshold before SDOUT will signal that the data is again valid. This corresponds to a 3 dB optical hysteresis.

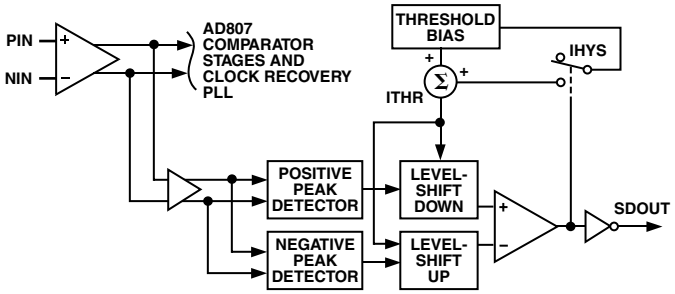


Figure 8. Signal Level Detect Circuit Block Diagram

Phase-Locked Loop

The phase-locked loop recovers clock and retimes data from NRZ data. The architecture uses a frequency detector to aid initial frequency acquisition; refer to Figure 9 for a block diagram. Note the frequency detector is always in the circuit. When the PLL is locked, the frequency error is zero and the frequency detector has no further effect. Since the frequency detector is always in the circuit, no control functions are needed to initiate acquisition or change mode after acquisition.

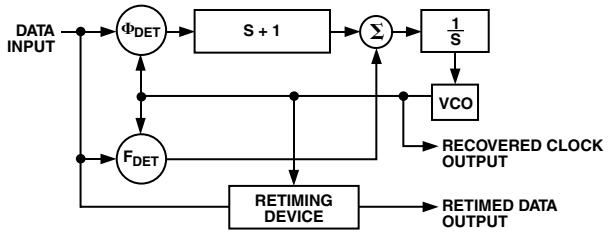


Figure 9. PLL Block Diagram

The frequency detector delivers pulses of current to the charge pump to either raise or lower the frequency of the VCO. During the frequency acquisition process the frequency detector output is a series of pulses of width equal to the period of the VCO. These pulses occur on the cycle slips between the data frequency and the VCO frequency. With a maximum density data pattern (1010 . . .), every cycle slip will produce a pulse at the frequency detector output. However, with random data, not every cycle slip produces a pulse. The density of pulses at the frequency detector output increases with the density of data transitions. The probability that a cycle slip will produce a pulse increases as the frequency error approaches zero. After the frequency error has been reduced to zero, the frequency detector output will have no further pulses. At this point the PLL begins the process of phase acquisition, with a settling time of roughly 2000 bit periods.

Jitter caused by variations of density of data transitions (pattern jitter) is virtually eliminated by use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCO phase to increase to above the average run rate set by the data frequency. The jitter created by a 2^7–1 pseudorandom code is 1/2 degree, and this is small compared to random jitter.

The jitter bandwidth for the PLL is 0.06% of the center frequency. This figure is chosen so that sinusoidal input jitter at 92 kHz will be attenuated by 3 dB.

The damping ratio of the PLL is user programmable with a single external capacitor. At 155 MHz, a damping ratio of 5 is obtained with a 0.15 μF capacitor. More generally, the damping ratio scales as $(f_{DATA} \times C_D)^{1/2}$.

A lower damping ratio allows a faster frequency acquisition; generally the acquisition time scales directly with the capacitor value. However, at damping ratios approaching one, the acquisition time no longer scales directly with capacitor value. The acquisition time has two components: frequency acquisition and phase acquisition. The frequency acquisition always scales with capacitance, but the phase acquisition is set by the loop bandwidth of the PLL and is independent of the damping ratio. Thus, the 0.06% fractional loop bandwidth sets a minimum acquisition time of 2000 bit periods. Note the acquisition time for a damping factor of one is 15,000 bit periods. This comprises 13,000 bit periods for frequency acquisition and 2,000 bit periods for phase acquisition. Compare this to the 400,000 bit periods acquisition time specified for a damping ratio of 5; this consists entirely of frequency acquisition, and the 2,000 bit periods of phase acquisition is negligible.

While a lower damping ratio affords faster acquisition, it also allows more peaking in the jitter transfer response (jitter peaking). For example, with a damping ratio of 10, the jitter peaking is 0.02 dB, but with a damping ratio of 1, the peaking is 2 dB.

Center Frequency Clamp (Figure 10)

An N-channel FET circuit can be used to bring the AD807 VCO center frequency to within ±10% of 155 MHz when SDOUT indicates a Loss of Signal (LOS). This effectively reduces the frequency acquisition time by reducing the frequency error between the VCO frequency and the input data frequency at clamp release. The N-FET can have "on" resistance as high as 1 kΩ and still attain effective clamping. However, the chosen N-FET should have greater than 10 MΩ "off" resistance and less than 100 nA leakage current (source and drain) so as not to alter normal PLL performance.

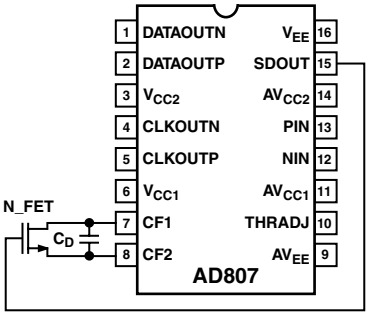


Figure 10. Center Frequency Clamp Schematic

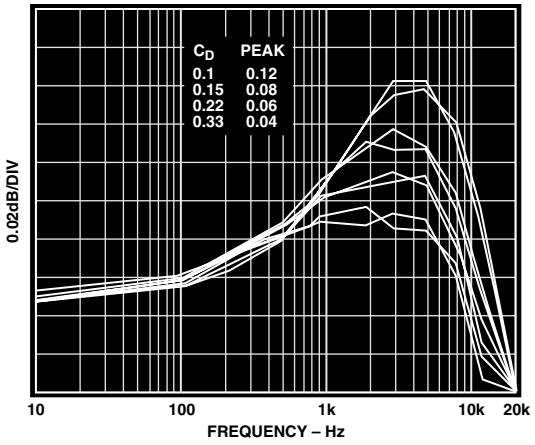


Figure 11. Jitter Transfer vs. C_D

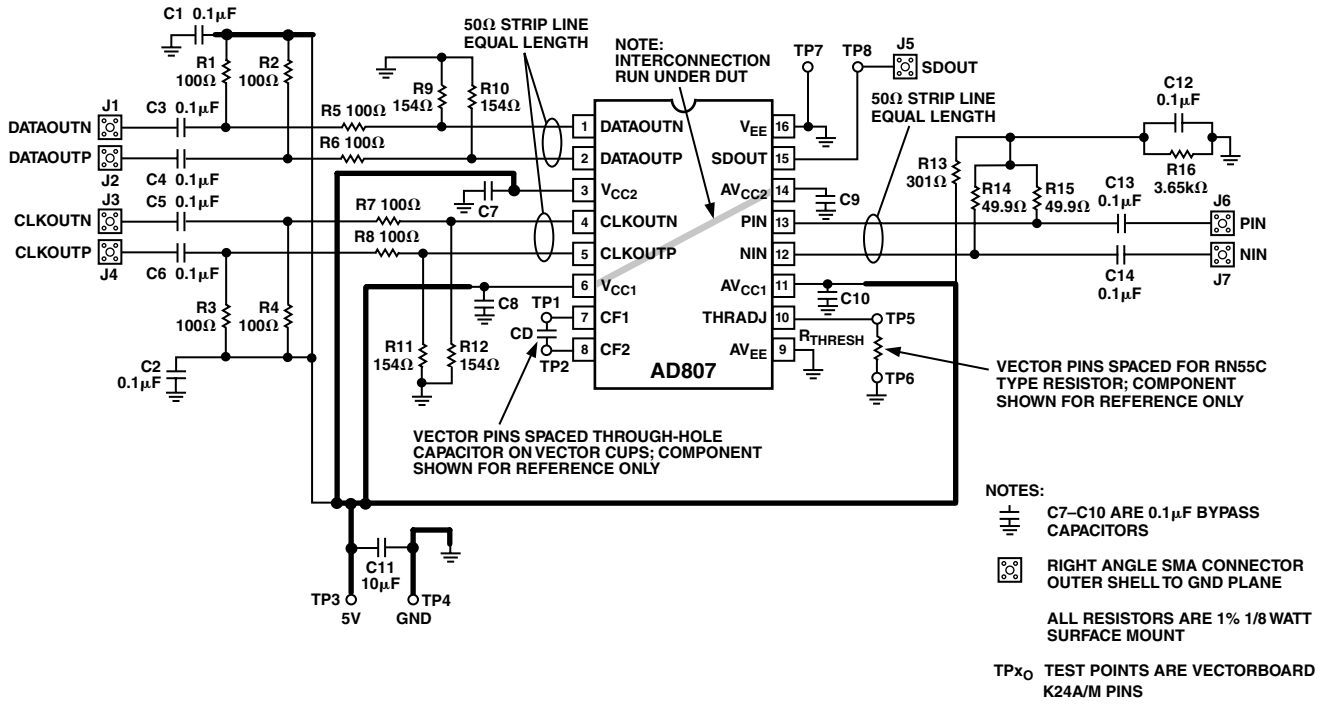


Figure 12. Evaluation Board Schematic

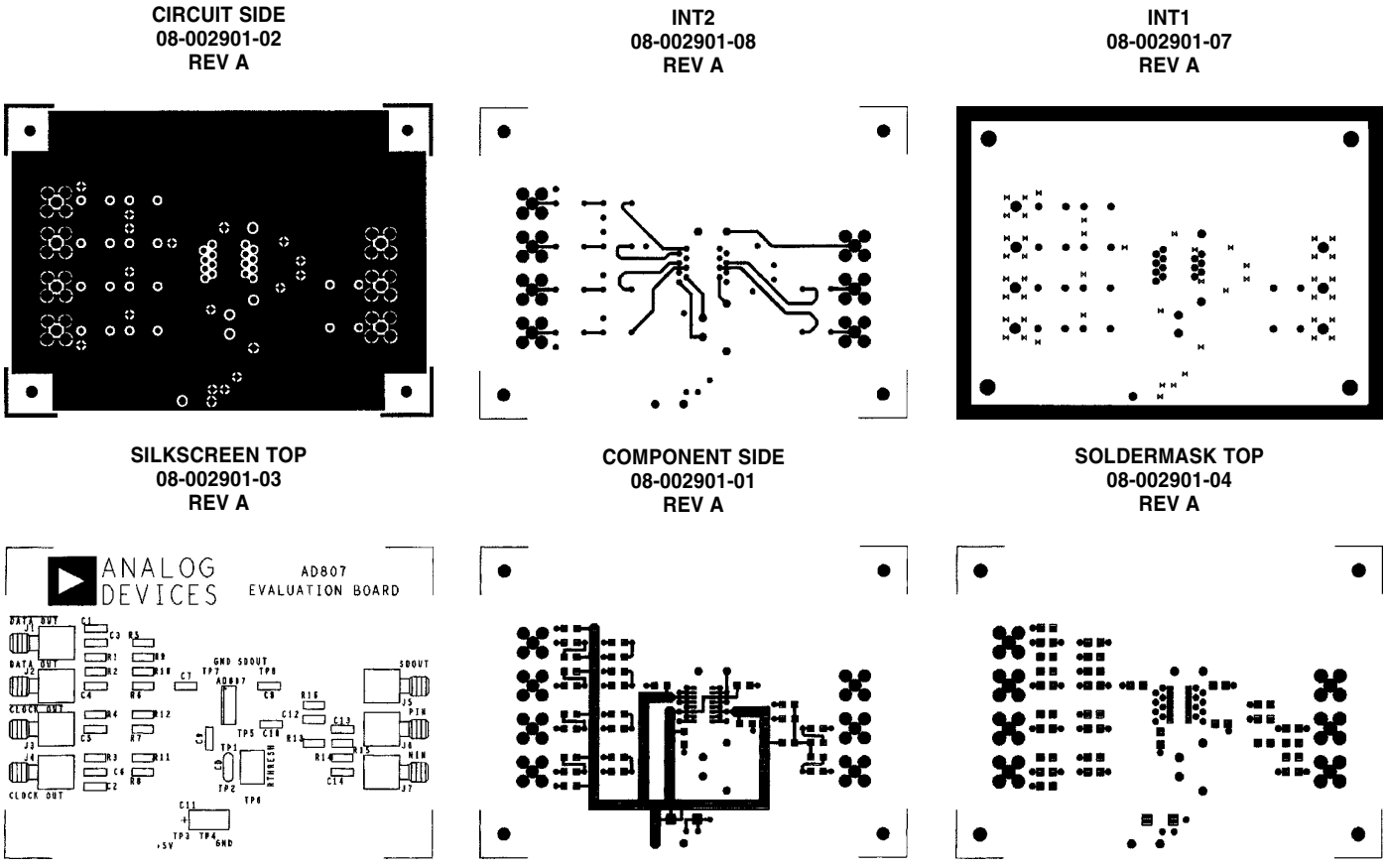


Figure 13. Evaluation Board Pictorials

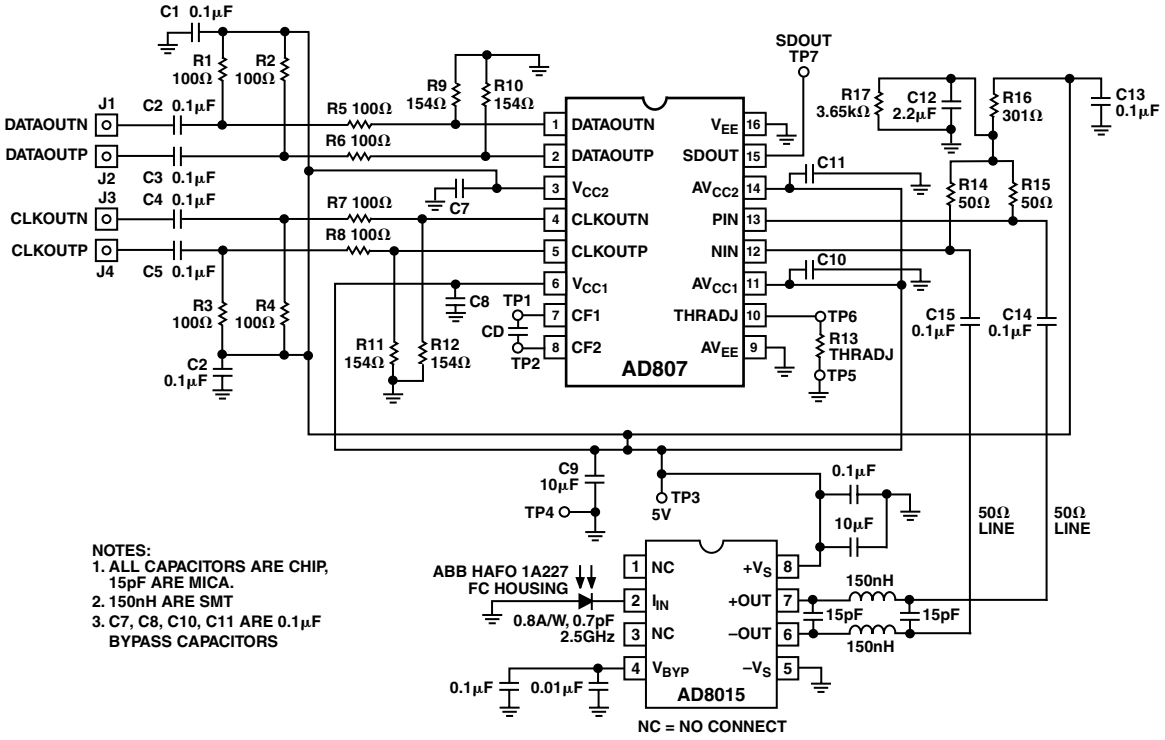


Figure 14. Low Cost 155 Mbps Fiber Optic Receiver Schematic

Table I. AD807—AD8015 Fiber Optic Receiver Circuit: Output Bit Error Rate and Output Jitter vs. Input Power

Average Optical Input Power (dBm)	Output Bit Error Rate	Output Jitter (ps rms)
–6.4	Loses Lock	
–6.5	7.5×10^{-3}	
–6.6	9.4×10^{-4}	
–6.7	0×10^{-14}	
–7.0 to –35.5	0×10^{-14}	<40
–36.0	3×10^{-12}	<40
–36.5	4.8×10^{-10}	
–37.0	2.8×10^{-8}	
–38.0	1.3×10^{-5}	
–39.0	1.0×10^{-3}	
–39.2	1.9×10^{-3}	
–39.3	Loses Lock	

APPLICATIONS

Low Cost 155 Mbps Fiber Optic Receiver

The AD807 and AD8015 can be used together for a complete 155 Mbps Fiber Optic Receiver (Quantizer and Clock Recovery, and Transimpedance Amplifier) as shown in Figure 14.

The PIN diode front end is connected to a single mode 1300 nm laser source. The PIN diode has 3.3 V reverse bias, 0.8 A/W responsively, 0.7 pF capacitance, and 2.5 GHz bandwidth.

The AD8015 outputs (P_{OUT} and N_{OUT}) drive a differential, constant impedance (50 Ω) low-pass filter with a 3 dB cutoff of 100 MHz. The outputs of the low-pass filter are ac coupled to the AD807 inputs (PIN and NIN). The AD807 PLL damping factor is set at 7 using a 0.22 μF capacitor.

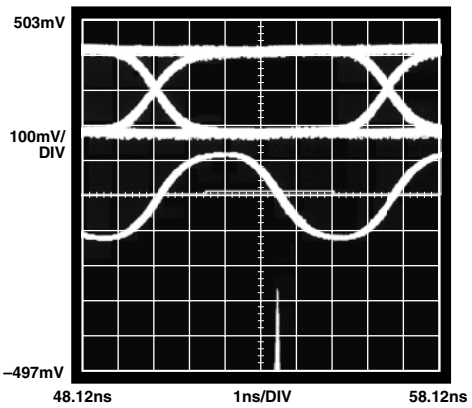


Figure 15. Receiver Output (Data) Eye Diagram, –7.0 dBm Optical Input

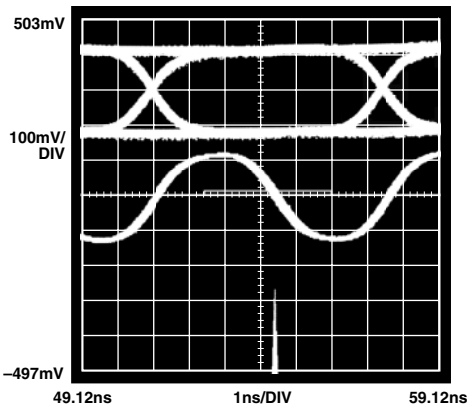


Figure 16. Receiver Output (Data) Eye Diagram, –36.0 dBm Optical Input

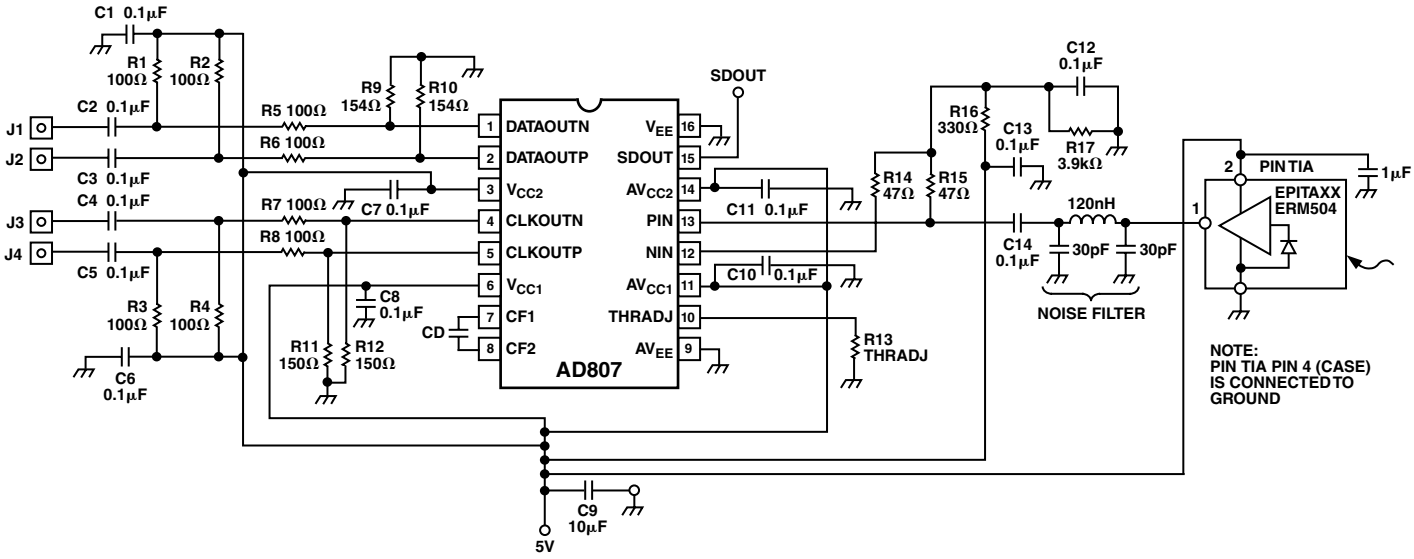


Figure 17. AD807 Application with Epitaxx PIN—Transimpedance Amplifier Module

The entire circuit was enclosed in a shielded box. Table I summarizes results of tests performed using a 2^{23}-1 PRN Sequence, and varying the average power at the PIN diode.

The circuit acquires and maintains lock with an average input power as low as –39.25 dBm.

Table II. AD807—Epitaxx ERM504 PIN TIA 155 Mbps Fiber Optic Receiver Circuit: Output Bit Error Rate and Output Jitter vs. Average Input Power

Average Optical Input Power (dBm)	Output Bit Error Rate	Output Jitter (ps rms)
0	0.0×10^{-10}	29
–3	0.0×10^{-10}	35
–10	0.0×10^{-10}	40
–20	0.0×10^{-10}	37
–30	0.0×10^{-10}	33
–32	0.0×10^{-10}	35
–34	0.0×10^{-10}	36
–35	0.0×10^{-10}	39
–35.5	0.0×10^{-10}	40
–36	0.0×10^{-10}	41
–37.0	0.0×10^{-10}	42
–37.6	0.5×10^{-10}	43
–38.0	4×10^{-6}	50

SONET (OC-3)/SDH (STM-1) Fiber Optic Receiver Circuit

A light wave receiver circuit for SONET/SDH application at 155 Mbps is shown in Figure 17, with test results given in Table II. The circuit operates from a single 5 V supply, and uses two major components: an Epitaxx ERM504 PIN-TIA module with AGC, and the AD807 IC.

A 120 MHz, third order, low-pass Butterworth filter at the output of the PIN-TIA module provides adequate bandwidth (70% of the bit rate), and attenuates high frequency (out of band) noise.

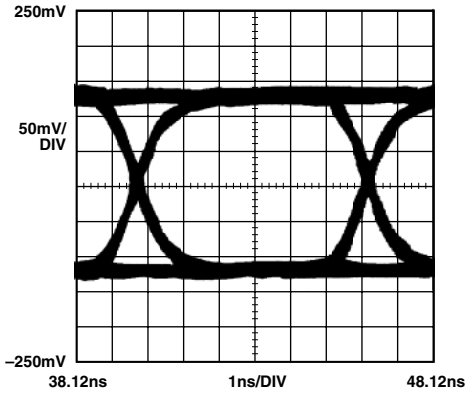


Figure 18. Receiver Output (Data) Eye Diagram, 0 dBm Optical Input

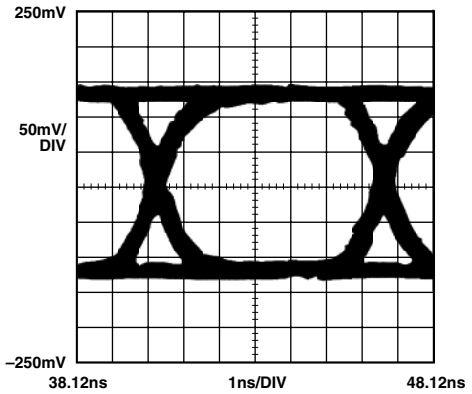


Figure 19. Receiver Output (Data) Eye Diagram, –38 dBm Optical Input

USING THE AD807

Ground Planes

Use of one ground plane for connections to both analog and digital grounds is recommended.

Power Supply Connections

Use of a 10 µF capacitor between V_{CC} and ground is recommended. Care should be taken to isolate the 5 V power trace to V_{CC2} (Pin 3). The V_{CC2} pin is used inside the device to provide the CLKOUT and DATAOUT signals.

Use of 0.1 µF capacitors between IC power supply and ground is recommended. Power supply decoupling should take place as close to the IC as possible. Refer to the schematic, Figure 12, for recommended connections.

Transmission Lines

Use of 50 Ω transmission lines are recommended for PIN, NIN, CLKOUT, and DATAOUT signals.

Terminations

Termination resistors should be used for PIN, NIN, CLKOUT, and DATAOUT signals. Metal, thick film, 1% tolerance resistors are recommended. Termination resistors for the PIN, NIN signals should be placed as close as possible to the PIN, NIN pins.

Connections from 5 V to load resistors for PIN, NIN, CLKOUT, and DATAOUT signals should be individual, not daisy chained. This will avoid crosstalk on these signals.

Loop Damping Capacitor, C_D

A ceramic capacitor may be used for the loop damping capacitor. Using a 0.15 µF, ±20% capacitor for a damping factor of five provides < 0.1 dB jitter peaking.

AD807 Output Squelch Circuit

A simple P-channel FET circuit can be used in series with the Output Signal ECL Supply (V_{CC2}, Pin 3) to squelch clock and data outputs when SDOUT indicates a loss of signal (Figure 20). The V_{CC2} supply pin draws roughly 61 mA (14 mA for each of 4 ECL loads, plus 5 mA for all 4 ECL output stages). This means that selection of a FET with ON RESISTANCE of 0.5 Ω will affect the common mode of the ECL outputs by only 31 mV.

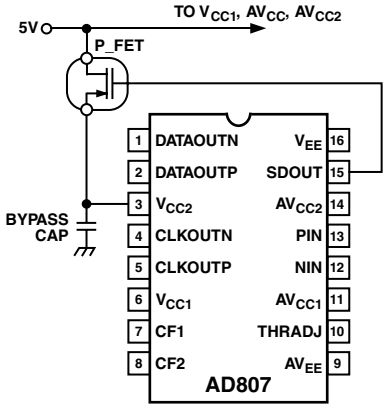
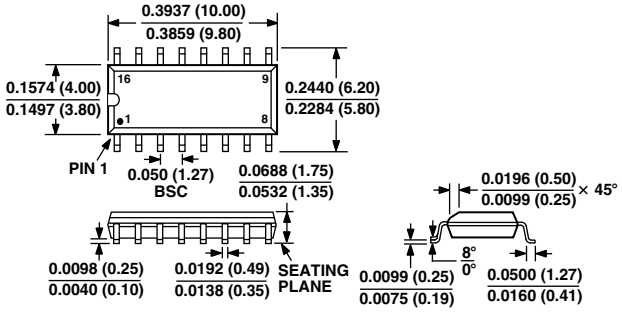


Figure 20. Squelch Circuit Schematic

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Small Outline IC Package (R-16A)



C00862–0–12/00 (rev. B)

PRINTED IN U.S.A.