260 MHz, 16 × 8 Buffered Video Crosspoint Switches

AD8110/AD8111

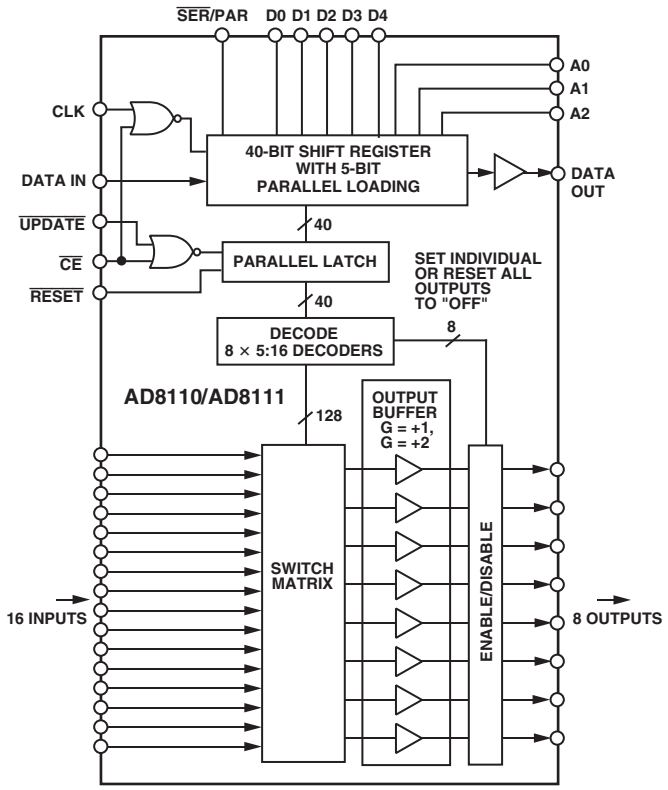
FEATURES

- 16 × 8 High-Speed Nonblocking Switch Arrays
  - AD8110: G = +1
  - AD8111: G = +2
- Serial or Parallel Switch Array Control
- Serial Data Out Allows "Daisy Chaining" of Multiple Crosspoints to Create Larger Switch Arrays
- Pin-Compatible with AD8108/AD8109 8 × 8 Switch Arrays
- For a 16 × 16 Array See AD8116
- Complete Solution
  - Buffered Inputs
  - Eight Output Amplifiers, AD8110 (G = +1), AD8111 (G = +2)
  - Drives 150 V Loads
- Excellent Video Performance
  - 60 MHz 0.1 dB Gain Flatness
  - 0.02% Differential Gain Error (R_L = 150 V)
  - 0.028 Differential Phase Error (R_L = 150 V)
- Excellent AC Performance
  - 260 MHz –3 dB Bandwidth
  - 500 V/ms Slew Rate
- Low Power of 50 mA
- Low All Hostile Crosstalk of –78 dB @ 5 MHz
- Output Disable Allows Direct Connection of Multiple Device Outputs
- Reset Pin Allows Disabling of All Outputs (Connected Through a Capacitor to Ground Provides "Power-On" Reset Capability)
- Excellent ESD Rating: Exceeds 4000 V Human Body Model
- 80-Lead LQFP Package (12 mm × 12 mm)

APPLICATIONS

- Routing of High-Speed Signals Including:
  - Composite Video (NTSC, PAL, S, SECAM)
  - Component Video (YUV, RGB)
  - Compressed Video (MPEG, Wavelet)
  - 3-Level Digital Video (HDB3)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8110 and AD8111 are high-speed 16 × 8 video crosspoint switch matrices. They offer a –3 dB signal bandwidth greater than 260 MHz, and channel switch times of less than 25 ns with 1% settling. With –78 dB of crosstalk and –97 dB isolation (@ 5 MHz), the AD8110/AD8111 are useful in many high-speed applications. The differential gain and differential phase of better than 0.02% and 0.02° respectively, along with 0.1 dB flatness out to 60 MHz, make the AD8110/AD8111 ideal for video signal switching.

The AD8110 and AD8111 include eight independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs so that off channels do not load the output bus. The AD8110 has a gain of +1, while the AD8111 offers a gain of +2. They operate on voltage supplies of ±5 V while consuming only 50 mA of idle current. The channel switching is performed via a serial digital control (which can accommodate "daisy chaining" of several devices) or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8110/AD8111 is packaged in an 80-lead LQFP package and is available over the extended industrial temperature range of –40°C to +85°C.

Rev. B
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AD8110/AD8111–SPECIFICATIONS (V_S = ±5 V, T_A = +25°C, R_L = 1 kΩ unless otherwise noted.)

Parameter	Conditions	AD8110/AD8111 Min	Typ	Max	Unit	Reference
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	200 mV p-p, R_L = 150 Ω	300/190	390/260		MHz	TPC 1, 7
	2 V p-p, R_L = 150 Ω		150		MHz	TPC 1, 7
Propagation Delay	2 V p-p, R_L = 150 Ω		5		ns	
Slew Rate	2 V Step, R_L = 150 Ω		500		V/µs	
Settling Time	0.1%, 2 V Step, R_L = 150 Ω		40		ns	TPC 6, 12
Gain Flatness	0.05 dB, 200 mV p-p, R_L = 150 Ω		60/40		MHz	TPC 1, 7
	0.05 dB, 2 V p-p, R_L = 150 Ω		65/40		MHz	TPC 1, 7
	0.1 dB, 200 mV p-p, R_L = 150 Ω		80/57		MHz	TPC 1, 7
	0.1 dB, 2 V p-p, R_L = 150 Ω		70/57		MHz	TPC 1, 7
NOISE/DISTORTION PERFORMANCE						
Differential Gain Error	NTSC or PAL, R_L = 1 kΩ		0.01		%	
	NTSC or PAL, R_L =150 Ω		0.02		%	
Differential Phase Error	NTSC or PAL, R_L = 1 kΩ		0.01		Degrees	
	NTSC or PAL, R_L = 150 Ω		0.02		Degrees	
Crosstalk, All Hostile	f = 5 MHz		–78/–85		dB	TPC 2, 8
	f = 10 MHz		–78/–85		dB	TPC 2, 8
Off Isolation, Input-Output	f = 5 MHz, R_L =150 Ω, One Channel		–97/–103		dB	TPC 17, 23
Input Voltage Noise	0.01 MHz to 50 MHz		15		nV/$\sqrt{\text{Hz}}$	TPC 14, 20
DC PERFORMANCE						
Gain Error	R_L = 1 kΩ		0.04/0.1	0.07/0.5	%	
	R_L = 150 Ω		0.15/0.25		%	
Gain Matching	No Load, Channel-Channel			0.02/1.0	%	
	R_L = 1 kΩ, Channel-Channel			0.09/1.0	%	
Gain Temperature Coefficient			0.5/8		ppm/°C	
OUTPUT CHARACTERISTICS						
Output Impedance	DC, Enabled		0.2		Ω	18, 24
	Disabled		10/0.001		MΩ	15, 21
Output Disable Capacitance	Disabled		2		pF	
Output Leakage Current	Disabled, AD8110 Only		1/NA		µA	
Output Voltage Range	No Load	±2.5	±3		V	
Output Current		20	40		mA	
Short Circuit Current			65		mA	
INPUT CHARACTERISTICS						
Input Offset Voltage	Worst Case (All Configurations)		5	20	mV	29, 35
	Temperature Coefficient		12		µV/°C	30, 36
Input Voltage Range		±2.5/±1.25	±3/±1.5		V	
Input Capacitance	Any Switch Configuration		2.5		pF	
Input Resistance		1	10		MΩ	
Input Bias Current	Per Output Selected		2	5	µA	
SWITCHING CHARACTERISTICS						
Enable On Time			60		ns	
Switching Time, 2 V Step	50% $\overline{\text{UPDATE}}$ to 1% Settling		25		ns	
Switching Transient (Glitch)	Measured at Output		20/30		mV p-p	16, 22
POWER SUPPLIES						
Supply Current	AVCC, Outputs Enabled, No Load		38		mA	
	AVCC, Outputs Disabled		15		mA	
	AVEE, Outputs Enabled, No Load		38		mA	
	AVEE, Outputs Disabled		15		mA	
	DVCC		11		mA	
Supply Voltage Range			±4.5 to ±5.5		V	
PSRR	f = 100 kHz		75/78		dB	13, 19
	f = 1 MHz		–55/–58		dB	
OPERATING TEMPERATURE RANGE						
Temperature Range	Operating (Still Air)		–40 to +85		°C	
θ_{JA}	Operating (Still Air)		48		°C/W	

Specifications subject to change without notice.

TIMING CHARACTERISTICS (Serial)

Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Serial Data Setup Time	t_1	20			ns
CLK Pulsewidth	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulsewidth	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			180	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off	–			8	ns
Data Load Time, CLK = 5 MHz, Serial Mode	–		8		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times	–			100	ns
$\overline{\text{RESET}}$ Time	–	200			ns

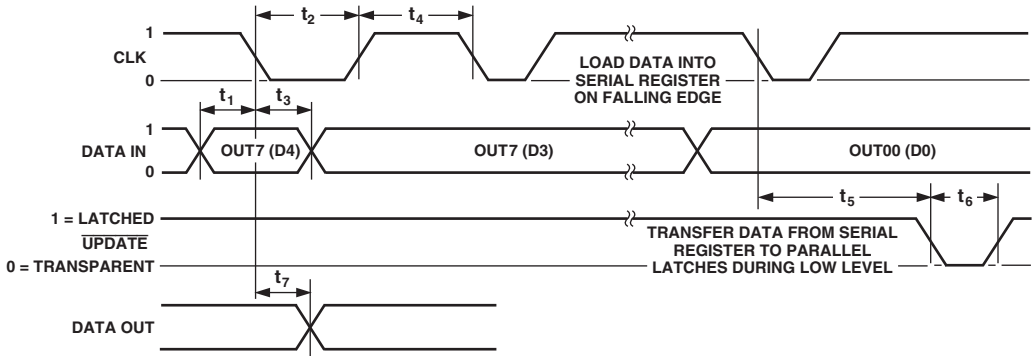


Figure 1. Timing Diagram, Serial Mode

Table I. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	–400 µA min	–400 µA max	3.0 mA min

TIMING CHARACTERISTICS (Parallel)

Parameter	Symbol	Limit Min	Limit Max	Unit
Data Setup Time	t_1	20		ns
CLK Pulsewidth	t_2	100		ns
Data Hold Time	t_3	20		ns
CLK Pulse Separation	t_4	100		ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0		ns
$\overline{\text{UPDATE}}$ Pulsewidth	t_6	50		ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off	–		8	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times	–		100	ns
$\overline{\text{RESET}}$ Time	–	200		ns

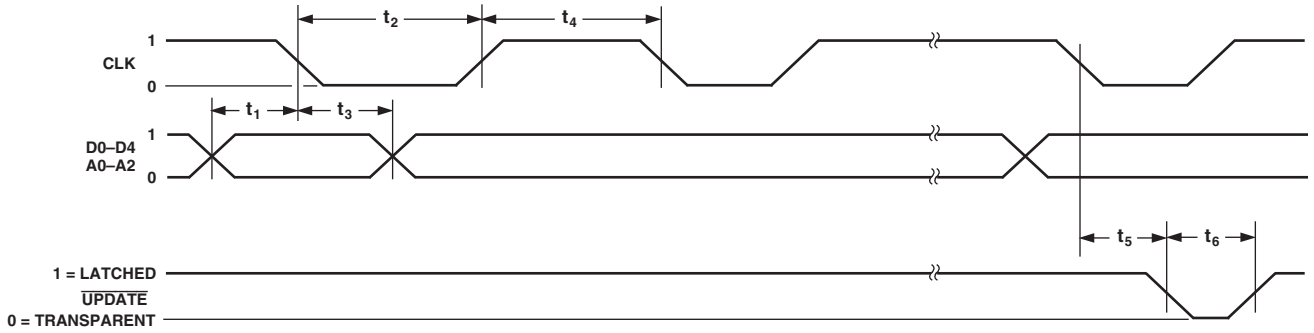


Figure 2. Timing Diagram, Parallel Mode

Table II. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 μA max	–400 μA min	–400 μA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.0 V
Internal Power Dissipation[2]
AD8110/AD8111 80-Lead Plastic LQFP (ST) . . . . . 2.6 W
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air (T_A = 25°C):
80-lead plastic LQFP (ST): θ_{JA} = 48°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8110/AD8111 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8110/AD8111 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

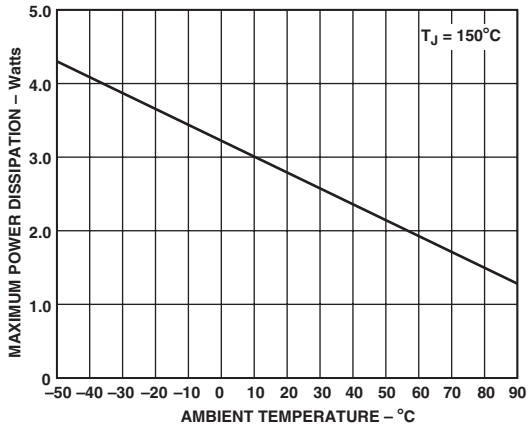


Figure 3. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8110/AD8111 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table III. Operation Truth Table

$\overline{CE}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	$\overline{SER}$/PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	↑	Data $_i$	Data $_{i-40}$	1	0	The data on the serial DATA IN line is loaded into serial register. The first bit clocked into the serial register appears at DATA OUT 40 clocks later.
0	1	↑	D0 . . . D4, A0 . . . A2	NA in Parallel Mode	1	1	The data on the parallel data lines, D0–D4, are loaded into the 40-bit serial shift register location addressed by A0–A2.
0	0	X	X	X	1	X	Data in the 40-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

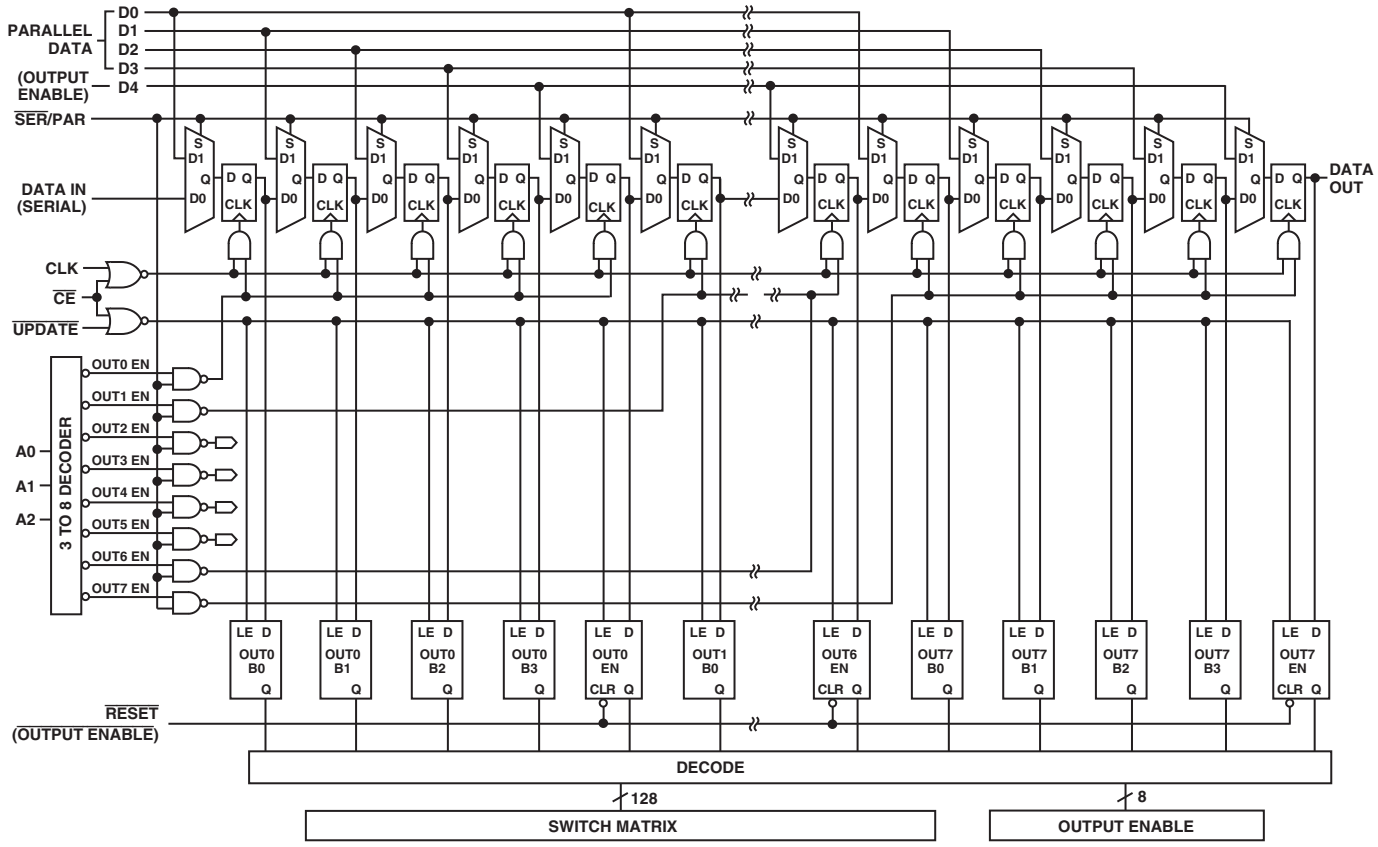
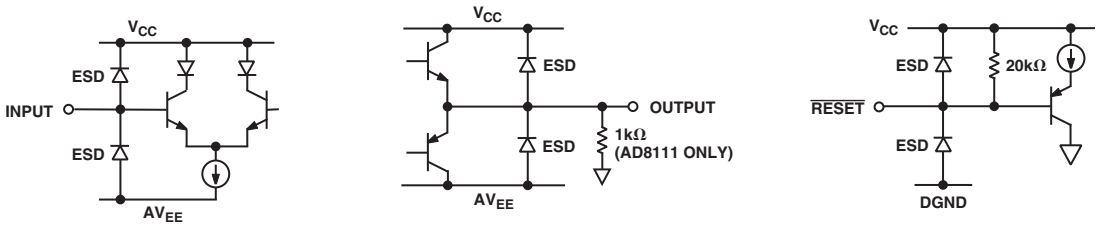


Figure 4. Logic Diagram

PIN FUNCTION DESCRIPTIONS

Pin Name	Pin Numbers	Pin Description
INxx	66, 68, 70, 72, 74, 76, 78, 1, 3, 5, 7, 9, 11, 13, 15, 64	Analog Inputs; xx = Channel Numbers 00 Through 15.
DATA IN	57	Serial Data Input, TTL Compatible.
CLK	58	Clock, TTL Compatible. Falling Edge Triggered.
DATA OUT	59	Serial Data Out, TTL Compatible.
$\overline{\text{UPDATE}}$	56	Enable (Transparent) "Low." Allows serial register to connect directly to switch matrix. Data latched when "High."
$\overline{\text{RESET}}$	61	Disable Outputs, Active "Low."
$\overline{\text{CE}}$	60	Chip Enable, Enable "Low." *Must be "low" to clock in and latch data.*
$\overline{\text{SER}}$/PAR	55	Selects Serial Data Mode, "Low" or Parallel Data Mode, "High." *Must be connected.*
OUTyy	41, 38, 35, 32, 29, 26, 23, 20	Analog Outputs yy = Channel Numbers 00 Through 07.
AGND	2, 4, 6, 8, 10, 12, 14, 16, 46 65, 67, 69, 71, 73, 75, 77	Analog Ground for Inputs and Switch Matrix.
DVCC	63, 79	5 V for Digital Circuitry.
DGND	62, 80	Ground for Digital Circuitry.
AVEE	17, 45	–5 V for Inputs and Switch Matrix.
AVCC	18, 44	+5 V for Inputs and Switch Matrix.
AGNDxx	42, 39, 36, 33, 30, 27, 24, 21	Ground for Output Amp, xx = Output Channel Numbers 00 Through 07. *Must be connected.*
AVCCxx/yy	43, 37, 31, 25, 22, 19	+5 V for Output Amplifier that is shared by Channel Numbers xx and yy. *Must be connected.*
AVEExx/yy	40, 34, 28, 22	–5 V for Output Amplifier that is shared by Channel Numbers xx and yy. *Must be connected.*
A0	54	Parallel Data Input, TTL Compatible (Output Select LSB).
A1	53	Parallel Data Input, TTL Compatible (Output Select).
A2	52	Parallel Data Input, TTL Compatible (Output Select MSB).
D0	51	Parallel Data Input, TTL Compatible (Input Select LSB).
D1	50	Parallel Data Input, TTL Compatible (Input Select).
D2	49	Parallel Data Input, TTL Compatible (Input Select).
D3	48	Parallel Data Input, TTL Compatible (Input Select MSB).
D4	47	Parallel Data Input, TTL Compatible (Output Enable).

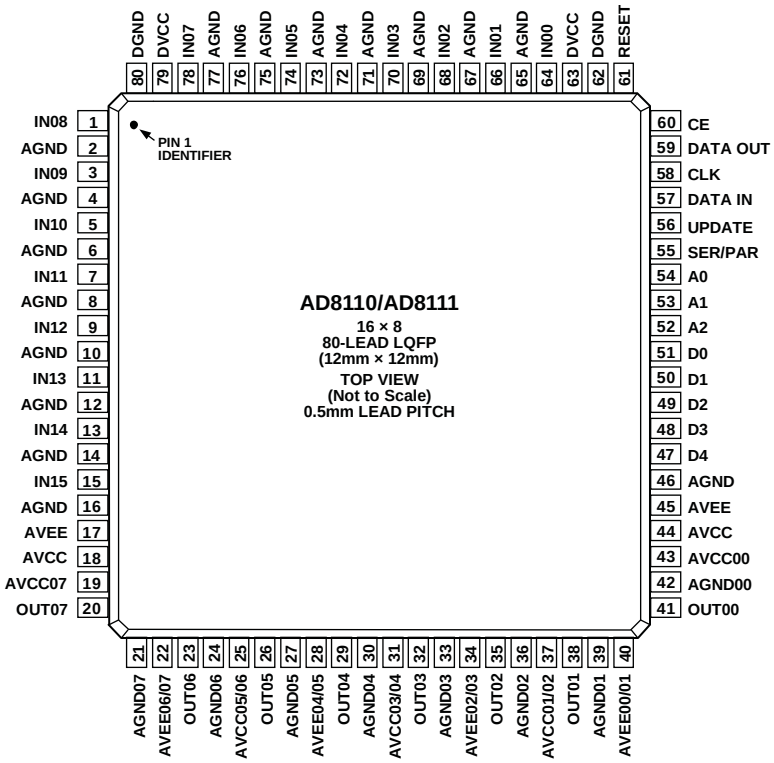


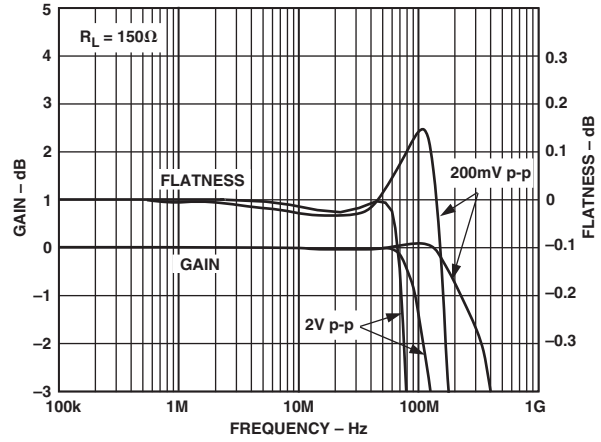
a. Analog Input *b. Analog Output* *c. $\overline{\text{Reset}}$ Input*

d. Logic Input *e. Logic Output*

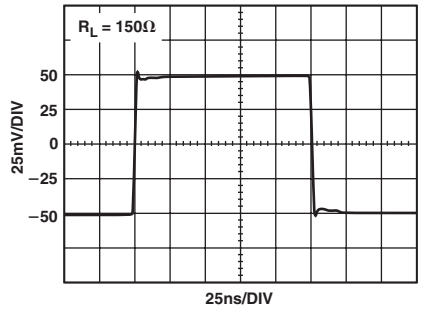
Figure 5. I/O Schematics

PIN CONFIGURATION

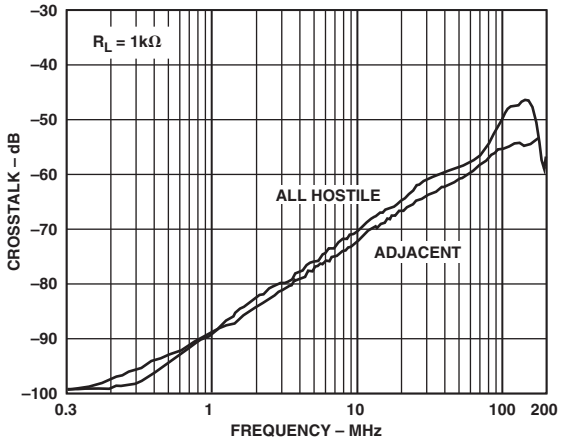




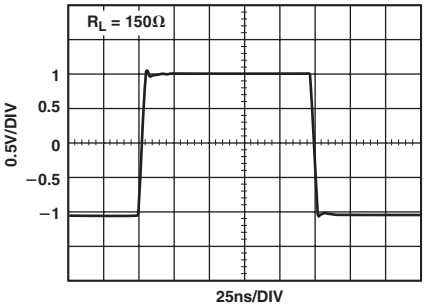
TPC 1. AD8110 Frequency Response



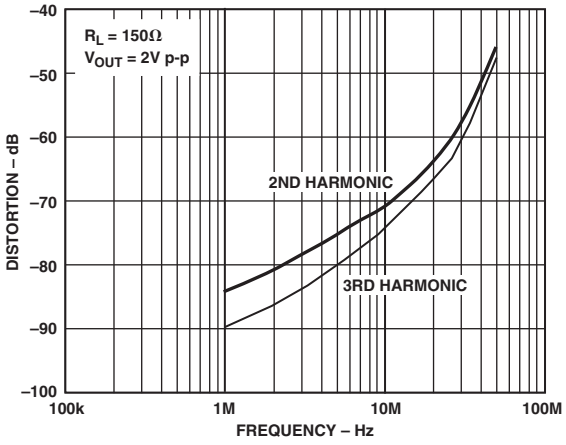
TPC 4. AD8110 Step Response, 100 mV Step



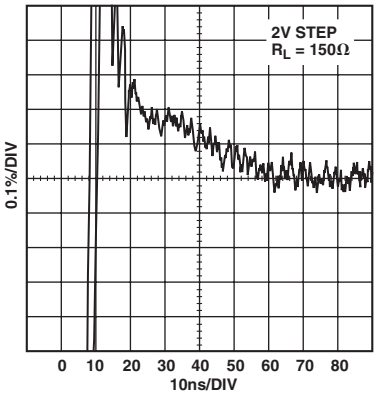
TPC 2. AD8110 Crosstalk vs. Frequency



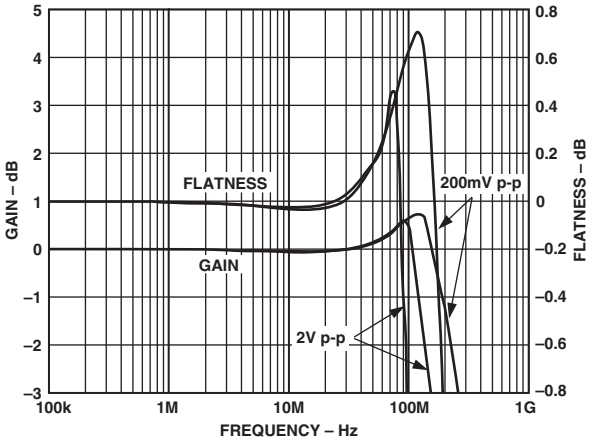
TPC 5. AD8110 Step Response, 2 V Step



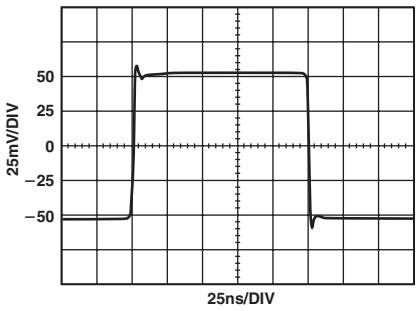
TPC 3. AD8110 Distortion vs. Frequency



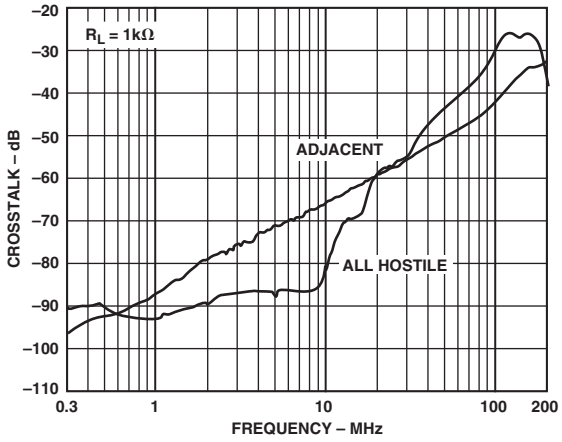
TPC 6. AD8110 Settling Time



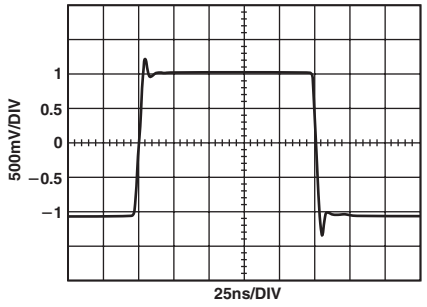
TPC 7. AD8111 Frequency Response



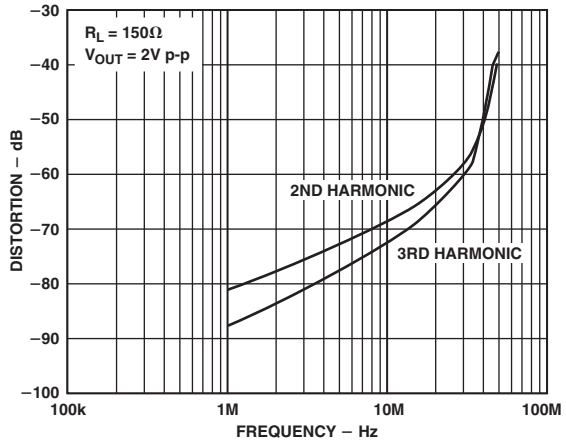
TPC 10. AD8111 Step Response, 100 mV Step



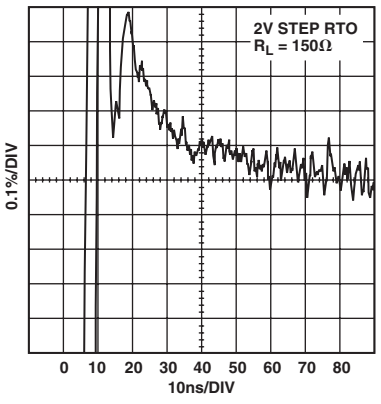
TPC 8. AD8111 Crosstalk vs. Frequency



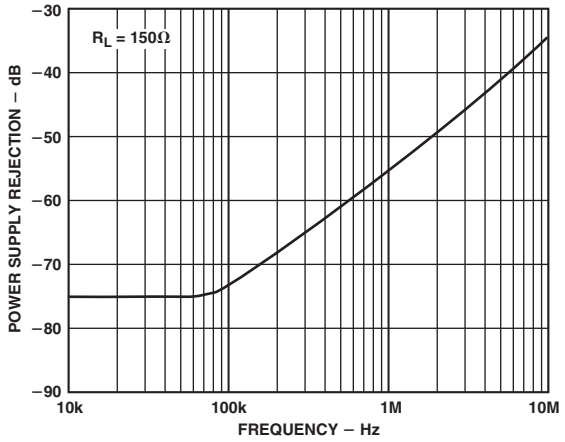
TPC 11. AD8111 Step Response, 2 V Step



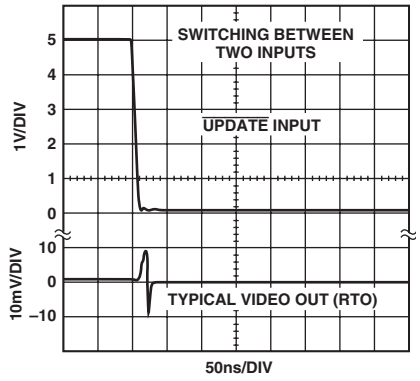
TPC 9. AD8111 Distortion vs. Frequency



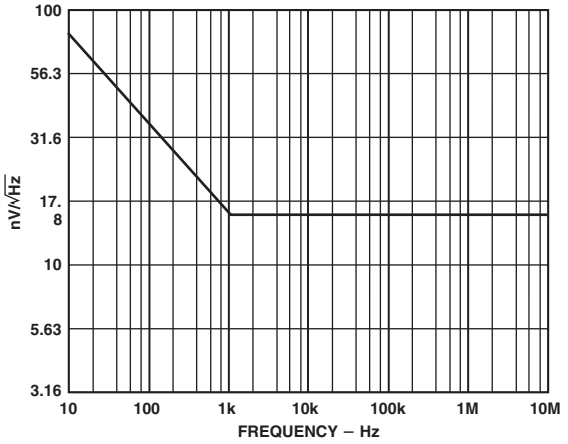
TPC 12. AD8111 Settling Time



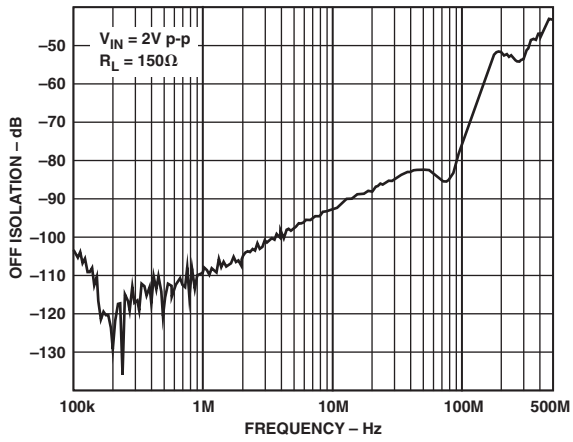
TPC 13. AD8110 PSRR vs. Frequency



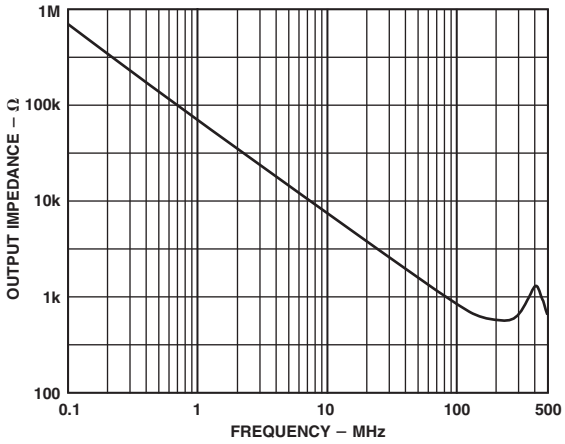
TPC 16. AD8110 Switching Transient (Glitch)



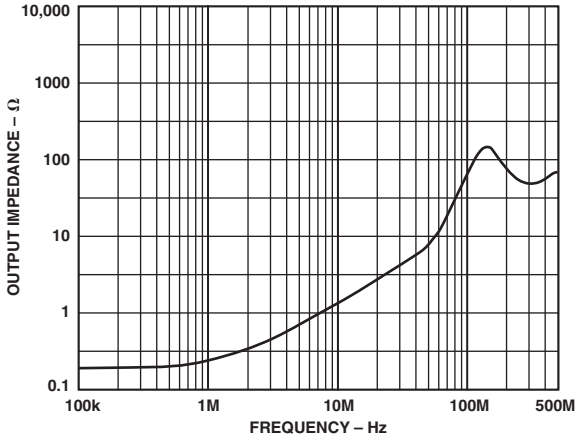
TPC 14. AD8110 Voltage Noise vs. Frequency



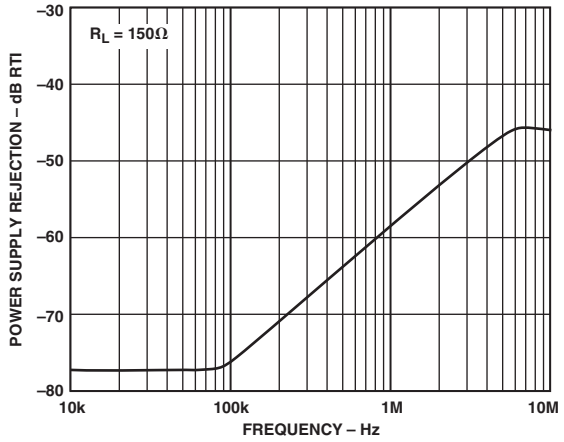
TPC 17. AD8110 Off Isolation, Input-Output



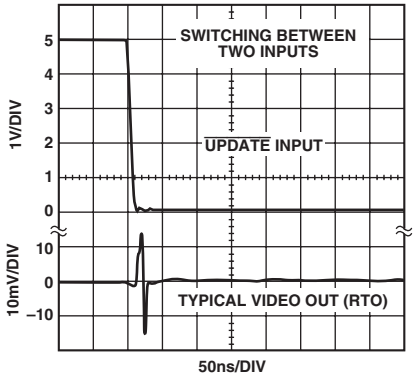
TPC 15. AD8110 Output Impedance, Disabled



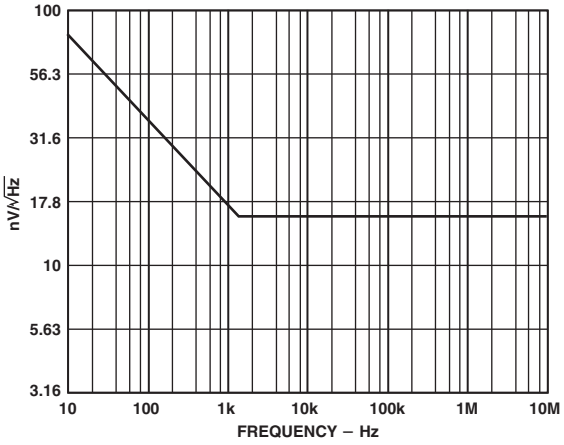
TPC 18. AD8110 Output Impedance, Enabled



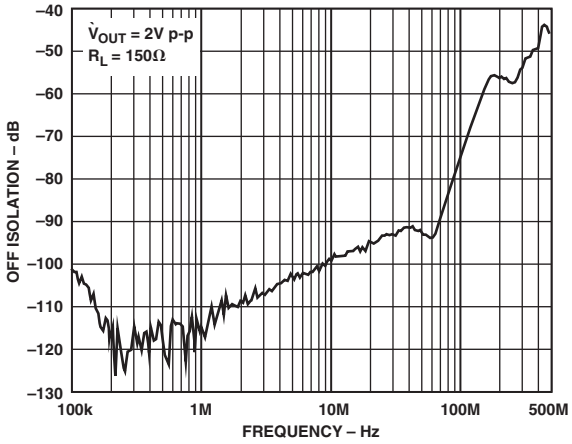
TPC 19. AD8111 PSRR vs. Frequency



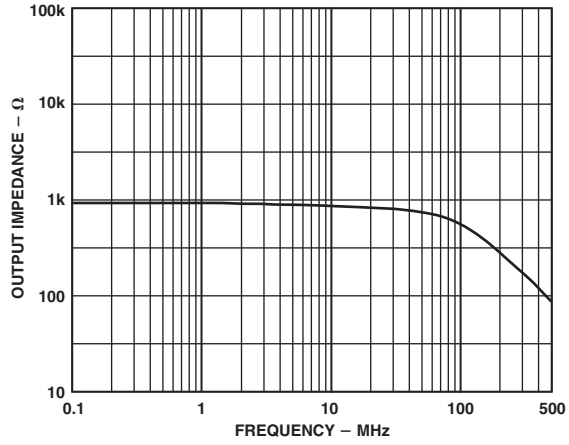
TPC 22. AD8111 Switching Transient (Glitch)



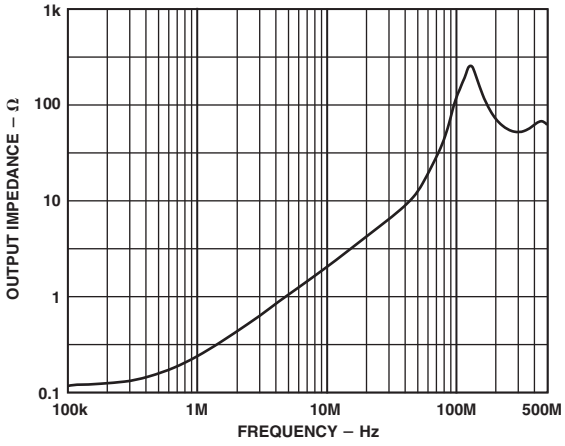
TPC 20. AD8111 Voltage Noise vs. Frequency



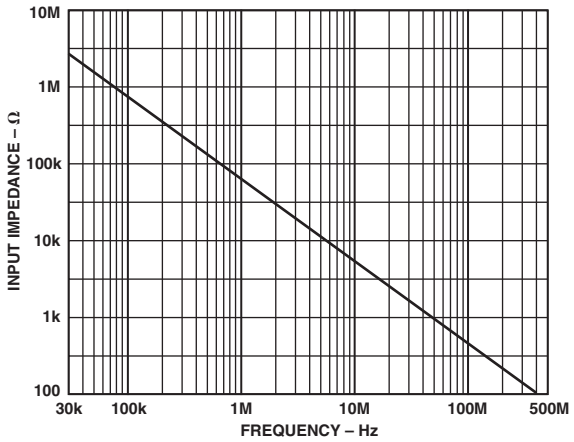
TPC 23. AD8111 Off Isolation, Input-Output



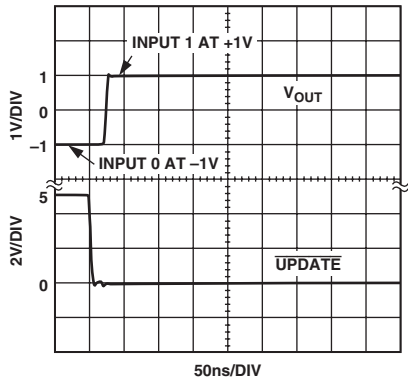
TPC 21. AD8111 Output Impedance, Disabled



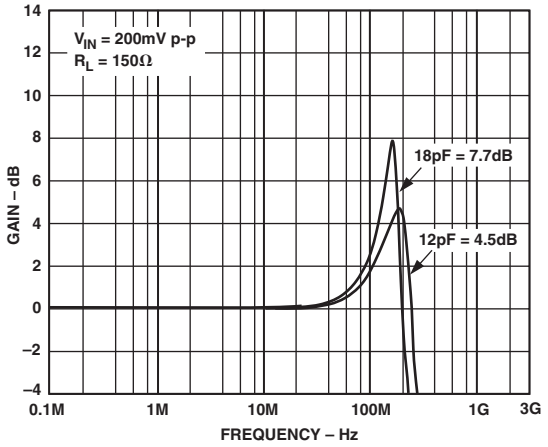
TPC 24. AD8111 Output Impedance, Enabled



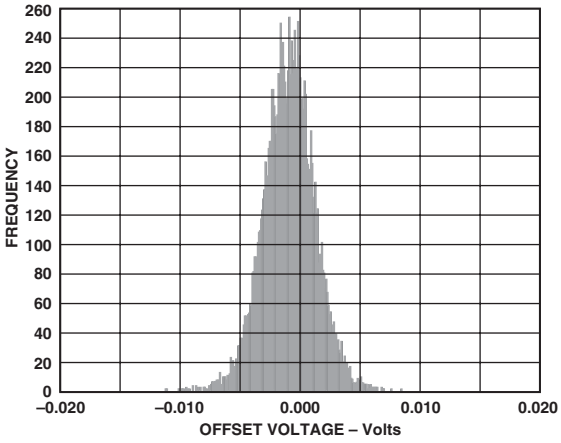
TPC 25. AD8110 Input Impedance vs. Frequency



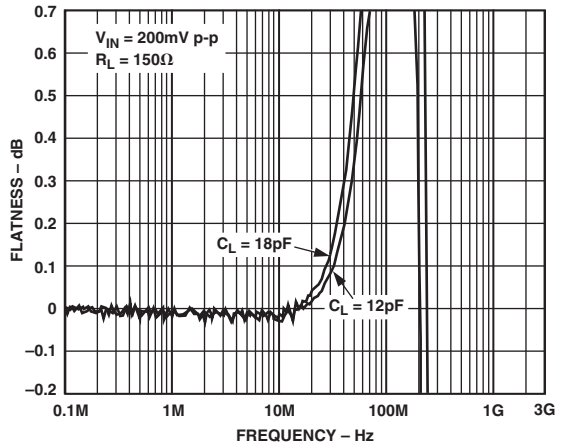
TPC 28. AD8110 Switching Time



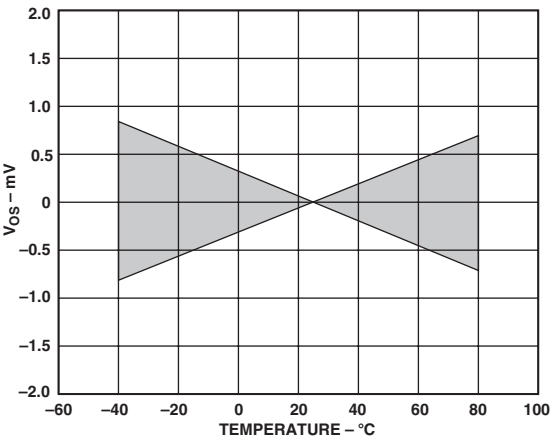
TPC 26. AD8110 Frequency Response vs. Capacitive Load



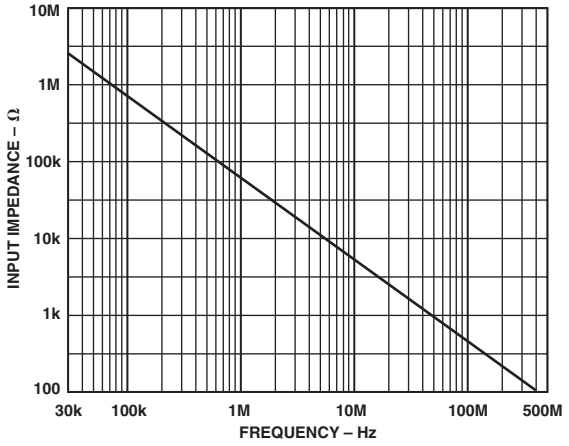
TPC 29. AD8110 Offset Voltage Distribution



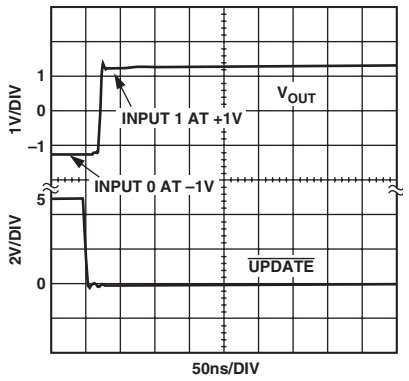
TPC 27. AD8110 Flatness vs. Capacitive Load



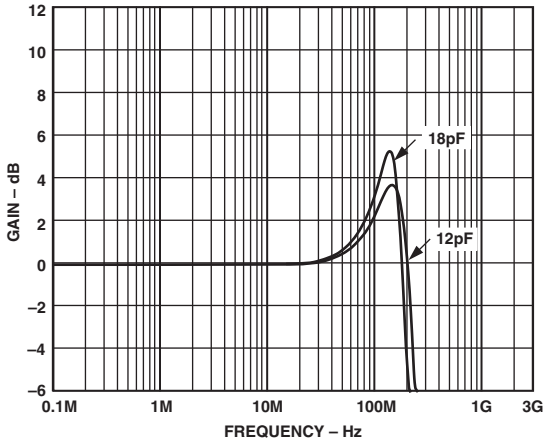
TPC 30. AD8110 Offset Voltage vs. Temperature (Normalized at 25°C)



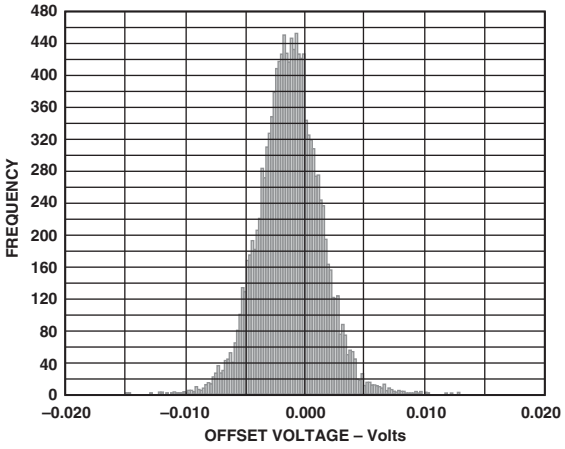
TPC 31. AD8111 Input Impedance vs. Frequency



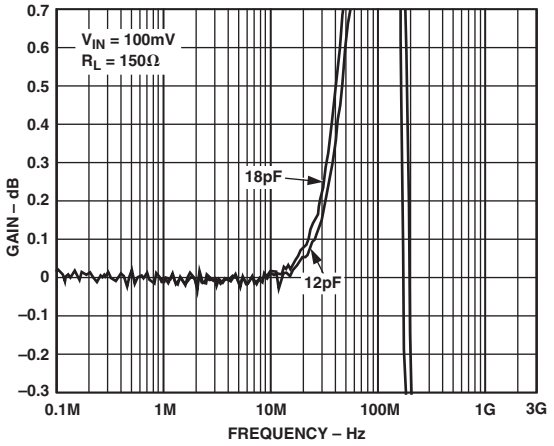
TPC 34. AD8111 Switching Time



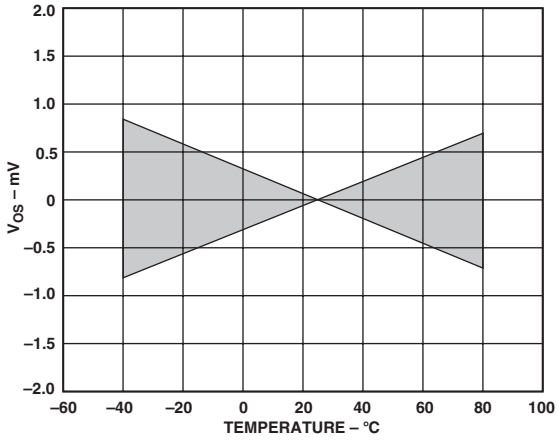
TPC 32. AD8111 Frequency Response vs. Capacitive Load



TPC 35. AD8111 Offset Voltage Distribution (RTI)



TPC 33. AD8111 Flatness vs. Capacitive Load



TPC 36. AD8111 Offset Voltage Drift vs. Temperature (Normalized at 25°C)

THEORY OF OPERATION

The AD8110 (G = +1) and AD8111 (G = +2) share a common core architecture consisting of an array of 128 transconductance (gm) input stages organized as eight 16:1 multiplexers with a common, 16-line analog input bus. Each multiplexer is basically a folded-cascode high-speed voltage feedback amplifier with 16 input stages. The input stages are NPN differential pairs whose differential current outputs are combined at the output stage, which contains the high impedance node, compensation and a complementary emitter follower output buffer. In the AD8110, the output of each multiplexer is fed directly back to the inverting inputs of its 16 gm stages. In the AD8111, the feedback network is a voltage divider consisting of two equal resistors.

This switched-gm architecture results in a low power crosspoint switch that is able to directly drive a back terminated video load (150 Ω) with low distortion (differential gain and differential phase errors are better than 0.02% and 0.02°, respectively). This design also achieves high input resistance and low input capacitance without the signal degradation and power dissipation of additional input buffers. However, the small input bias current at any input will increase almost linearly with the number of outputs programmed to that input.

The output disable feature of these crosspoints allows larger switch matrices to be built simply by busing together the outputs of multiple 16 × 8 ICs. However, while the disabled output impedance of the AD8110 is very high (10 MΩ), that of the AD8111 is limited by the resistive feedback network (which has a nominal total resistance of 1 kΩ) that appears in parallel with the disabled output. If the outputs of multiple AD8111s are connected through separate back termination resistors, the loading due to these finite output impedances will lower the effective back termination impedance of the overall matrix. This problem is eliminated if the outputs of multiple AD8111s are connected directly and share a single back termination resistor for each output of the overall matrix. This configuration increases the capacitive loading of the disabled AD8111 on the output of the enabled AD8111.

APPLICATIONS

The AD8110/AD8111 have two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 40 bits can be provided that will update the entire matrix each time. The second option allows for changing a single output's programming via a parallel interface. The serial option requires fewer signals, but requires more time (clock cycles) for changing the programming, while the parallel programming technique requires more signals, but can change a single output at a time and requires fewer clock cycles to complete programming.

Serial Programming

The serial programming mode uses the device pins $\overline{CE}$, CLK, DATA IN, $\overline{UPDATE}$, and $\overline{SER}$/PAR. The first step is to assert a LOW on $\overline{SER}$/PAR in order to enable the serial programming mode. $\overline{CE}$ for the chip must be LOW to allow data to be clocked into the device. The $\overline{CE}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{UPDATE}$ signal should be HIGH during the time that data is shifted into the device's serial port. Although the data will still shift in when $\overline{UPDATE}$ is LOW, the transparent, asynchronous latches will allow the shifting data to reach the matrix. This will cause the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every down edge of CLK. A total of 40 data bits must be shifted in to complete the programming. For each of the eight outputs, there are four bits (D0–D3) that determine the source of its input followed, by one bit (D4) that determines the enabled state of the output. If D4 is LOW (output disabled) the four associated bits (D0–D3) do not matter, because no input will be switched to that output.

The most significant output address data is shifted in first, then following in sequence until the least significant output address data is shifted in. At this point $\overline{UPDATE}$ can be taken LOW, which will cause the programming of the device according to the data that was just shifted in. The $\overline{UPDATE}$ registers are asynchronous and when $\overline{UPDATE}$ is LOW (and $\overline{CE}$ is LOW), they are transparent.

If more than one AD8110/AD8111 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK, $\overline{CE}$, $\overline{UPDATE}$ and $\overline{SER}$/PAR pins should be connected in parallel and operated as described above. The serial data is input to the DATA IN pin of the first device of the chain, and it will ripple on through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence will be 40 times the number of devices in the chain.

Parallel Programming

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output at a time. Since this takes only one CLK/$\overline{UPDATE}$ cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the $\overline{RESET}$ signal *does not reset all registers* in the AD8110/AD8111. When taken low, the $\overline{RESET}$ signal will only set each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs will not be active at the same time.

After initial power-up, the internal registers in the device will generally have random data, even though the $\overline{RESET}$ signal was asserted. If parallel programming is used to program one output, that output will be properly programmed, but the rest of the device will have a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that *all outputs be programmed to a desired state after power-up.*

This will ensure that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output or more at a time.

In a similar fashion, if both $\overline{CE}$ and $\overline{UPDATE}$ are taken LOW after initial power-up, the random power-up data in the shift register will be programmed into the matrix. Therefore, in order to prevent the crosspoint from being programmed into an unknown state *do not apply low logic levels to both $\overline{CE}$ and $\overline{UPDATE}$ after power is initially applied.* Programming the full shift register one time to a desired state by either serial or parallel programming after initial power-up will eliminate the possibility of programming the matrix to an unknown state.

To change an output's programming via parallel programming, $\overline{SER}$/PAR and $\overline{UPDATE}$ should be taken HIGH and $\overline{CE}$ should be taken LOW. The CLK signal should be in the HIGH state. The address of the output that is to be programmed should be put on A0–A2. The first four data bits (D0–D3) should contain the information that identifies the input that is programmed to the output that is addressed. The fourth data bit (D4) will determine the enabled state of the output. If D4 is LOW (output disabled), the data on D0–D3 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a HIGH-to-LOW transition of the CLK signal. The matrix will not be programmed, however, until the $\overline{UPDATE}$ signal is taken low. Thus, it is possible to latch in new data for several or all of the outputs first via successive negative transitions of CLK while $\overline{UPDATE}$ is held high, and then have all the new data take effect when $\overline{UPDATE}$ goes LOW. This technique should be used when programming the device for the first time after power-up when using parallel programming.

POWER-ON RESET

When powering up the AD8110/AD8111 it is usually desirable to have the outputs come up in the disabled state. The $\overline{RESET}$ pin, when taken LOW will cause all outputs to be in the disabled state. However, the $\overline{RESET}$ signal *does not reset all registers* in the AD8110/AD8111. This is important when operating in the parallel programming mode. Please refer to that section for information about programming internal registers after power-up. Serial programming will program the entire matrix each time, so no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix or else the matrix can enter unknown states. To prevent this, *do not apply logic low signals to both $\overline{CE}$ and $\overline{UPDATE}$ initially after power-up.* The shift register should first be loaded with the desired data, and then $\overline{UPDATE}$ can be taken LOW to program the device.

The $\overline{RESET}$ pin has a 20 kΩ pull-up resistor to DVDD that can be used to create a simple power-up reset circuit. A capacitor from $\overline{RESET}$ to ground will hold $\overline{RESET}$ LOW for some time while the rest of the device stabilizes. The LOW condition will cause all the outputs to be disabled. The capacitor will then charge through the pull-up resistor to the HIGH state; thus allowing full programming capability of the device.

GAIN SELECTION

The 16 × 8 crosspoints come in two versions depending on the desired gain of the analog circuit paths. The AD8110 device is unity gain and can be used for analog logic switching and other applications where unity gain is desired. The AD8110 can also be used for the input and interior sections of larger crosspoint arrays where termination of output signals is not usually used. The AD8110 outputs have a very high impedance when their outputs are disabled.

For devices that will be used to drive a terminated cable with its outputs, the AD8111 can be used. This device has a built-in gain of two that eliminates the need for a gain-of-two buffer to drive a video line. Because of the presence of the feedback network in these devices, the disabled output impedance is about 1 kΩ.

If external amplifiers are used to provide a gain = +2, Analog Devices' AD8079 provides a fixed G = +2 function.

CREATING LARGER CROSSPOINT ARRAYS

The AD8110/AD8111 are high-density building blocks for creating crosspoint arrays of dimensions larger than 16 × 8. Various features such as output disable, chip enable, and gain-of-one- and-two options are useful for creating larger arrays. For very large arrays, they can be used along with the AD8116, a 16 × 16 video crosspoint device. In addition, when required for customizing a crosspoint array size, they can be used with the AD8108 and AD8109, a pair (unity gain and gain-of-two) of 8 × 8 video crosspoint switches.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices that are required. The 16 × 8 architecture of the AD8110/AD8111 contains 128 "points," which is a factor of 32 greater than a 4 × 1 crosspoint. The PC board area and power consumption savings are readily apparent when compared to using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Some nonblocking crosspoint architectures will require more than this minimum as calculated above. Also, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to "wire-OR" the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at a diagram. Figure 6 illustrates this concept for a 32 × 8 crosspoint array.

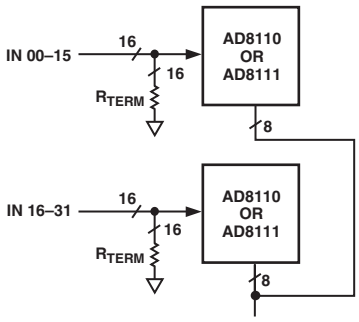


Figure 6. A 32 × 8 Crosspoint Array Using Two AD8110s or Two AD8111s

The inputs are each uniquely assigned to each of the 32 inputs of the two devices and terminated appropriately. The outputs are wire-ORed together in pairs. The output from only one of a wired OR pair should be enabled at any given time. The device programming software must be properly written to cause this to happen.

At some point, the number of outputs that are wire-ORed becomes too great to maintain system performance. This will vary according to which system specifications are most important. It will also depend on whether the matrix consists of AD8110s or AD8111s. The output disabled impedance of the AD8110 is much higher than that of the AD8111, so its disabled parasitics will have a smaller effect on the one output that is enabled. For example, a 128 × 8 crosspoint can be created with eight AD8110/AD8111s. This design will have 128 separate inputs and have the corresponding outputs of each device wire-ORed together in groups of eight.

Using additional crosspoint devices in the design can lower the number of outputs that must be wire-ORed together. Figure 7 shows a block diagram of a system using eight AD8110s and two AD8111s to create a nonblocking, gain-of-two, 128 × 8 crosspoint that restricts the wire-ORing at the output to only four outputs. These devices are the AD8110, which has a higher disabled output impedance than the AD8111.

Additionally, by using the lower four outputs from each of the two Rank 2 AD8111s, a blocking 128 × 16 crosspoint array can be realized. There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices will accumulate and the bandwidth limitations of the devices will compound. In addition, the extra devices will consume more current and take up more board space. Once again, the overall system design specifications will determine how to make the various tradeoffs.

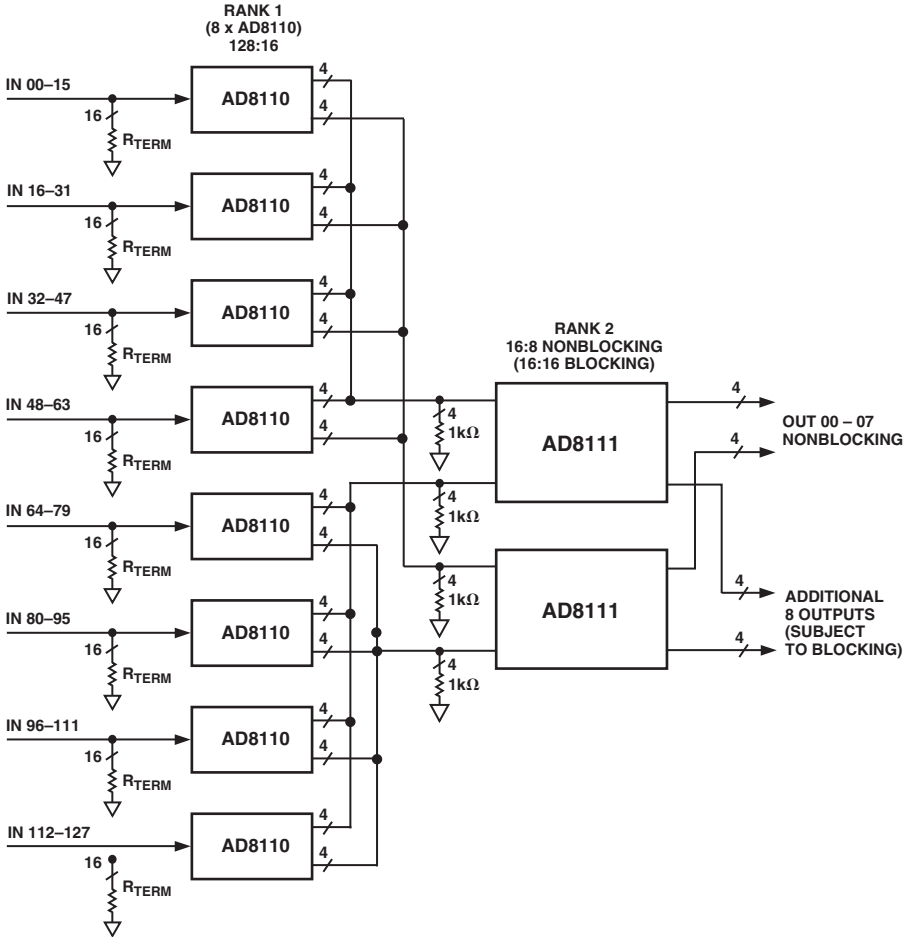


Figure 7. A Gain-of-Two 128 × 8 Nonblocking Crosspoint Array (128 × 16 Blocking)

Multichannel Video

The excellent video specifications of the AD8110/AD8111 make them ideal candidates for creating composite video crosspoint switches. These can be made quite dense by taking advantage of the AD8110/AD8111's high level of integration and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the AD8110/AD8111 requiring more than one crosspoint channel per video channel.

Some systems use twisted-pair wiring to carry video signals. These systems utilize differential signals and can lower costs because they use lower cost cables, connectors and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the video signals are differential; there is a positive and negative (or inverted) version of the signals. These complementary signals are transmitted onto each of the two wires of the twisted pair, yielding a first order zero common-mode signal. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that make up the video channel. Thus, one differential video channel is assigned to a pair of crosspoint channels, both input and output. For a single AD8110/AD8111, eight differential video channels can be assigned to the 16 inputs and four to the outputs. This will effectively form an 8×4 differential crosspoint switch.

Programming such a device will require that inputs and outputs be programmed in pairs. This information can be deduced by inspection of the programming format of the AD8110/AD8111 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One two-circuit format that is commonly being used in systems such as satellite TV, digital cable boxes and higher quality VCRs, is called S-video or Y/C video. This format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance, chroma or C) on a second channel.

Since S-video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems will be the same.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, blue) directly from the image sensors. RGB is also the usual format used by computers internally for graphics. RGB can also be converted to Y, R-Y, B-Y format, sometimes called YUV format. These three-circuit, video standards are referred to as component analog video.

The component video standards require three crosspoint channels per video channel to handle the switching function. In a fashion similar to the two-circuit video formats, the inputs and outputs are assigned in groups of three and the appropriate logic programming is performed to route the video signals.

CROSSTALK

Many systems, such as broadcast video, that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in proximity in a system, as will undoubtedly be the case in a system that uses the AD8110/AD8111, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more AD8110/AD8111s.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field and sharing of common impedances. This section will explain these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (e.g., free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields will then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot be simply added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

For a practical AD8110/AD8111 circuit, it is required that it be mounted to some sort of circuit board in order to connect it to power supplies and measurement equipment. Great care has been taken to create a characterization board that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that a system's crosstalk is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas of crosstalk when attempting to minimize its effect.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques will be discussed for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by:

$$|XT| = 20 \log_{10}\left(Asel(s)/Atest(s)\right)$$

where $s = jw$ is the Laplace transform variable, *Asel(s)* is the amplitude of the crosstalk-induced signal in the selected channel and *Atest(s)* is the amplitude of the test signal. It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal will have a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 × 8 matrix of the AD8110/AD8111, we can examine the number of crosstalk terms that can be considered for a single channel, say IN00 input. IN00 is programmed to connect to one of the AD8110/AD8111 outputs where the measurement can be made.

We can first measure the crosstalk terms associated with driving a test signal into each of the other 15 inputs one at a time. We can then measure the crosstalk terms associated with driving a parallel test signal into all 15 other inputs taken two at a time in all possible combinations; and then three at a time, etc., until, finally, there is only one way to drive a test signal into all 15 other inputs.

Each of these cases is legitimately different from the others and might yield a unique value depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then to specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other (not used for measurement) outputs are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8110/AD8111s is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure "all hostile" crosstalk. Su˘s term means that the crosstalk to the selected channel is measured, while all other system channels are driven in parallel. In general, this will yield the worst crosstalk number, but this is not always the case due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements will generally be higher than those of more distant channels, so they can serve as a worst-case measure for any other one-channel or two-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8110/AD8111 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (IN07 in the middle for this example) can be programmed to drive OUT03. The input to IN07 is just terminated to ground (via 50 or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), with all other outputs except OUT03 disabled. Since grounded IN07 is programmed to drive OUT03, there should be no signal present. Any signal that is present can be attributed to the other 15 hostile input signals, because no other outputs are driven. (They are all disabled.) Thus, this method measures the all-hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel (IN00 for example) is driven and all outputs other than a given output (IN03 in the middle) are programmed to connect to IN00. OUT03 is programmed to connect to IN15 (far away from IN00), which is terminated to ground. Thus OUT03 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT03 can be attributed to the output crosstalk of the other seven hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies the magnitude of the crosstalk will be given by:

$$|XT| = 20 \log_{10}\left[\left(R_S C_M\right) \times s\right]$$

where R_S is the source resistance, C_M is the mutual capacitance between the test signal circuit and the selected circuit, and s is the Laplace transform variable.

From the equation it can be observed that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8110/AD8111 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk will be higher than the minimum obtainable due to the high output currents. These currents will induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8110/AD8111.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by:

$$|XT| = 20 \log_{10}(Mxy \times s / R_L)$$

where *Mxy* is the mutual inductance of output *x* to output y, and R_L is the load resistance on the measured output. This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB Layout

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8110/AD8111 is designed to help keep the crosstalk to a minimum. Each input is separated from each other input by an analog ground pin. All of these AGNDs should be directly connected to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths and physical separation for the inputs. All of these help to reduce crosstalk.

Each output is separated from its two neighboring outputs by an analog ground pin in addition to an analog supply pin of one polarity or the other. Each of these analog supply pins provides power to the output stages of only the two nearest outputs. These supply pins and analog grounds provide shielding, physical separation and a low impedance supply for the outputs. Individual bypassing of each of these supply pins with a 0.01 μF chip capacitor directly to the ground plane minimizes high frequency output crosstalk via the mechanism of sharing common impedances.

Each output also has an on-chip compensation capacitor that is individually tied to the nearby analog ground pins AGND00 through AGND07. This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. These AGNDxx signals should all be directly connected to the ground plane.

The input and output signals will have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The only place the input and output signals surface is at the input termination resistors and the output series back termination resistors. These signals should also be separated, to the extent possible, as soon as they emerge from the IC package.

OUTLINE DIMENSIONS

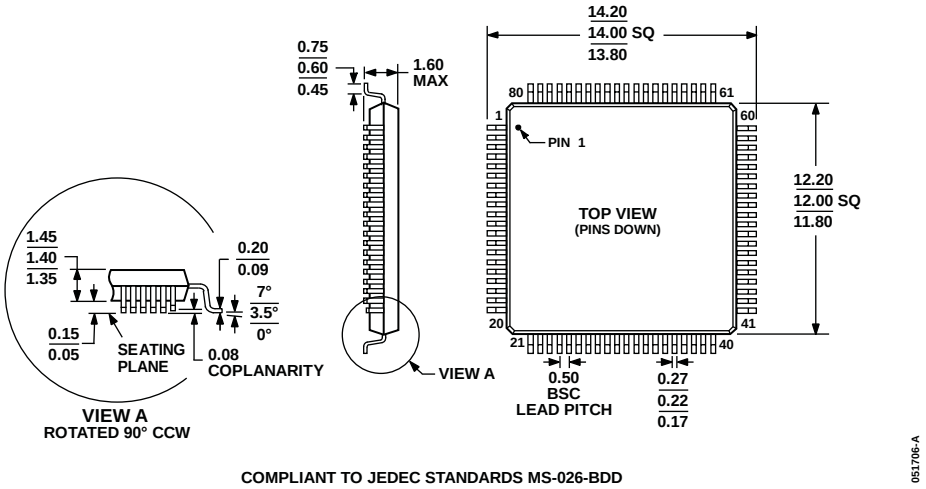


Figure 8. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8110ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD8111ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1

[1] Z = RoHS-Compliant Part.

REVISION HISTORY

5/15—Rev. A to Rev. B

Changes to Crosstalk, All Hostile Parameter and Off Isolation, Input-Output Parameter....2
Changes to Areas of Crosstalk Section....18
Deleted Evaluation Board Section and Figure 8; Renumbered Sequentially....20
Deleted Figure 9....21
Moved Outline Dimensions, Ordering Guide, and Revisions History....21
Updated Outline Dimensions....21
Changes to Ordering Guide....21
Deleted Figure 10 and Figure 11....22
Deleted Figure 12 and Figure 13....23
Deleted Figure 14, Controlling the Evaluation Board from a PC Section, and Figure 15....24
Deleted Overshoot on PC Printer Ports' Data Lines Section and Figure 16....25

2/02—Rev. 0 to Rev. A

Changed MQFP to LQFP....Universal
Comment Added to Outline Dimensions....26

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