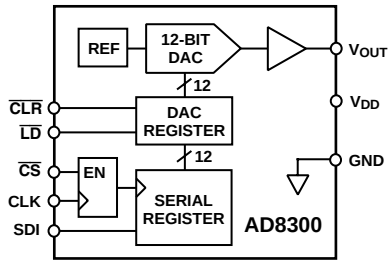
+3 Volt, Serial Input Complete 12-Bit DAC

AD8300

FEATURES
Complete 12-Bit DAC
No External Components
Single +3 Volt Operation
0.5 mV/Bit with 2.0475 V Full Scale
6 μs Output Voltage Settling Time
Low Power: 3.6 mW
Compact SO-8 1.5 mm Height Package

APPLICATIONS
Portable Communications
Digitally Controlled Calibration
Servo Controls
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8300 is a complete 12-bit, voltage-output digital-to-analog converter designed to operate from a single +3 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in single-supply +3 volt systems. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V making this device ideal for battery operated applications.

The 2.0475 V full-scale voltage output is laser trimmed to maintain accuracy over the operating temperature range of the device. The binary input data format provides an easy-to-use one-half-millivolt-per-bit software programmability. The voltage outputs are capable of sourcing 5 mA.

A double buffered serial data interface offers high speed, three-wire, DSP and microcontroller compatible inputs using data in (SDI), clock (CLK) and load strobe ($\overline{LD}$) pins. A chip select ($\overline{CS}$) pin simplifies connection of multiple DAC packages by enabling the clock input when active low. Additionally, a $\overline{CLR}$ input sets the output to zero scale at power on or upon user demand.

The AD8300 is specified over the extended industrial (–40°C to +85°C) temperature range. AD8300s are available in plastic DIP, and low profile 1.5 mm height SO-8 surface mount packages.

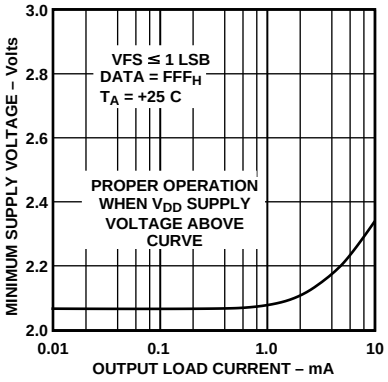


Figure 1. Minimum Supply Voltage vs. Load

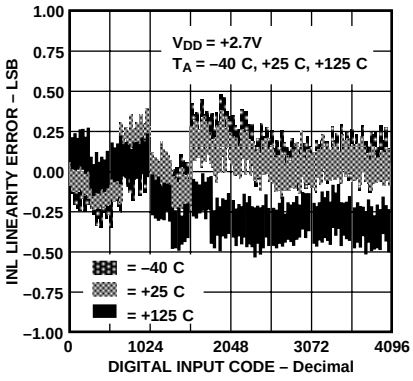


Figure 2. Linearity Error vs. Digital Code and Temperature

REV. A

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AD8300–SPECIFICATIONS

+3 V OPERATION (@ V_{DD} = +5 V ± 10%, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	[Note 1]	12			Bits
Relative Accuracy	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[2]	DNL	Monotonic	–1	±1/2	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	mV
Full-Scale Voltage[3]	V_{FS}	Data = FFF_H	2.039	2.0475	2.056	Volts
Full-Scale Tempco	TCV_{FS}	[Notes 3, 4]		16		ppm/°C
ANALOG OUTPUT						
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			5	mA
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			2	mA
Load Regulation	L_{REG}	R_L = 200 Ω to ∞, Data = 800_H		1.5	5	LSB
Output Resistance to GND	R_{OUT}	Data = 000_H		30		Ω
Capacitive Load	C_L	No Oscillation[4]		500		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.6	V
Logic Input High Voltage	V_{IH}		2.1			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS[4, 5]						
Clock Width High	t_{CH}		40			ns
Clock Width Low	t_{CL}		40			ns
Load Pulsewidth	t_{LDW}		50			ns
Data Setup	t_{DS}		15			ns
Data Hold	t_{DH}		15			ns
Clear Pulsewidth	t_{CLRW}		40			ns
Load Setup	t_{LD1}		15			ns
Load Hold	t_{LD2}		40			ns
Select	t_{CSS}		40			ns
Deselect	t_{CSH}		40			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time	t_S	To ±0.2% of Full Scale		7		µs
		To ±1 LSB of Final Value[6]		14		µs
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H		2.0		V/µs
DAC Glitch				15		nV/s
Digital Feedthrough				15		nV/s
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7		5.5	V
Positive Supply Current	I_{DD}	V_{DD} = 3 V, V_{IL} = 0 V, Data = 000_H		1.2	1.7	mA
		V_{DD} = 3.6 V, V_{IH} = 2.3 V, Data = FFF_H		1.9	3.0	mA
Power Dissipation	P_{DISS}	V_{DD} = 3 V, V_{IL} = 0 V, Data = 000_H		3.6	5.1	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.001	0.005	%/%

NOTES

[1]LSB = 0.5 mV for 0 V to +2.0475 V output range.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

+5 V OPERATION (@ V_{DD} = +5 V ± 10%, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	[Note 1]	12			Bits
Relative Accuracy	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[2]	DNL	Monotonic	–1	±1/2	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	mV
Full-Scale Voltage[3]	V_{FS}	Data = FFF_H	2.039	2.0475	2.056	Volts
Full-Scale Tempco	TCV_{FS}	[Notes 3, 4]		16		ppm/°C
ANALOG OUTPUT						
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			5	mA
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			2	mA
Load Regulation	L_{REG}	R_L = 200 Ω to ∞, Data = 800_H		1.5	5	LSB
Output Resistance to GND	R_{OUT}	Data = 000_H		30		Ω
Capacitive Load	C_L	No Oscillation[4]		500		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS[4, 5]						
Clock Width High	t_{CH}		30			ns
Clock Width Low	t_{CL}		30			ns
Load Pulsewidth	t_{LDW}		30			ns
Data Setup	t_{DS}		15			ns
Data Hold	t_{DH}		15			ns
Clear Pulsewidth	t_{CLWR}		30			ns
Load Setup	t_{LD1}		15			ns
Load Hold	t_{LD2}		30			ns
Select	t_{CSS}		30			ns
Deselect	t_{CSH}		30			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time	t_S	To ±0.2% of Full Scale		6		µs
		To ±1 LSB of Final Value[6]		13		µs
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H		2.2		V/µs
DAC Glitch				15		nV/s
Digital Feedthrough				15		nV/s
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7		5.5	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V, V_{IL} = 0 V, Data = 000_H		1.2	1.7	mA
		V_{DD} = 5.5 V, V_{IH} = 2.3 V, Data = FFF_H		2.8	4.0	mA
Power Dissipation	P_{DISS}	V_{DD} = 5 V, V_{IL} = 0 V, Data = 000_H		6	5.1	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±10%		0.001	0.006	%/%

NOTES

[1] 1 LSB = 0.5 mV for 0 V to +2.0475 V output range.

[2] The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3] Includes internal voltage reference error.

[4] These parameters are guaranteed by design and not subject to production testing.

[5] All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[6] The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V, +7 V
Logic Inputs to GND ..... –0.3 V, +7 V
V_{OUT} to GND .....–0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_J \text{ Max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Lead Plastic DIP Package (N-8) ..... 103°C/W
8-Lead SOIC Package (SO-8) ..... 158°C/W
Maximum Junction Temperature (T_J Max) ..... 150°C
Operating Temperature Range .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

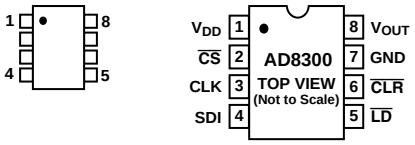
ORDERING GUIDE

Model	INL	Temp	Package Description	Package Options
AD8300AN	±2	XIND	8-Lead P-DIP	N-8
AD8300AR	±2	XIND	8-Lead SOIC	SO-8

NOTES
XIND = –40°C to +85°C.
The AD8300 contains 630 transistors. The die size measures 72 mil × 65 mil.

PIN CONFIGURATIONS

SO-8 Plastic DIP



PIN DESCRIPTIONS

Pin #	Name	Function
1	V_{DD}	Positive power supply input. Specified range of operation +2.7 V to +5.5 V.
2	$\overline{CS}$	Chip Select, active low input. Disables shift register loading when high. Does not affect $\overline{LD}$ operation.
3	CLK	Clock input, positive edge clocks data into shift register.
4	SDI	Serial Data Input, input data loads directly into the shift register, MSB first.
5	$\overline{LD}$	Load DAC register strobes, active low. Transfers shift register data to DAC register. See Truth Table I for operation. Asynchronous active low input.
6	$\overline{CLR}$	Resets DAC register to zero condition. Asynchronous active low input.
7	GND	Analog and Digital Ground.
8	V_{OUT}	DAC voltage output, 2.0475 V full scale with 0.5 mV per bit. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.

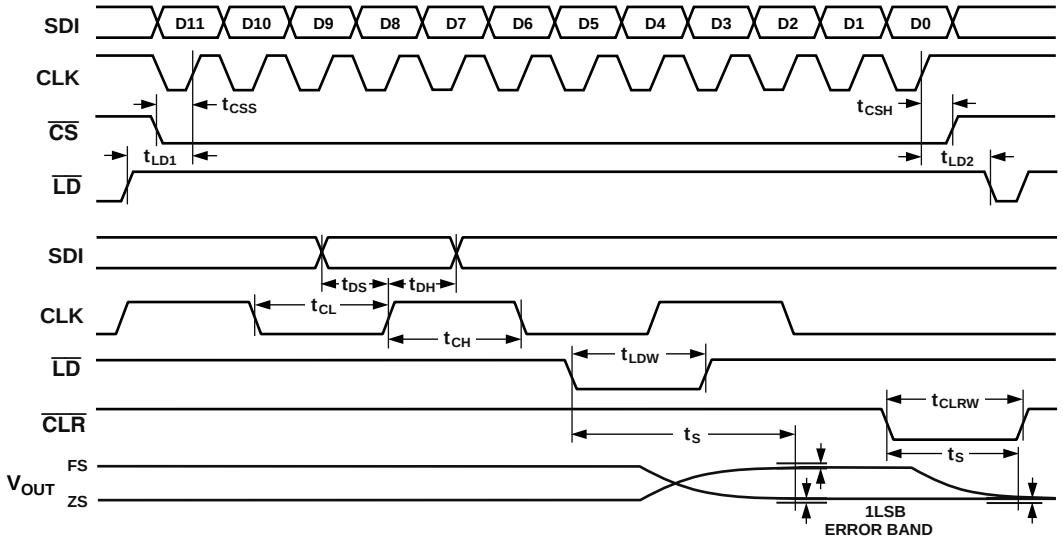


Figure 3. Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8300 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



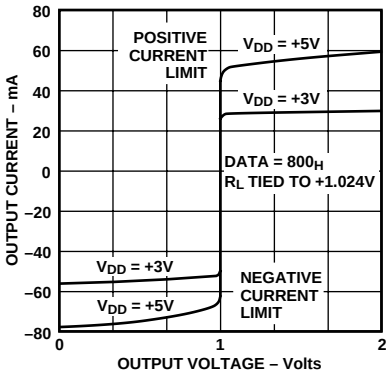


Figure 4. I_{OUT} vs. V_{OUT}

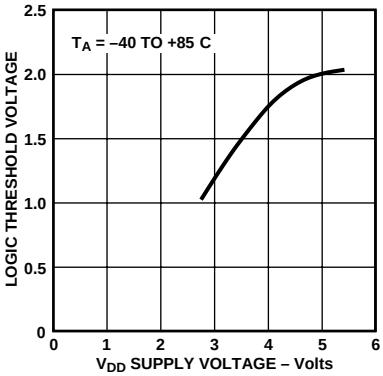


Figure 5. Logic Input Threshold Voltage vs. V_{DD}

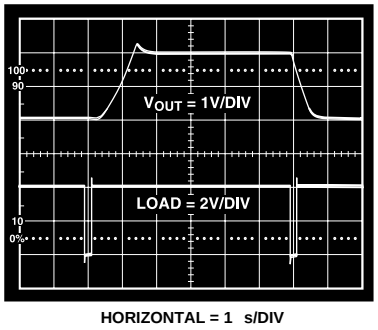


Figure 6. Detail Settling Time

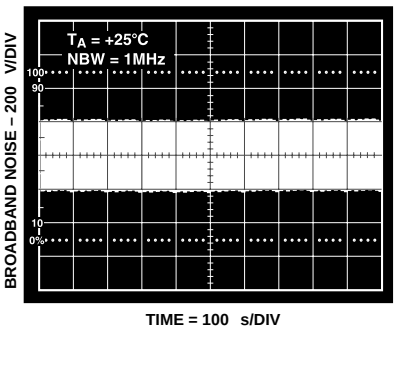


Figure 7. Broadband Noise

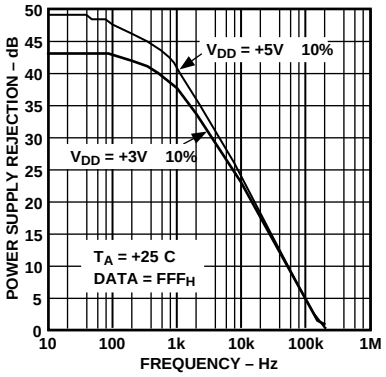


Figure 8. Power Supply Rejection vs. Frequency

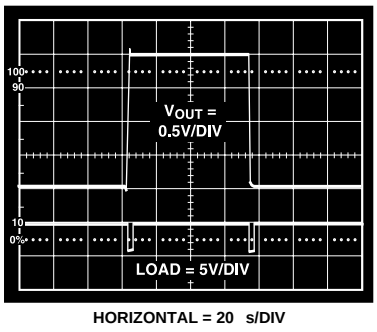


Figure 9. Large Signal Settling Time

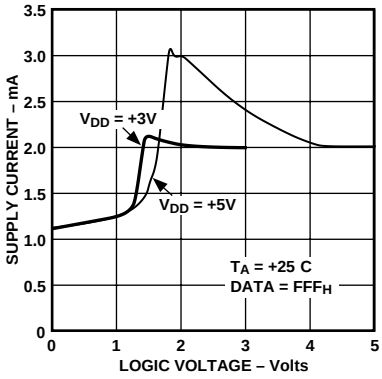


Figure 10. Supply Current vs. Logic Input Voltage

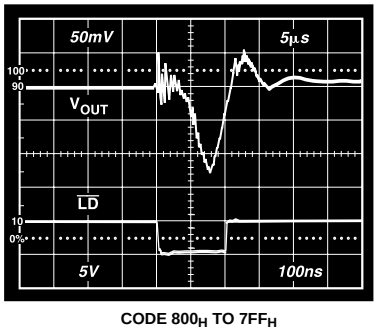


Figure 11. Midscale Transition Performance

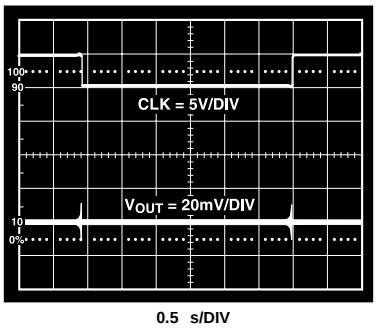


Figure 12. Digital Feedthrough vs. Time

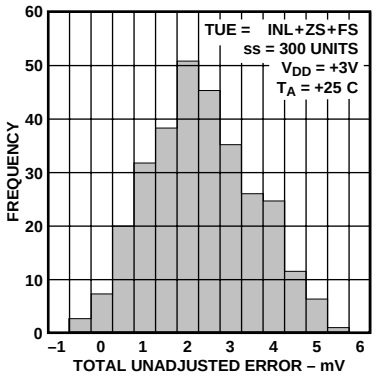


Figure 13. Total Unadjusted Error Histogram

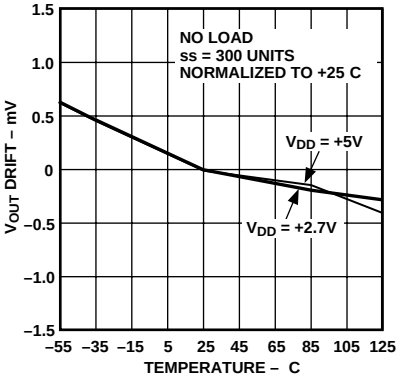


Figure 14. Zero-Scale Voltage Drift vs. Temperature

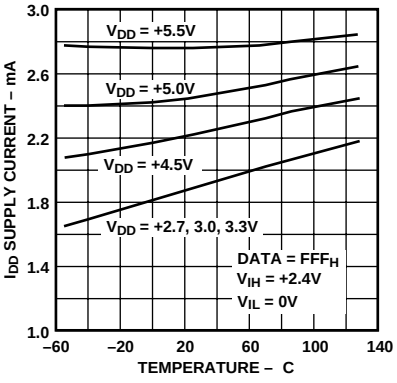


Figure 15. Supply Current vs. Temperature

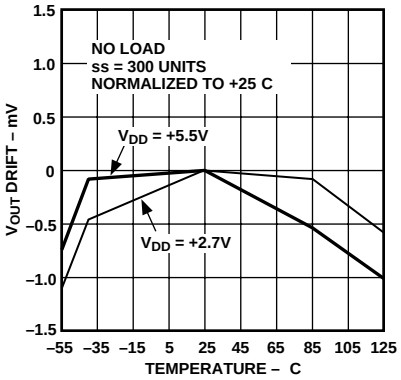


Figure 16. Full-Scale Voltage Drift vs. Temperature

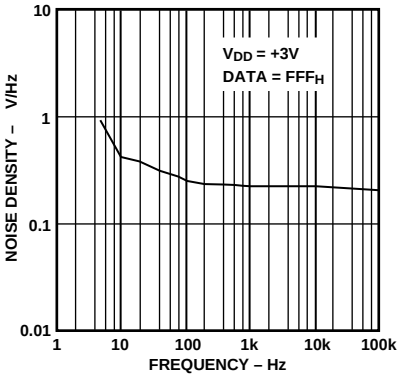


Figure 17. Output Voltage Noise Density vs. Frequency

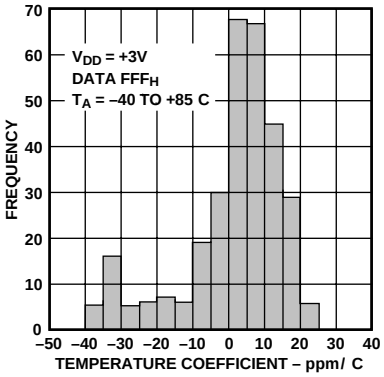


Figure 18. Full-Scale Output Tempco Histogram

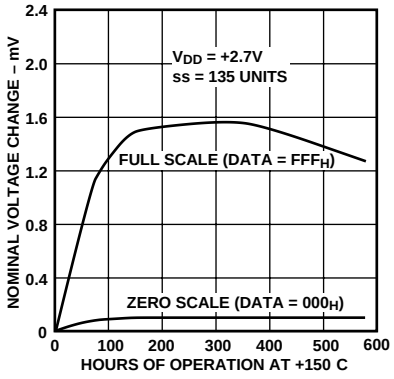


Figure 19. Long Term Drift Accelerated by Burn-In

Table I. Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{CLR}$	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
H	X	H	H	No Effect	Latched
L	L	H	H	No Effect	Latched
L	H	H	H	No Effect	Latched
L	↑	H	H	Shift-Register-Data Advanced One Bit	Latched
↑	L	H	H	No Effect	Latched
H	X	H	↓	No Effect	Updated with Current Shift Register Contents
H	X	H	L	No Effect	Transparent
H	X	L	X	No Effect	Loaded with All Zeros
H	X	↑	H	No Effect	Latched All Zeros

NOTES
1. ↑ = Positive Logic Transition; ↓ = Negative Logic Transition; X = Don't Care.
2. Do not clock in serial data while $\overline{LD}$ is LOW.
3. Data loads MSB first.

OPERATION

The AD8300 is a complete ready to use 12-bit digital-to-analog converter. Only one +3 V power supply is necessary for operation. It contains a 12-bit laser-trimmed digital-to-analog converter, a curvature-corrected bandgap reference, rail-to-rail output op amp, serial-input register, and DAC register. The serial data interface consists of a serial-data-input (SDI) clock (CLK), and load strobe pins ($\overline{LD}$) with an active low $\overline{CS}$ strobe. In addition an asynchronous $\overline{CLR}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit device with an output that swings from GND potential to 0.4 volt generated from the internal bandgap voltage, see Figure 20. It uses a laser-trimmed segmented R-2R ladder which is switched by N-channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage that provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured with a gain of approximately five in order to set the 2.0475 volt full-scale output (0.5 mV/LSB). See Figure 20 for an equivalent circuit schematic of the analog section.

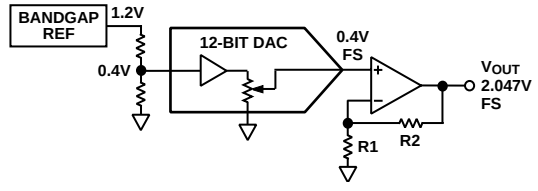


Figure 20. Equivalent AD8300 Schematic of Analog Portion

The op amp has a 2 µs typical settling time to 0.4% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also negative transition settling time to within the last 6 LSB of zero volts has an extended settling time. See the oscilloscope photos in the typical performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 21 shows an equivalent output schematic of the rail-to-rail amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

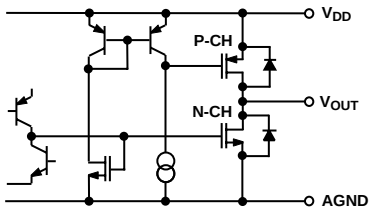


Figure 21. Equivalent Analog Output Circuit

The rail-to-rail output stage achieves the minimum operating supply voltage capability shown in Figure 2. The N-channel output pull-down MOSFET shown in Figure 21 has a 35 Ω on resistance which sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. Figure 18 provides a histogram of total output performance of full-scale vs. temperature which is dominated by the reference performance.

POWER SUPPLY

The very low power consumption of the AD8300 is a direct result of a circuit design optimizing use of a CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the AD8300 is strongly dependent on the actual logic input voltage levels present on the SDI, CLK, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic

V_{OH} and V_{OL} voltage levels. Consequently, for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the logic input pins provides the lowest standby dissipation of 1.2 mA with a +3.3 V power supply.

As with any analog system, it is recommended that the AD8300 power supply be bypassed on the same PC card that contains the chip. Figure 8 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifiers used in the AD8300 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +2.7 V to +5.5 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD8300 is possible down to +2.1 volts. The minimum operating supply voltage versus load current plot in Figure 2 provides information for operation below V_{DD} = +2.7 V.

TIMING AND CONTROL

The AD8300 has a separate serial-input register from the 12-bit DAC register that allows preloading of a new data value MSB first into the serial register without disturbing the present DAC output voltage value. Data can only be loaded when the $\overline{CS}$ pin is active low. After the new value is fully loaded in the serial-input register, it can be asynchronously transferred to the DAC register by strobing the $\overline{LD}$ pin. The DAC register uses a level sensitive $\overline{LD}$ strobe that should be returned high before any new data is loaded into the serial-input register. At any time the contents of the DAC resister can be reset to zero by strobing the $\overline{CLR}$ pin which causes the DAC output voltage to go to zero volts. All of the timing requirements are detailed in Figure 3 along with Table I. Control Logic Truth Table.

All digital inputs are protected with a Zener type ESD protection structure (Figure 22) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is loading one or more of the digital inputs with a 5 V CMOS logic input voltage level while operating the AD8300 on a +3.3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the +5 V CMOS meets the V_{IL} input requirement of the AD8300 operating at 3 V. See Figure 5 for the effect on digital logic input threshold versus operating V_{DD} supply voltage.

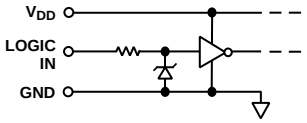


Figure 22. Equivalent Digital Input ESD Protection

Unipolar Output Operation

This is the basic mode of operation for the AD8300. The AD8300 has been designed to drive loads as low as 400 Ω in parallel with 500 pF. The code table for this operation is shown in Table II.

APPLICATIONS INFORMATION

See DAC8512 data sheet for additional application circuit ideas.

Table II. Unipolar Code Table

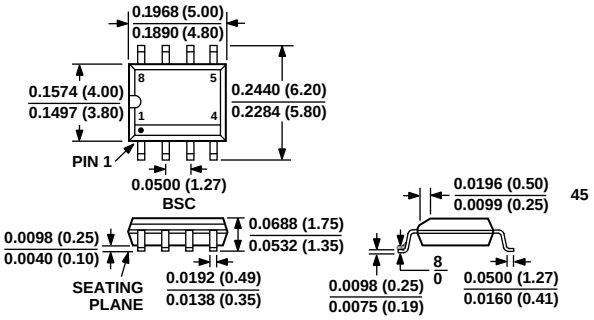
Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+2.0475
801	2049	+1.0245
800	2048	+1.0240
7FF	2047	+1.0235
000	0	+0.0000

C1968a–0–5/99

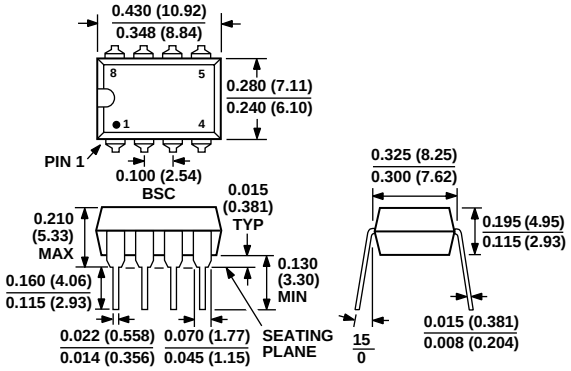
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



8-Lead Plastic DIP (N-8)



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