100 dB Range (10 nA to 1 mA) Logarithmic Converter

Data Sheet

AD8305

FEATURES

- **Optimized for fiber optic photodiode interfacing**
- **Measures current over 5 decades**
  - **Law conformance 0.1 dB from 10 nA to 1 mA**
- **Single- or dual-supply operation (3 V to 12 V total)**
- **Full log-ratio capabilities**
- **Nominal slope of 10 mV/dB (200 mV/decade)**
- **Nominal intercept of 1 nA (set by external resistor)**
  - **Optional adjustment of slope and intercept**
- **Complete and temperature stable**
- **Rapid response time for a given current level**
- **Miniature 16-lead chip scale package**
  - **(LFCSP 3 mm × 3 mm)**
- **Low power: ~5 mA quiescent current**

APPLICATIONS

- **Optical power measurement**
- **Wide range baseband logarithmic compression**
- **Measurement of current and voltage ratios**
- **Optical absorbance measurement**

FUNCTIONAL BLOCK DIAGRAM

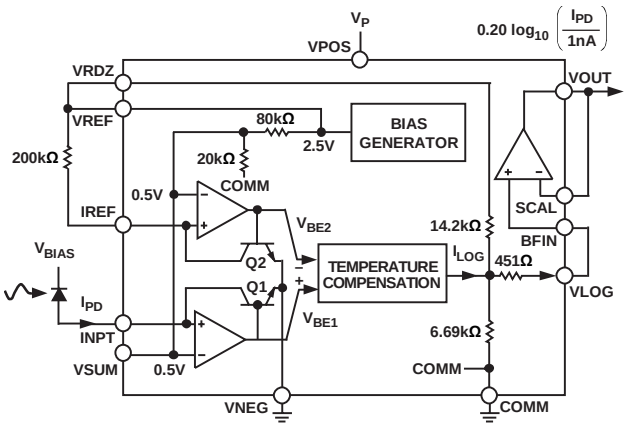


Figure 1.

GENERAL DESCRIPTION

The AD8305[1] is an inexpensive microminiature logarithmic converter optimized for determining optical power in fiber optic systems. It uses an advanced implementation of a classic translinear (junction based) technique to provide a large dynamic range in a versatile and easily used form. A single-supply voltage of between 3 V and 12 V is adequate; dual supplies may optionally be used. The low quiescent current (typically 5 mA) permits use in battery-operated applications.

The input current, I_{PD}, of 10 nA to 1 mA applied to the INPT pin is the collector current of an optimally scaled NPN transistor, which converts this current to a voltage (V_{BE}) with a precise logarithmic relationship. A second such converter is used to handle the reference current (I_{REF}) applied to pin I_{REF}. These input nodes are biased slightly above ground (0.5 V). This is generally acceptable for photodiode applications where the anode does not need to be grounded. Similarly, this bias voltage is easily accounted for in generating I_{REF}. The output of the logarithmic front end is available at Pin VLOG.

The basic logarithmic slope at this output is nominally 200 mV/decade (10 mV/dB). Thus, a 100 dB range corresponds to an output change of 1 V. When this voltage (or the buffer output) is applied to an ADC that permits an external reference voltage to be employed, the AD8305 voltage reference output of 2.5 V at Pin VREF can be used to improve the scaling accuracy. Suitable ADCs include the AD7810 (serial 10-bit), AD7823 (serial 8-bit), and AD7813 (parallel, 8-bit or 10-bit). Other values of the logarithmic slope can be provided using a simple external resistor network.

The logarithmic intercept (also known as the reference current) is nominally positioned at 1 nA by the use of the externally generated current, I_{REF}, of 10 μA, provided by a 200 kΩ resistor connected between VREF, at 2.5 V, and the reference input, IREF, at 0.5 V. The intercept can be adjusted over a wide range by varying this resistor. The AD8305 can also operate in a log ratio mode, with the numerator current applied to INPT and the denominator current applied to IREF.

A buffer amplifier is provided for driving a substantial load, for use in raising the basic slope of 10 mV/dB to higher values, as a precision comparator (threshold detector), or in implementing low-pass filters. Its rail-to-rail output stage can swing to within 100 mV of the positive and negative supply rails, and its peak current sourcing capacity is 25 mA.

It is a fundamental aspect of translinear logarithmic converters that the small signal bandwidth falls as the current level diminishes, and the low frequency noise-spectral density increases. At the 10 nA level, the bandwidth of the AD8305 is about 50 kHz and increases in proportion to I_{PD} up to a maximum value of about 15 MHz. Using the buffer amplifier, the increase in noise level at low currents can be addressed by using it to realize low-pass filters of up to three poles.

The AD8305 is available in a 16-lead LFCSP package and is specified for operation from −40°C to +85°C.

[1] Protected by U.S. Patent No. 5,519,308.

Rev. C Document Feedback

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REVISION HISTORY

9/2017—Rev. B to Rev. C

Changed CP-16-2 to CP-16-27 ... Throughout
Updated Outline Dimensions ... 24
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4/2010—Rev. A to Rev. B

Updated Data Sheet ... Universal
Change to Figure 2 and Table 3 ... 5
Added Power Supply Sequencing Section ... 12
Added Figure 34; Renumbered Sequentially ... 12
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3/2003—Rev. 0 to Rev. A

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SPECIFICATIONS

V_P = 5 V, V_N = 0 V, T_A = 25°C, R_{REF} = 200 kΩ, and VRDZ connected to VREF, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT INTERFACE	Pin 4, INPT, Pin 3, IREF				
Specified Current Range, I_{PD}	Flows toward INPT pin	10			nA
				1	mA
Input Current Min/Max Limits	Flows toward INPT pin			10	mA
Reference Current, I_{REF}, Range	Flows toward IREF pin	10			nA
				1	mA
Summing Node Voltage	Internally preset; may be altered by the user	0.46	0.5	0.54	V
Temperature Drift	−40°C < T_A < +85°C		0.015		mV/°C
Input Offset Voltage	$V_{INPT} - V_{SUM}$, $V_{IREF} - V_{SUM}$	−20		+20	mV
LOGARITHMIC OUTPUT	Pin 9, VLOG				
Logarithmic Slope		190	200	210	mV/dec
	−40°C < T_A < +85°C	185		215	mV/dec
Logarithmic Intercept[1]		0.3	1	1.7	nA
	−40°C < T_A < +85°C	0.1		2.5	nA
Law Conformance Error	10 nA < I_{PD} < 1 mA		0.1	0.4	dB
Wideband Noise[2]	I_{PD} > 1 μA		0.7		mV√Hz
Small Signal Bandwidth[2]	I_{PD} > 1 μA		0.7		MHz
Maximum Output Voltage			1.7		V
Minimum Output Voltage	Limited by V_N = 0 V		0.01		V
Output Resistance		4.375	5	5.625	kΩ
REFERENCE OUTPUT	Pin 2, VREF				
Voltage With Reference to Ground		2.435	2.5	2.565	V
	−40°C < T_A < +85°C	2.4		2.6	V
Maximum Output Current	Sourcing (grounded load)		20		mA
Incremental Output Resistance	Load current < 10 mA		2		Ω
OUTPUT BUFFER	Pin 10, BFIN; Pin 11, SCAL; Pin 12, VOUT				
Input Offset Voltage		−20		+20	mV
Input Bias Current	Flowing out of Pin 10 or Pin 11		0.4		mA
Incremental Input Resistance			35		MΩ
Output Range	R_L = 1 kΩ to ground		V_P − 0.1		V
Incremental Output Resistance	Load current < 10 mA		0.5		Ω
Peak Source/Sink Current			25		mA
Small Signal Bandwidth	GAIN = 1		15		MHz
Slew Rate	0.2 V to 4.8 V output swing		15		V/μs
POWER SUPPLY	Pin 8, VPOS; Pin 6 and Pin 7, VNEG				
Positive Supply Voltage	($V_P - V_N$) ≤ 12 V	3	5	12	V
Quiescent Current			5.4	6.5	mA
Negative Supply Voltage (Optional)	($V_P - V_N$) ≤ 12 V	−5.5	0		V

[1] Other values of logarithmic intercept can be achieved by adjusting R_{REF}.
[2] Output noise and incremental bandwidth are functions of input current, measured using output buffer connected for GAIN = 1.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage $V_P - V_N$	12 V
Input Current	20 mA
Internal Power Dissipation	500 mW
θ_{JA}[1]	30°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] With package die paddle soldered to thermal pad containing nine vias connected to inner and bottom layers.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

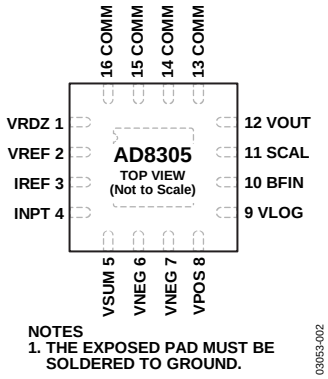


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VRDZ	Top of a Resistive Divider Network that Offsets V_{LOG} to Position the Intercept. Normally connected to VREF; may also be connected to ground when bipolar outputs are to be provided.
2	VREF	Reference Output Voltage of 2.5 V.
3	IREF	Accepts (Sinks) Reference Current, I_{REF}.
4	INPT	Accepts (Sinks) Photodiode Current, I_{PD}. Usually connected to photodiode anode such that photo current flows into INPT.
5	VSUM	Guard Pin. Used to shield the INPT current line and for optional adjustment of the INPT and I_{REF} node potential.
6, 7	VNEG	Optional Negative Supply, V_N (this pin is usually grounded; for details of usage, see the Applications section.
8	VPOS	Positive Supply, $(V_P - V_N) \leq 12$ V.
9	VLOG	Output of the Logarithmic Front End.
10	BFIN	Buffer Amplifier Noninverting Input.
11	SCAL	Buffer Amplifier Inverting Input.
12	VOUT	Buffer Output.
13 to 16	COMM	Analog Ground.
	EPAD	The exposed pad must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V, V_N = 0 V, R_{REF} = 200 kΩ, T_A = 25°C, unless otherwise noted.

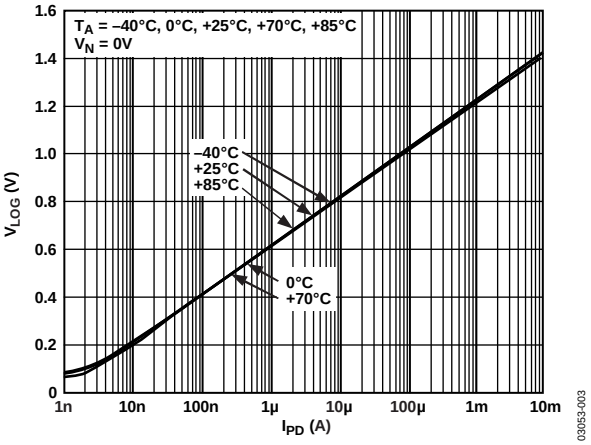


Figure 3. V_{LOG} vs. I_{PD} for Multiple Temperatures

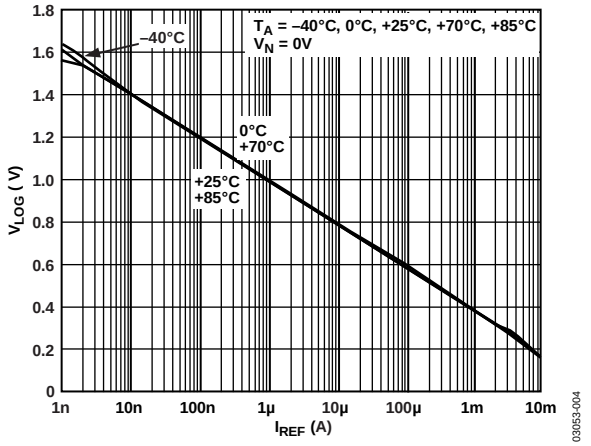


Figure 4. V_{LOG} vs. I_{REF} for Multiple Temperatures

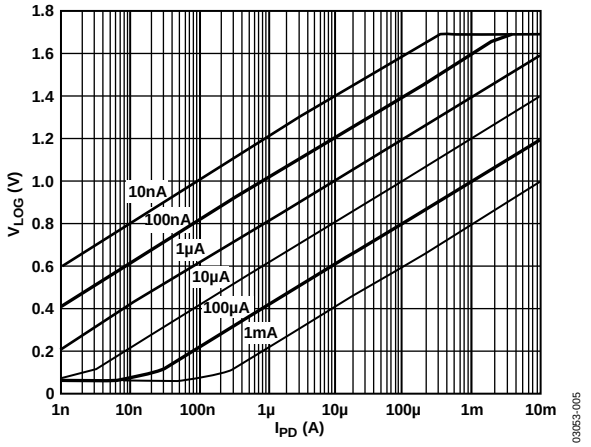


Figure 5. V_{LOG} vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)

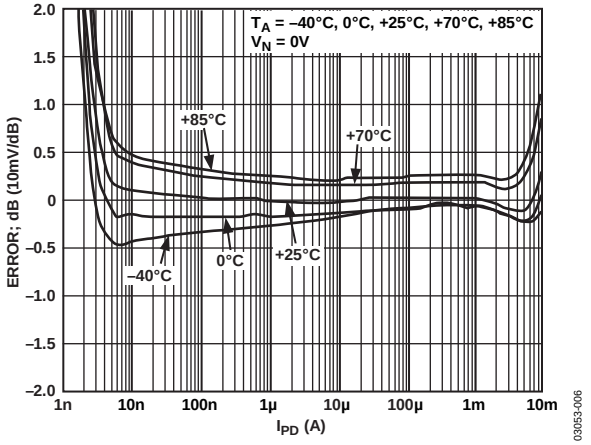


Figure 6. Law Conformance Error vs. I_{PD} (at I_{REF} = 10 µA) for Multiple Temperatures, Normalized to 25°C

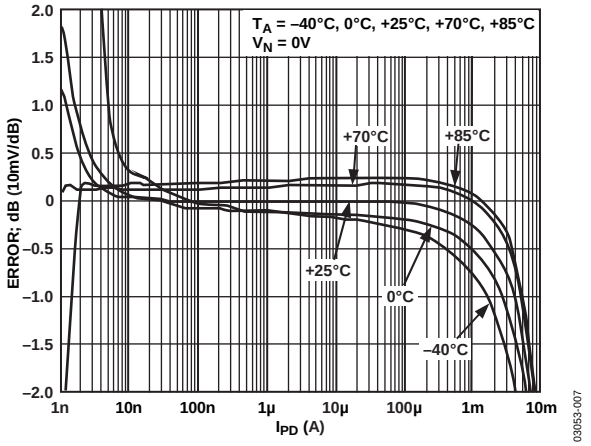


Figure 7. Law Conformance Error vs. I_{REF} (at I_{PD} = 10 µA) for Multiple Temperatures, Normalized to 25°C

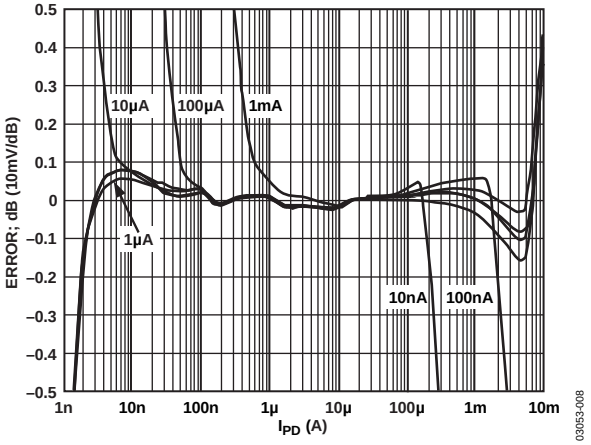


Figure 8. Law Conformance Error vs. IPD for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)

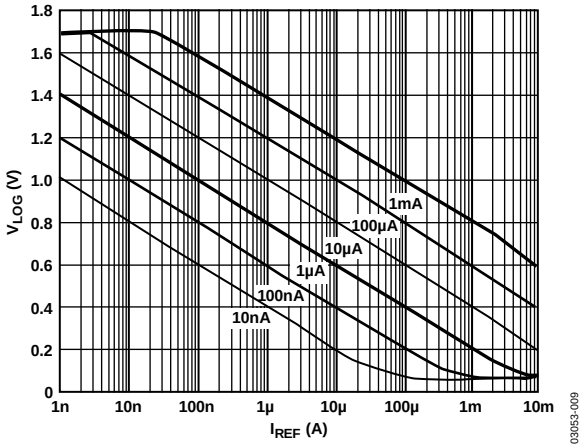


Figure 9. V_{LOG} vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)

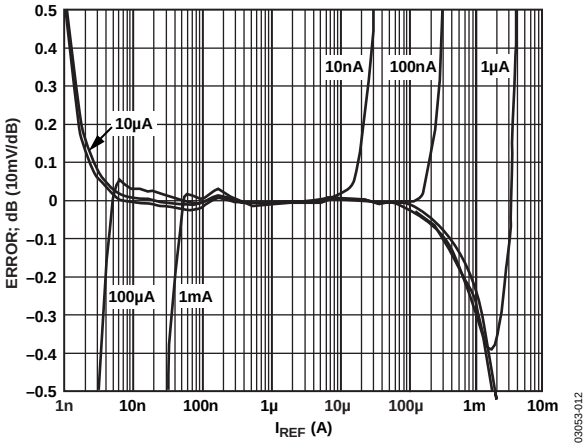


Figure 12. Law Conformance Error vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)

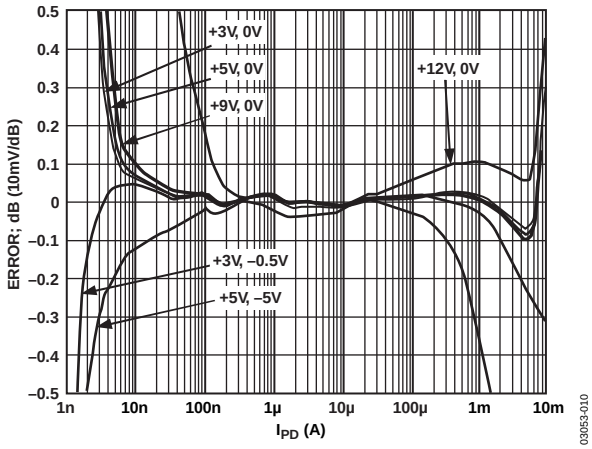


Figure 10. Law Conformance Error vs. I_{PD} for Various Supply Conditions (See Annotations)

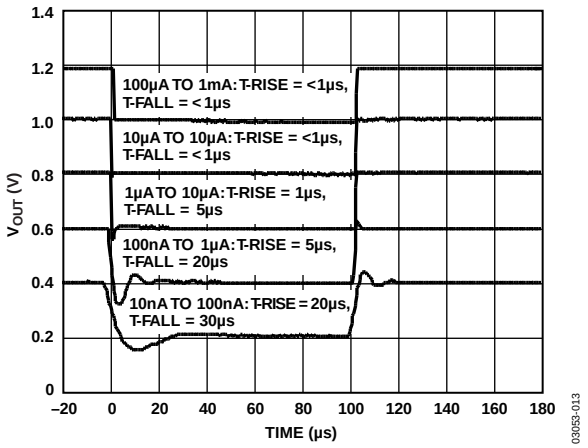


Figure 13. Pulse Response – I_{PD} to V_{OUT} (G = 1)

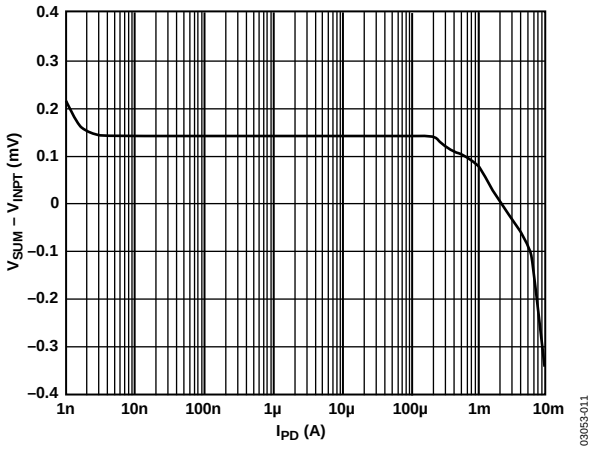


Figure 11. $V_{INPT} – V_{SUM}$ vs. I_{PD}

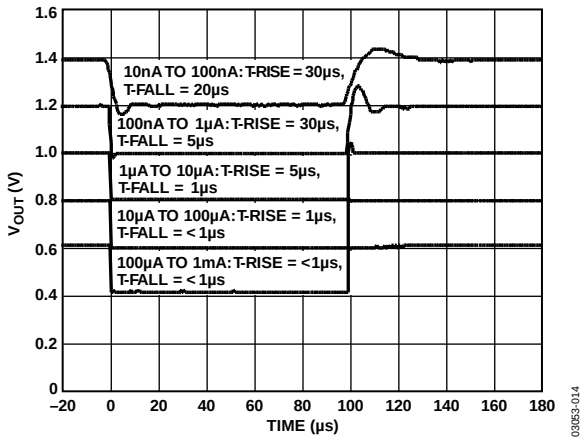


Figure 14. Pulse Response – I_{REF} to V_{OUT} (G = 1)

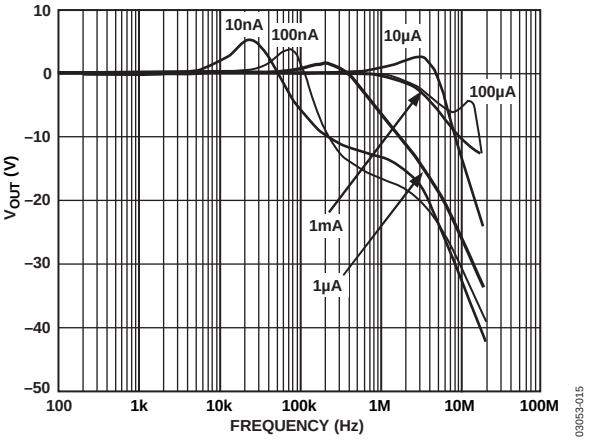


Figure 15. Small Signal AC Response (5% Sine Modulation), from I_{PD} to V_{OUT} ($G = 1$) for I_{PD} in Decade Steps from 10 nA to 1 mA, $I_{REF} = 10\ \mu A$

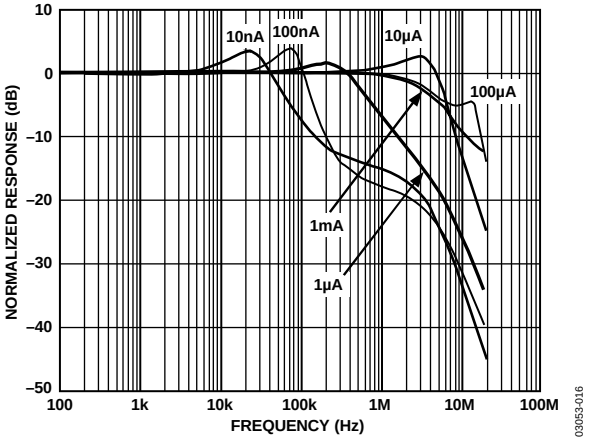


Figure 16. Small Signal AC Response (5% Sine Modulation), from I_{REF} to V_{OUT} ($G = 1$) for I_{REF} in Decade Steps from 10 nA to 1 mA, $I_{PD} = 10\ \mu A$

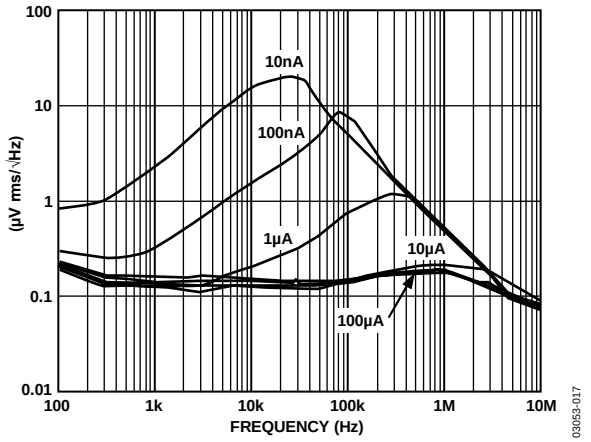


Figure 17. Spot Noise Spectral Density at V_{OUT} ($G = 1$) vs. Frequency for I_{PD} in Decade Steps from 10 nA to 1 mA

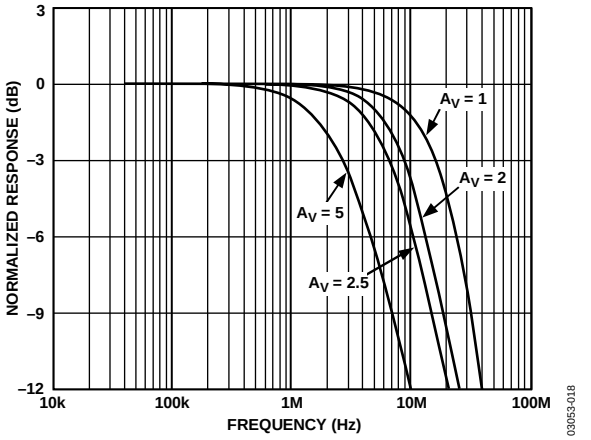


Figure 18. Small Signal AC Response of the Buffer for Various Closed-Loop Gains ($R_L = 1\ k\Omega$ $C_L < 2\ pF$)

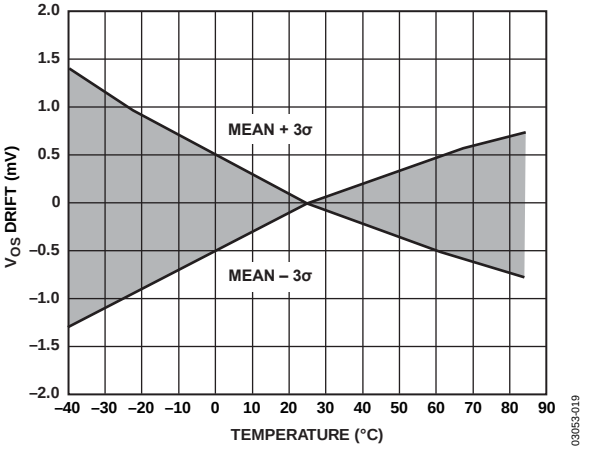


Figure 19. Buffer Input Offset Drift vs. Temperature (3σ to Either Side of Mean)

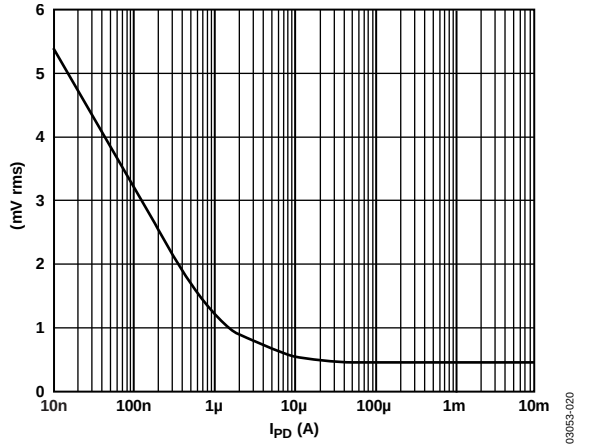


Figure 20. Total Wideband Noise Voltage at V_{OUT} vs. I_{PD} ($G = 1$)

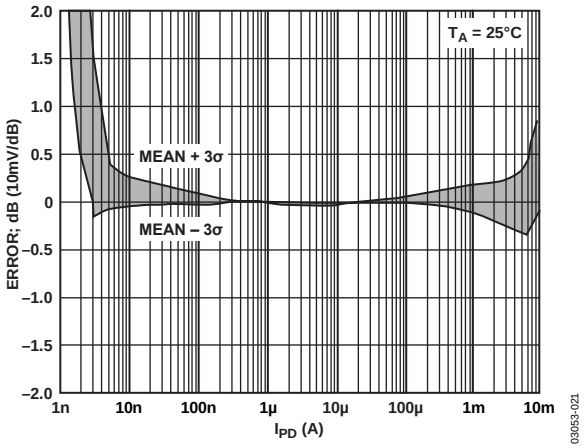


Figure 21. Law Conformance Error Distribution (3σ to Either Side of Mean)

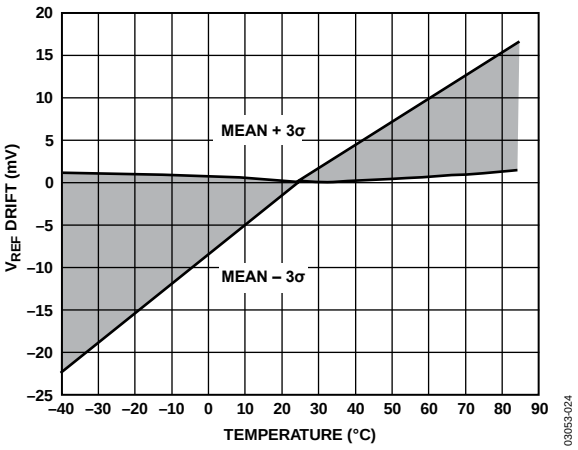


Figure 24. V_{REF} Drift vs. Temperature (3σ to Either Side of Mean)

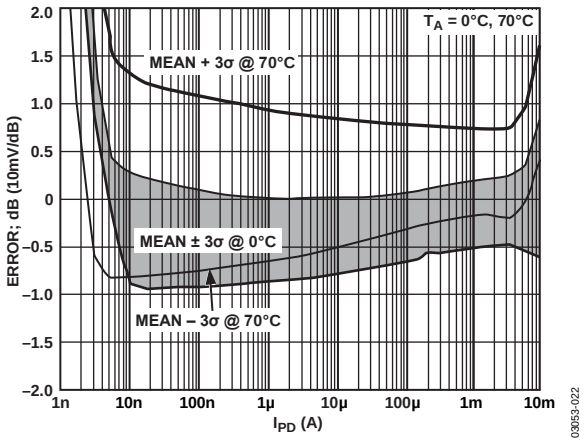


Figure 22. Law Conformance Error Distribution (3σ to Either Side of Mean)

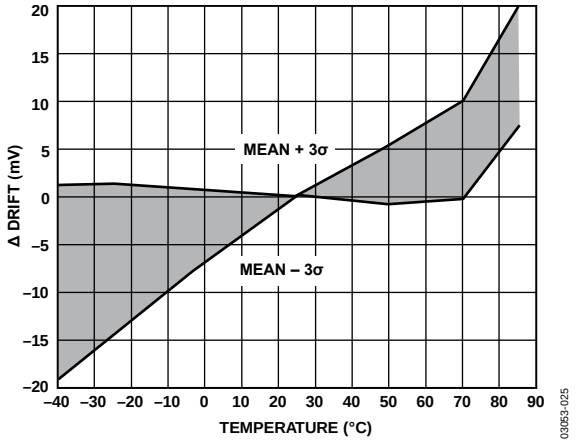


Figure 25. $V_{REF} - V_{IREF}$ Drift vs. Temperature (3σ to Either Side of Mean)

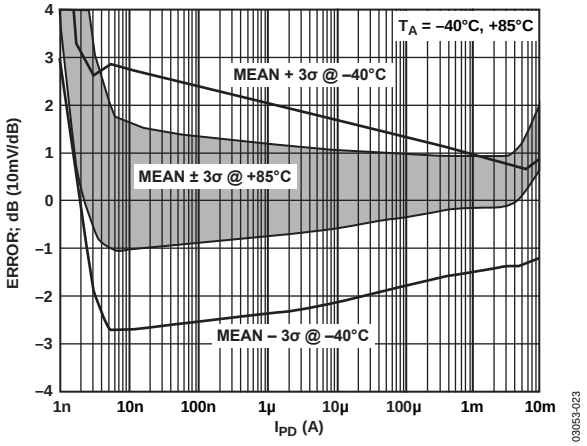


Figure 23. Law Conformance Error Distribution (3σ to Either Side of Mean)

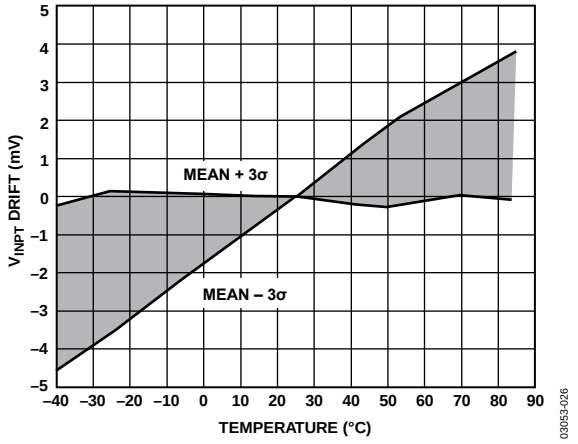


Figure 26. V_{INPT} Drift vs. Temperature (3σ to Either Side of Mean)

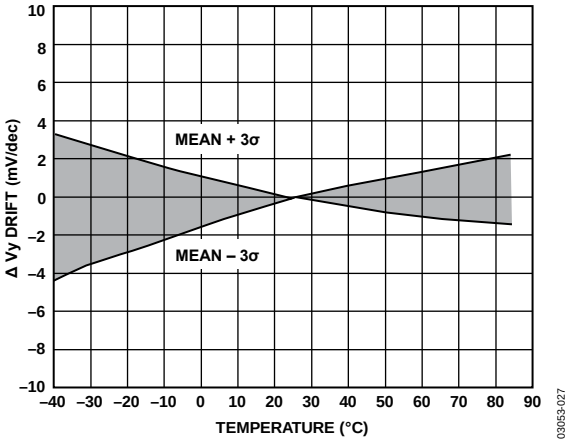


Figure 27. Slope Drift vs. Temperature (3σ to Either Side of Mean of 200 mV/decade)

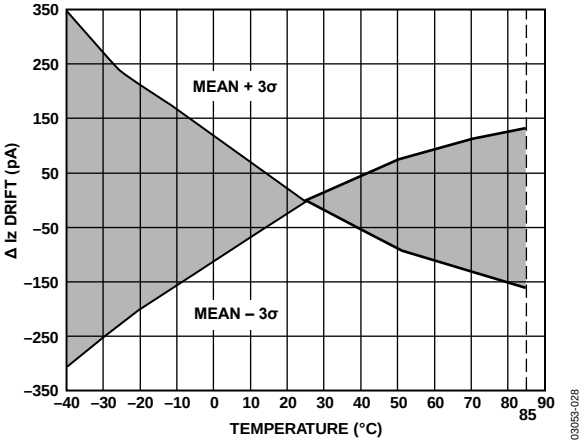


Figure 28. Intercept Drift vs. Temperature (3σ to Either Side of Mean of 1 nA)

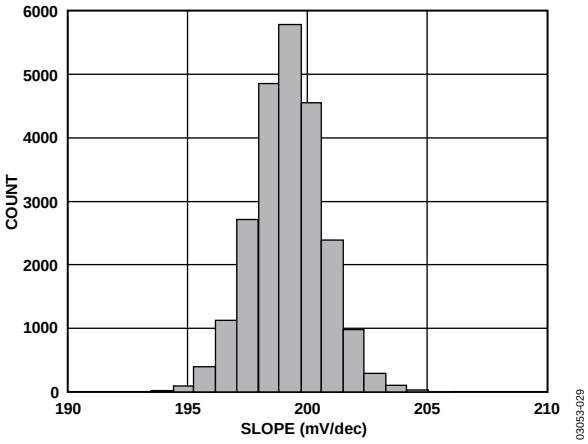


Figure 29. Distribution of Logarithmic Slope (Nominally 200 mV/decade) Sample >22,000

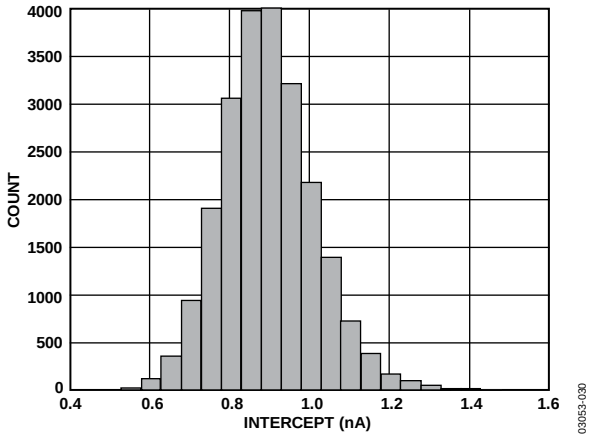


Figure 30. Distribution of Logarithmic Intercept (Nominally 1 nA when R_{REF} = 200 kΩ ± 0.1%) Sample >22,000

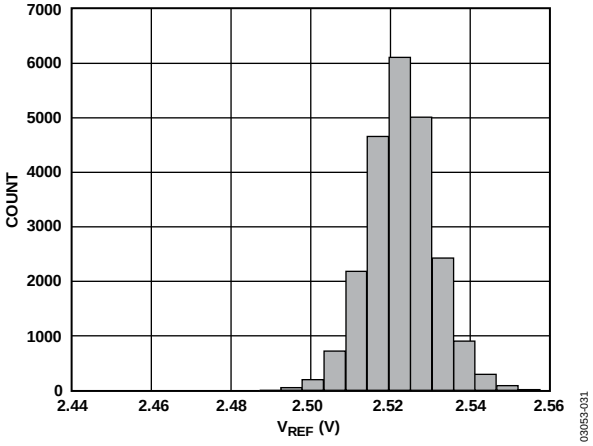


Figure 31. Distribution of V_{REF} (R_L = 100 kΩ) Sample >22,000

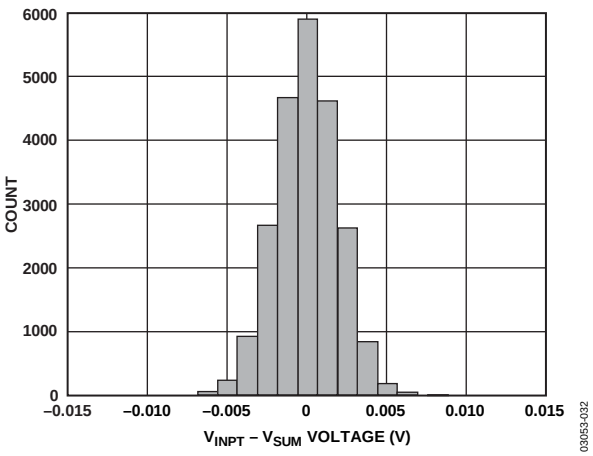


Figure 32. Distribution of Offset Voltage (V_{INPT} – V_{SUM}) Sample >22,000

GENERAL STRUCTURE

The AD8305 addresses a wide variety of interfacing conditions to meet the needs of fiber optic supervisory systems, and is also useful in many nonoptical applications. These notes explain the structure of this unique style of translinear log amp. Figure 33 is a simplified schematic showing the key elements.

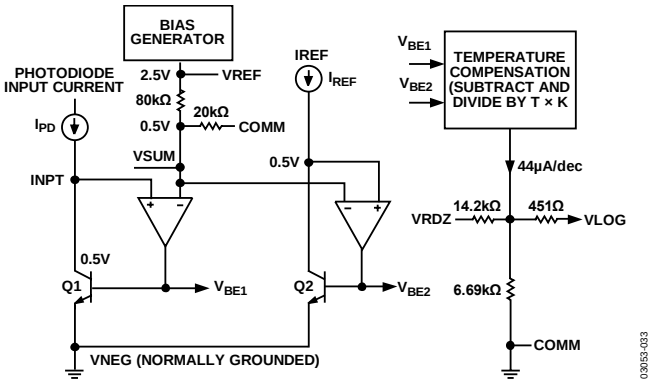


Figure 33. Simplified Schematic

The photodiode current, I_{PD}, is received at Pin INPT. The voltage at this node is essentially equal to those on the two adjacent guard pins, VSUM and IREF, due to the low offset voltage of the JFET op amp. Transistor Q1 converts the input current I_{PD} to a corresponding logarithmic voltage, as shown in Equation 1. A finite positive value of V_{SUM} is needed to bias the collector of Q1 for the usual case of a single-supply voltage. This is internally set to 0.5 V, that is, one fifth of the reference voltage of 2.5 V appearing on Pin VREF. The resistance at the VSUM pin is nominally 16 kΩ; this voltage is not intended as a general bias source.

The AD8305 also supports the use of an optional negative supply voltage, V_N, at Pin VNEG. When V_N is −0.5 V or more negative, VSUM may be connected to ground; thus, INPT and IREF assume this potential. This allows operation as a voltage-input logarithmic converter by the inclusion of a series resistor at either or both inputs. Note that the resistor setting I_{REF} needs to be adjusted to maintain the intercept value. It should also be noted that the collector-emitter voltages of Q1 and Q2 are now the full V_N, and effects due to self-heating causes errors at large input currents.

The input dependent, V_{BE1}, of Q1 is compared with the reference V_{BE2} of a second transistor, Q2, operating at I_{REF}. This is generated externally, to a recommended value of 10 µA. However, other values over a several-decade range can be used with a slight degradation in law conformance (see Figure 3).

THEORY

The base emitter voltage of a bipolar junction transistor (BJT) can be expressed by Equation 1, which immediately shows its basic logarithmic nature:

$$V_{BE} = kT/qIn(I_C/I_S) \quad (1)$$

where:

I_C is its collector current.
I_S is a scaling current, typically only 10^{-17} A.
kT/q is the thermal voltage, proportional to absolute temperature (PTAT) and is 25.85 mV at 300 K.

The current, I_S, is never precisely defined and exhibits an even stronger temperature dependence, varying by a factor of roughly a billion between −35°C and +85°C. Thus, to make use of the BJT as an accurate logarithmic element, both of these temperature dependencies must be eliminated.

The difference between the base-emitter voltages of a matched pair of BJTs, one operating at the photodiode current I_{PD} and the second operating at a reference current I_{REF}, can be written as:

$$\begin{aligned} V_{BE1} - V_{BE2} &= kT/q\ In(I_C/I_S) - kT/q\ In(I_{REF}/I_S) \\ &= In(10)kT/q log_{10}(I_{PD}/I_{REF}) \\ &= 59.5\ mV log_{10}(I_{PD}/I_{REF})(T = 300\ K) \end{aligned} \quad (2)$$

The uncertain and temperature dependent saturation current IS, which appears in Equation 1, has thus been eliminated. To eliminate the temperature variation of kT/q, this difference voltage is processed by what is essentially an analog divider. Effectively, it puts a variable under Equation 2. The output of this process, which also involves a conversion from voltage-mode to current-mode, is an intermediate, temperature-corrected current:

$$I_{LOG} = I_Y\ log_{10}(I_{PD}/I_{REF}) \quad (3)$$

where I_Y is an accurate, temperature-stable scaling current that determines the slope of the function (the change in current per decade). For the AD8305, I_Y is 44 µA, resulting in a temperature independent slope of 44 mA/decade, for all values of I_{PD} and I_{REF}. This current is subsequently converted back to a voltage-mode output, V_{LOG}, scaled 200 mV/decade.

It is apparent that this output should be zero for $I_{PD} = I_{REF}$ and would need to swing negative for smaller values of input current. To avoid this, I_{REF} would need to be as small as the smallest value of I_{PD}. However, it is impractical to use such a small reference current as 1 nA. Accordingly, an offset voltage is added to V_{LOG} to shift it upward by 0.8 V when Pin VRDZ is directly connected to VREF. This has the effect of moving the intercept to the left by four decades, from 10 µA to 1 nA:

$$I_{LOG} = I_Y\ log_{10}(I_{PD}/I_{INTC}) \quad (4)$$

where I_{INTC} is the operational value of the intercept current. To disable this offset, Pin VRDZ should be grounded, then the intercept I_{INTC} is simply I_{REF}. Because values of $I_{PD} < I_{INTC}$ result in a negative VLOG, a negative supply of sufficient value is

required to accommodate this situation (see the Using a Negative Supply section).

The voltage, V_{LOG}, is generated by applying I_{LOG} to an internal resistance of 4.55 kΩ, formed by the parallel combination of a 6.69 kΩ resistor to ground and the 14.2 kΩ resistor to the VRDZ pin. When the VLOG pin is unloaded and the intercept repositioning is disabled by grounding VRDZ, the output current, I_{LOG}, generates a voltage at the VLOG pin of

$$\begin{aligned} V_{LOG} &= I_{LOG} \times 4.55\ k\Omega \\ &= 44\ \mu A \times 4.55\ k\Omega \times log_{10}(I_{PD}/I_{REF}) \\ &= V_Y\ log_{10}(I_{PD}/I_{REF}) \end{aligned} \quad (5)$$

where V_Y = 200 mV/decade, or 10 mV/dB. Note that any resistive loading on VLOG lowers this slope and also result in an overall scaling uncertainty due to the variability of the on-chip resistors. Consequently, this practice is not recommended.

V_{LOG} may also swing below ground when dual supplies (V_P and V_N) are used. When V_N = −0.5 V or larger, the input pins INPT and IREF may now be positioned at ground level by simply grounding VSUM.

MANAGING INTERCEPT AND SLOPE

When using a single supply, VRDZ should be directly connected to VREF to allow operation over the entire five-decade input current range. As noted previously, this introduces an accurate offset voltage of 0.8 V at the VLOG pin, equivalent to four decades, resulting in a logarithmic transfer function that can be written as

$$\begin{aligned} V_{LOG} &= V_Y\ log_{10}(10^4 \times I_{PD}/I_{REF}) \\ &= V_Y\ log_{10}\ (I_{PD}/I_{INTC}) \end{aligned} \quad (6)$$

where $I_{INTC} = I_{REF}/104$.

Thus, the effective intercept current I_{INTC} is only one ten-thousandth of I_{REF}, corresponding to 1 nA when using the recommended value of I_{REF} = 10 mA.

The slope can be reduced by attaching a resistor to the VLOG pin. This is strongly discouraged, in view of the fact that the on-chip resistors do not ratio correctly to the added resistance. Also, it is rare that one would want to lower the basic slope of 10 mV/dB; if this is needed, it should be effected at the low impedance output of the buffer, which is provided to avoid such miscalibration and also allow higher slopes to be used.

The AD8305 buffer is essentially an uncommitted op amp with rail-to-rail output swing, good load-driving capabilities, and a unity-gain bandwidth of >12 MHz. In addition to allowing the introduction of gain, using standard feedback networks and thereby increasing the slope voltage V_Y, the buffer can be used to implement multipole low-pass filters, threshold detectors, and a variety of other functions. Further details of these can be found in the AD8304 data sheet.

RESPONSE TIME AND NOISE CONSIDERATIONS

The response time and output noise of the AD8305 are fundamentally a function of the signal current, I_{PD}. For small currents, the bandwidth is proportional to I_{PD}, as shown in Figure 15. The output low frequency voltage-noise spectral-density is a function of I_{PD} (Figure 17) and also increases for small values of I_{REF}. Details of the noise and bandwidth performance of translinear log amps can be found in the AD8304 data sheet.

POWER SUPPLY SEQUENCING

Some applications may result in the presence of large input signal current (>1 mA) prior to the AD8305 being powered on. In such cases, it is recommended that power supply sequencing be implemented such that the AD8305 is powered on prior to the photodiode or current source.

In those applications where it is not possible to implement supply sequencing, VSUM should be driven externally by a low impedance source. In applications where a low impedance bias source is not readily available, the circuit shown in Figure 34 can be used.

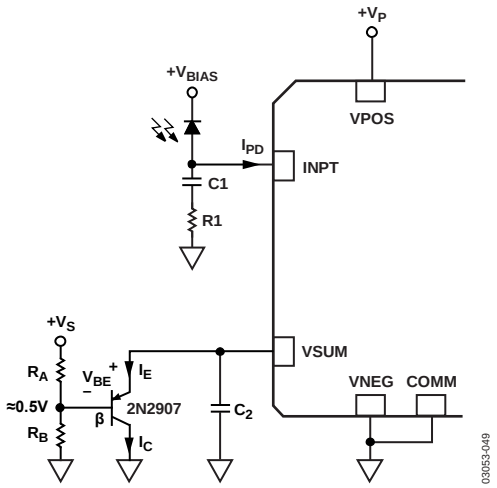


Figure 34. VSUM Biasing Circuit for Applications Where Large Input Signals Are Present Prior to AD8305 Power-On

The 2N2907 transistor used in Figure 34 is a common PNP-type switching transistor. R_a and R_b are selected such that the voltage at the base of the transistor is ~0.5 V.

In general, $V_S \times [R_b/(R_a + R_b)]$ should equal approximately 0.5 V. Setting R_a = 5 kΩ and R_b = 1 kΩ, results in 500 μA of additional quiescent current for a 3 V supply under normal operation. Larger resistor values may be used for this divider network by choosing a transistor with a higher β than the 2N2907.

Given a typical V_{be} of 0.7 V, the voltage at VSUM is ~1.2 V when the AD8305 is off and a large input signal is being applied. Once the AD8305 is powered on the voltage at VSUM is pulled down to its nominal value of 0.5 V. The circuit in Figure 34 is tested for 3 V to 5 V positive supplies over the full temperature range for the AD8305. C_1, and R_1 are the components that make up

the input compensation network and C_2 is the recommended bypassing capacitor on VSUM.

If board space limits the amount of external circuitry to the AD8305 it is possible to eliminate the transistor in Figure 34 and connect the resistor divider directly to VSUM. In this case the bias voltage at VSUM and INPT is set by the resistor values selected for the divider, not the internal biasing of the AD8305.

APPLICATIONS INFORMATION

The AD8305 is easy to use in optical supervisory systems and in similar situations where a wide ranging current is to be converted to its logarithmic equivalent, which is represented in decibel terms. Basic connections for measuring a single-current input are shown in Figure 35, which also includes various nonessential components.

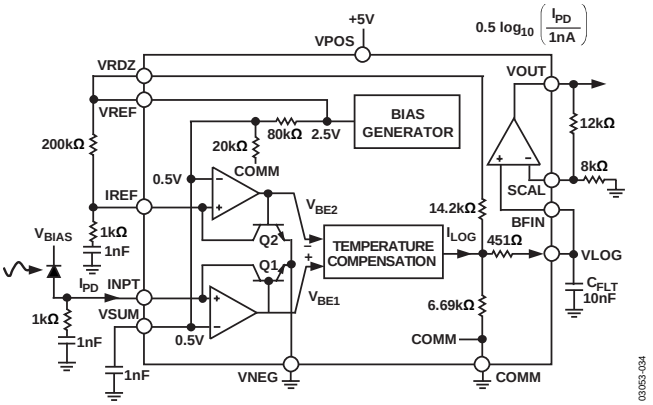


Figure 35. Basic Connections for Fixed Intercept Use

The 2 V difference in voltage between the VREF and INPT pins in conjunction with the external 200 kΩ resistor R_{REF} provide a reference current, I_{REF}, of 10 μA into Pin IREF. Connecting pin VRDZ to VREF raises the voltage at VLOG by 0.8 V, effectively lowering the intercept current, I_{INTC}, by a factor of 104 to position it at 1 nA. A wide range of other values for I_{REF}, from under 100 nA to over 1 mA, may be used. The effect of such changes is shown in Figure 5.

Any temperature variation in R_{REF} must be taken into account when estimating the stability of the intercept. Also, the overall noise increases when using very low values of I_{REF}. In fixed intercept applications, there is little benefit in using a large reference current, since this only compresses the low current end of the dynamic range when operated from a single supply, here shown as 5 V. The capacitor between VSUM and ground is recommended to minimize the noise on this node and to help provide a clean reference current.

Because the basic scaling at VLOG is 0.2 V/decade, and a swing of 4 V at the buffer output would correspond to 20 decades, it is often useful to raise the slope to make better use of the rail-to-rail voltage range. For illustrative purposes, the circuit in Figure 35 provides an overall slope of 0.5 V/ decade (25 mV/dB). Thus, using I_{REF} = 10 μA, V_{LOG} runs from 0.2 V at I_{PD} = 10 nA to 1.4 V at I_{PD} = 1 mA while the buffer output runs from 0.5 V to 3.5 V, corresponding to a dynamic range of 120 dB (electrical, that is, 60 dB optical power).

The optional capacitor from VLOG to ground forms a single-pole low-pass filter in combination with the 4.55 kΩ resistance at this pin. For example, using a C_{FLT} of 10 nF, the −3 dB corner frequency is 3.5 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multipole filters are more effective in reducing the total noise; examples are provided in the AD8304 data sheet.

The dynamic response of this overall input system is influenced by the external RC networks connected from the two inputs (INPT, IREF) to ground. These are required to stabilize the input systems over the full current range. The bandwidth changes with the input current due to the widely varying pole frequency. The RC network adds a zero to the input system to ensure stability over the full range of input current levels. The network values shown in Figure 35 usually suffice, but some experimentation may be necessary when the photodiode capacitance is high.

Although the two current inputs are similar, some care is needed to operate the reference input at extremes of current (<100 nA) and temperature (<0°C). Modifying the RC network to 4.7 nF and 2 kΩ is recommended for measuring 10 nA at −40°C. By inspecting the transient response to perturbations in I_{REF} at representative current levels, the capacitor value can be adjusted to provide fast rise and fall times with acceptable settling. To fine tune the network zero, the resistor value should be adjusted.

CALIBRATION

The AD8305 has a nominal slope and intercept of 200 mV/decade and 1 nA, respectively. These values are untrimmed, and the slope alone may vary as much as 7.5% over temperature. For this reason, it is recommended that a simple calibration be done to achieve increased accuracy.

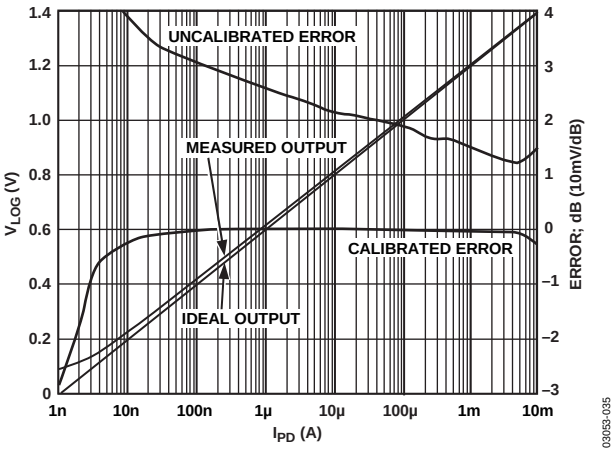


Figure 36. Using Two-Point Calibration to Increase Measurement Accuracy

Figure 36 shows the improvement in accuracy when using a two point calibration method. To perform this calibration, apply two known currents, I_1 and I_2, in the linear operating range between 10 nA and 1 mA. Measure the resulting output, V_1 and V_2, respectively, and calculate the slope m and intercept b.

$$m = (V_1 - V_2)/[log_{10}(I_1) - log_{10}(I_2)] \quad (7)$$

$$b = V_1 - m \times log_{10}(I_1) \quad (8)$$

The same calibration is performed with two known optical powers, P_1 and P_2. This allows for calibration of the entire measurement system while providing a simplified relationship between the incident optical power and V_{LOG} voltage.

$$m = (V_1 - V_2)/(P_1 - P_2) \quad (9)$$

$$b = V_1 - m \times P_1 \quad (10)$$

The uncalibrated error line in Figure 36 is generated assuming that the slope of the measured output was 200 mV/ decade when in fact it was actually 194 mV/decade. Correcting for this discrepancy decreased measurement error up to 3 dB.

USING A NEGATIVE SUPPLY

Most applications of the AD8305 require only a single supply of 3.0 V to 5.5 V. However, to provide further versatility, dual supplies may be employed, as illustrated in Figure 37.

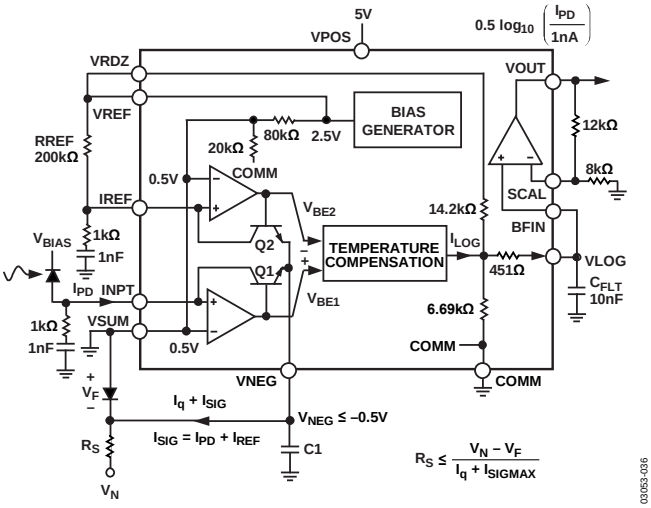


Figure 37. Negative Supply Application

The use of a negative supply, V_N, allows the summing node to be placed at ground level whenever the input transistor (Q1 in Figure 33) has a sufficiently negative bias on its emitter. When $V_{NEG} = -0.5$ V, the V_{CE} of Q1 and Q2 is the same as for the default case when VSUM is grounded. This bias does not need to be accurate, and a poorly defined source can be used. The source does, however, need to be able to support the quiescent current as well as the INPT and IREF signal current. For example, it may be convenient to utilize a forward-biased junction voltage of about 0.7 V or a Schottky barrier voltage of a little over 0.5 V. The effect of supply on the dynamic range and accuracy can be seen in Figure 10.

With the summing node at ground, the AD8305 may now be used as a voltage-input log amp at either the numerator input, INPT, or the denominator input, IREF, by inserting a suitably scaled resistor from the voltage source to the relevant pin. The overall accuracy for small input voltages is limited by the voltage offset at the inputs of the JFET op amps.

The use of a negative supply also allows the output to swing below ground, thereby allowing the intercept to correspond to a midrange value of I_{PD}. However, the voltage, V_{LOG}, remains referenced to the ACOM pin, and while it does not swing negative for default operating conditions, it is free to do so, thus, adding a resistor from VLOG to the negative supply lowers all values of VLOG, which raises the intercept. The disadvantage of this method is that the slope is reduced by the shunting of the external resistor, and the poorly defined ratio of on-chip and off-chip resistances causes errors in both the slope and the intercept.

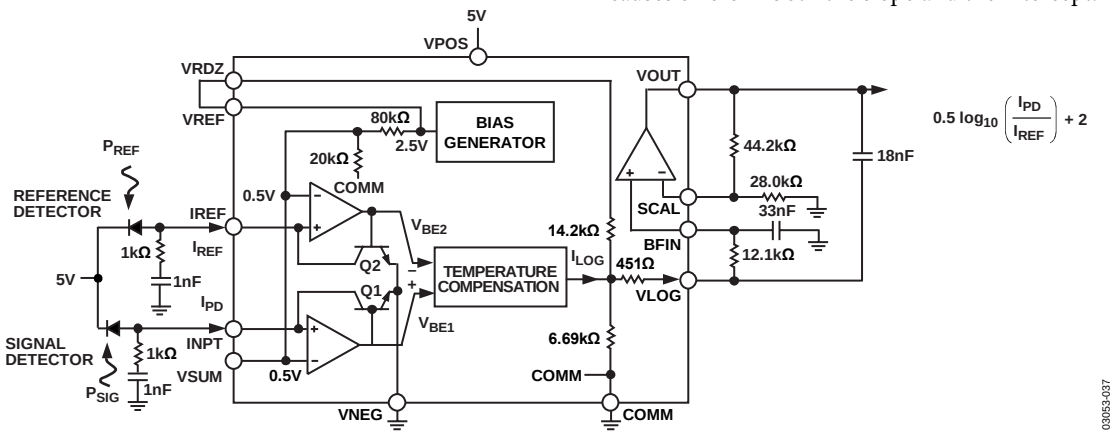


Figure 38. Optical Absorbance Measurement

LOG-RATIO APPLICATIONS

It is often desirable to determine the ratio of two currents, for example, in absorbance measurements. These are commonly used to assess the attenuation of a passive optical component, such as an optical filter or variable optical attenuator. In these situations, a reference detector is used to measure the incident power entering the component. The exiting power is then measured using a second detector and the ratio is calculated to determine the attenuation factor. Because the AD8305 is fundamentally a ratiometric device, having nearly identical logging systems for both numerator and denominator (I_{PD} and I_{REF}, respectively), it can greatly simplify such measurements.

Figure 38 illustrates the AD8305 log-ratio capabilities in optical absorbance measurements. Here a reference detector diode is used to provide the reference current, I_{REF}, proportional to the optical reference power level. A second detector measures the transmitted signal power, proportional to I_{PD}. The AD8305 calculates the logarithm of the ratio of these two currents, as shown in Equation 11, and which is reformulated in power terms in Equation 12. Both of these equations include the internal factor of 10,000 introduced by the output offset applied to V_{LOG} via pin VRDZ. If the true (nonoffset) log ratio shown in Equation 4 is preferred, VRDZ should be grounded to remove the offset. As already noted, the use of a negative supply at Pin VNEG allows both V_{LOG} and the buffer output to swing below ground, and also allow the input pins INPT and IREF to be set to ground potential. Therefore, the AD8305 may also be used to determine the log ratio of two voltages.

Figure 38 also illustrates how a second order Sallen-Key low-pass filter can be realized using two external capacitors and one resistor. Here, the corner frequency is set to 1 kHz and the filter Q is chosen to provide an optimally flat (overshoot-free) pulse response. To scale this frequency either up or down, simply scale the capacitors by the appropriate factor. Note that one of the resistors needed to realize this filter is the output resistance of 4.55 kΩ present at Pin VLOG. While this does not ratio exactly to the external resistor, which may slightly alter the Q of the filter, the effect on pulse response is be negligible for most purposes. Note that the gain of the buffer (×2.5) is an integral part of this illustrative filter design; in general, the filter may be redesigned for other closed-loop gains.

The transfer characteristics can be expressed in terms of optical power. If we assume that the two detectors have equal responsivities, the relationship is

$$V_{OUT} = 0.5\ V\ log_{10}(10^4 \times P_{SIG}/P_{REF}) \quad (11)$$

Using the identity $\log_{10}(AB) = \log_{10}A + \log_{10}B$ and defining the attenuation as $-10 \times \log_{10}(P_{SIG}/P_{REF})$, the overall transfer characteristic can be written as

$$V_{OUT} = 2 - 50\ mV/dB \times \alpha \quad (12)$$

where $\alpha = -10 \times \log_{10}(P_{SIG}/P_{REF})$

Figure 39 illustrates the linear-in-dB relationship between the absorbance and the output of the circuit in Figure 38.

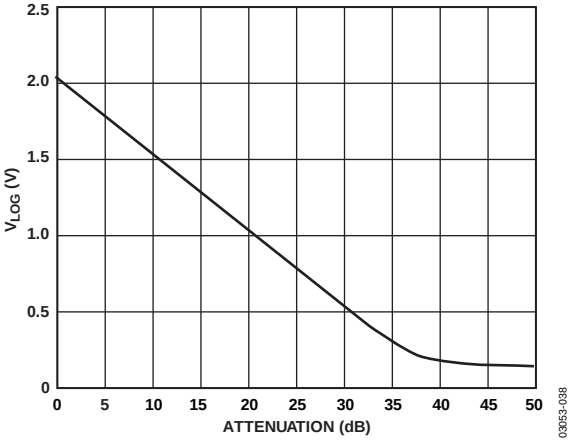


Figure 39. Example of an Absorbance Transfer Function

REVERSING THE INPUT POLARITY

Some applications may require interfacing to a circuit that sources current rather than sinks current, such as connecting to the cathode side of a photodiode. Figure 40 shows the use of a current mirror circuit. This allows for simultaneous monitoring of the optical power at the cathode, and a data recovery path using a transimpedance amplifier at the anode. The modified Wilson mirror provides a current gain very close to unity and a high output resistance. Figure 41 shows measured transfer function and law conformance performance of the AD8305 in conjunction with this current mirror interface.

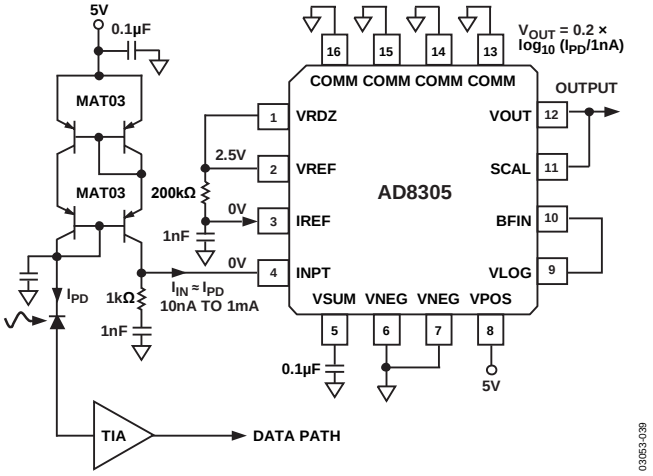


Figure 40. Wilson Current Mirror for Cathode Interfacing

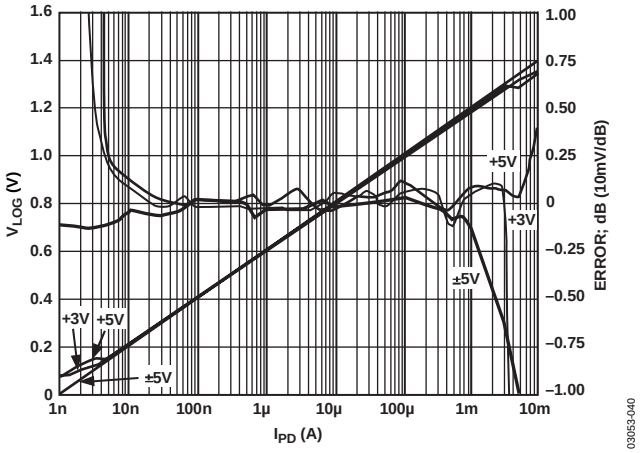


Figure 41. Log Output and Error Using Current Mirror with Various Supplies

CHARACTERIZATION METHODS

During the characterization of the AD8305, the device was treated as a precision current-input logarithmic converter, because it is not practical for several reasons to generate accurate photocurrents by illuminating a photodiode. The test currents are generated by using well calibrated current sources, such as the Keithley 236, or by using a high value resistor from a voltage source to the input pin. Great care is needed when using very small input currents. For example, the triax output connection from the current generator was used with the guard tied to VSUM. The input trace on the PC board was guarded by connecting adjacent traces to VSUM.

These measures are needed to minimize the risk of leakage current paths. With 0.5 V as the nominal bias on the INPT pin, a leakage-path resistance of 1 GΩ to ground would subtract 0.5 nA from the input, which amounts to an error of −0.44 dB for a source current of 10 nA. Additionally, the very high output resistance at the input pins and the long cables commonly needed during characterization allow 60 Hz and RF emissions to introduce substantial measurement errors. Careful guarding techniques are essential to reduce the pickup of these spurious signals.

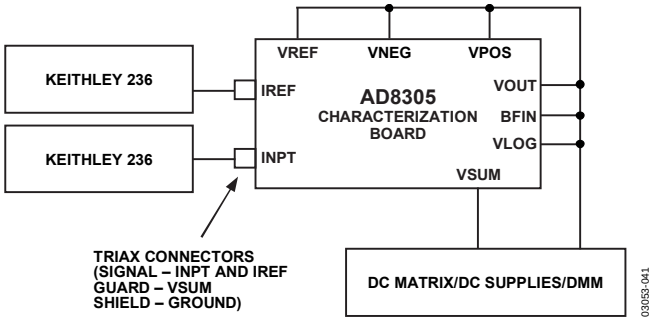


Figure 42. Primary Characterization Setup

The primary characterization setup shown in Figure 42 is used to measure V_{REF}, the static (dc) performance, logarithmic conformance, slope and intercept, the voltages appearing at pins VSUM, INPT and IREF, and the buffer offset and V_{REF} drift with temperature. To ensure stable operation over the full current range of I_{REF} and temperature extremes, filter components of C1 = 4.7 nF and R13 = 2 kΩ are used at pin to IREF ground. In some cases, a fixed resistor between pins VREF and IREF was used in place of a precision current source. For the dynamic tests, including noise and bandwidth measurements, more specialized setups are required.

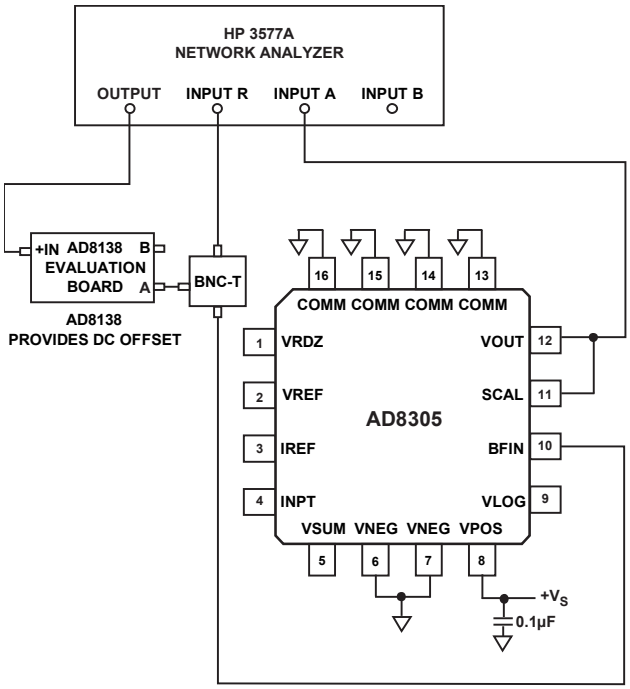


Figure 43. Configuration for Buffer Amplifier Bandwidth Measurement

Figure 43 shows the configuration used to measure the buffer amplifier bandwidth. The AD8138 evaluation board includes provisions to offset VLOG at the buffer input, allowing measurements over the full range of I_{PD} using a single supply. The network analyzer input impedances were set to 1 MΩ.

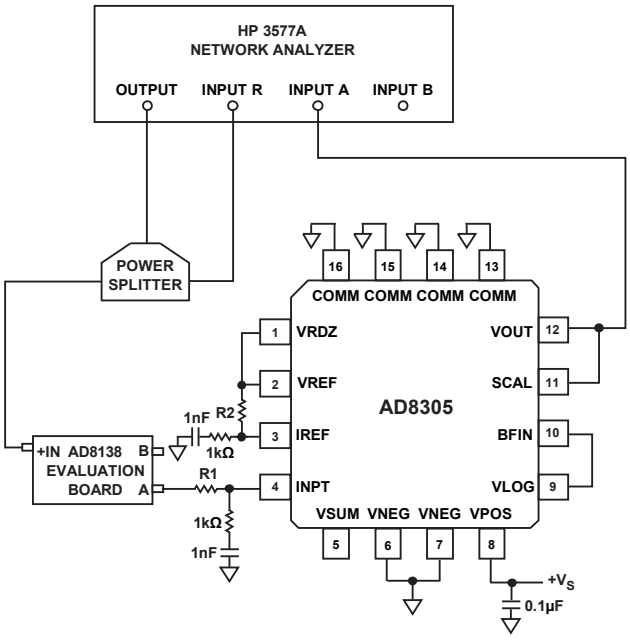


Figure 44. Configuration for Logarithmic Amplifier Bandwidth Measurement

The setup shown in Figure 44 was used for frequency response measurements of the logarithmic amplifier section. The AD8138 output is offset to 1.5 V dc and modulated to a depth of 5% at frequency. R1 is chosen (over a wide range of values up to 1.0 GΩ) to provide I_{PD}. The buffer was used to deload VLOG from the measurement system.

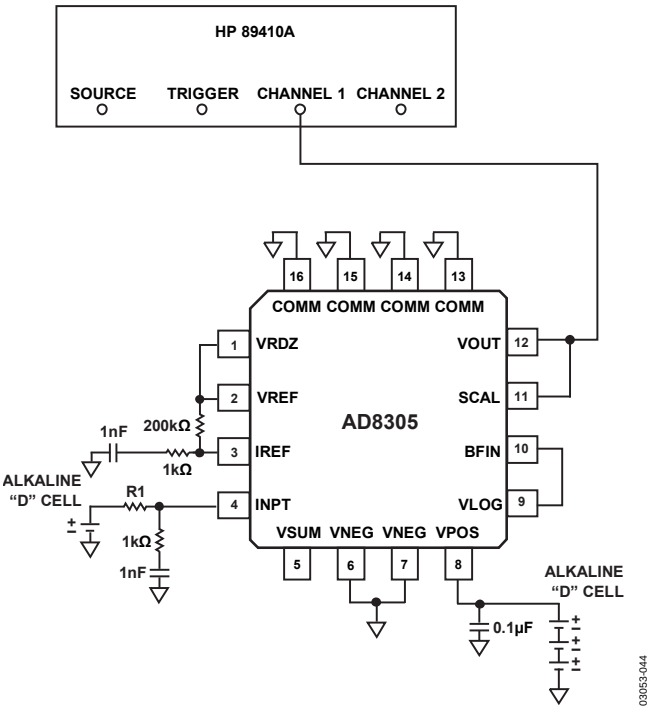


Figure 45. Configuration for Noise Spectral Density Measurement

The configuration in Figure 45 is used to measure the noise performance. Batteries provide both the supply voltage and the input current to minimize the introduction of spurious noise and ground loop effects. The entire evaluation system, including the current setting resistors, is mounted in a closed aluminum enclosure to provide additional shielding to external noise sources.

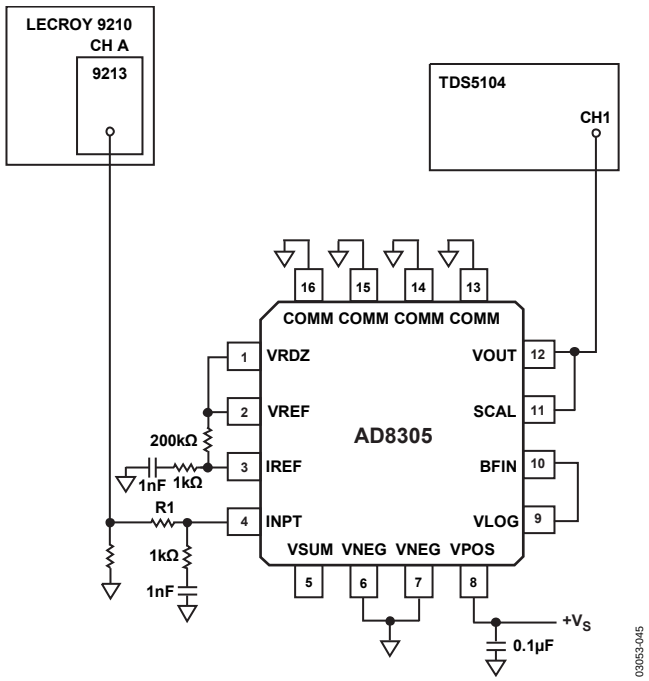


Figure 46. Configuration for Logarithmic Amplifier Pulse Response Measurement

Figure 46 shows the setup used to make the pulse response measurements. As with the bandwidth measurement, the VLOG is connected directly to BFIN and the buffer amplifier is configured for unity gain. The output of the buffer is connected through a short cable to the TDS5104 scope with input impedance set to 1 MΩ. The LeCroy's output is offset to create the initial pedestal current for a given value of R1, the pulse then creates one-decade current step.

EVALUATION BOARD

An evaluation board is available for the AD8305, the schematic for which is shown in Figure 49. It can be configured for a wide variety of experiments. The buffer gain is factory-set to unity, providing a slope of 200 mV/decade, and the intercept is set to 1 nA. Table 4 describes the various configuration options.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
P1	Supply interface. Provides access to supply pins, VNEG, COMM, and VPOS.	P1 = installed
P2, R8, R9, R10, R11, R17, R18	Monitor Interface. By adding 0 Ω resistors to R8, R9, R10, R11, R17, and R18, the VRDZ, VREF, VSUM, VOUT, and VLOG pin voltages can be monitored using a high impedance probe.	P2 = not installed R8 = R9 = R10 = open (size 0603) R17 = R18 = open (size 0603)
R2, R3, R4, R6, R14, C2, C7, C9, C10	Buffer amplifier/output interface. The logarithmic slope of the AD8305 can be altered using the buffer's gain-setting resistors, R2 and R3. R4, R14, and C2 allow variation in the buffer loading. R6, C7, C9, and C10 are provided for a variety of filtering applications.	R2 = R6 = 0 Ω (size 0603) R3 = R4 = open (size 0603) R11 = R14 = 0 Ω (size 0603) C2 = C7 = open (size 0603) C9 = C10 = open (size 0603) VLOG = VOUT = installed
R1, R7, R19, R20	Intercept adjustment. The voltage dropped across resistor R1 determines the intercept reference current, nominally set to 10 μA using a 200 kΩ 1% resistor. R7 and R19 can be used to adjust the output-offset voltage at the VLOG output.	R1 = 200 kΩ (size 0603) R7 = R19 = 0 Ω (size 0603) R20 = open (size 0603)
R12, R15, C3, C4, C5, C6	Supply Decoupling.	C3 = C4 = 0.01 μF (size 0603) C5 = C6 = 0.1 μF (size 0603) R12 = R15 = 0 Ω (size 0603)
C11	VSUM decoupling capacitor.	C11 = 1 nF (size 0603)
R13, R16, C1, C8	Input compensation. Provides essential HF compensation at the input pins, INPT and IREF.	R13 = R16 = 1 kΩ (size 0603) C1 = C8 = 1 nF (size 0603)
IREF, INPT, PD, LK1, R5	Input interface. The test board is configured to accept a current through the SMA connector labeled INPT. An SC-style packaged photodiode can be used in place of the INPT SMA for optical interfacing. By removing R1 and adding a 0 Ω short for R5, a second current can be applied to the IREF input (also SMA) for evaluating the AD8305 in log-ratio applications.	IREF = INPT = installed PD = not installed LK1 = installed R5 = open (size 0603)
J1	SC-Style Photodiode. Allows for direct mounting of SC style photodiodes.	J1 = not installed

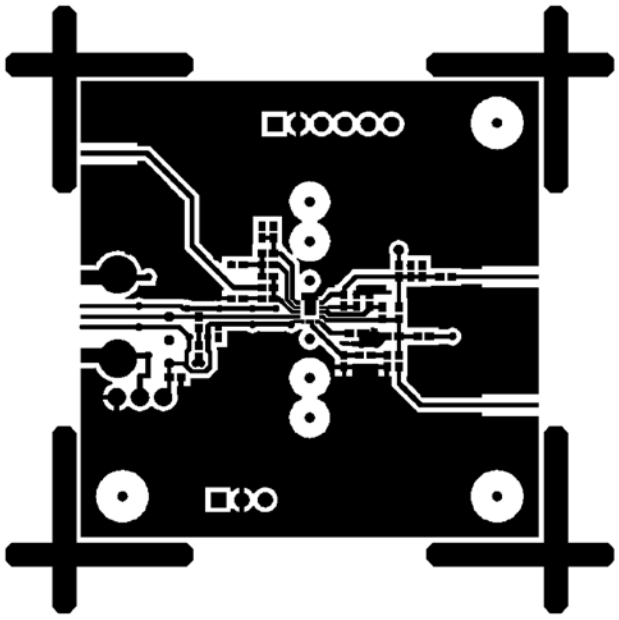


Figure 47. Component Side Layout

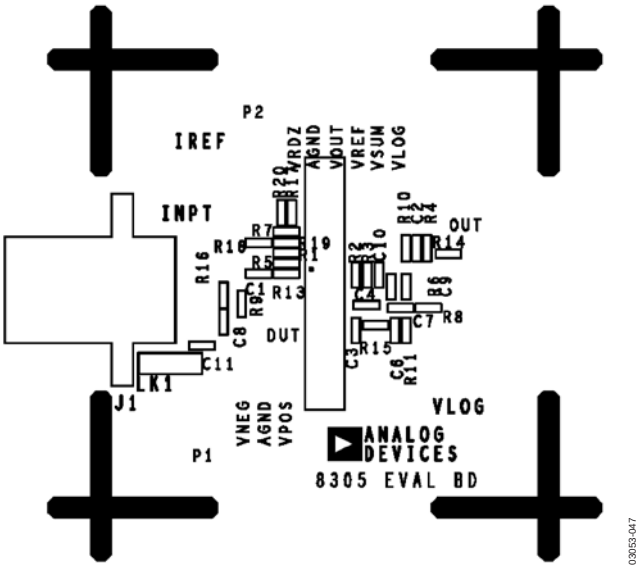


Figure 48. Component Side Silkscreen

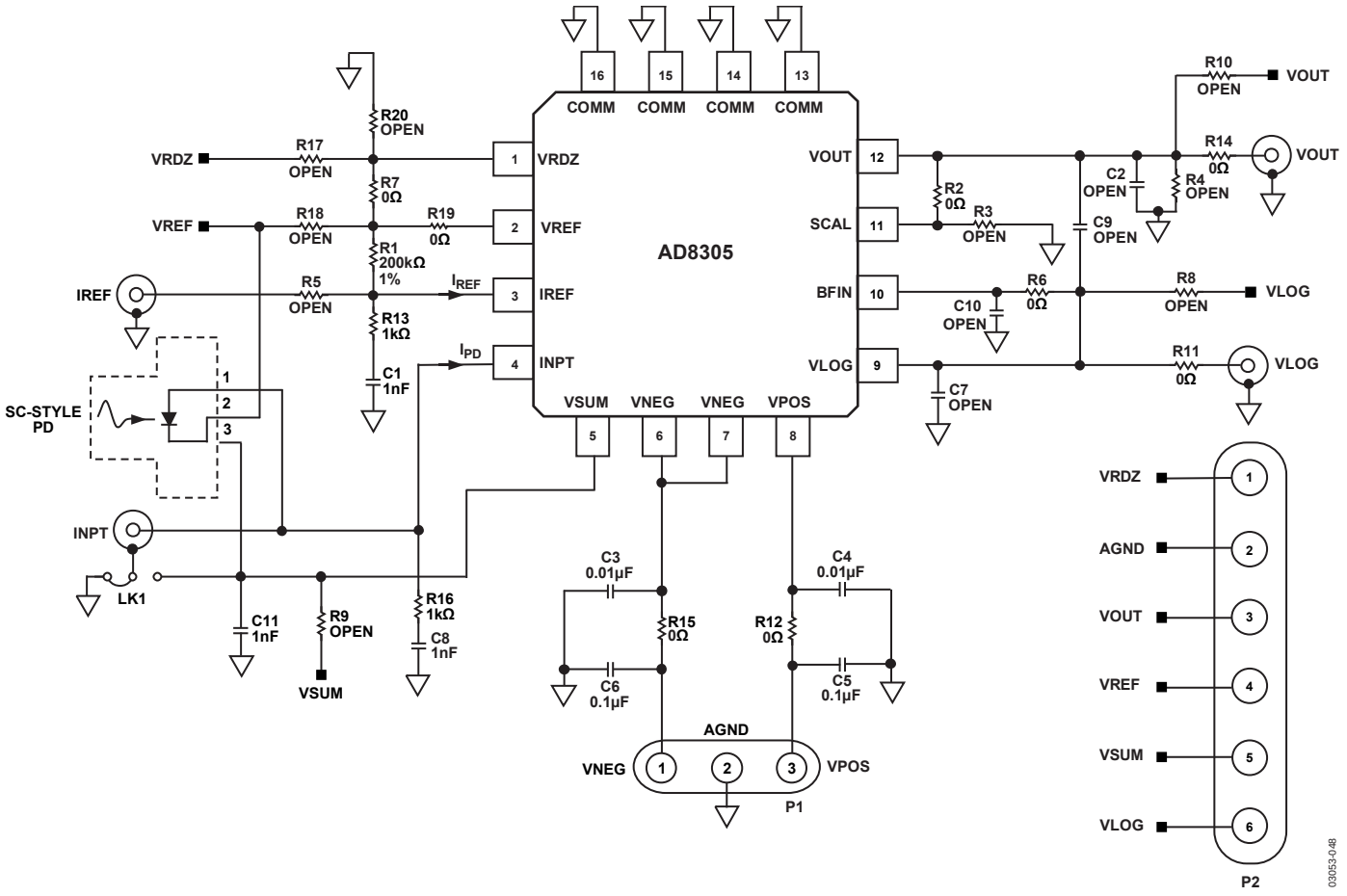


Figure 49. Evaluation Board Schematic

OUTLINE DIMENSIONS

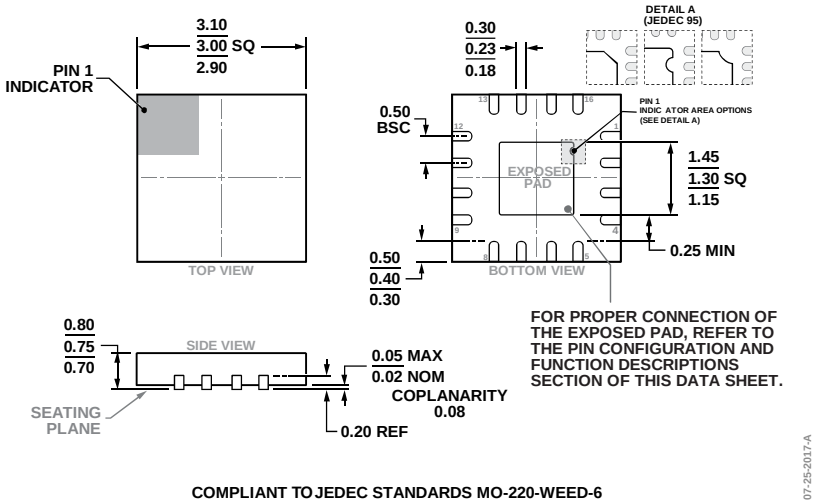


Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD8305ACP-R2	−40°C to +85°C	16-Lead LFCSP	CP-16-21	250	JEA
AD8305ACP-REEL7	−40°C to +85°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-21	1500	JEA
AD8305ACPZ-R2	−40°C to +85°C	16-Lead LFCSP	CP-16-21	250	JEA#
AD8305ACPZ-RL7	−40°C to +85°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-21	1500	JEA#
AD8305-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part; # denotes lead-free product may be top or bottom marked.

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