5 V CATV Line Driver Fine Step Output Power Control

AD8323

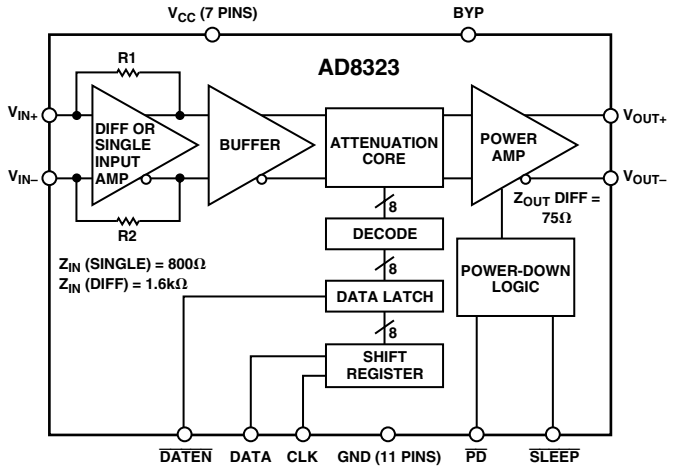
FEATURES

- Supports DOCSIS Standard for Reverse Path Transmission
- Gain Programmable in 0.75 dB Steps Over a 53.5 dB Range
- Low Distortion at 60 dBmV Output
  - –56 dBc SFDR at 21 MHz
  - –55 dBc SFDR at 42 MHz
- Output Noise Level
  - –48 dBmV in 160 kHz
- Maintains 75 Ω Output Impedance Power-Up and Power-Down Condition
- Upper Bandwidth: 100 MHz (Full Gain Range)
- 5 V Supply Operation
- Supports SPI Interfaces

APPLICATIONS

- Gain-Programmable Line Driver
  - HFC High-Speed Data Modems
  - Interactive Set-Top Boxes
  - PC Plug-in Modems
- General-Purpose Digitally Controlled Variable Gain Block

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8323 is a low-cost, digitally controlled, variable gain amplifier optimized for coaxial line driving applications such as cable modems that are designed to the MCNS-DOCSIS upstream standard. An 8-bit serial word determines the desired output gain over a 53.5 dB range resulting in gain changes of 0.7526 dB/LSB.

The AD8323 comprises a digitally controlled variable attenuator of 0 dB to –53.5 dB, which is preceded by a low noise, fixed gain buffer and is followed by a low distortion high power amplifier. The AD8323 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load, such as coaxial cable.

Distortion performance of –56 dBc is achieved with an output level up to 60 dBmV at 21 MHz bandwidth. A key performance and cost advantage of the AD8323 results from the ability to maintain a constant 75 Ω output impedance during power-up and power-down conditions. This eliminates the need for external 75 Ω termination, resulting in twice the effective output voltage when compared to a standard operational amplifier. In addition, this device has a sleep mode function that reduces the quiescent current to 4 mA.

The AD8323 is packaged in a low-cost 28-lead TSSOP, operates from a single 5 V supply, and has an operational temperature range of –40°C to +85°C.

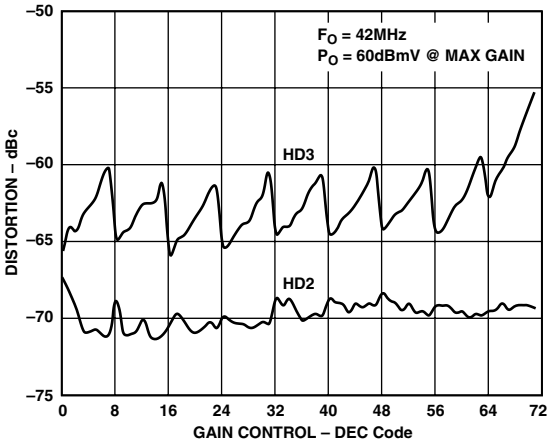


Figure 1. Harmonic Distortion vs. Gain Control

REV. 0

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AD8323—SPECIFICATIONS (T_A = 25°C, V_S = 5 V, R_L = R_{IN} = 75 Ω, V_{IN} = 116 mV p-p, V_{OUT} measured through a 1:1 transformer[1] with an insertion loss of 0.5 dB @ 10 MHz unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	Output = 60 dBmV, Max Gain		116		mV p-p
Noise Figure	Max Gain, f = 10 MHz		13.8		dB
Input Resistance	Single-Ended Input		800		Ω
	Differential Input		1600		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Gain Range		52.5	53.5	54.5	dB
Maximum Gain	Gain Code = 71 Dec	26.5	27.5	28.5	dB
Minimum Gain	Gain Code = 0 Dec	–27	–26	–25	dB
Gain Scaling Factor			0.7526		dB/LSB
OUTPUT CHARACTERISTICS					
Bandwidth (–3 dB)	All Gain Codes		100		MHz
Bandwidth Roll-Off	f = 65 MHz		1.3		dB
Bandwidth Peaking	f = 65 MHz		0		dB
Output Noise Spectral Density	Max Gain, f = 10 MHz		–34		dBmV in 160 kHz
	Min Gain, f = 10 MHz		–48		dBmV in 160 kHz
	Power-Down Mode, f = 10 MHz		–68		dBmV in 160 kHz
1 dB Compression Point	Max Gain, f = 10 MHz		18.5		dBm
Differential Output Impedance	Power-Up and Power-Down		75 ± 20%		Ω
OVERALL PERFORMANCE					
Second Order Harmonic Distortion	f = 21 MHz, P_{OUT} = 60 dBmV @ Max Gain		–77		dBc
	f = 42 MHz, P_{OUT} = 60 dBmV @ Max Gain		–71		dBc
	f = 65 MHz, P_{OUT} = 60 dBmV @ Max Gain		–64		dBc
Third Order Harmonic Distortion	f = 21 MHz, P_{OUT} = 60 dBmV @ Max Gain		–56		dBc
	f = 42 MHz, P_{OUT} = 60 dBmV @ Max Gain		–55		dBc
	f = 65 MHz, P_{OUT} = 60 dBmV @ Max Gain		–53		dBc
Gain Linearity Error	f = 10 MHz, Code to Code		±0.3		dB
Output Settling to 1 mV					
Due to Gain Change	Min to Max Gain		60		ns
Due to Input Step Change	Max Gain, V_{IN} = 0 V to 116 mV p-p		30		ns
Signal Feedthrough	Max Gain, $\overline{PD}$ = 0, f = 42 MHz		–30		dBc
POWER CONTROL					
Power-Up Settling Time to 1 mV	Max Gain, V_{IN} = 0		300		ns
Power-Down Settling Time to 1 mV	Max Gain, V_{IN} = 0		40		ns
Between Burst Transients[2]	Equivalent Output = 31 dBmV		3		mV p-p
	Equivalent Output = 60 dBmV		30		mV p-p
POWER SUPPLY					
Operating Range		4.75	5	5.25	V
Quiescent Current	Power-Up Mode	123	133	140	mA
	Power-Down Mode	30	35	40	mA
	Sleep Mode	2	4	7	mA
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES
[1]TOKO 617DB-A0070 used for above specifications. MACOM ETC-1-IT-15 can be substituted.
[2]Between Burst Transients measured at the output of a 42 MHz diplexer.

Specifications subject to change without notice.

LOGIC INPUTS (TTL/CMOS Compatible Logic) ($\overline{DATEN}$, CLK, SDATA, $\overline{PD}$, $\overline{SLEEP}$, V_{CC} = 5 V: Full Temperature Range)

Parameter	Min	Typ	Max	Unit
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, $\overline{DATEN}$	0		20	nA
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, $\overline{DATEN}$	–600		–100	nA
Logic "1" Current (V_{INH} = 5 V) $\overline{PD}$	50		190	µA
Logic "0" Current (V_{INL} = 0 V) $\overline{PD}$	–250		–30	µA
Logic "1" Current (V_{INH} = 5 V) $\overline{SLEEP}$	50		190	µA
Logic "0" Current (V_{INL} = 0 V) $\overline{SLEEP}$	–250		–30	µA

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} = 5 V, $T_R = T_F$ = 4 ns, f_{CLK} = 8 MHz unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Clock Pulsewidth (T_{WH})	16.0			ns
Clock Period (T_C)	32.0			ns
Setup Time SDATA vs. Clock (T_{DS})	5.0			ns
Setup Time $\overline{DATEN}$ vs. Clock (T_{ES})	15.0			ns
Hold Time SDATA vs. Clock (T_{DH})	5.0			ns
Hold Time $\overline{DATEN}$ vs. Clock (T_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{DATEN}$, Clock (T_R, T_F)			10	ns

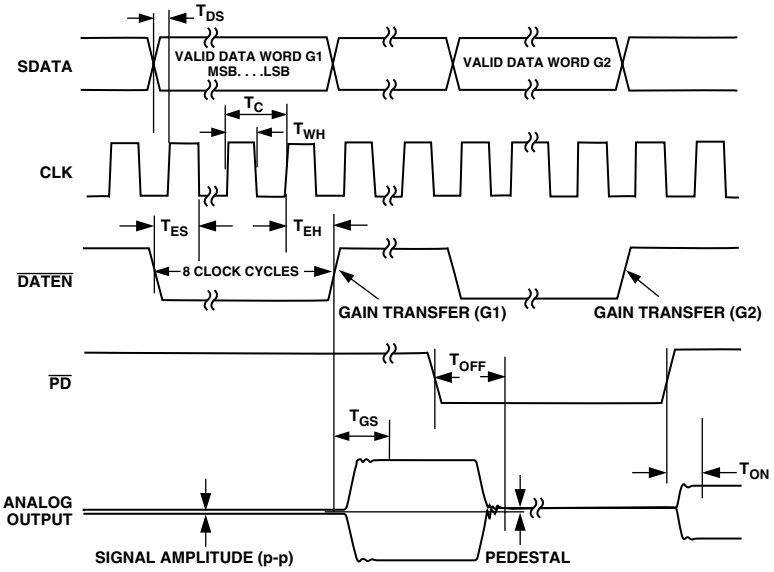


Figure 2. Serial Interface Timing

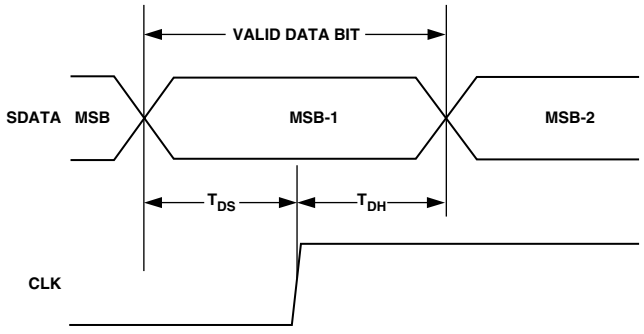


Figure 3. SDATA Timing

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $+V_S$
- Pins 5, 9, 10, 19, 20, 23, 27 . . . . . 6 V

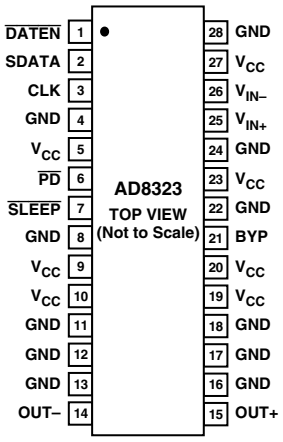
Input Voltages
- Pins 25, 26 . . . . . ±0.5 V
- Pins 1, 2, 3, 6, 7 . . . . . –0.8 V to +5.5 V

Internal Power Dissipation
- TSSOP . . . . . 0.9 W

Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 seconds . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	θ_{JA}	Package Option
AD8323ARU	–40°C to +85°C	28-Lead TSSOP	67.7°C/W*	RU-28
AD8323ARU-REEL	–40°C to +85°C	28-Lead TSSOP	67.7°C/W*	RU-28
AD8323-EVAL		Evaluation Board		

*Thermal Resistance measured on SEMI standard 4-layer board.

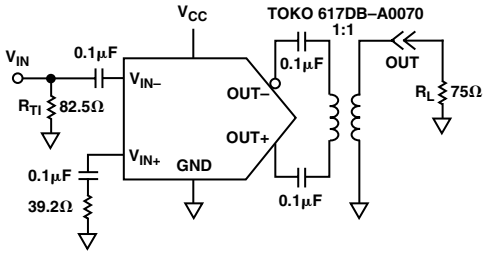
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8323 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

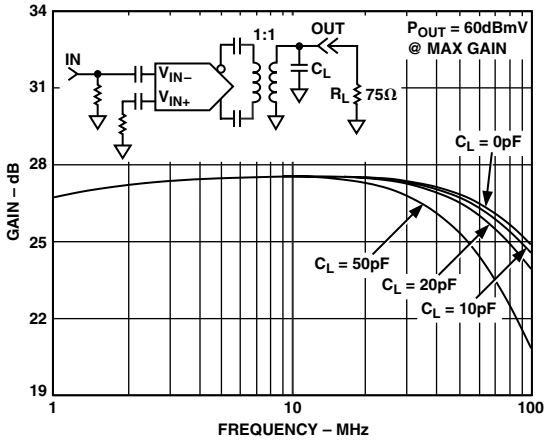


PIN FUNCTION DESCRIPTIONS

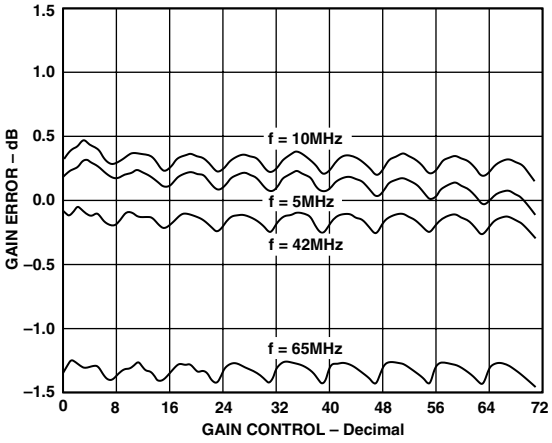
Pin No.	Mnemonic	Description
1	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
2	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (Most Significant Bit) first.
3	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
4, 8, 11,12, 13, 16, 17, 18, 22, 24, 28	GND	Common External Ground Reference.
5, 9, 10, 19, 20, 23, 27	V_{CC}	Common Positive External Supply Voltage. A 0.1 µF capacitor must decouple each pin.
6	$\overline{\text{PD}}$	Logic "0" powers down the part. Logic "1" powers up the part.
7	$\overline{\text{SLEEP}}$	Low Power Sleep Mode. In the Sleep mode, the AD8323's supply current is reduced to 4 mA. A Logic "0" powers down the part (High Z_{OUT} State) and a Logic "1" powers up the part.
14	OUT–	Negative Output Signal.
15	OUT+	Positive Output Signal.
21	BYP	Internal Bypass. This pin must be externally ac-coupled (0.1 µF cap).
25	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. For single-ended inverting operation, use a 0.1 µF decoupling capacitor and a 39.2 Ω resistor between V_{IN+} and ground.
26	$V_{IN–}$	Inverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.



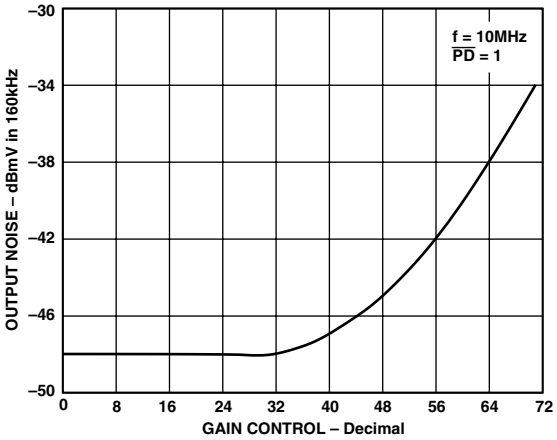
TPC 1. Basic Test Circuit



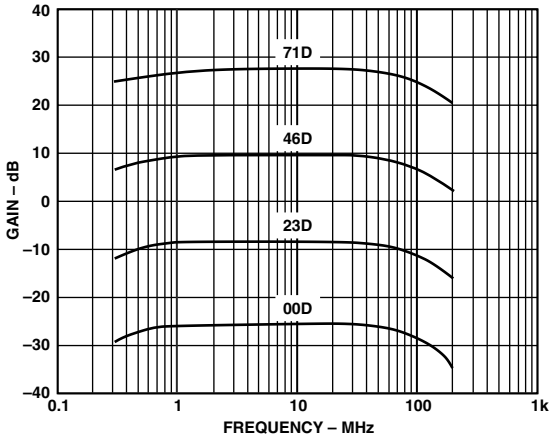
TPC 4. AC Response for Various Cap Loads



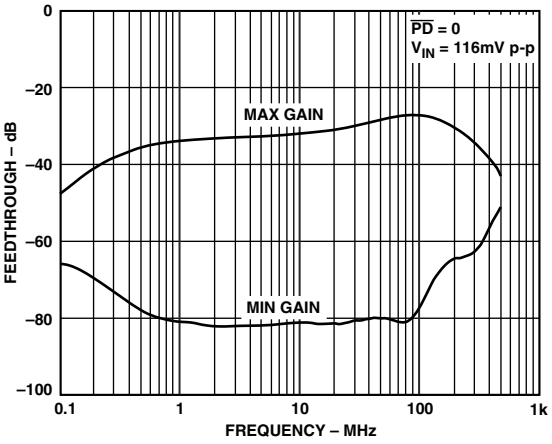
TPC 2. Gain Error vs. Gain Control



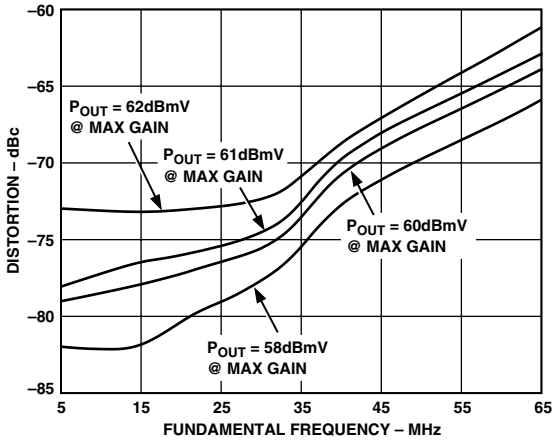
TPC 5. Output Referred Noise vs. Gain Control



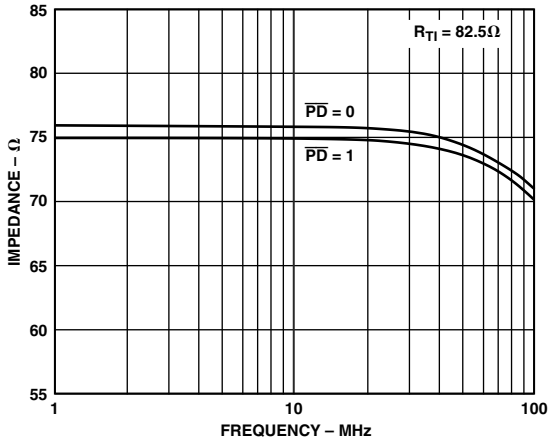
TPC 3. AC Response



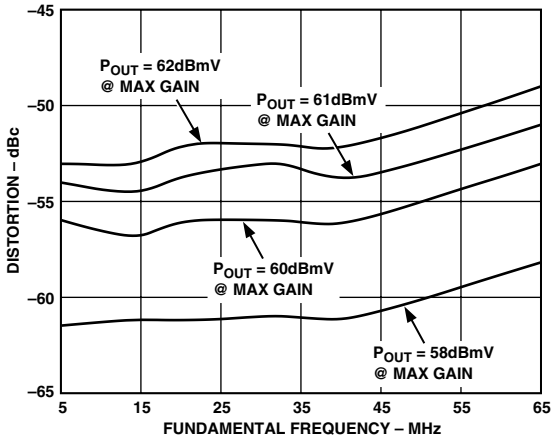
TPC 6. Input Signal Feedthrough vs. Frequency



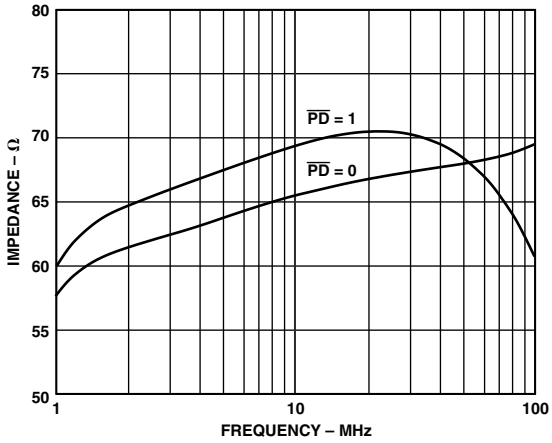
TPC 7. Second Order Harmonic Distortion vs. Frequency for Various Output Levels



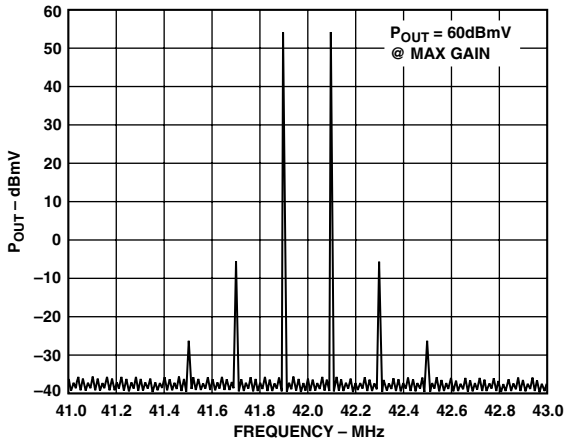
TPC 10. Input Impedance vs. Frequency



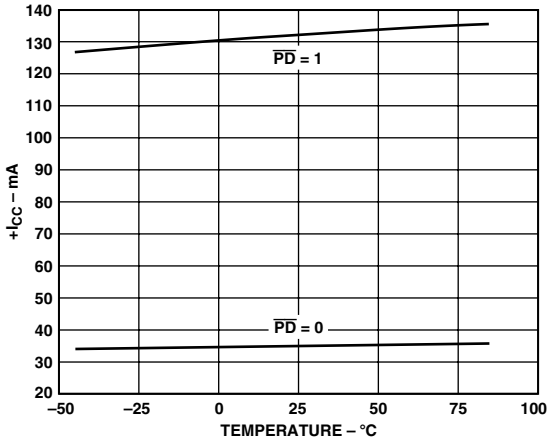
TPC 8. Third Order Harmonic Distortion vs. Frequency for Various Output Levels



TPC 11. Output Impedance vs. Frequency



TPC 9. Two-Tone Intermodulation Distortion



TPC 12. Supply Current vs. Temperature

APPLICATIONS

General Application

The AD8323 is primarily intended for use as the upstream power amplifier (PA) in DOCSIS (Data Over Cable Service Interface Specifications) certified cable modems and CATV set-top boxes. Upstream data is modulated in QPSK or QAM format, and done with DSP or a dedicated QPSK/QAM modulator. The amplifier receives its input signal from the QPSK/QAM modulator or from a DAC. In either case the signal must be low-pass filtered before being applied to the amplifier. Because the distance from the cable modem to the central office will vary with each subscriber, the AD8323 must be capable of varying its output power by applying gain or attenuation to ensure that all signals arriving at the central office are of the same amplitude. The upstream signal path contains components such as a transformer and diplexer that will result in some amount of power loss. Therefore, the amplifier must be capable of providing enough power into a 75 Ω load to overcome these losses without sacrificing the integrity of the output signal.

Operational Description

The AD8323 is composed of four analog functions in the power-up or forward mode. The input amplifier (preamp) can be used single-ended or differentially. If the input is used in the differential configuration, it is imperative that the input signals are 180 degrees out of phase and of equal amplitudes. This will ensure the proper gain accuracy and harmonic performance. The preamp stage drives a vernier stage that provides the fine tune gain adjustment. The 0.7526 dB step resolution is implemented in this stage and provides a total of approximately 5.25 dB of attenuation. After the vernier stage, a DAC provides the bulk of the AD8323's attenuation (8 bits or 48 dB). The signals in the preamp and vernier gain blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC into the output stage, which amplifies these currents to the appropriate levels necessary to drive a 75 Ω load. The output stage utilizes negative feedback to implement a differential 75 Ω output impedance. This eliminates the need for external matching resistors needed in typical video (or video filter) termination requirements.

SPI Programming and Gain Adjustment

Gain programming of the AD8323 is accomplished using a serial peripheral interface (SPI) and three digital control lines, $\overline{\text{DATEN}}$, SDATA, and CLK. To change the gain, eight bits of data are streamed into the serial shift register through the SDATA port. The SDATA load sequence begins with a falling edge on the $\overline{\text{DATEN}}$ pin, thus activating the CLK line. Although the CLK line is now activated, no change in gain is yet observed at the output of the amplifier. With the CLK line activated, data on the SDATA line is clocked into the serial shift register Most Significant Bit (MSB) first, on the rising edge of each CLK pulse. Because only a 7-bit shift register is used, the MSB of the 8-bit word is a "don't care" bit and is shifted out of the register on the eighth clock pulse. A rising edge on the $\overline{\text{DATEN}}$ line latches the contents of the shift register into the attenuator core resulting in a well controlled change in the output signal level. The serial interface timing for the AD8323 is shown in Figures 2 and 3. The programmable gain range of the AD8323 is –26 dB to +27.5 dB and scales 0.7526 dB per least significant bit (LSB). Because the AD8323 was characterized with a TOKO transformer, the stated gain values already take into account the losses associated with the transformer.

The gain transfer function is as follows:

$$A_V = 27.5\ dB - (0.7526\ dB \times (71 - CODE)) \text{ for } 0 \le CODE \le 71$$

where A_V is the gain in *dB* and *CODE* is the decimal equivalent of the 8-bit word.

Valid gain codes are from 0 to 71. Figure 4 shows the gain characteristics of the AD8323 for all possible values in an 8-bit word. Note that maximum gain is achieved at Code 71. From Code 72 through 127 the 5.25 dB of attenuation from the vernier stage is being applied over every eight codes, resulting in the sawtooth characteristic at the top of the gain range. Because the eighth bit is a "don't care" bit, the characteristic for codes 0 through 127 repeats from Codes 128 through 255.

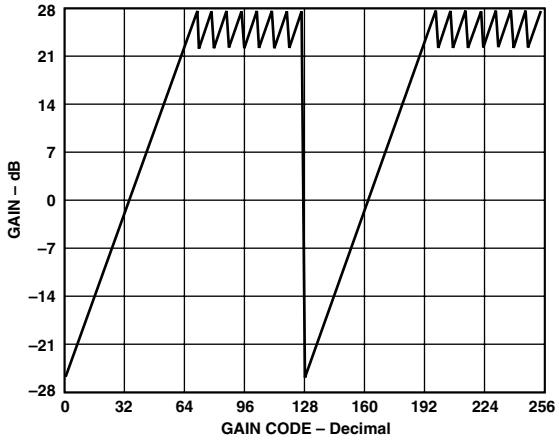


Figure 4. Gain vs. Gain Code

Input Bias, Impedance, and Termination

The V_{IN+} and V_{IN-} inputs have a dc bias level of approximately $V_{CC}/2$, therefore the input signal should be ac-coupled. The differential input impedance is approximately 1600 Ω while the single-ended input impedance is 800 Ω. If the AD8323 is being operated in a single-ended input configuration with a desired input impedance of 75 Ω, the V_{IN+} and V_{IN-} inputs should be terminated as shown in Figure 5. If an input impedance other than 75 Ω is desired, the values of R1 and R2 in Figure 5 can be calculated using the following equations:

$$Z_{IN} = R1 \| 800$$

$$R2 = Z_{IN} \| R1$$

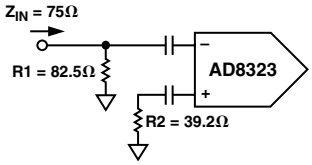


Figure 5. Single-Ended Input Termination

Output Bias, Impedance, and Termination

The differential output pins V_{OUT+} and V_{OUT-} are also biased to a dc level of approximately $V_{CC}/2$. Therefore, the outputs should be ac-coupled before being applied to the load. This may be accomplished by connecting 0.1 µF capacitors in series with the outputs as shown in the typical applications circuit of Figure 6. The differential output impedance of the AD8323 is internally maintained at 75 Ω, regardless of whether the amplifier is in forward transmit mode or reverse power-down mode, eliminating the need for external back termination resistors. A 1:1 transformer (TOKO #617DB-A0070) is used to couple the amplifier's differential output to the coaxial cable while maintaining a proper impedance match. If the output signal is being evaluated on standard 50 Ω test equipment, a 75 Ω to 50 Ω pad must be used to provide the test circuit with the correct impedance match.

Power Supply Decoupling, Grounding, and Layout Considerations

Careful attention to printed circuit board layout details will prevent problems due to associated board parasitics. Proper RF design technique is mandatory. The 5 V supply power should be delivered to each of the V_{CC} pins via a low impedance power bus to ensure that each pin is at the same potential. The power bus should be decoupled to ground with a 10 µF tantalum capacitor located in close proximity to the AD8323. In addition to the 10 µF capacitor, each V_{CC} pin should be individually decoupled to ground with a 0.1 µF ceramic chip capacitor located as close to the pin as possible. The pin labeled BYP (Pin 21) should also be decoupled with a 0.1 µF capacitor. The PCB should have a low-impedance ground plane covering all unused portions of the component side of the board, except in the area of the input and output traces (see Figure 11). It is important that all of the AD8323's ground pins are connected to the ground plane to ensure proper grounding of all internal nodes. The differential input and output traces should be kept as short and symmetrical as possible. In addition, the input and output traces should be kept far apart in order to minimize coupling (crosstalk) through the board. Following these guidelines will improve the overall performance of the AD8323 in all applications.

Initial Power-Up

When the 5 V supply is first applied to the V_{CC} pins of the AD8323, the gain setting of the amplifier is indeterminate. Therefore, as power is first applied to the amplifier, the $\overline{PD}$ pin should be held low (Logic 0) thus preventing forward signal transmission. After power has been applied to the amplifier, the gain can be set to the desired level by following the procedure in the SPI Programming and Gain Adjustment section. The $\overline{PD}$ pin can then be brought from Logic 0 to 1, enabling forward signal transmission at the desired gain level.

Asynchronous Power-Down

The asynchronous $\overline{PD}$ pin is used to place the AD8323 into "Between Burst" mode while maintaining a differential output impedance of 75 Ω. Applying a Logic 0 to the $\overline{PD}$ pin activates the on-chip reverse amplifier, providing a 74% reduction in consumed power. The supply current is reduced from approximately 133 mA to approximately 35 mA. In this mode of operation, between burst noise is minimized and the amplifier can no longer transmit in the upstream direction. In addition to the $\overline{PD}$ pin, the AD8323 also incorporates an asynchronous $\overline{SLEEP}$ pin, which may be used to place the amplifier in a high output impedance state and further reduce the supply current to approximately 4 mA. Applying a Logic 0 to the $\overline{SLEEP}$ pin places the amplifier into $\overline{SLEEP}$ mode. Transitioning into or out of $\overline{SLEEP}$ mode will result in a transient voltage at the output of the amplifier. Therefore, use only the $\overline{PD}$ pin for DOCSIS compliant "Between Burst" operation.

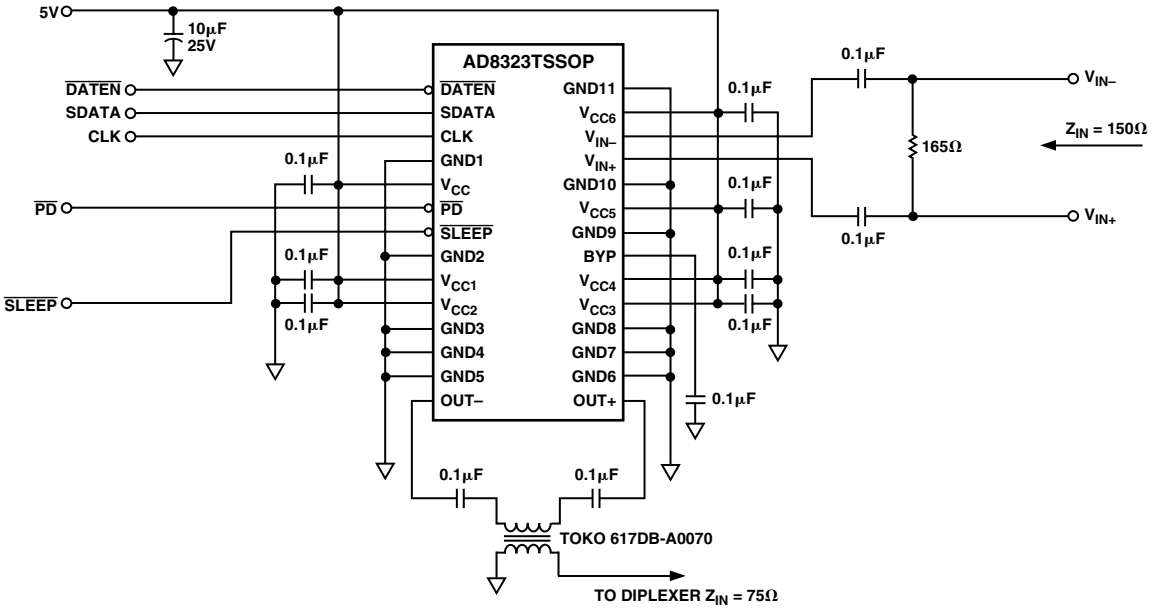


Figure 6. Typical Applications Circuit

Distortion, Adjacent Channel Power, and DOCSIS

In order to deliver 58 dBmV of high fidelity output power required by DOCSIS, the PA should be able to deliver about 60 dBmV to 61 dBmV in order to make up for losses associated with the transformer and diplexer. It should be noted that the AD8323 was characterized with the TOKO 617DB-A0070 transformer. TPC 7 and TPC 8 show the AD8323 second and third harmonic distortion performance versus fundamental frequency for various output power levels. These figures are useful for determining the inband harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency will be sharply attenuated by the low-pass filter function of the diplexer. Another measure of signal integrity is adjacent channel power or ACP. DOCSIS section 4.2.9.1.1 states, "Spurious emissions from a transmitted carrier may occur in an adjacent channel that could be occupied by a carrier of the same or different symbol rates." Figure 7 shows the measured ACP for a 16 QAM, 60 dBmV signal, taken at the output of the AD8323 evaluation board (see Figure 13 for evaluation board schematic). The transmit channel width and adjacent channel width in Figure 7 correspond to symbol rates of 160 $K_{SYM/SEC}$. Table I shows the ACP results for the AD8323 for all conditions in DOCSIS Table 4-7 "Adjacent Channel Spurious Emissions."

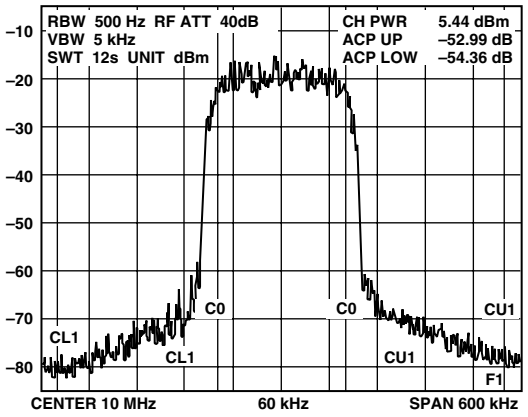


Figure 7. Adjacent Channel Power

Table I. ACP Performance for All DOCSIS Conditions (All Values in dBc)

TRANSMIT CHANNEL SYMBOL RATE	ADJACENT CHANNEL SYMBOL RATE				
	160 $K_{SYM/SEC}$	320 $K_{SYM/SEC}$	640 $K_{SYM/SEC}$	1280 $K_{SYM/SEC}$	2560 $K_{SYM/SEC}$
160 $K_{SYM/SEC}$	–53.0	–53.8	–55.0	–56.6	–56.3
320 $K_{SYM/SEC}$	–52.7	–53.4	–53.8	–54.8	–55.4
640 $K_{SYM/SEC}$	–53.8	–52.9	–53.3	–53.6	–54.2
1280 $K_{SYM/SEC}$	–53.7	–53.4	–53.0	–53.3	–53.5
2560 $K_{SYM/SEC}$	–55.4	–54.0	–53.6	–53.1	–53.3

Noise and DOCSIS

At minimum gain, the AD8323's output noise spectral density is 10 nV/$\sqrt{Hz}$ measured at 10 MHz. DOCSIS Table 4-8, "Spurious Emissions in 5 MHz to 42 MHz," specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 $K_{SYM/SECOND}$ is:

$$\left(20\log\left(\sqrt{\left(\frac{10\text{ nV}}{\sqrt{\text{Hz}}}\right)^2\times 160\text{ kHz}}\right)\right)+60=-48\text{ dBmV}$$

Comparing the computed noise power of –48 dBmV to the 8 dBmV signal yields –56 dBc, which meets the required level of –53 dBc set forth in DOCSIS Table 4-8. As the AD8323's gain is increased from this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal to noise ratio that improves with gain. In transmit disable mode, the output noise spectral density computed over 160 $K_{SYM/SECOND}$ is 1.0 nV/$\sqrt{Hz}$ or –68 dBmV.

Evaluation Board Features and Operation

The AD8323 evaluation board (Part # AD8323-EVAL) and control software can be used to control the AD8323 upstream cable driver via the parallel port of a PC. A standard printer cable connected between the parallel port and the evaluation board is used to feed all the necessary data to the AD8323 by means of the Windows-based, Microsoft Visual Basic control software. This package provides a means of evaluating the amplifier by providing a convenient way to program the gain/attenuation as well as offering easy control of the amplifiers' asynchronous $\overline{PD}$ and $\overline{SLEEP}$ pins. With this evaluation kit the AD8323 can be evaluated with either a single-ended or differential input configuration. The amplifier can also be evaluated with or without the PULSE diplexer in the output signal path. To remove the diplexer from the signal path, move the 0 Ω chip resistor at JP5 so the output signal is directed away from the diplexer and toward the CABLE port of the evaluation board. Also, remove the 0 Ω resistor at JP4. A schematic of the evaluation board is provided in Figure 13.

Overshoot on PC Printer Ports

The data lines on some PC parallel printer ports have excessive overshoot that may cause communications problems when presented to the CLK pin of the AD8323 (TP5 on the evaluation board). The evaluation board was designed to accommodate a series resistor and shunt capacitor (R1 and C15) to filter the CLK signal if required.

Transformer and Diplexer

A 1:1 transformer is needed to couple the differential outputs of the AD8323 to the cable while maintaining a proper impedance match. The specified transformer is available from TOKO (Part # 617DB-A0070); however, MA/COM part # ETC-1-1T-15 can also be used. The evaluation board is equipped with the TOKO transformer, but is also designed to accept the MA/COM transformer. The PULSE diplexer included on the evaluation board provides a high-order low-pass filter function, typically used in the upstream path. The ability of the PULSE diplexer to achieve DOCSIS compliance is neither expressed nor implied by Analog Devices Inc. Data on the diplexer should be obtained from PULSE.

Differential Inputs

The AD8323-EVAL evaluation board is designed to accommodate a Mini-Circuits T1-6T-KK81 1:1 transformer for the purpose of converting a single-ended (ground-referenced) input signal to differential inputs. Figure 8 and the following paragraphs identify two options for providing differential input signals to the AD8323 evaluation board.

Single-Ended-to-Differential Input (Figure 8, Option 1)
Install the Mini-Circuits T1-6T-KK81 1:1 transformer in the T1 location of the evaluation board. Place 0 Ω chip resistors at locations JP1, JP2, and JP3 such that the signal coming in V_{IN+} is directed toward the transformer and the differential signal coming out of the transformer is directed toward TP13 and TP14. For 75 Ω input impedance, install 39.2 Ω resistors in R5 and R6 located on the back side of the evaluation board. In this configuration the input signal must be applied to the V_{IN+} port of the evaluation board from a single-ended 75 Ω signal source. For input impedances other than 75 Ω, the correct value for R5 and R6 can be computed using the following equation:

$$\left(R5 = R6 = R\right), Desired\ Impedance = 2 \times \left(R \| 800\right)$$

Differential Input (Figure 8, Option 2)
If a differential signal source is available, it may be applied directly to both the V_{IN+} and V_{IN-} input ports of the evaluation board. In this case, 0 Ω chip resistors should be placed at locations R8, JP1, JP2, and JP3 such that the V_{IN+} and V_{IN-} signals are directed toward TP13 and TP14. Referring to Figure 8, Option 2, a differential input impedance of 150 Ω can be achieved by using a 165 Ω resistor for R7. For input impedances other than 150 Ω, the correct value for R7 can be computed using the following equation:

$$Desired\ Impedance = \left(R7 \| 1600\right)$$

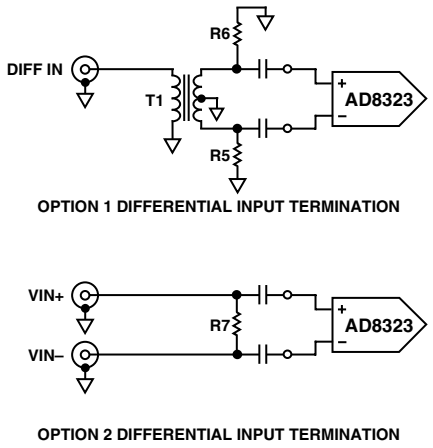


Figure 8. Differential Input Termination Options

Installing the Visual Basic Control Software
To install the "CABDRIVE_23" evaluation board control software, close all Windows applications and then run "SETUP.EXE" located on Disk 1 of the AD8323 Evaluation Software. Follow the on-screen instructions and insert Disk 2 when prompted to do so. Enter the path of the directory into which the software will be installed and select the button in the upper left corner to complete the installation.

Running the Software
To invoke the control software, go to START -> PROGRAMS -> CABDRIVE_23, or select the AD8323.EXE icon from the directory containing the software.

Controlling the Gain/Attenuation of the AD8323
The slide bar controls the AD8323's gain/attenuation, which is displayed in dB and in V/V. The gain scales at 0.7526 dB per LSB with the valid codes being from decimal 0 to 71. The gain code (i.e., position of the slide bar) is displayed in decimal, binary, and hexadecimal (see Figure 9).

POWER-UP, POWER-DOWN AND SLEEP

The "Power-Up" and "Power-Down" buttons select the mode of operation of the AD8323 by controlling the logic level on the asynchronous $\overline{PD}$ pin. The "Power-Up" button applies a Logic 1 to the $\overline{PD}$ pin putting the AD8323 in forward transmit mode. The "Power-Down" button applies a Logic 0 to the $\overline{PD}$ pin selecting reverse mode, where the forward signal transmission is disabled while a back termination of 75 Ω is maintained. Checking the "Enable SLEEP Mode" box applies a Logic 0 to the asynchronous $\overline{SLEEP}$ pin, putting the AD8323 into SLEEP mode.

Memory Section
The "MEMORY" section of the software provides a convenient way to alternate between two gain settings. The "X->M1" button stores the current value of the gain slide bar into memory while the "RM1" button recalls the stored value, returning the gain slide bar to that level. The "X->M2" and "RM2" buttons work in the same manner.

EVALUATION BOARD FEATURES AND OPERATION

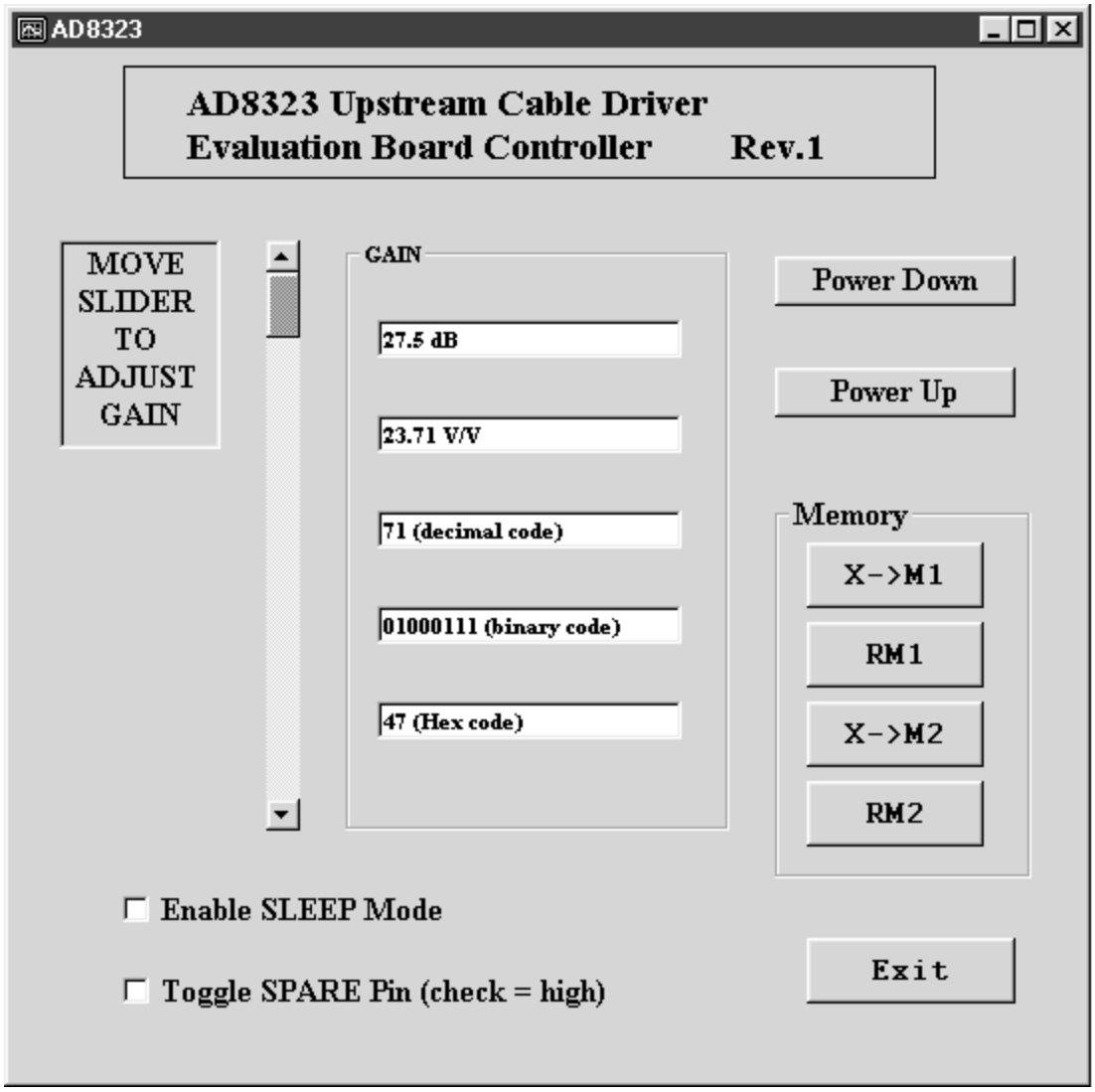


Figure 9. Screen Display of Windows-Based Control Software

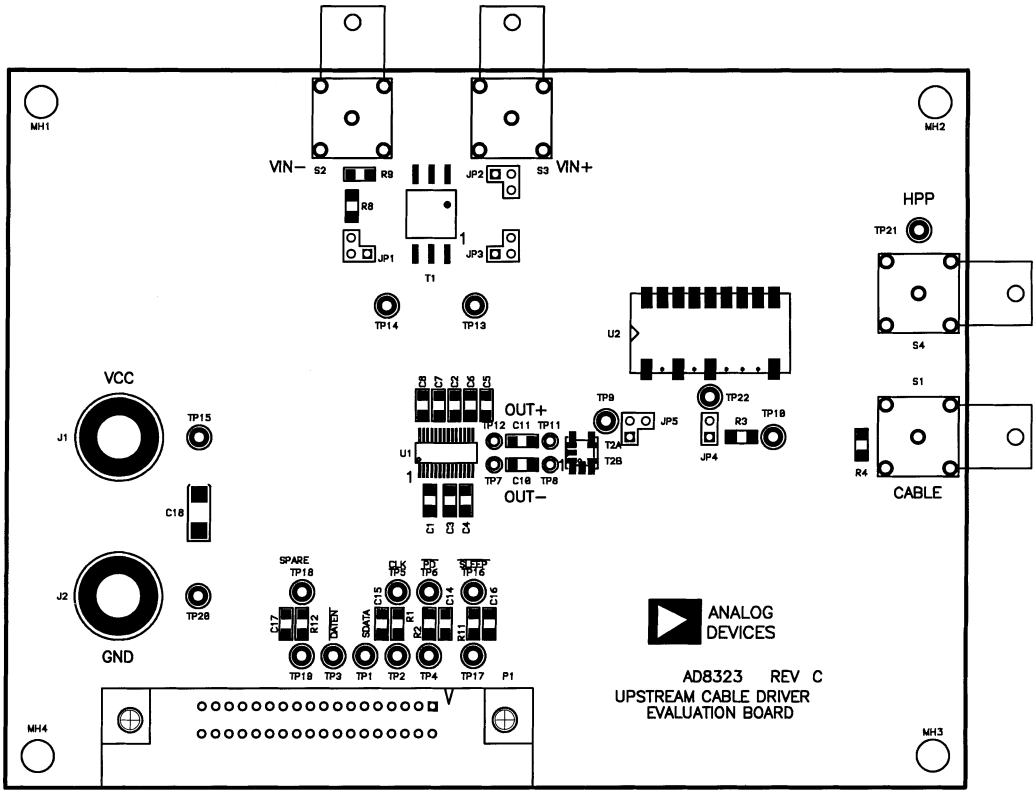


Figure 10. Evaluation Board—Assembly (Component Side)

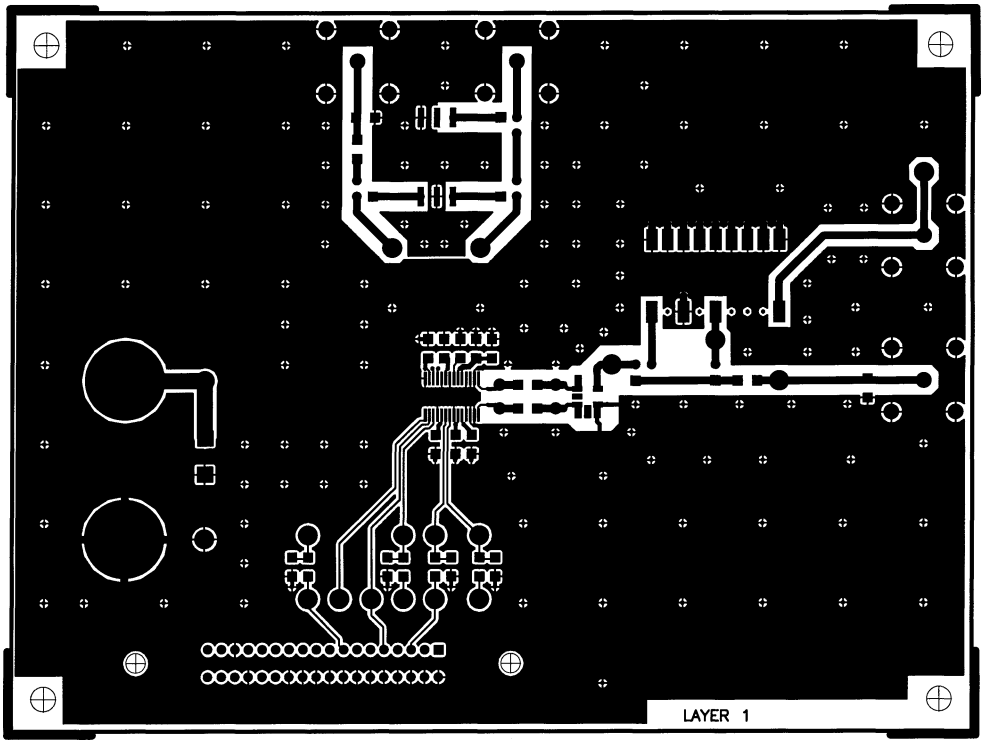


Figure 11. Evaluation Board Layout (Component Side)

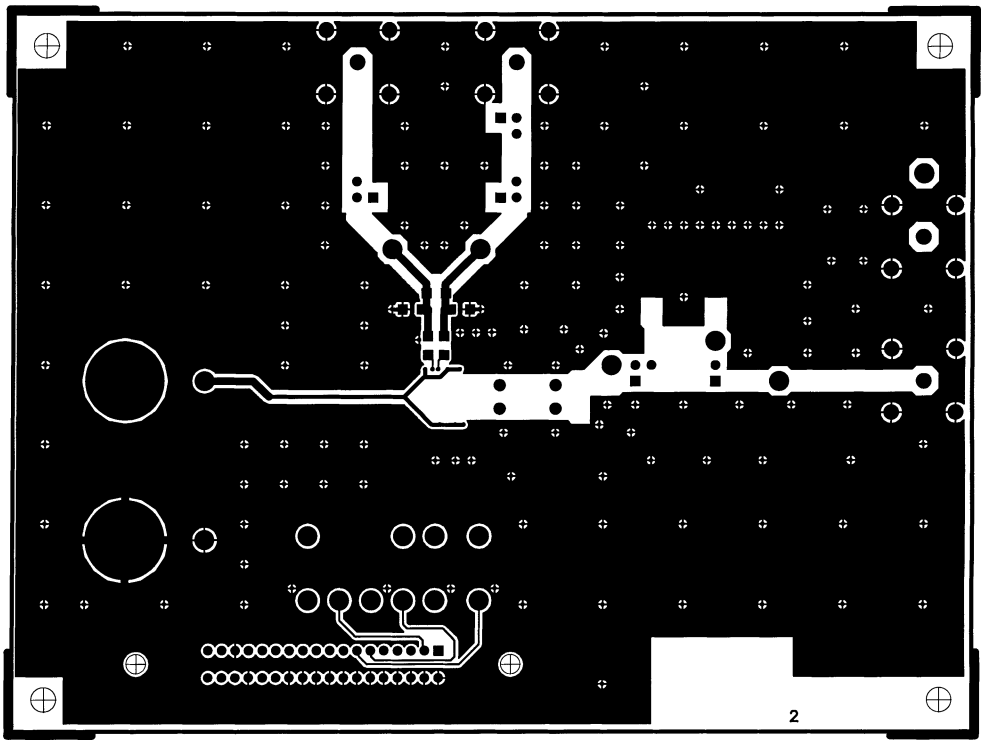


Figure 12. Evaluation Board—Solder Side

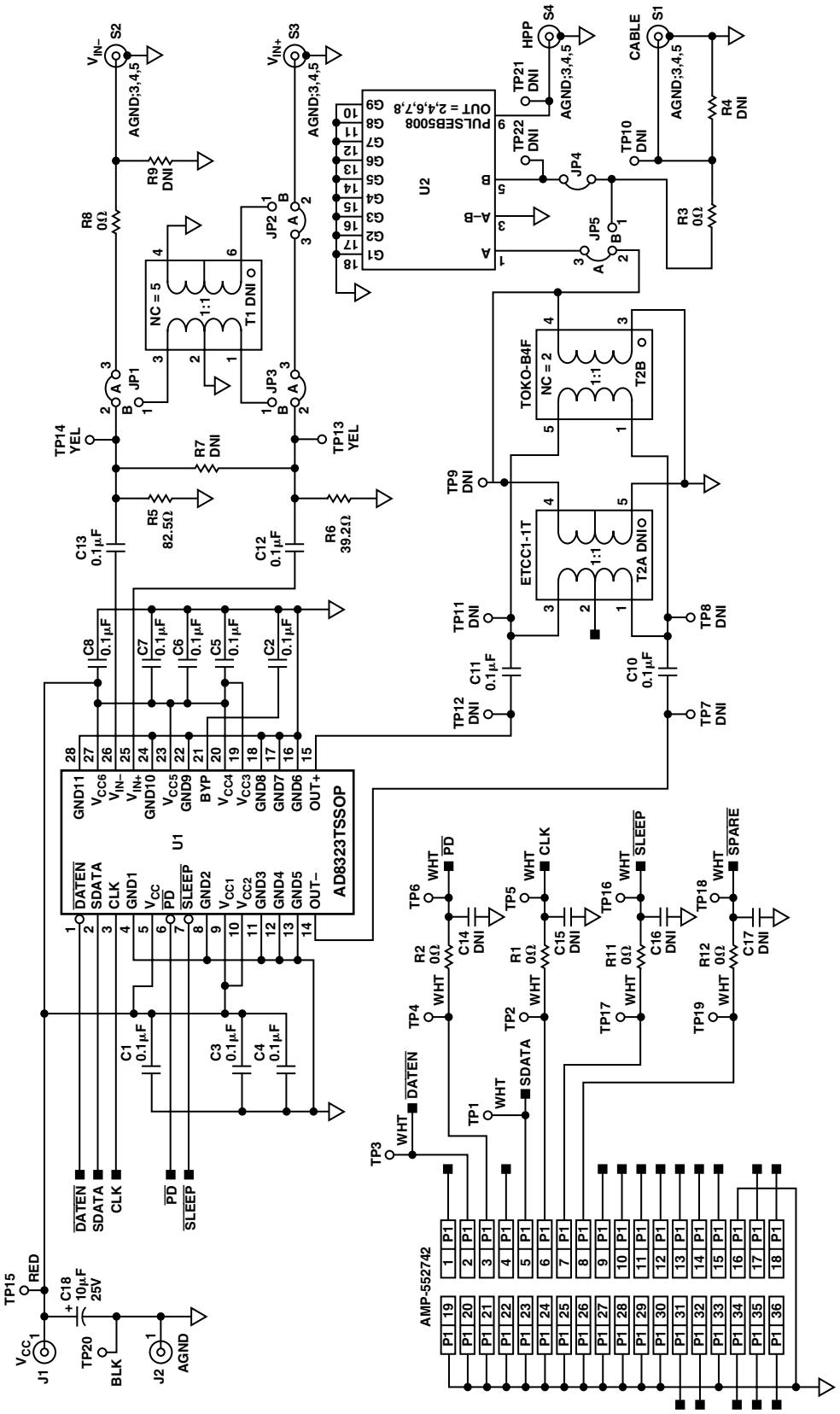


Figure 13. Evaluation Board Schematic

EVALUATION BOARD BILL OF MATERIALS

AD8323 Evaluation Board Rev. C SINGLE-ENDED INVERTING INPUT – Revised – June 22, 2000

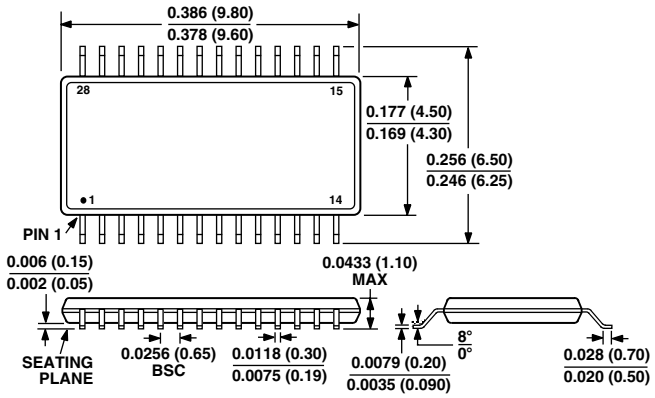
Qty.	Description	Vendor	Ref Desc.
1	10 µF 16 V. 'C' size tantalum chip capacitor	ADS# 4-7-6	C18
12	0.1 µF 50 V. 1206 size ceramic chip capacitor	ADS# 4-5-18	C1–8, 10–13
6	0 Ω 1/8 W. 1206 size chip resistor	ADS# 3-18- 88	R1–3, 8, 11, 12
1	39.2 Ω 1% 1/8 W. 1206 size chip resistor	ADS# 3-18-113	R6
1	82.5 Ω 1% 1/8 W. 1206 size chip resistor	ADS# 3-18-189	R5
2	Yellow Test Point [INPUTS] (Bisco TP104-01-04)	ADS# 12-18-32	TP13, 14
10	White Test Point [DATA] (Bisco TP104-01-09)	ADS# 12-18-42	TP1–6, 16–19
1	Red Test Point [V_{CC}] (Bisco TP104-01-02)	ADS# 12-18-43	TP15
1	Black Test Point [A.GND] (Bisco TP104-01-00)	ADS# 12-18-44	TP20
3	0 Ω 0805 size chip resistors	ADS# 3-27-22	JP1–3
4	75 Ω right-angle BNC Telegartner # J01003A1949	ADS# 12-6-28	VIN+, VIN–, HPP, CABLE
1	Centronics type 36 pin Right-Angle Connector	ADS# 12-3-50	P1
2	5-way Metal Binding Post (E F Johnson # 111-2223-001)	ADS# 12-7-7	VCC, GND
1	1:1 Transformer TOKO # 617DB - A0070	TOKO	T2 B
1	Diplexer PULSE*	PULSE	U2
1	AD8323 (TSSOP) UPSTREAM Cable Driver	ADI# AD8323XRU	U1
1	AD8323 REV. C Evaluation PC board	D C S	Evaluation PC Board
4	#4 - 40 × 1/4 inch STAINLESS panhead machine screw	ADS# 30-1-1	
4	#4 - 40 × 3/4 inch long aluminum round stand-off	ADS# 30-16-3	
2	# 2 - 56 × 3/8 inch STAINLESS panhead machine screw	ADS# 30-1-17	(p1 hardware)
2	# 2 steel flat washer	ADS# 30-6-6	(p1 hardware)
2	# 2 steel internal tooth lockwasher	ADS# 30-5-2	(p1 hardware)
3	# 2 STAINLESS STEEL hex. machine nut	ADS# 30-7-6	(p1 hardware)

DO NOT INSTALL C14–C17, R4, R7, R9, T1, T2A, TP7–TP12, TP21, TP22.
*PULSE Diplexer part #'s B5008 (42 MHz), CX6002 (42 MHz), B5009 (65 MHz).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)



C02045–2.5–7/00 (Rev. 0)

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