16-Bit, 25 MSPS/65 MSPS/80 MSPS/105 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC)

Data Sheet **AD9650**

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS output supply
- SNR
  - 82 dBFS at 30 MHz input and 105 MSPS data rate
  - 83 dBFS at 9.7 MHz input and 25 MSPS data rate
- SFDR
  - 90 dBc at 30 MHz input and 105 MSPS data rate
  - 95 dBc at 9.7 MHz input and 25 MSPS data rate
- Low power
  - 328 mW per channel at 105 MSPS
  - 119 mW per channel at 25 MSPS
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 300 MHz
- Analog input range of 2.7 V p-p
- Optional on-chip dither
- Integrated ADC sample-and-hold inputs
- Differential analog inputs with 500 MHz bandwidth
- ADC clock duty cycle stabilizer

APPLICATIONS

- Industrial instrumentation
- X-Ray, MRI, and ultrasound equipment
- High speed pulse acquisition
- Chemical and spectrum analysis
- Direct conversion receivers
- Multimode digital receivers
- Smart antenna systems
- General-purpose software radios

GENERAL DESCRIPTION

The AD9650 is a dual, 16-bit, 25 MSPS/65 MSPS/80 MSPS/105 MSPS analog-to-digital converter (ADC) designed for digitizing high frequency, wide dynamic range signals with input frequencies of up to 300 MHz.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers, and shared integrated voltage reference, which eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data can be routed directly to the two external 16-bit output ports or multiplexed on a single 16-bit bus. These outputs can be set to either 1.8 V CMOS or LVDS.

FUNCTIONAL BLOCK DIAGRAM

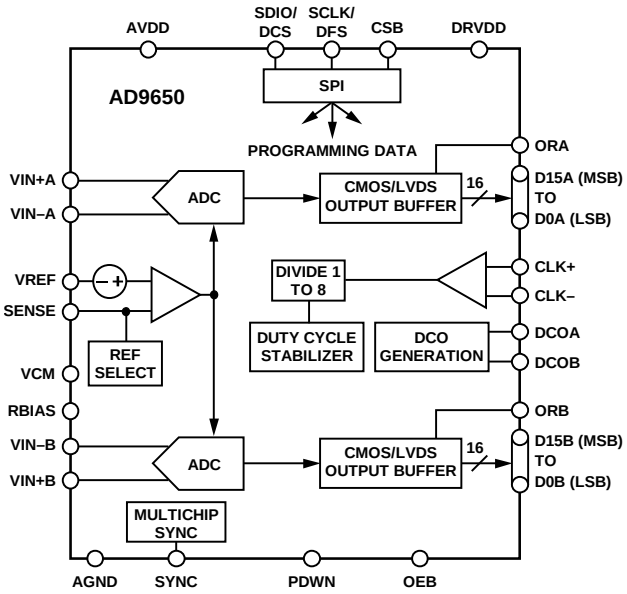


Figure 1.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9650 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. On-chip dither option for improved SFDR performance with low power analog input.
2. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.
3. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs.
4. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, and test modes.
5. Pin compatible with the AD9268 and other dual families, AD9269, AD9251, AD9231, and AD9204. This allows a simple migration across resolutions and bandwidth.

Rev. B
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REVISION HISTORY

12/14—Rev. A to Rev. B

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11/11—Rev. 0 to Rev. A

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7/10—Revision 0: Initial Version

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 1.

		AD9650BCPZ-25			AD9650BCPZ-65			AD9650BCPZ-80			AD9650BCPZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full		16			16			16			16		Bits
ACCURACY														
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.2	±0.5		±0.2	±0.5		±0.4	±0.70		±0.4	±0.7	% FSR
Gain Error	Full		±0.4	±2.5		±0.4	±2.5		±0.4	±2.5		±0.4	±2.5	% FSR
Differential Nonlinearity (DNL)[1]	Full	−1		+1.3	−1		+1.3	−1		+1.3	−1		+1.3	LSB
	25°C		±0.7			±0.7			±0.7			±0.7		LSB
Integral Nonlinearity (INL)[1]	Full			±3			±5			±6			±6	LSB
	25°C		±1.6			±2.5			±2.5			±3		LSB
MATCHING CHARACTERISTIC														
Offset Error	Full		±0.1	±0.4		±0.1	±0.4		±0.1	±0.4		±0.1	±0.4	% FSR
Gain Error	Full		±0.5	±1.3		±0.5	±1.3		±0.5	±1.3		±0.5	±1.3	% FSR
TEMPERATURE DRIFT														
Offset Error	Full		±2			±2			±2			±2		ppm/°C
Gain Error	Full		±15			±15			±15			±15		ppm/°C
INTERNAL VOLTAGE REFERENCE														
Output Voltage Error (1.35 V Mode)	Full		±7	±14		±7	±14		±7	±14		±7	±14	mV
Load Regulation at 1.0 mA	Full		10			10			10			10		mV
INPUT REFERRED NOISE														
VREF = 1.35 V	25°C		1.5			1.5			1.5			1.5		LSB rms
ANALOG INPUT														
Input Span, VREF = 1.35 V	Full		2.7			2.7			2.7			2.7		V p-p
Input Capacitance[2]	Full		11			11			11			11		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9			0.9		V
REFERENCE INPUT RESISTANCE	Full		6			6			6			6		kΩ
POWER SUPPLIES														
Supply Voltage														
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current														
IAVDD[1]	Full		125	131		202	209		267	275		332	340	mA
IDRVDD[1] (1.8 V CMOS)	Full		8			23			29			36		mA
IDRVDD[1] (1.8 V LVDS)	Full		72			86			90			100		mA
POWER CONSUMPTION														
DC Input	Full		237	254		397	408		522	537		656	675	mW
Sine Wave Input[1] (DRVDD = 1.8 V CMOS Output Mode)	Full		240			405			533			663		mW
Sine Wave Input[1] (DRVDD = 1.8 V LVDS Output Mode)	Full		355			520			642			778		mW
Standby Power[3]	Full		50			50			50			50		mW
Power-Down Power	Full		0.25	2.5		0.25	2.5		0.25	2.5		0.25	2.5	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK+ and CLK− pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, DCS disabled, unless otherwise noted.

Table 2.

		AD9650BCPZ-25			AD9650BCPZ-65			AD9650BCPZ-80			AD9650BCPZ-105			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)														
f_{IN} = 9.7 MHz	25°C		83			83			83			82.5		dBFS
f_{IN} = 30 MHz	25°C		81.5			82			82			82		dBFS
	Full	81.8			81.5			81.6			80.5			dBFS
f_{IN} = 70 MHz	25°C		79.5			81			81			80		dBFS
f_{IN} = 141 MHz[2]	25°C					79.5			80			80		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)														
f_{IN} = 9.7 MHz	25°C		82.2			82			82			82		dBFS
f_{IN} = 30 MHz	25°C		80			81.2			82			80.4		dBFS
	Full	81.5			81			80.7			80			dBFS
f_{IN} = 70 MHz	25°C		78			79.2			78.5			78.8		dBFS
f_{IN} = 141 MHz[2]	25°C					75			75.1			75.5		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)														
f_{IN} = 9.7 MHz	25°C		13.5			13.5			13.5			13.3		Bits
f_{IN} = 30 MHz	25°C		13.0			13.2			13.2			13.2		Bits
f_{IN} = 70 MHz	25°C		12.7			13.0			13.0			13.0		Bits
f_{IN} = 141 MHz[2]	25°C					12.9			13.0			12.3		Bits
WORST SECOND OR THIRD HARMONIC														
f_{IN} =9.7 MHz	25°C		−95			−94			−95.5			−91		dBc
f_{IN} = 30 MHz	25°C		−85			−93			−92			−90		dBc
	Full			−91.5			−88			−87			−87	dBc
f_{IN} = 70 MHz	25°C		−87			−86			−86			−92		dBc
f_{IN} = 141 MHz	25°C					−79			−79			−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)														
f_{IN} = 9.7 MHz	25°C		95			94			95.5			91		dBc
f_{IN} = 30 MHz	25°C		85			93			92			90		dBc
	Full	91.5			88			87			87			dBc
f_{IN} = 70 MHz	25°C		87			86			86			92		dBc
f_{IN} = 141 MHz	25°C					79			79			80		dBc
WORST OTHER (HARMONIC OR SPUR)														
f_{IN} = 9.7 MHz	25°C		−110			−105			−105			−100		dBc
f_{IN} = 30 MHz	25°C		−102			−105			−105			−101		dBc
	Full			−97			−97			−97			−94	dBc
f_{IN} = 70 MHz	25°C		−97			−97			−97			−97		dBc
f_{IN} = 141 MHz	25°C					−97			−97			−88		dBc
TWO-TONE SFDR														
f_{IN} = 7.2 MHz (−7 dBFS), 8.4 MHz (−7 dBFS)	25°C		87											
f_{IN} = 25 MHz (−7 dBFS), 30 MHz (−7 dBFS)	25°C		84			90			87			87		dBc
f_{IN} = 125 MHz (−7 dBFS), 128 MHz (−7 dBFS)	25°C					83			83			84		dBc
CROSSTALK[3]	Full		−105			−105			−105			−105		dBFS
ANALOG INPUT BANDWIDTH	25°C		500			500			500			500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Measurements made with a divide-by-4 clock rate to minimize the effects of clock jitter on the SNR performance.
[3] Crosstalk is measured with a 170 MHz tone at −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		9		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (V_{IN} = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	290	345	400	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, V_{IN} = −1.0 dBFS differential input, 1.35 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

		AD9650BCPZ-25			AD9650BCPZ-65			AD9650BCPZ-80			AD9650BCPZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS														
Input Clock Rate	Full			200			520			640			640	MHz
Conversion Rate[1]														
DCS Enabled	Full	20		25	20		65	20		80	20		105	MSPS
DCS Disabled	Full	10		25	10		65	10		80	10		105	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	40			15.4			12.5			9.5			ns
CLK Pulse Width High (t_{CH})														
Divide-by-1 Mode, DCS Enabled	Full	12	20	28	4.65	7.70	10.75	3.75	6.25	8.75	2.85	4.75	6.65	ns
Divide-by-1 Mode, DCS Disabled	Full	19	20	21	7.33	7.70	8.07	5.95	6.25	6.55	4.5	4.75	5.0	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			0.8			0.8			ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.100			0.090			0.080			0.075		ps rms
DATA OUTPUT PARAMETERS														
CMOS Mode														
Data Propagation Delay (t_{PD})	Full	2.8	3.5	4.2	2.8	3.5	4.2	2.8	3.5	4.2	2.8	3.5	4.2	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.1			3.1			3.1			3.1		ns
DCO to Data Skew (t_{SKEW})	Full	−0.6	−0.4	0	−0.6	−0.4	0	−0.6	−0.4	0	−0.6	−0.4	0	ns
LVDS Mode														
Data Propagation Delay (t_{PD})	Full	2.9	3.7	4.5	2.9	3.7	4.5	2.9	3.7	4.5	2.9	3.7	4.5	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.9			3.9			3.9			3.9		ns
DCO to Data Skew (t_{SKEW})	Full	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	−0.1	+0.2	+0.5	ns
CMOS Mode Pipeline Delay (Latency)	Full		12			12			12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/ Channel B	Full		12/12.5			12/12.5			12/12.5			12/12.5		Cycles
Wake-Up Time[3]	Full		500			500			500			500		µs
Out-of-Range Recovery Time	Full		2			2			2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bit 0 through Bit 4 in SPI Register 0x17 (see Table 17).
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.3	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS[1]			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

[1] See Figure 93.

Timing Diagrams

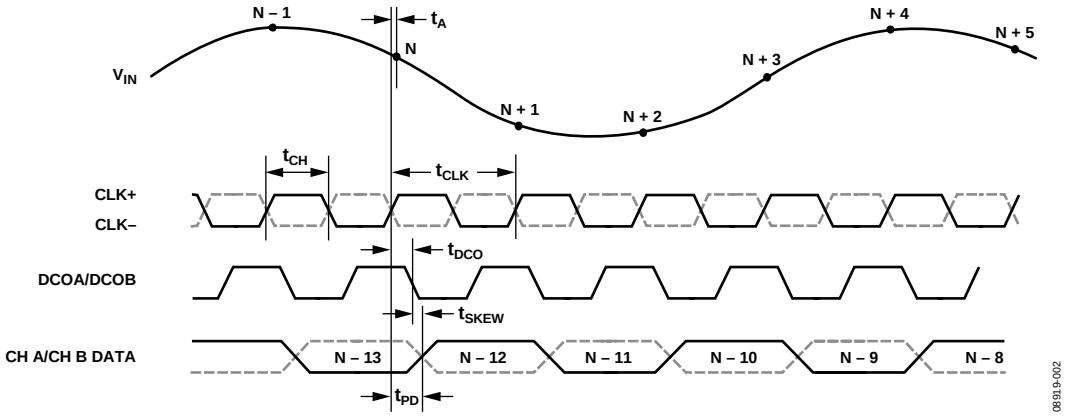


Figure 2. CMOS Default Output Mode Data Output Timing

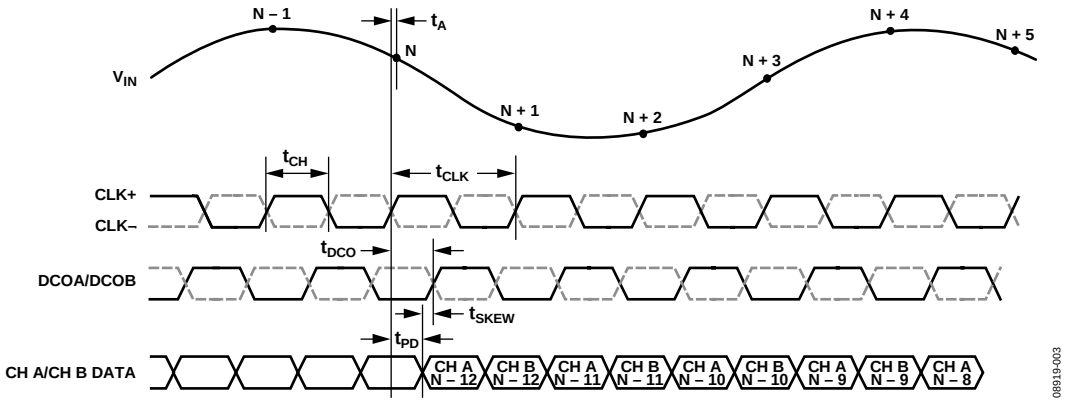


Figure 3. CMOS Interleaved Output Mode Data Output Timing

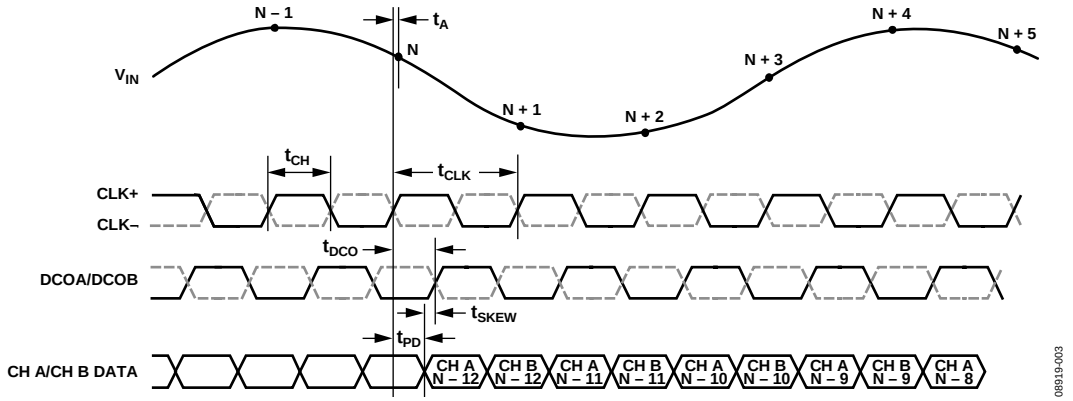


Figure 4. LVDS Mode Data Output Timing

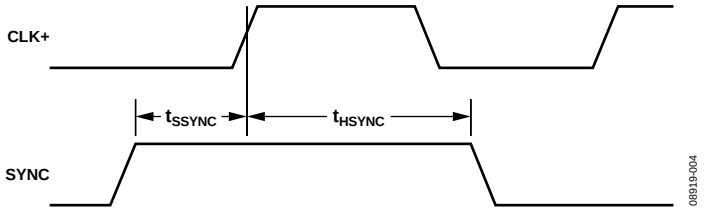


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical[1]	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0A/D0B Through D15A/D15B to AGND	−0.3 V to DRVDD + 0.2 V
DCOA/DCOB to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1] The inputs and outputs are rated to the supply voltage (AVDD or DRVDD) + 0.2 V but should not exceed 2.1 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints and maximizes the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
64-Lead LFCSP (CP-64-6)	0	18.5	1.0		°C/W
	1.0	16.1		9.2	°C/W
	2.5	14.5			°C/W

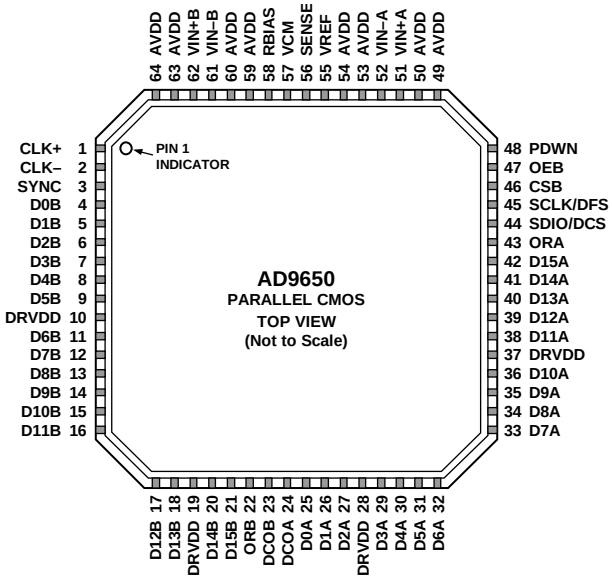
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

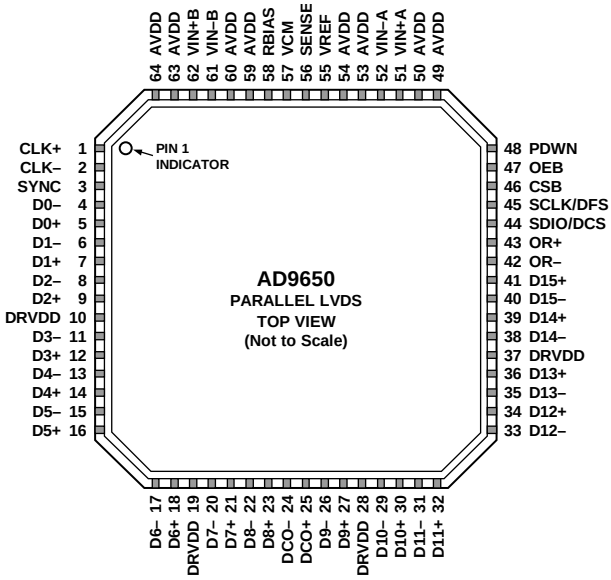
08919-005

Figure 6. LFCSP Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
58	RBIAS	Input/output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
25	D0A	Output	Channel A CMOS Output Data (LSB).
26	D1A	Output	Channel A CMOS Output Data.
27	D2A	Output	Channel A CMOS Output Data.
29	D3A	Output	Channel A CMOS Output Data.
30	D4A	Output	Channel A CMOS Output Data.
31	D5A	Output	Channel A CMOS Output Data.
32	D6A	Output	Channel A CMOS Output Data.

Pin No.	Mnemonic	Type	Description
33	D7A	Output	Channel A CMOS Output Data.
34	D8A	Output	Channel A CMOS Output Data.
35	D9A	Output	Channel A CMOS Output Data.
36	D10A	Output	Channel A CMOS Output Data.
38	D11A	Output	Channel A CMOS Output Data.
39	D12A	Output	Channel A CMOS Output Data.
40	D13A	Output	Channel A CMOS Output Data.
41	D14A	Output	Channel A CMOS Output Data.
42	D15A	Output	Channel A CMOS Output Data (MSB).
43	ORA	Output	Channel A Overrange Output.
4	D0B	Output	Channel B CMOS Output Data (LSB).
5	D1B	Output	Channel B CMOS Output Data.
6	D2B	Output	Channel B CMOS Output Data.
7	D3B	Output	Channel B CMOS Output Data.
8	D4B	Output	Channel B CMOS Output Data.
9	D5B	Output	Channel B CMOS Output Data.
11	D6B	Output	Channel B CMOS Output Data.
12	D7B	Output	Channel B CMOS Output Data.
13	D8B	Output	Channel B CMOS Output Data.
14	D9B	Output	Channel B CMOS Output Data.
15	D10B	Output	Channel B CMOS Output Data.
16	D11B	Output	Channel B CMOS Output Data.
17	D12B	Output	Channel B CMOS Output Data.
18	D13B	Output	Channel B CMOS Output Data.
20	D14B	Output	Channel B CMOS Output Data.
21	D15B	Output	Channel B CMOS Output Data (MSB).
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES
1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

08919-006

Figure 7. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
58	RBIAS	Input/output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
5	D0+	Output	Channel A/Channel B LVDS Output Data 0—True (LSB).
4	D0−	Output	Channel A/Channel B LVDS Output Data 0—Complement (LSB).
7	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
6	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
9	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
8	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
12	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.

Pin No.	Mnemonic	Type	Description
11	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
14	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
13	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
16	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
15	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
18	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
17	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
21	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
20	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
23	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
22	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
27	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
26	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
30	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
29	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
32	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
31	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
34	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
33	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
36	D13+	Output	Channel A/Channel B LVDS Output Data 13—True.
35	D13−	Output	Channel A/Channel B LVDS Output Data 13—Complement.
39	D14+	Output	Channel A/Channel B LVDS Output Data 14—True.
38	D14−	Output	Channel A/Channel B LVDS Output Data 14—Complement.
41	D15+	Output	Channel A/Channel B LVDS Output Data 15—True (MSB).
40	D15−	Output	Channel A/Channel B LVDS Output Data 15—Complement (MSB).
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS disabled, 1.35 V internal reference, 2.7 V p-p differential input, VIN = −1.0 dBFS, and 32k sample, T_A = 25°C, unless otherwise noted.

AD9650-25

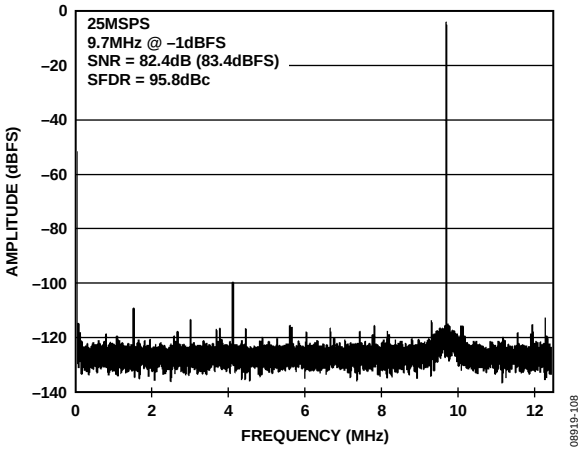


Figure 8. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz

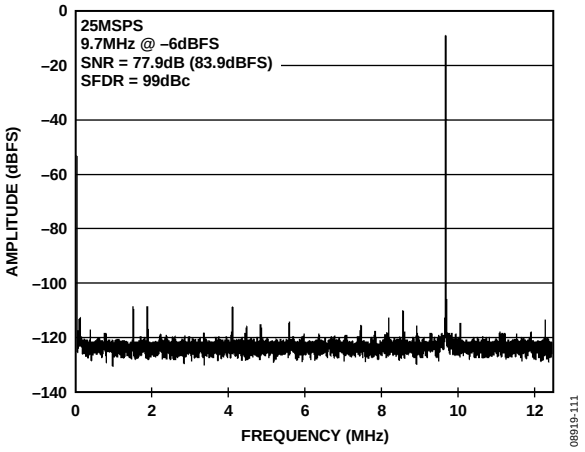


Figure 11. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz at −6 dBFS with Dither Disabled

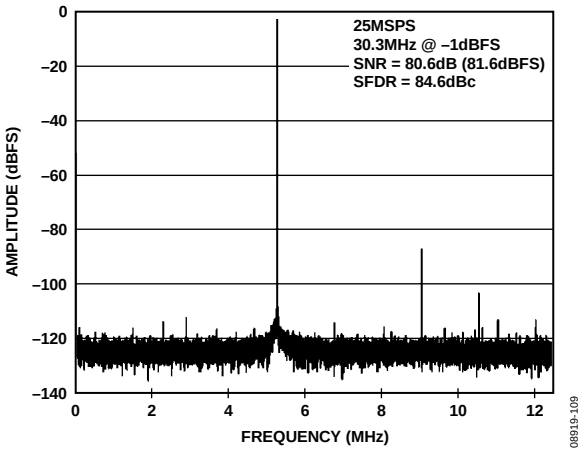


Figure 9. AD9650-25 Single-Tone FFT with f_{IN} = 30.3 MHz

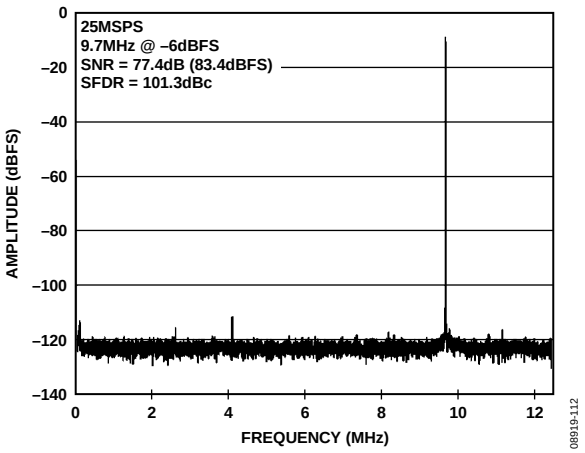


Figure 12. AD9650-25 Single-Tone FFT with f_{IN} = 9.7 MHz at −6 dBFS with Dither Enabled

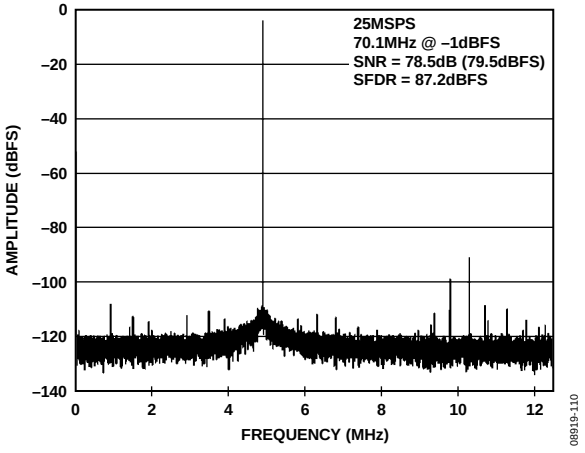


Figure 10. AD9650-25 Single-Tone FFT with f_{IN} = 70.1 MHz

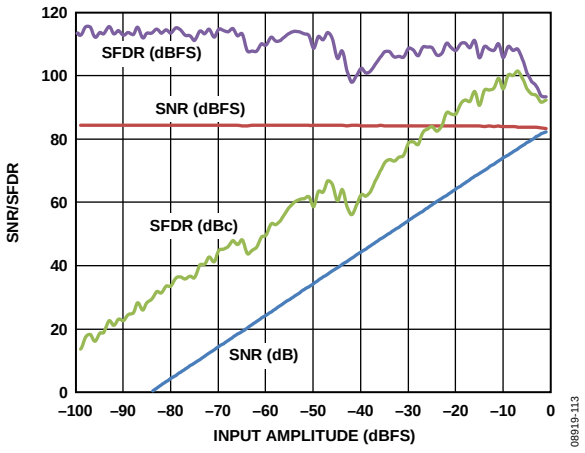


Figure 13. AD9650-25 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 9.7 MHz

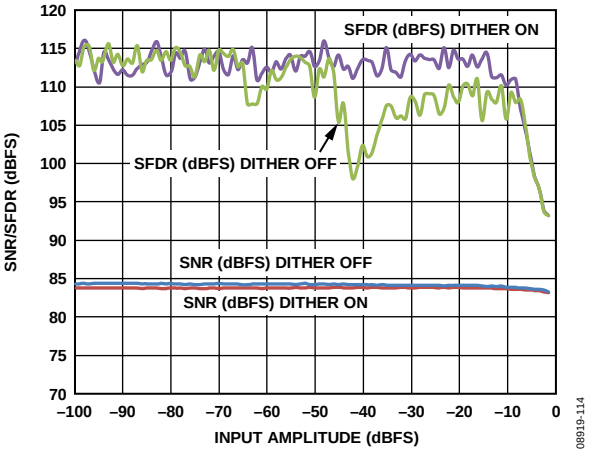


Figure 14. AD9650-25 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 9.7 MHz with and Without Dither Enabled

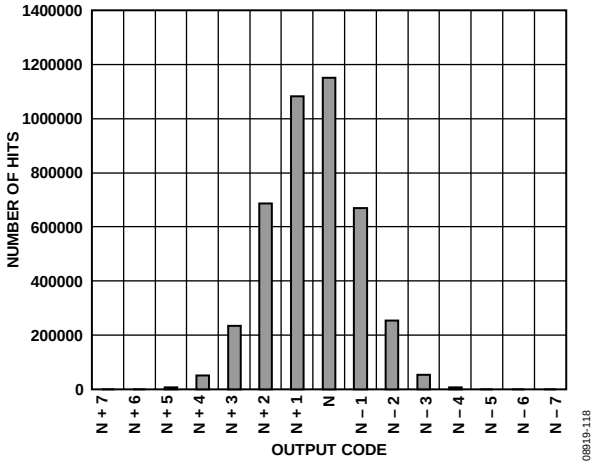


Figure 17. AD9650-25 Grounded Input Histogram

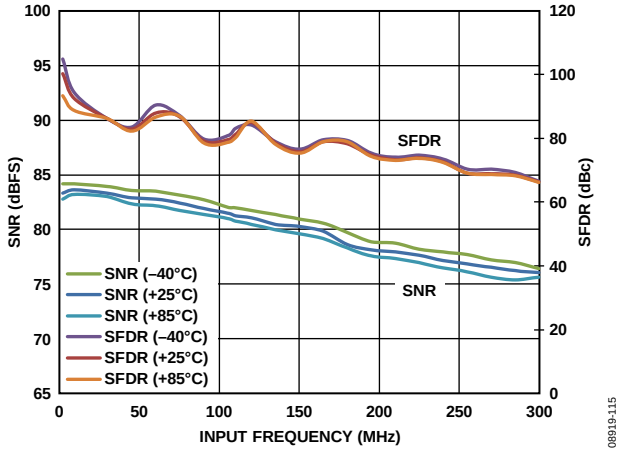


Figure 15. AD9650-25 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 2.7 V p-p Full Scale

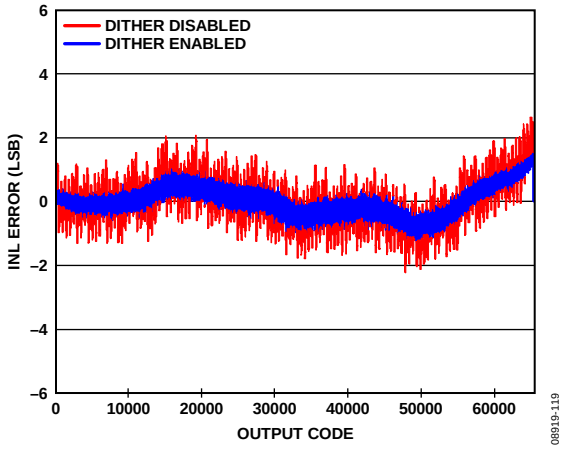


Figure 18. AD9650-25 INL with f_{IN} = 9.7 MHz

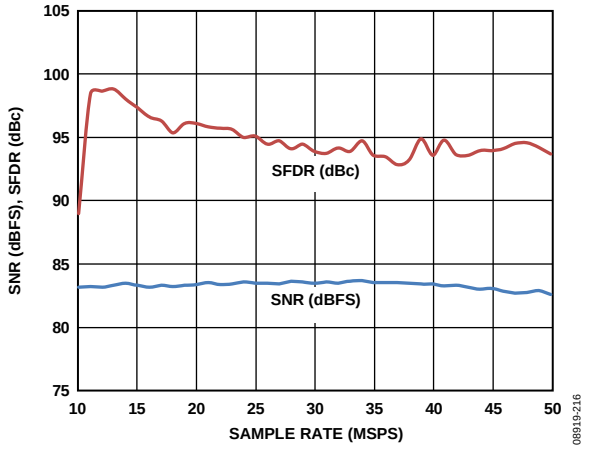


Figure 16. AD9650-25 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 9.7 MHz

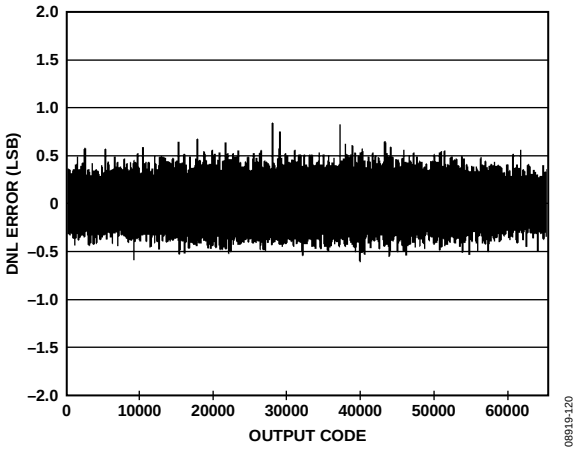


Figure 19. AD9650-25 DNL with f_{IN} = 9.7 MHz

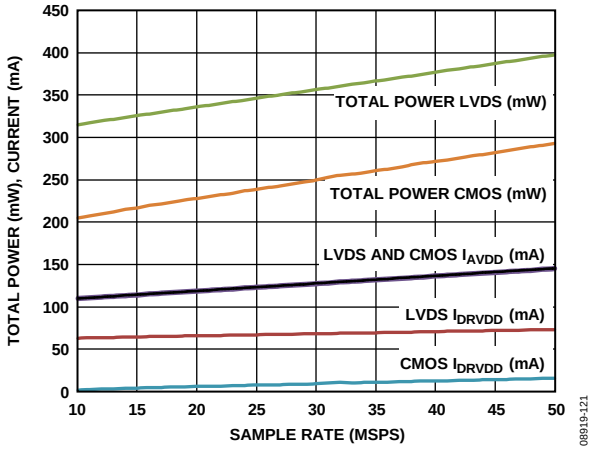


Figure 20. AD9650-25 Power and Current vs. Sample Rate

AD9650-65

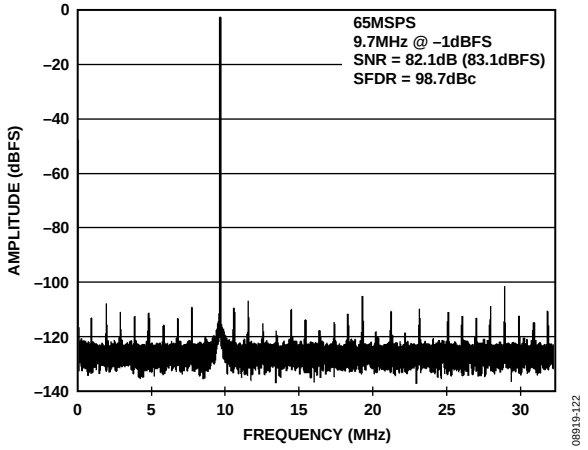


Figure 21. AD9650-65 Single-Tone FFT with f_{IN} = 9.7 MHz

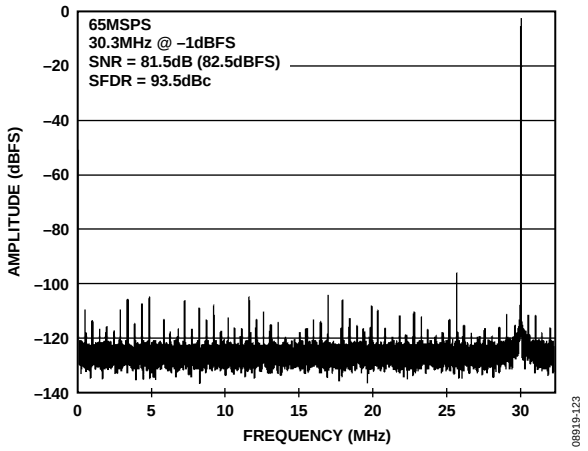


Figure 22. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz

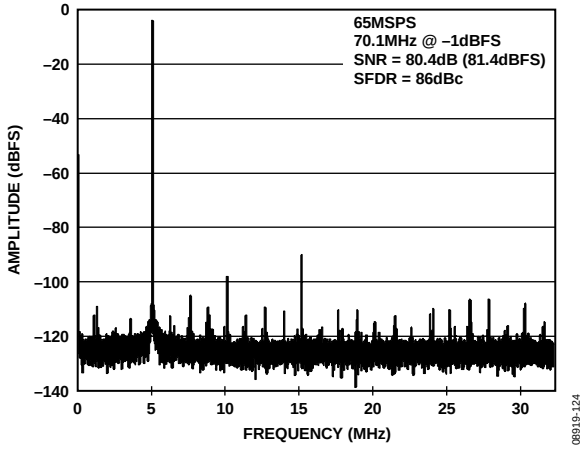


Figure 23. AD9650-65 Single-Tone FFT with f_{IN} = 70.1 MHz

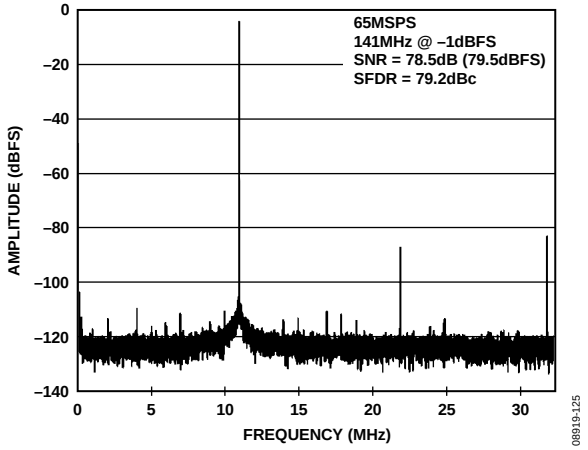


Figure 24. AD9650-65 Single-Tone FFT with f_{IN} = 141 MHz

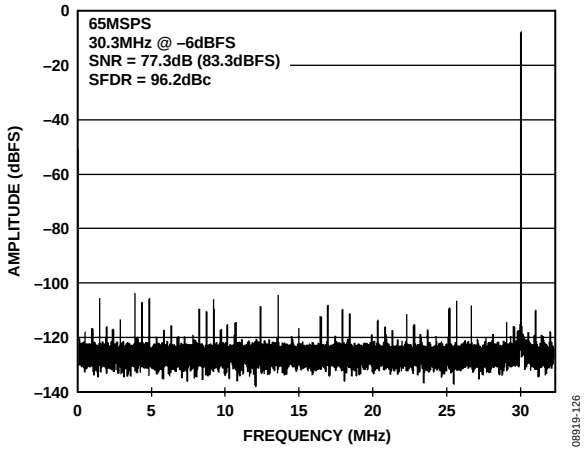


Figure 25. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Disabled

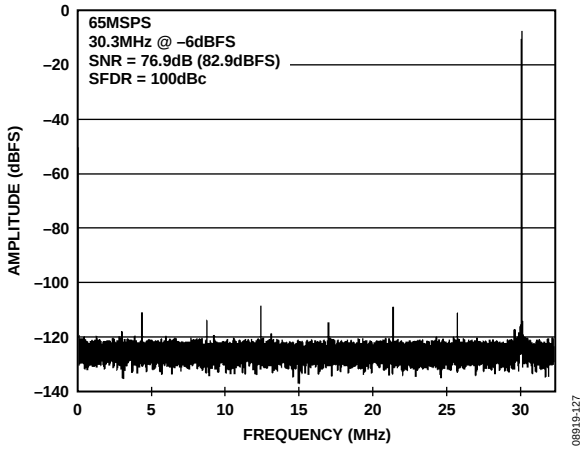


Figure 26. AD9650-65 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Enabled

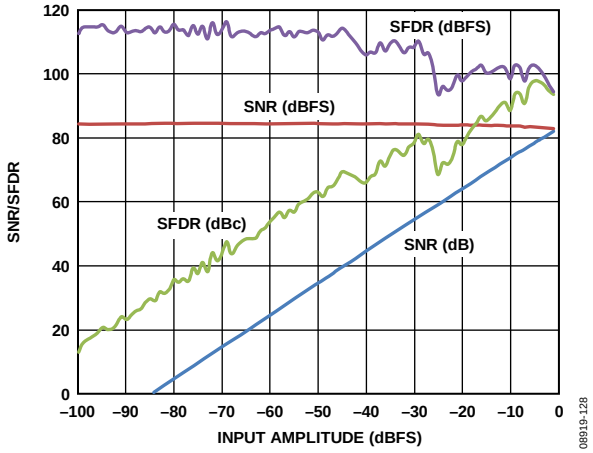


Figure 27. AD9650-65 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} =30.3 MHz

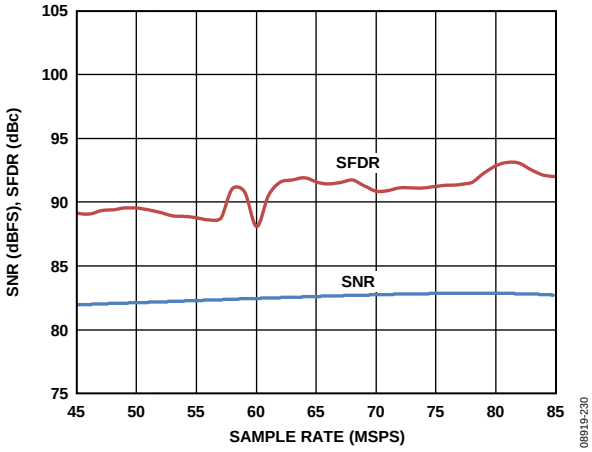


Figure 30. AD9650-65 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 30 MHz

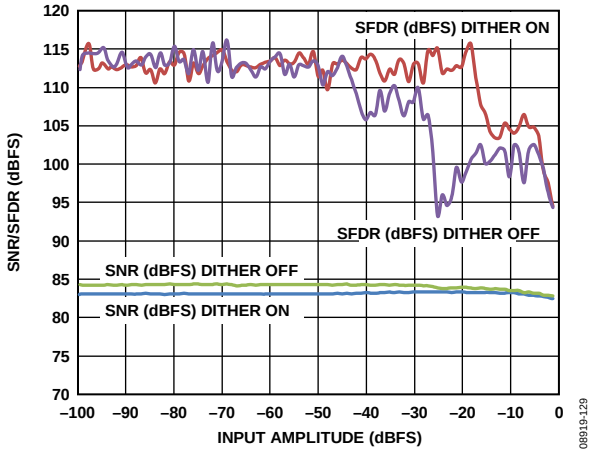


Figure 28. AD9650-65 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz with and Without Dither Enabled

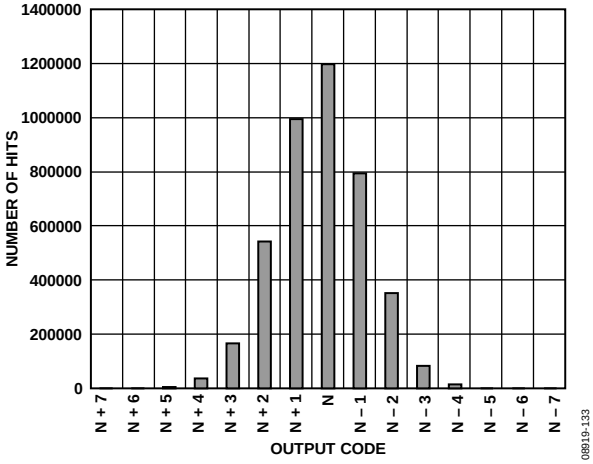


Figure 31. AD9650-65 Grounded Input Histogram

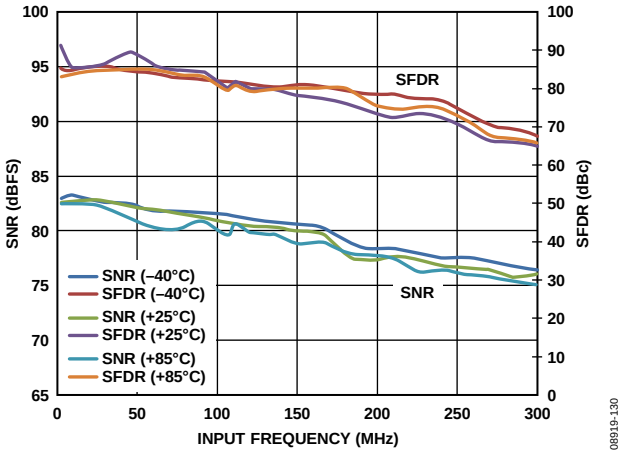


Figure 29. AD9650-65 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 2.7 V p-p Full Scale

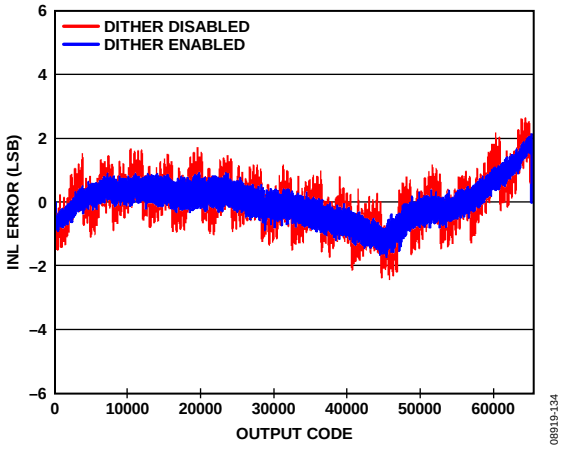


Figure 32. AD9650-65 INL with f_{IN} = 9.7 MHz

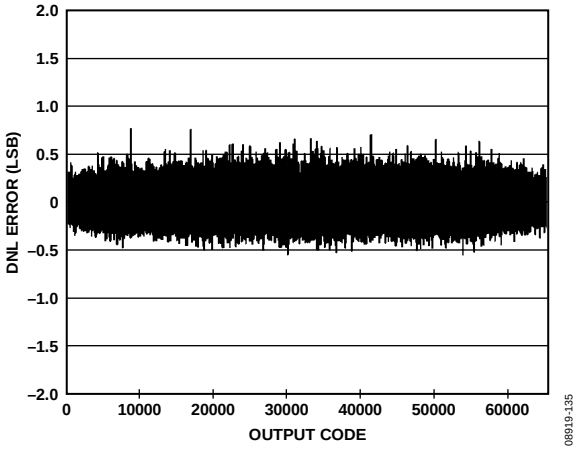


Figure 33. AD9650-65 DNL with f_{IN} = 9.7 MHz

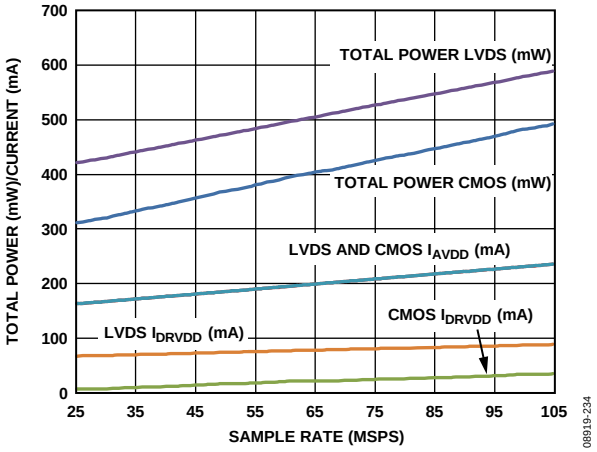


Figure 34. AD9650-65 Power and Current vs. Sample Rate

AD9650-80

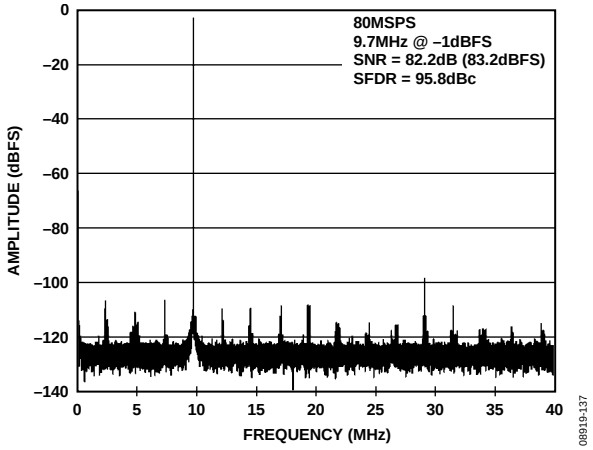


Figure 35. AD9650-80 Single-Tone FFT with f_{IN} = 9.7 MHz

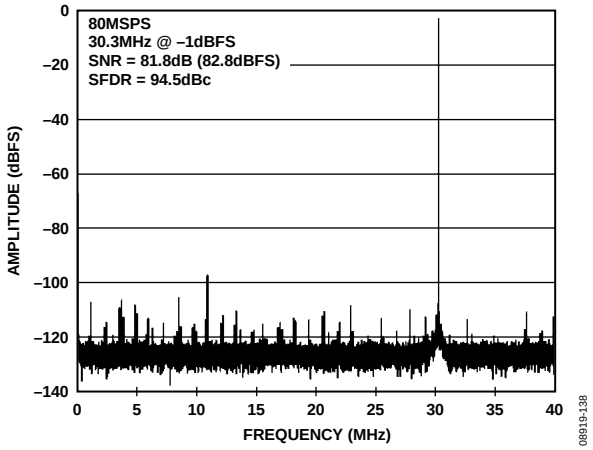


Figure 36. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz

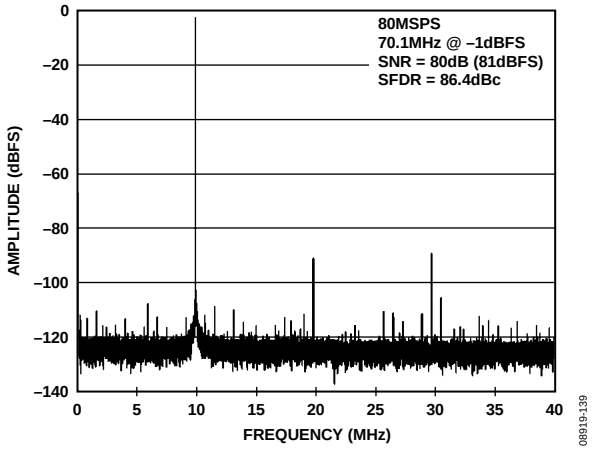


Figure 37. AD9650-80 Single-Tone FFT with f_{IN} = 70.1 MHz

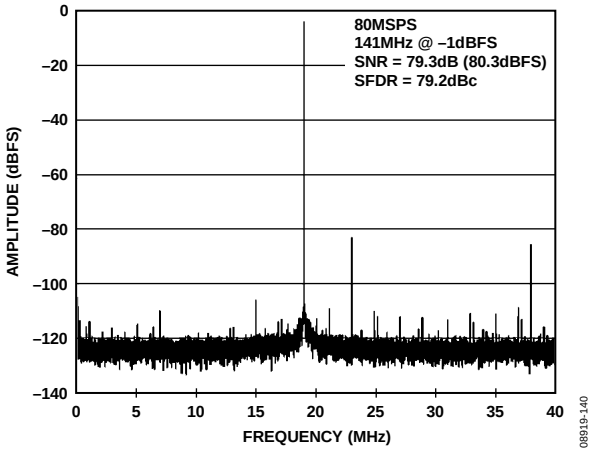


Figure 38. AD9650-80 Single-Tone FFT with f_{IN} = 141 MHz

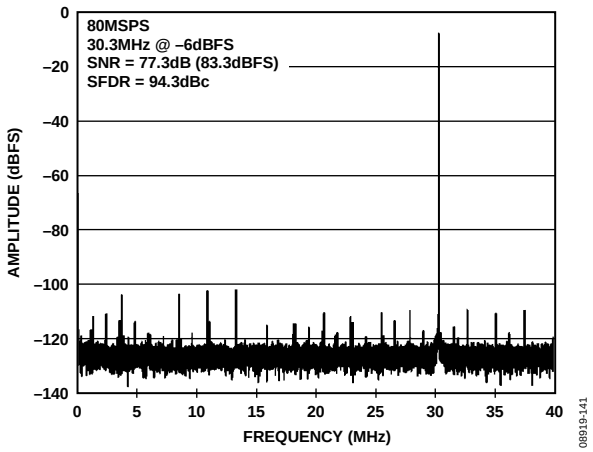


Figure 39. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Disabled

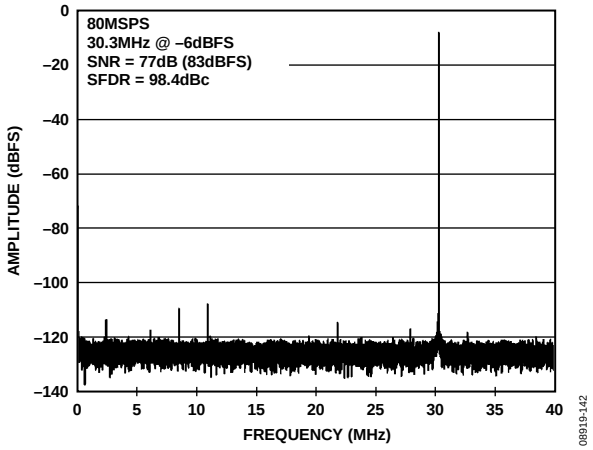


Figure 40. AD9650-80 Single-Tone FFT with f_{IN} = 30.3 MHz at –6 dBFS with Dither Enabled

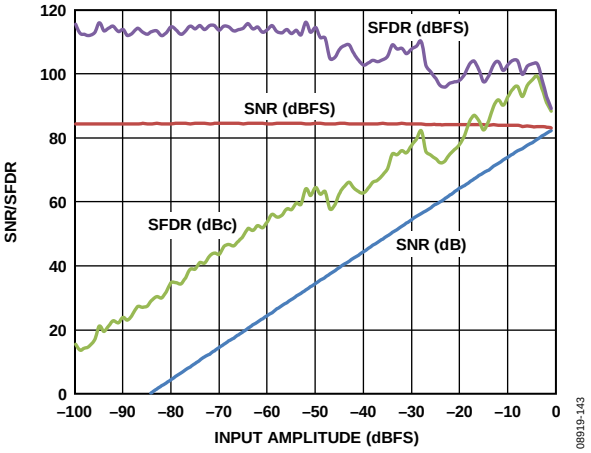


Figure 41. AD9650-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz

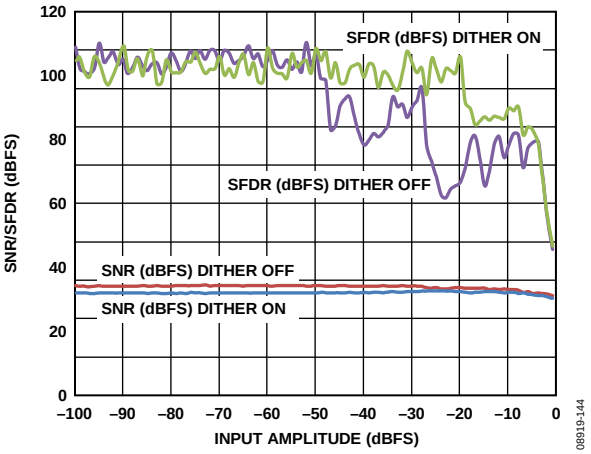


Figure 42. AD9650-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz with and Without Dither Enabled

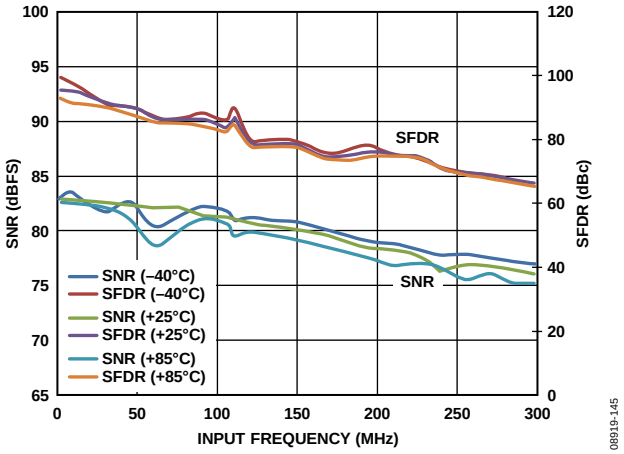


Figure 43. AD9650-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

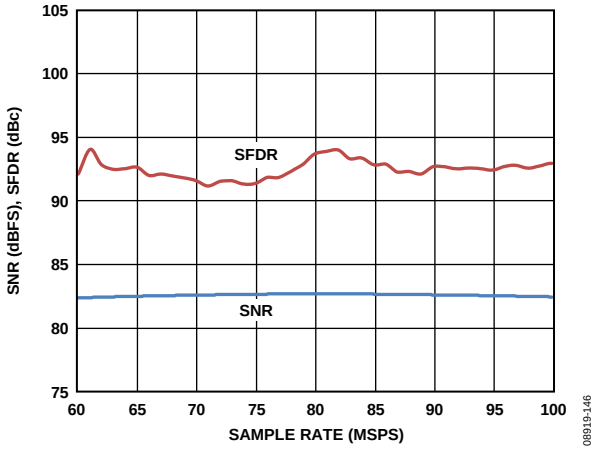


Figure 44. AD9650-80 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 30 MHz

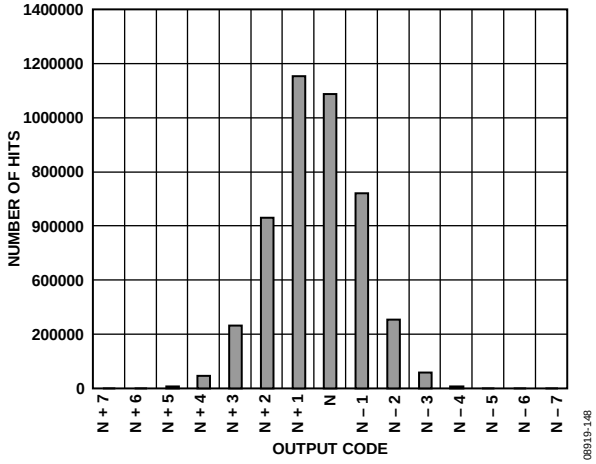


Figure 45. AD9650-80 Grounded Input Histogram

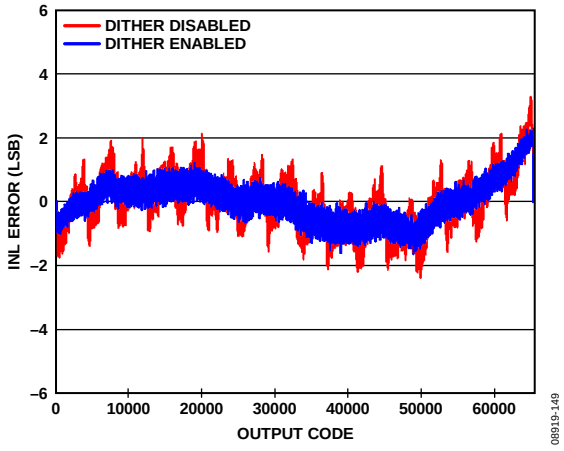


Figure 46. AD9650-80 INL with f_{IN} = 9.7 MHz

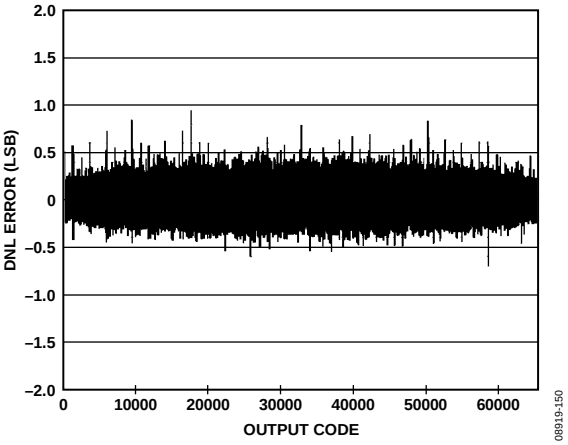


Figure 47. AD9650-80 DNL with f_{IN} = 9.7 MHz

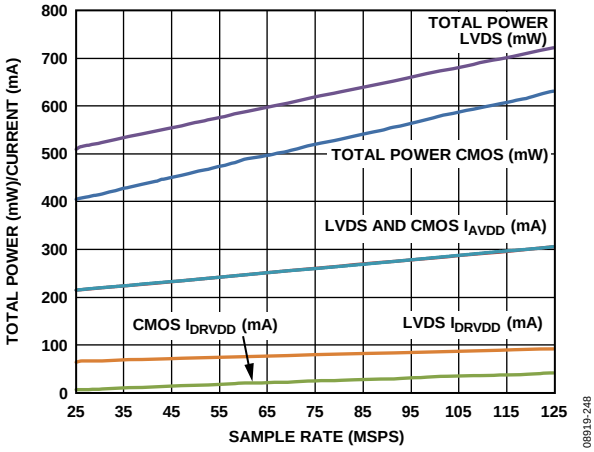


Figure 48. AD9650-80 Power and Current vs. Sample Rate

AD9650-105

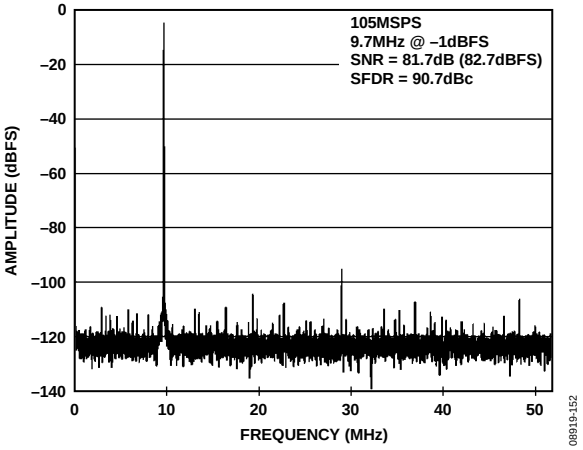


Figure 49. AD9650-105 Single-Tone FFT with f_{IN} = 9.7 MHz

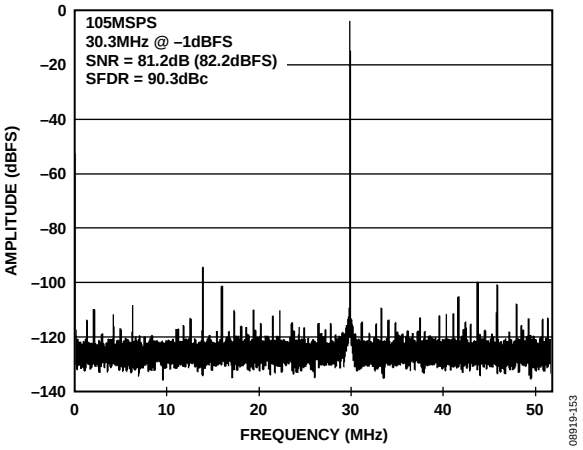


Figure 50. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz

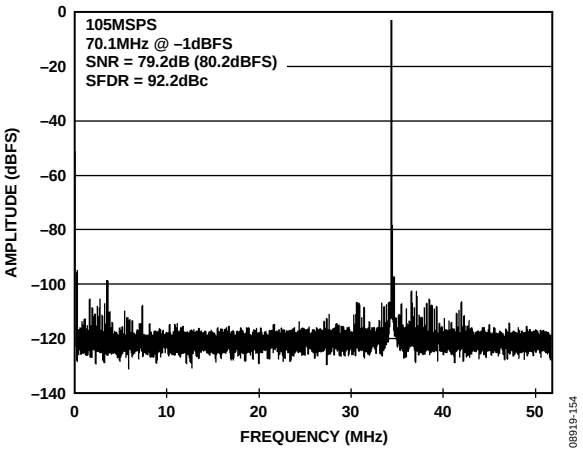


Figure 51. AD9650-105 Single-Tone FFT with f_{IN} = 70.1 MHz

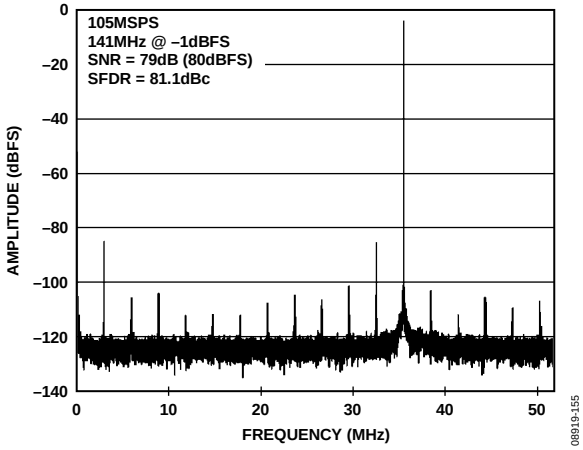


Figure 52. AD9650-105 Single-Tone FFT with f_{IN} = 141 MHz

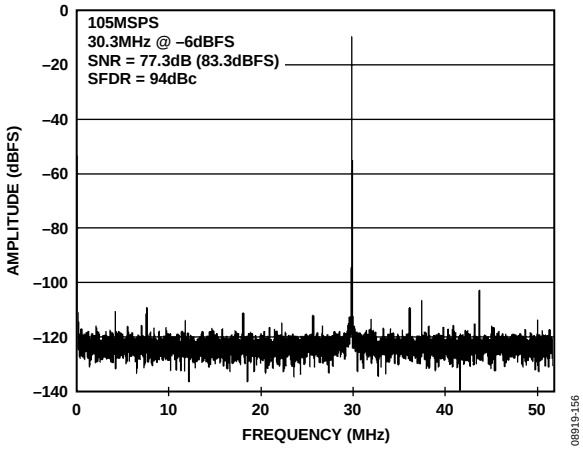


Figure 53. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Disabled

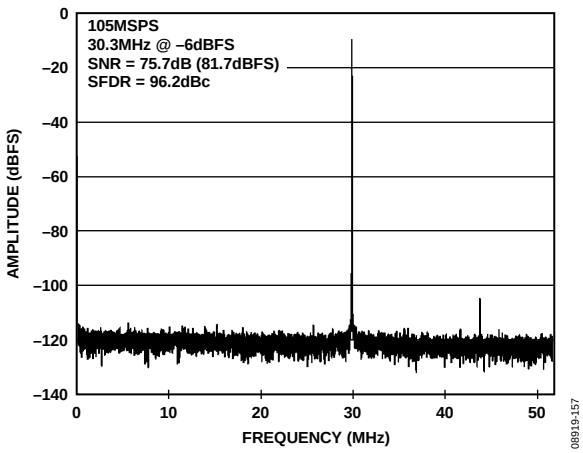


Figure 54. AD9650-105 Single-Tone FFT with f_{IN} = 30.3 MHz @ –6 dBFS with Dither Enabled

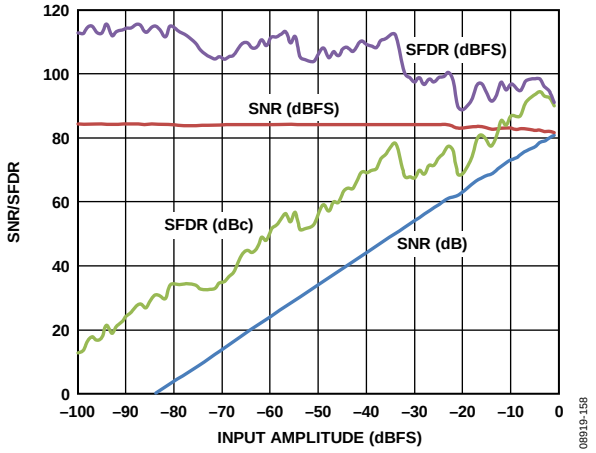


Figure 55. AD9650-105 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz

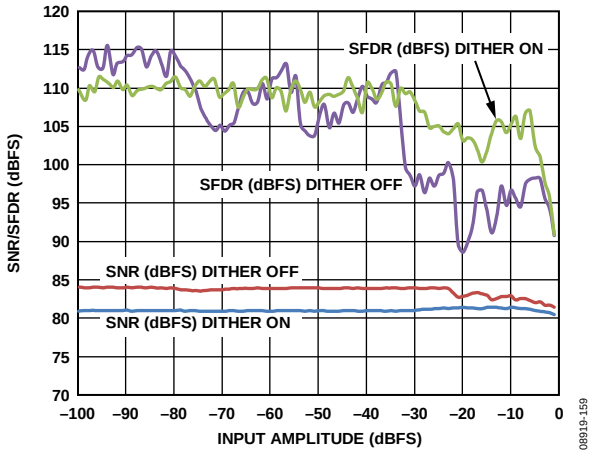


Figure 56. AD9650-105 Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30.3 MHz with and Without Dither Enabled

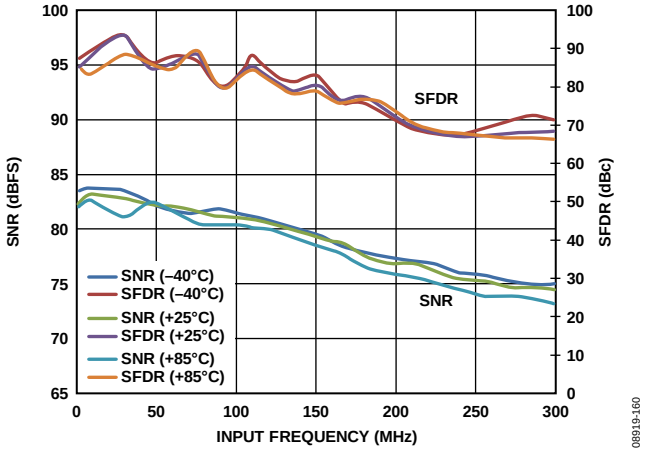


Figure 57. AD9650-105 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

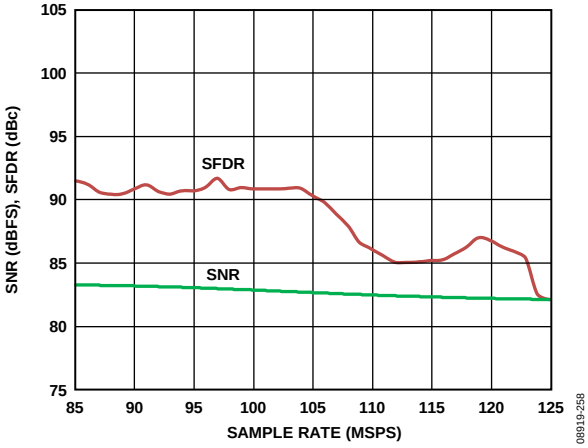


Figure 58. AD9650-105 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 30 MHz

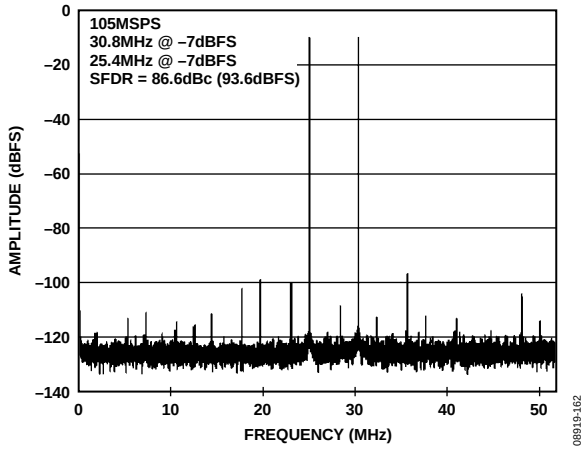


Figure 59. AD9650-105 Two-Tone FFT with f_{IN1} = 25.4 MHz and f_{IN2} = 30.8 MHz

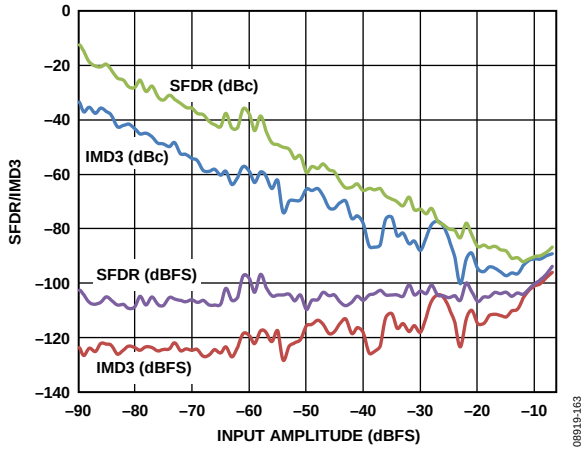


Figure 60. AD9650-105 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 25.4 MHz, f_{IN2} = 30.8 MHz, f_S = 105 MSPS

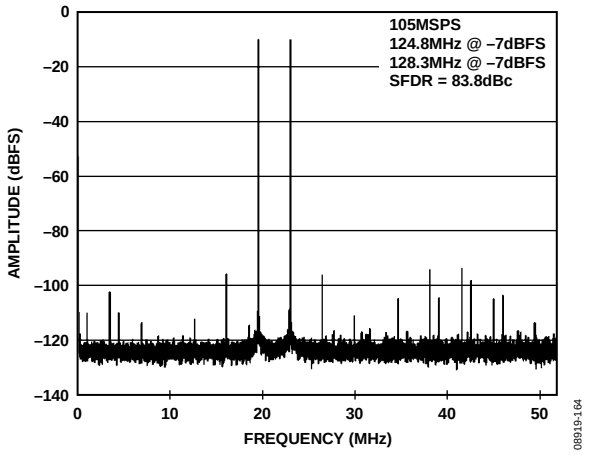


Figure 61. AD9650-105 Two-Tone FFT with f_{IN1} = 124.8 MHz and f_{IN2} = 128.3 MHz

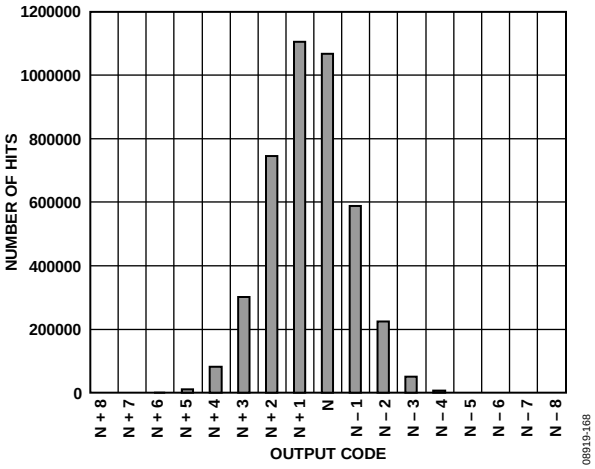


Figure 64. AD9650-105 Grounded Input Histogram

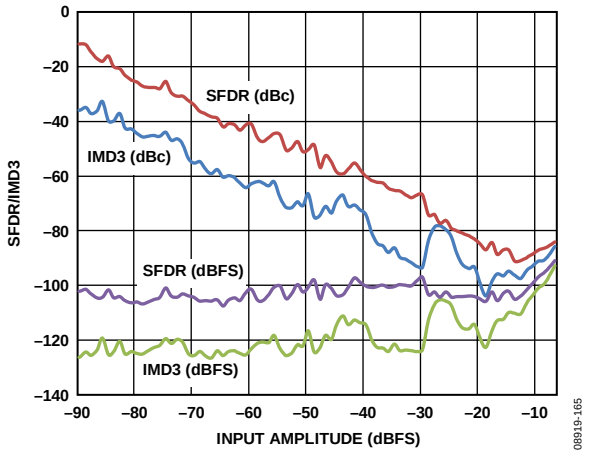


Figure 62. AD9650-105 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 128.3 MHz, f_{IN2} = 124.8 MHz, f_s = 105 MSPS

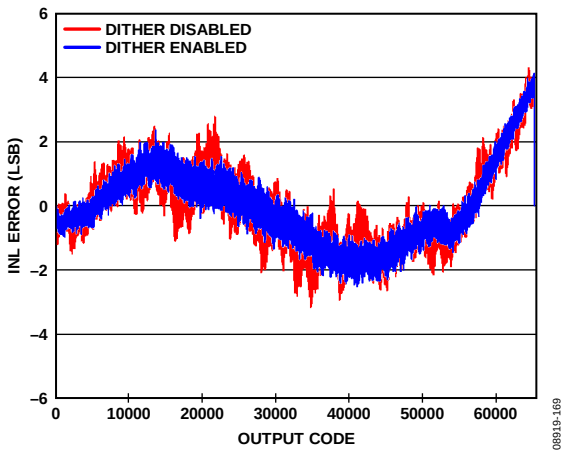


Figure 65. AD9650-105 INL with f_{IN} = 9.7 MHz

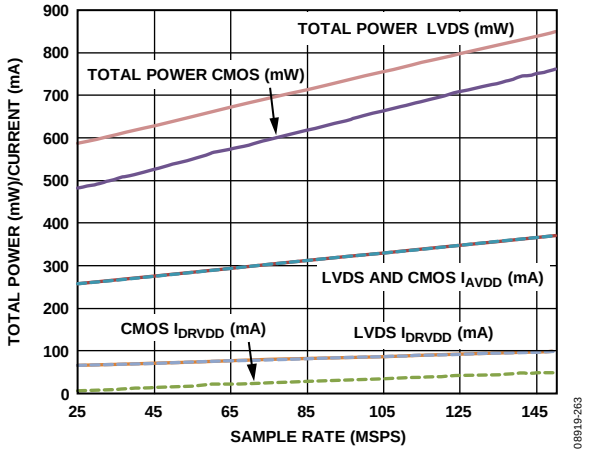


Figure 63. AD9650-105 Power and Current vs. Sample Rate

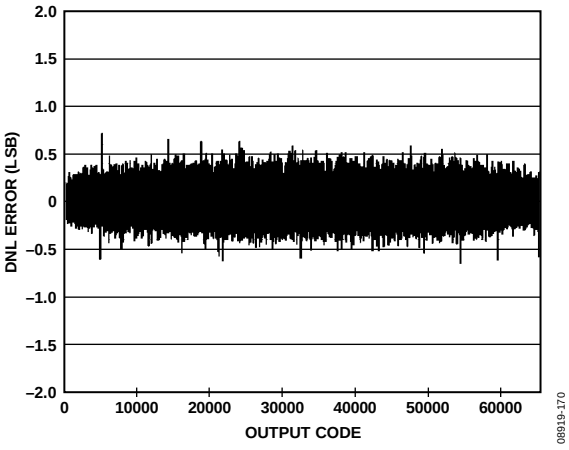


Figure 66. AD9650-105 DNL with f_{IN} = 9.7 MHz

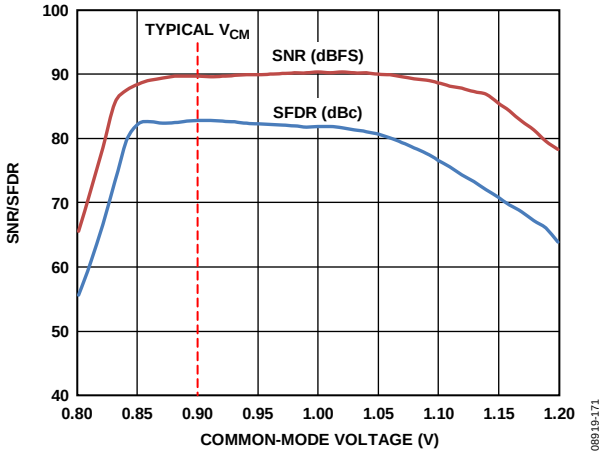


Figure 67. SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 30.3 MHz

EQUIVALENT CIRCUITS

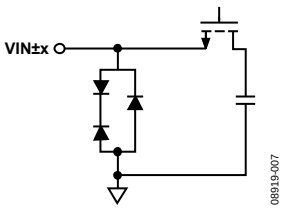


Figure 68. Equivalent Analog Input Circuit

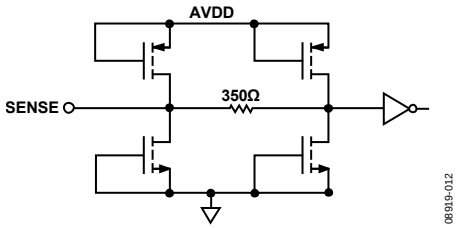


Figure 73. Equivalent SENSE Circuit

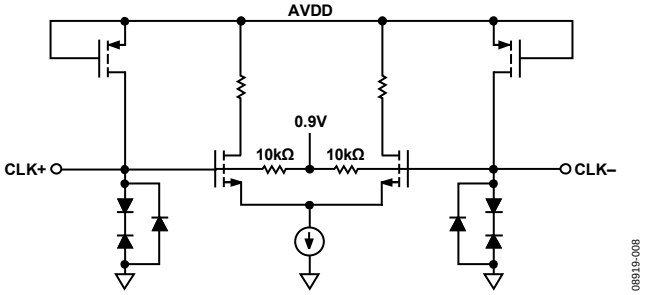


Figure 69. Equivalent Clock Input Circuit

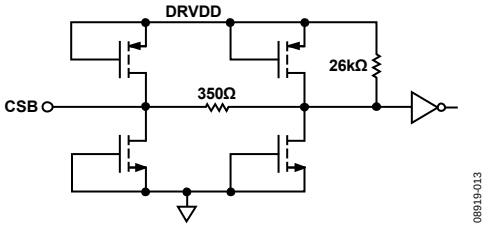


Figure 74. Equivalent CSB Input Circuit

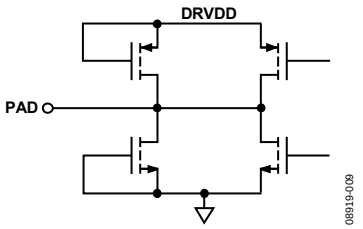


Figure 70. Digital Output

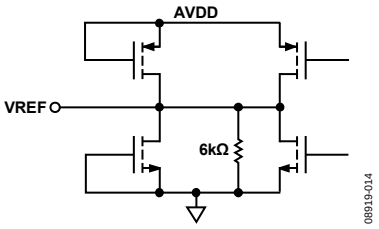


Figure 75. Equivalent VREF Circuit

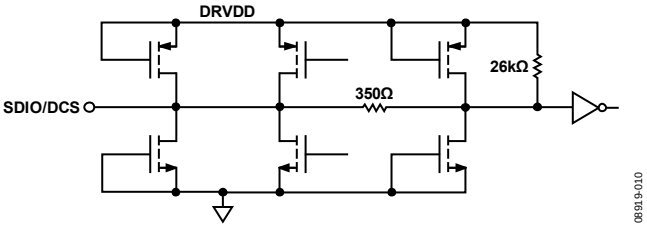


Figure 71. Equivalent SDIO/DCS Circuit

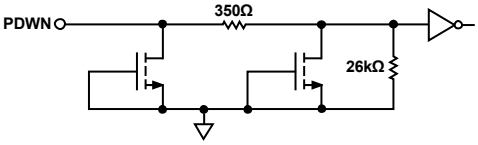


Figure 76. Equivalent PDWN Input Circuit

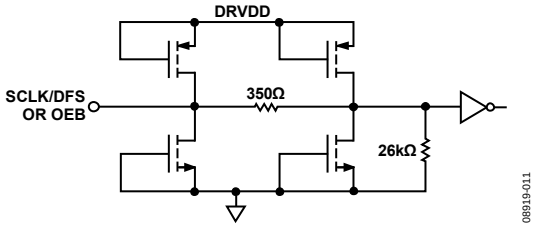


Figure 72. Equivalent SCLK/DFS or OEB Input Circuit

THEORY OF OPERATION

The AD9650 dual-core analog-to-digital converter (ADC) is used for digitizing high frequency, wide dynamic range signals with input frequencies of up to 300 MHz. The user can sample any $f_S/2$ frequency segment from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. The ADCs can also be operated with independent analog inputs.

In quadrature applications, the AD9650 can be used as a baseband or direct down-conversion receiver, in which one ADC is used for I input data, and the other is used for Q input data.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9650 are accomplished using a 3-wire, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9650 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined, switched-capacitor ADC. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9650 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 77). When the input is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within ½ of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject (visit www.analog.com).

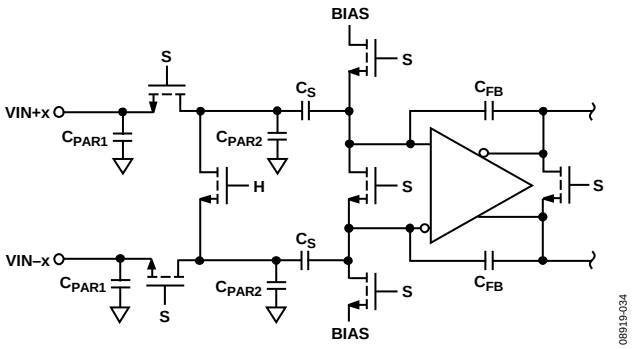


Figure 77. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+x and VIN−x should be matched, and the inputs should be differentially balanced.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by this buffer to 2 × VREF.

Input Common Mode

The analog inputs of the AD9650 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that VCM = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 67). An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Common-Mode Voltage Servo

In applications where there may be a voltage loss between the VCM output of the AD9650 and the analog inputs, the common-mode voltage servo can be enabled. When the inputs are ac-coupled and a resistance of >100 Ω is placed between the VCM output and the analog inputs, a significant voltage drop can occur and the common-mode voltage servo should be enabled. Setting Bit 0 in Register 0x0F to a logic high enables the VCM servo mode. In this mode, the AD9650 monitors the common-mode input level at the analog inputs and adjusts the VCM output level to keep the common-mode input voltage at an optimal level. If both channels are operational, Channel A is monitored. However, if Channel A is in power-down or standby mode, the Channel B input is monitored.

Dither

The AD9650 has an optional dither mode that can be selected for one or both channels. Dithering is the act of injecting a known but random amount of white noise, commonly referred to as dither, into the input of the ADC. Dithering has the effect of improving the local linearity at various points along the ADC transfer function. Dithering can significantly improve the SFDR when quantizing small-signal inputs, typically when the input level is below −6 dBFS.

As shown in Figure 78, the dither that is added to the input of the ADC through the dither DAC is precisely subtracted out digitally to minimize SNR degradation. When dithering is enabled, the dither DAC is driven by a pseudorandom number generator (PN gen). In the AD9650, the dither DAC is precisely calibrated to result in only a very small degradation in SNR and SINAD.

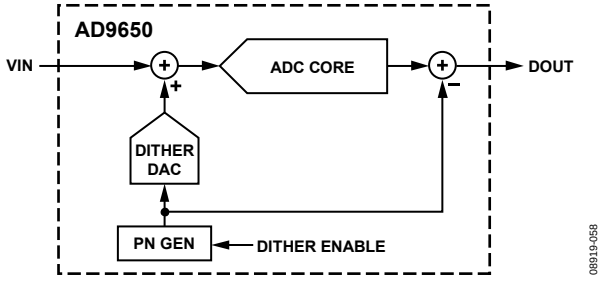


Figure 78. Dither Block Diagram

Large-Signal FFT

In most cases, dithering does not improve SFDR for large-signal inputs close to full scale, for example, with a −1 dBFS input. For large-signal inputs, the SFDR is typically limited by front-end sampling distortion, which dithering cannot improve. However, even for such large-signal inputs, dithering may be useful for certain applications because it makes the noise floor whiter. As is common in pipeline ADCs, the AD9650 contains small DNL errors caused by random component mismatches that produce spurs or tones that make the noise floor somewhat randomly colored part-to-part. Although these tones are typically at very low levels and do not limit SFDR when the ADC is quantizing large-signal inputs, dithering converts these tones to noise and produces a whiter noise floor.

Small-Signal FFT

For small-signal inputs, the front-end sampling circuit typically contributes very little distortion, and, therefore, the SFDR is likely to be limited by tones caused by DNL errors due to random component mismatches. Therefore, for small-signal inputs (typically, those below −6 dBFS), dithering can significantly improve SFDR by converting these DNL tones to white noise.

Static Linearity

Dithering also removes sharp local discontinuities in the INL transfer function of the ADC and reduces the overall peak-to-peak INL.

In receiver applications, utilizing dither helps to reduce DNL errors that cause small-signal gain errors. Often this issue is overcome by setting the input noise 5 dB to 10 dB above the converter noise. By using dither within the converter to correct the DNL errors, the input noise requirement can be reduced.

Differential Input Configurations

Optimum performance is achieved while driving the AD9650 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9650 (see Figure 79), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

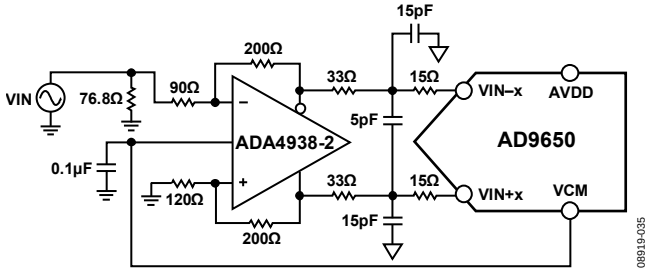


Figure 79. Differential Input Configuration Using the ADA4938-2

For baseband applications in which SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 80. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

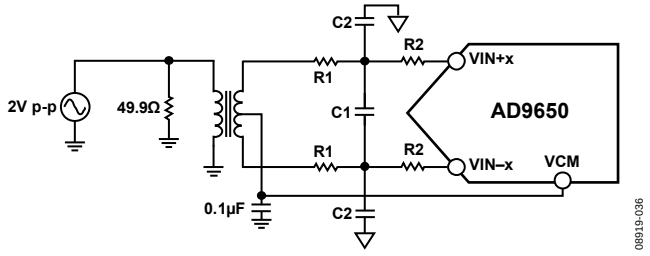


Figure 80. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9650. For applications in which SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 81). In this configuration, the input is ac-coupled, and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 10 displays recommended values to set the RC network. At higher input frequencies, good performance can be achieved by using a ferrite bead in series with a resistor and removing the capacitors. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 10. Example RC Network

Frequency Range (MHz)	R1 Series (Ω Each)	C1 Differential (pF)	R2 Series (Ω Each)	C2 Shunt (pF Each)
0 to 100	33	5	15	15
100 to 200	10	5	10	10
100 to 300	10[1]	Remove	66	Remove

[1] In this configuration, R1 is a ferrite bead with a value of 10 Ω at 100 MHz.

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 82. See the AD8352 data sheet for more information.

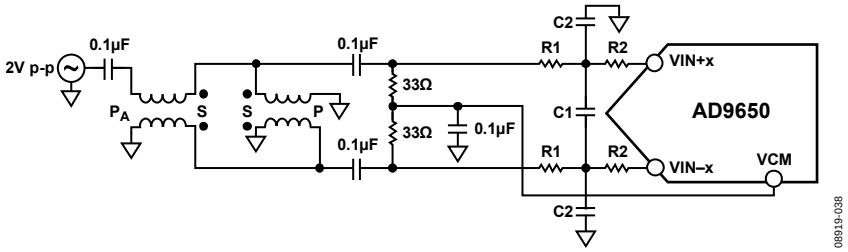


Figure 81. Differential Double Balun Input Configuration

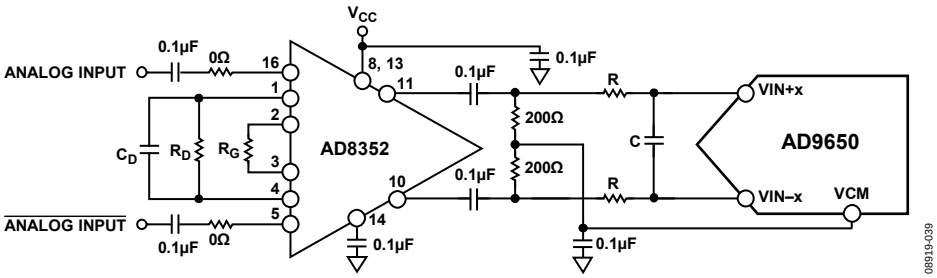


Figure 82. Differential Input Configuration Using the AD8352

VOLTAGE REFERENCE

The AD9650 can be configured for a stable 1.35 V internal reference or a user-applied external reference. The input range of the ADC always equals twice the voltage at the reference pin (VREF) for either an internal or an external reference. Table 11 shows a summary of the internal and external reference connections.

Internal Reference Connection

A stable and accurate 1.35 V reference is built into the AD9650, allowing a 2.7 V p-p full-scale input. To configure the AD9650 for an internal reference, the SENSE pin must be tied low. In addition, to achieve optimal noise performance, it is recommended that the VREF pin be decoupled by 1.0 µF and 0.1 µF capacitors close to the pin. Figure 83 shows the configuration for the internal reference connection.

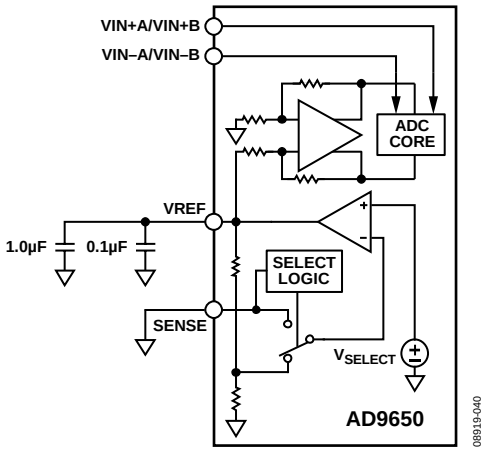


Figure 83. Internal Reference Configuration

If the internal reference of the AD9650 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 84 shows how the internal reference voltage is affected by loading.

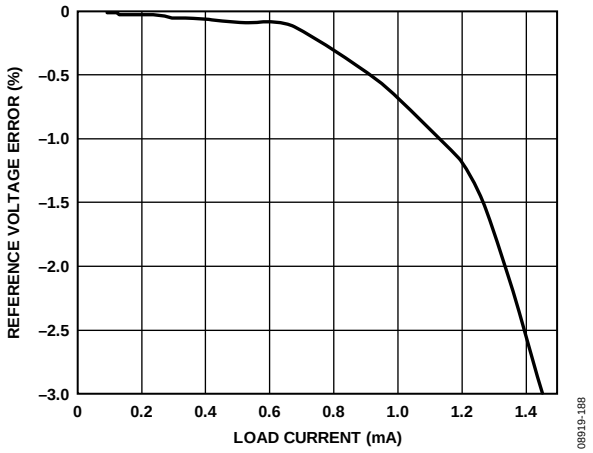


Figure 84. Reference Voltage Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 85 shows the typical drift characteristics of the internal reference in 1.35 V mode.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 6 kΩ load (see Figure 75). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.35 V.

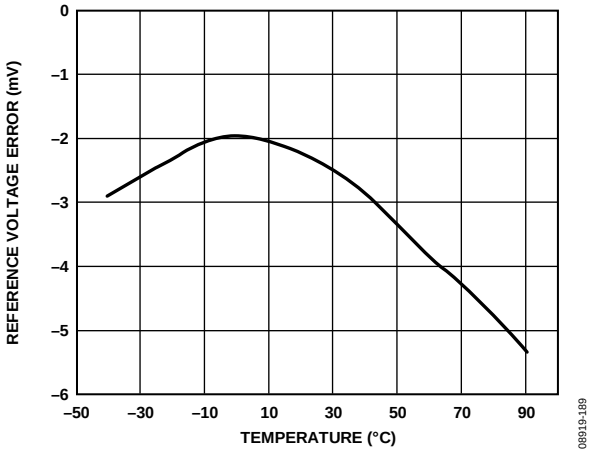


Figure 85. Typical VREF Drift

Table 11. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Internal Reference	AGND to 0.2	1.35	2.7
External Reference	AVDD	N/A	2 × external reference

Clock Input Considerations

For optimum performance, the AD9650 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 86) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

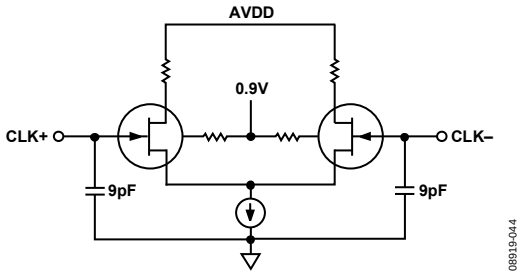


Figure 86. Equivalent Clock Input Circuit

Clock Input Options

The AD9650 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 87 and Figure 88 show two preferred methods for clocking the AD9650 (at clock rates up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun's secondary windings limit the clock excursions into the AD9650 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9650 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

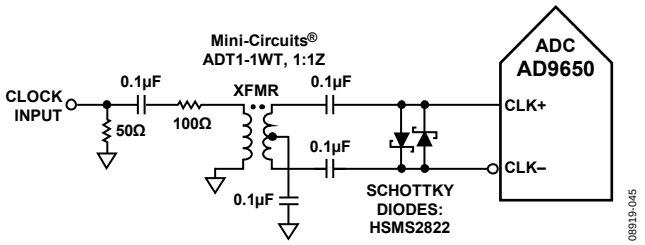


Figure 87. Transformer-Coupled Differential Clock (Up to 200 MHz)

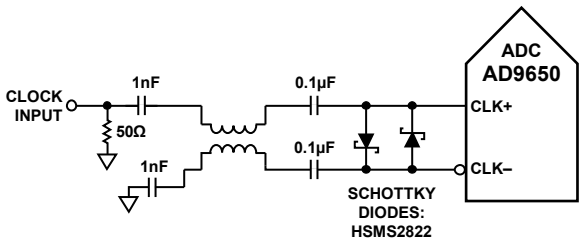


Figure 88. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 89. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518 clock drivers offer excellent jitter performance.

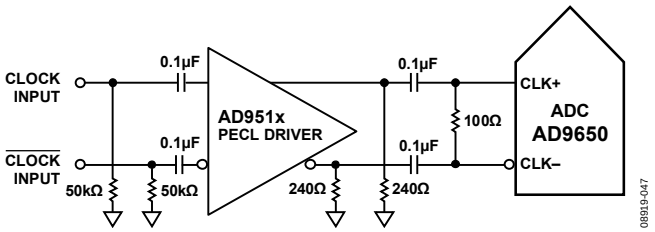


Figure 89. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 90. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518 clock drivers offer excellent jitter performance.

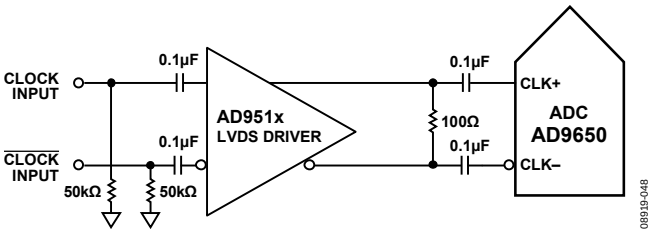


Figure 90. Differential LVDS Sample Clock (Up to 625 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, the CLK+ pin should be driven directly from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor (see Figure 91).

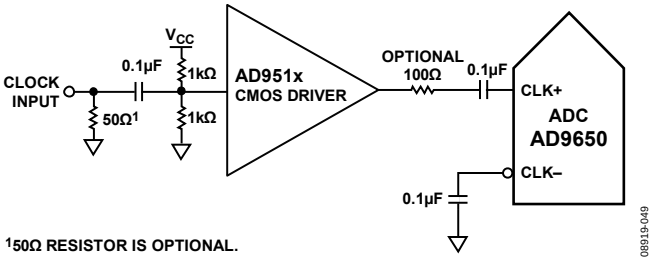


Figure 91. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9650 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. For divide ratios of 1, 2, 4, or 8, the duty cycle stabilizer (DCS) is optional. For other divide ratios, divide-by-3, -5, -6, and -7, the duty cycle stabilizer must be enabled for proper part operation.

The AD9650 clock divider can be synchronized using the external SYNC input. Bit 0 to Bit 2 of Register 0x100 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. The AD9650 requires a tight tolerance on the clock duty cycle to maintain dynamic performance characteristics.

The AD9650 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9650. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS enabled.

Jitter in the rising edge of the input is still of paramount concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. For inputs near full scale, the degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification.

Improvements in SNR can be achieved for IF undersampling applications by minimizing the effects of aperture jitter. This can be accomplished by applying a high frequency clock input and using the integrated clock divider to achieve the desired sample rate of the ADC core. Inherently, the jitter performance of the AD9650 improves as the frequency of the clock increases. This is a result of the slew rate of the clock affecting the noise performance of the ADC, where fast transition edges result in the best performance. Figure 92 shows the improvement in SNR for the different clock divide ratios for the 1 V p-p and 2 V p-p sinusoidal clock inputs. Measurements in Figure 92 were taken for the AD9650BCPZ-105 where the input frequency was 141 MHz. The same analysis can be performed for the various speed grades of the AD9650 family of parts.

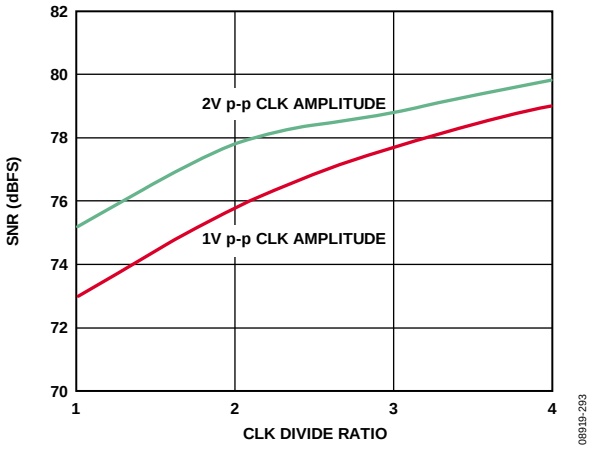


Figure 92. SNR vs. CLK Divide Ratio for f_{IN} = 141 MHz and a Sample Rate of 105 MSPS

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9650. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources.

Refer to the AN-501 Application Note and the AN-756 Application Note (visit www.analog.com) for more information about jitter performance as it relates to ADCs.

CHANNEL/CHIP SYNCHRONIZATION

The AD9650 has a SYNC input that offers the user flexible synchronization options for synchronizing the clock divider. The clock divider sync feature is useful for guaranteeing synchronized sample clocks across multiple ADCs. The input clock divider can be enabled to synchronize on a single occurrence of the SYNC signal or on every occurrence.

The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. The SYNC input should be driven using a single-ended CMOS-type signal.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD9650 varies with its sample rate. In CMOS output mode, the digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (IDRVDD) can be calculated as

$$IDRVDD = VDRVDD \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (32 plus two DCO outputs in the case of the AD9650).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is

determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers reduces digital power consumption.

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9650 is placed in power-down mode. In this state, the ADC typically dissipates 3.3 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9650 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and must be recharged when returning to normal operation.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required.

DIGITAL OUTPUTS

The AD9650 output drivers can be configured to interface with 1.8 V CMOS logic families. The AD9650 can also be configured for LVDS outputs (standard ANSI or reduced output swing mode) using a DRVDD supply voltage of 1.8 V.

In CMOS output mode, the output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The default output mode is CMOS, with each channel output on a separate bus, as shown in Figure 2. The output can also be configured for interleaved CMOS via the SPI port. In interleaved CMOS mode, the data for both channels is output through the Channel A output pins, and the Channel B output is placed into high impedance mode. The timing diagram for interleaved CMOS output mode is shown in Figure 3.

The output data format can be selected for either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 12).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Table 12. SCLK/DFS Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Offset binary (default)	DCS disabled
AVDD	Twos complement	DCS enabled (default)

Digital Output Enable Function (OEB)

The AD9650 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the OEB pin or through the SPI. If the OEB pin is low, the output data drivers and DCOs are enabled. If the OEB pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

When using the SPI, the data outputs and DCO of each channel can be independently three-stated by using the output enable bar bit (Bit 4) in Register 0x14.

TIMING

The AD9650 provides latched data with a pipeline delay of 12 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9650. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9650 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The AD9650 provides two data clock output (DCO) signals intended for capturing the data in an external register. In CMOS output mode, the data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. In LVDS output mode, the DCO and data output switching edges are closely aligned. Additional delay can be added to the DCO output using SPI Register 0x17 to increase the data setup time. In this case, the Channel A output data is valid on the rising edge of DCO, and the Channel B output data is valid on the falling edge of DCO. See Figure 2, Figure 3, and Figure 4 for a graphical timing description of the output modes.

Table 13. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	ORx
$V_{IN+} - V_{IN-}$	< –VREF – 0.5 LSB	0000 0000 0000 0000	1000 0000 0000 0000	1
$V_{IN+} - V_{IN-}$	= –VREF	0000 0000 0000 0000	1000 0000 0000 0000	0
$V_{IN+} - V_{IN-}$	= 0 V	1000 0000 0000 0000	0000 0000 0000 0000	0
$V_{IN+} - V_{IN-}$	= +VREF – 1.0 LSB	1111 1111 1111 1111	0111 1111 1111 1111	0
$V_{IN+} - V_{IN-}$	> +VREF – 0.5 LSB	1111 1111 1111 1111	0111 1111 1111 1111	1

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9650 includes built-in test features designed to enable verification of the integrity of each channel as well as facilitate board level debugging. A BIST (built-in self-test) feature is included that verifies the integrity of the digital datapath of the AD9650. Various output test options are also provided to place predictable values on the outputs of the AD9650.

BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9650 signal path. When enabled, the test runs from an internal pseudorandom noise (PN) source through the digital datapath starting at the ADC block output. The BIST sequence runs for 512 cycles and stops. The BIST signature value for Channel A or Channel B is placed in Register 0x24 and Register 0x25. If one channel is chosen, its BIST signature is written to the two registers. If both channels are chosen, the results from Channel A are placed in the BIST signature registers.

The outputs are not disconnected during this test; therefore, the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or reset from the beginning, based on the value programmed in Register 0x0E, Bit 2. The BIST signature result varies based on the channel configuration.

OUTPUT TEST MODES

The output test modes are shown in Table 17. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9650 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK/DFS pin, the SDIO/DCS pin, and the CSB pin (see Table 14). The SCLK/DFS (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

Table 14. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active-low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 93 and Table 5.

Other modes involving the CSB are available. When the CSB is held low indefinitely, which permanently enables the device, this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI secondary pin functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

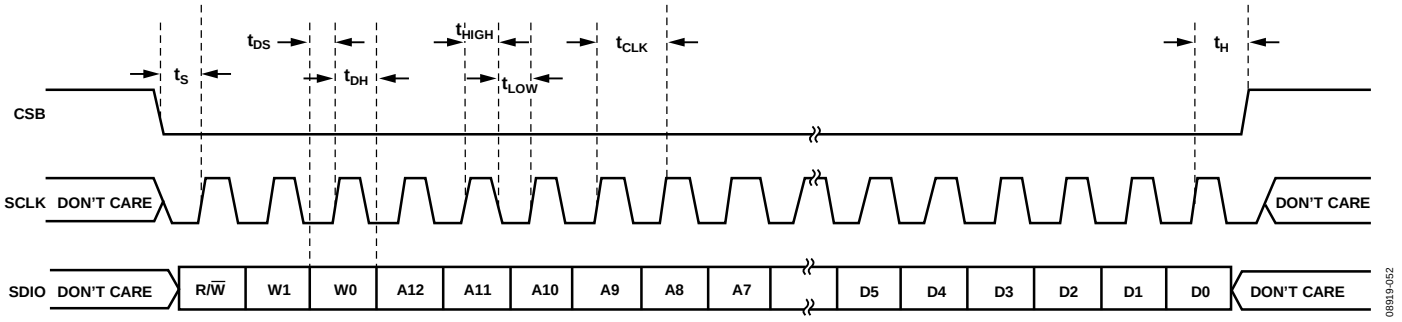


Figure 93. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 14 comprise the physical interface between the user programming device and the serial port of the AD9650. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9650 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI is not being used. When the pins are strapped to AVDD or ground during device power-on, they are associated with a specific function. The Digital Outputs section describes the strappable functions supported on the AD9650.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS pin, the SCLK/DFS pin, the OEB pin, and the PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, output enable, and power-down feature control. In this mode, the CSB chip select bar should be connected to AVDD, which disables the serial port interface.

When the device is in SPI mode, the PDWN and OEB pins remain active. For SPI control of output enable and power-down, the OEB and PDWN pins should be set to their default states.

Table 15. Mode Selection

Pin	External Voltage	Configuration
SDIO/DCS	AVDD (default)	Duty cycle stabilizer enabled
	AGND	Duty cycle stabilizer disabled
SCLK/DFS	AVDD	Twos complement enabled
	AGND (default)	Offset binary enabled
OEB	AVDD	Outputs in high impedance
	AGND (default)	Outputs enabled
PDWN	AVDD	Chip in power-down or standby
	AGND (default)	Normal operation

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9650 part-specific features are described in detail following Table 17, the external memory map register table.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, set the clock divider phase, and enable the sync
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set the output mode, including LVDS
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x30); and the digital feature control register (Address 0x100).

The memory map register table (see Table 17) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining register, Register 0x100, is documented in the Memory Map Register Table section.

Open Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x17).

Default Values

After the AD9650 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 17.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 through Address 0x18 and Address 0x30 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed differently for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 17 affect the entire part or the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 17 are not currently supported for this device.

Table 17. Memory Map Registers

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration (global)	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles are mirrored so that LSB-first mode or MSB-first mode registers correctly, regardless of shift mode.
0x01	Chip ID (global)	8-bit Chip ID[7:0] (AD9650 = 0x3B, default)								0x3B	Read only.
0x02	Chip grade (global)	Open	Speed grade ID 001 = 105 MSPS 010 = 80 MSPS 011 = 65 MSPS 100 = 25 MSPS			Open	Open	Open	Open		Speed grade ID used to differentiate devices; read only.
Channel Index and Transfer Registers											
0x05	Channel index	Open	Open	Open	Open	Open	Open	Data Channel B (default)	Data Channel A (default)	0x03	Bits are set to determine which device on the chip receives the next write command; applies to local registers only.
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions											
0x08	Power modes (local)	1	Open	External power-down pin function (local) 0 = pdwn 1 = stndby	Open	Open	Open	Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = normal operation		0x80	Determines various generic modes of chip operation.
0x09	Global clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer (default)	0x00	
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically cause the duty cycle stabilizer to become active.

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x0D	Test mode (local)	Open	Open	Reset PN long gen	Reset PN short gen	Open	Output test mode 000 = off (default) 001 = midscale short 010 = positive FS 011 = negative FS 100 = alternating checkerboard 101 = PN long sequence 110 = PN short sequence 111 = one/zero word toggle			0x00	When this register is set, the test data is placed on the output pins in place of normal data.
0x0E	BIST enable (global)	Open	Open	Open	Open	Open	Reset BIST sequence	Open	BIST enable	0x04	
0x0F	ADC input (global)	Open	Open	Open	Open	Open	Open	Open	Common-mode servo enable	0x00	
0x14	Output mode	Drive strength 0 = ANSI LVDS; 1 = reduced swing LVDS (global)	Output type 0 = CMOS 1 = LVDS (global)	CMOS output interleave enable (global)	Output enable bar (local)	Open (must be written low)	Output invert (local)	Output format 00 = offset binary 01 = twos complement 01 = gray code 11 = offset binary (local)		0x00	Configures the outputs and the format of the data.
0x16	Clock phase control (global)	Invert DCO clock	Open	Open	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			0x00	Allows selection of clock delays into the input clock divider.
0x17	DCO output delay (global)	Open	Open	Open	DCO clock delay (delay = 2500 ps × register value/31) 00000 = 0 ps 00001 = 81 ps 00010 = 161 ps … 11110 = 2419 ps 11111 = 2500 ps					0x00	
0x24	BIST signature LSB (local)	BIST signature[7:0]								0x00	Read only.
0x25	BIST signature MSB (local)	BIST signature[15:8]								0x00	Read only.
0x30	Dither enable (local)	Open	Open	Open	Dither enable	Open	Open	Open	Open	0x00	
Digital Feature Control											
0x100	SYNC control (global)	Open	Open	Open	Open	Open	Clock divider next SYNC only	Clock divider SYNC enable	Master SYNC enable	0x00	

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SYNC Control (Register 0x100)

Bits[7:3]—Reserved

Bit 2—Clock Divider Next SYNC Only

If the master SYNC enable bit (Address 0x100, Bit 0) and the clock divider SYNC enable bit (Address 0x100, Bit 1) are high, Bit 2 allows the clock divider to synchronize to the first SYNC pulse it receives and to ignore the rest. The clock divider SYNC enable bit (Address 0x100, Bit 1) resets after it synchronizes.

Bit 1—Clock Divider SYNC Enable

Bit 1 gates the SYNC pulse to the clock divider. The SYNC signal is enabled when Bit 1 is high and Bit 0 is high. This is continuous SYNC mode.

Bit 0—Master SYNC Enable

Bit 0 must be high to enable any of the SYNC functions. If the SYNC capability is not used, this bit should remain low to conserve power.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9650 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements that are needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9650, it is recommended that two separate 1.8 V supplies be used. Use one supply for the analog outputs (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the AD9650. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

LVDS Operation

The AD9650 defaults to CMOS output mode on power-up. If LVDS operation is desired, this mode must be programmed, using the SPI configuration registers after power-up. When the AD9650 powers up in CMOS mode with LVDS termination resistors (100 Ω) on the outputs, the DRVDD current can be higher than the typical value until the part is placed in LVDS mode. This additional DRVDD current does not cause damage to the AD9650, but it should be taken into account when considering the maximum DRVDD current for the part.

To avoid this additional DRVDD current, the AD9650 outputs can be disabled at power-up by taking the OEB pin high. After the part is placed in LVDS mode via the SPI port, the OEB pin can be taken low to enable the outputs.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the AD9650 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged to prevent solder wicking through the vias, which can compromise the connection.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. For detailed information about packaging and PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

VCM

The VCM pin should be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 80.

RBIAS

The AD9650 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

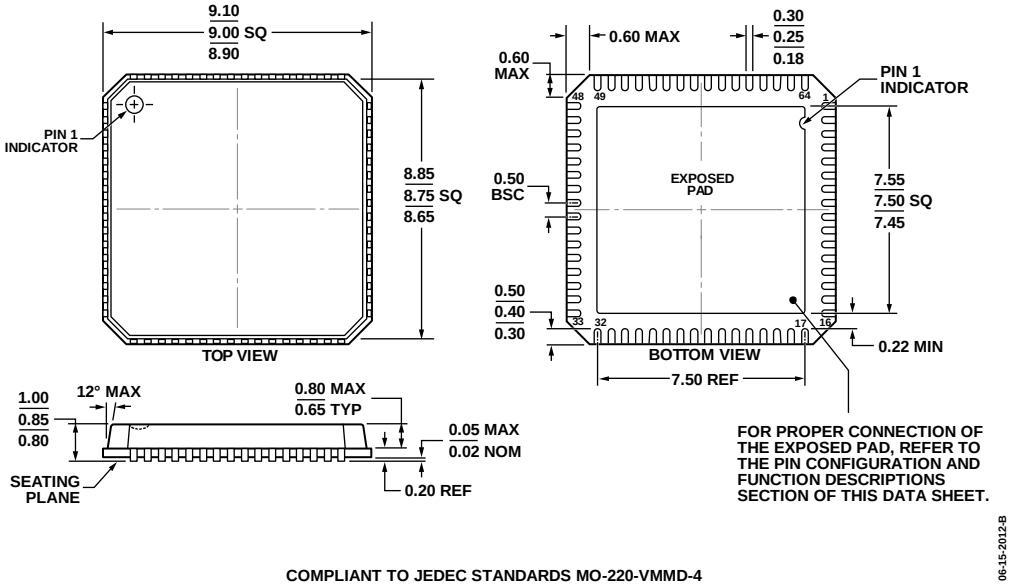
Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9650 to keep these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 94. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9650BCPZ-25	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZRL7-25	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZ-65	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZRL7-65	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZ-80	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZRL7-80	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZ-105	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650BCPZRL7-105	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9650-25EBZ		Evaluation Board	
AD9650-65EBZ		Evaluation Board	
AD9650-80EBZ		Evaluation Board	
AD9650-105EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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