Complete 12-Bit 40 MSPS Imaging Signal Processor

AD9821

FEATURES

Differential Sensor Input with 1 V p-p Input Range
0 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA)
Low Noise Optical Black Clamp Circuit
Analog Preblanking Function
12-Bit 40 MSPS A/D Converter (ADC)
3-Wire Serial Digital Interface
3 V Single-Supply Operation
Low Power: 150 mW @ 3 V Supply
48-Lead LQFP Package

APPLICATIONS

Digital Still Cameras Using CMOS Imagers
Industrial/Scientific Imaging

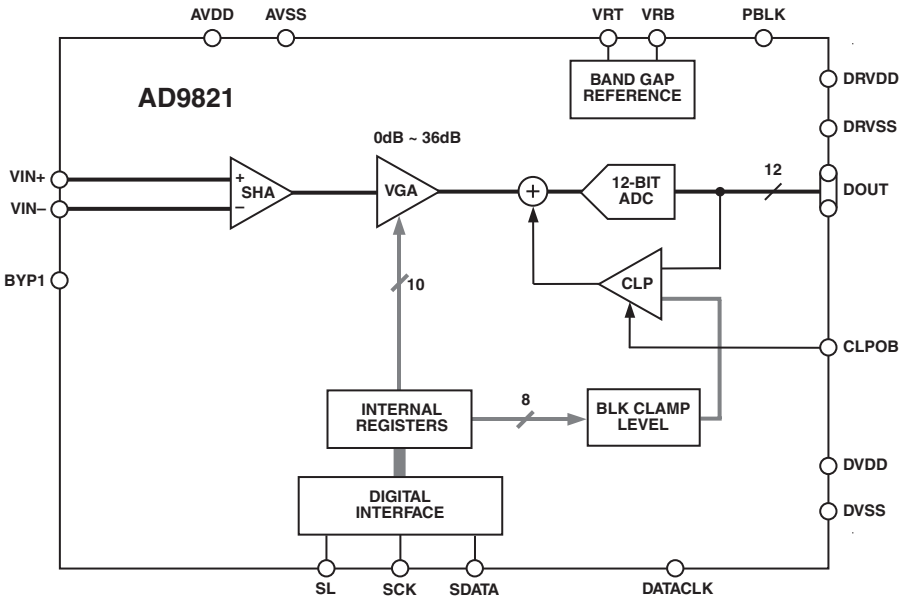
GENERAL DESCRIPTION

The AD9821 is a complete analog signal processor for imaging applications that do not require Correlated Double Sampling (CDS). It features a 40 MHz single-channel architecture designed to sample and condition the outputs of CMOS imagers and CCD arrays already containing on-chip CDS. The AD9821's signal chain consists of a differential input sample-and-hold amplifier (SHA), digitally controlled variable gain amplifier (VGA), black level clamp, and a 12-bit ADC.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, and power-down modes.

The AD9821 operates from a single 3 V power supply, typically dissipates 150 mW, and is packaged in a 48-lead LQFP.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD9821–SPECIFICATIONS

GENERAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 40 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–20		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.7		3.6	V
POWER CONSUMPTION				
Normal Operation		(Specified under Each Mode of Operation)		
Power-Down Modes				
Standby		5		mW
Total Power-Down		1		mW
MAXIMUM CLOCK RATE	40			MHz
A/D CONVERTER				
Resolution	12			Bits
Differential Nonlinearity (DNL)		±0.5		LSB
No Missing Codes	12			Bits Guaranteed
Full-Scale Input Voltage		2.0		V
Data Output Coding		Straight Binary		
VOLTAGE REFERENCE				
Reference Top Voltage (VRT)		2.0		V
Reference Bottom Voltage (VRB)		1.0		V

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (DRVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.)

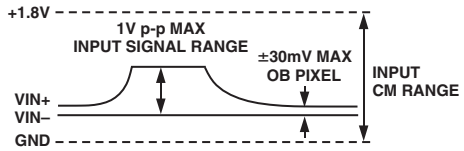
Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V

Specifications subject to change without notice.

IMAGER-MODE SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 40 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Notes
POWER CONSUMPTION		150		mW	See TPC 1 for Power vs. Sample Rate
MAXIMUM CLOCK RATE	40			MHz	
ANALOG INPUTS (VIN+, VIN–)					
Input Common-Mode Range*	0		1.8	V	Linear operating range for VIN+, VIN–
Max Input Amplitude*	1.0			V p-p	Defined as VIN+ minus VIN–
Max Optical Black Pixel Amplitude*		±30		mV	For stable Clamp at max VGA gain
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					See Figure 11 for VGA Gain Curve
Min Gain (VGA Gain Code 00)		0		dB	
Max Gain (VGA Gain Code 1023)		36		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC Output
Min Clamp Level		0		LSB	
Max Clamp Level		255		LSB	
SYSTEM PERFORMANCE					Specifications Include Entire Signal Chain
Gain Accuracy					
Min Gain	–1	0	+1	dB	
Max Gain	34.5	35.5	36.5	dB	
Peak Nonlinearity, 500 mV Input		0.3		%	12 dB Gain Applied
Total Output Noise		0.5		LSB rms	AC Grounded Input, 6 dB Gain Applied
Power Supply Rejection (PSR)		40		dB	Measured with Step Change on Supply
POWER-UP RECOVERY TIME					Normal Clock Signals Applied
Reference Standby Mode		1		ms	
Total Power-Down Mode		3		ms	
Power-Off Condition		10		ms	

*Input Signal Characteristics defined as follows:



Specifications subject to change without notice.

TIMING SPECIFICATIONS (C_L = 20 pF, f_{SAMP} = 40 MHz, Imager-Mode Timing in Figures 5 and 6, Serial Timing in Figures 7–9)

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK Clock Period	t_{CONV}	25	25		ns
DATACLK Hi/Low Pulsewidth	t_{ADC}	11	12.5		ns
CLPOB Pulsewidth*	t_{COB}	2	20		Pixels
Internal Clock Delay	t_{ID}		3.0		ns
DATA OUTPUTS					
Output Delay	t_{OD}		13	16	ns
Output Hold Time	t_H	7.0	7.6		ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{DV}	10			ns

*Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	With Respect To	Min	Max	Unit
AVDD1, AVDD2	AVSS	–0.3	+3.9	V
DVDD1, DVDD2	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
DATACLK	DVSS	–0.3	DVDD + 0.3	V
CLPOB, PBLK	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
VRT, VRB	AVSS	–0.3	AVDD + 0.3	V
BYP1, VIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9821KST	–20°C to +85°C	Thin Plastic Quad Flatpack (LQFP)	ST-48

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP Package

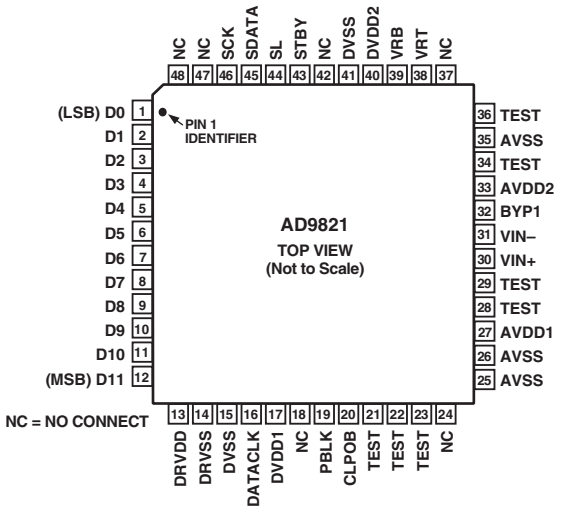
θ_{JA} = 56°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9821 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Type	Description
1–12	D0–D11	DO	Digital Data Outputs
13	DRVDD	P	Digital Output Driver Supply
14	DRVSS	P	Digital Output Driver Ground
15, 41	DVSS	P	Digital Ground
16	DATACLK	DI	Digital Data Output Latch Clock
17	DVDD1	P	Digital Supply
18, 24, 37, 42, 47, 48	NC	NC	Internally Not Connected. May be Tied High or Low.
19	PBLK	DI	Preblanking Clock Input
20	CLPOB	DI	Black Level Clamp Clock Input
21–23	TEST	DI	Test Use Only. Tie to VDD or VSS.
25, 26, 35	AVSS	P	Analog Ground
27	AVDD1	P	Analog Supply
28, 29	TEST	AO	Test Use Only. Tie to VDD or VSS.
30	VIN+	AI	Positive Analog Input for Imager Signal
31	VIN–	AI	Negative Analog Input for Imager Signal
32	BYP1	AO	Internal Bias Level Decoupling
33	AVDD2	P	Analog Supply
34, 36	TEST	AI	Test Use Only. Tie to VDD or VSS.
38	VRT	AO	ADC Top Reference Voltage Decoupling
39	VRB	AO	ADC Bottom Reference Voltage Decoupling
40	DVDD2	P	Digital Supply
43	STBY	DI	Standby Mode, Active High. Same as Total Power-Down Mode.
44	SL	DI	Serial Digital Interface Load Pulse
45	SDATA	DI	Serial Digital Interface Data
46	SCK	DI	Serial Digital Interface Clock

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9821 from a true straight line. The point used as "zero scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a Level 1, 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship 1 LSB = (ADC Full Scale/2^N codes) when N is the bit resolution of the ADC. For the AD9821, 1 LSB is 500 μV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the AD9821's power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Internal Delay for SHA
The internal delay (also called aperture delay) is the time delay that occurs from when the sampling edge is applied to the AD9821 until the actual sample of the input signal is held. The DATACLK samples the input signal during the transition from low to high, so the internal delay is measured from each clock's rising edge to the instant the actual internal sample is taken.

EQUIVALENT INPUT CIRCUITS

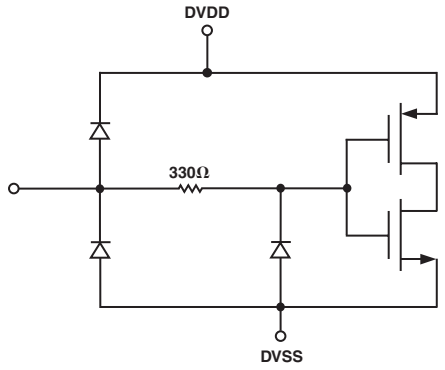


Figure 1. Digital Inputs— DATACLK, CLPOB, PBLK, SCK, SL

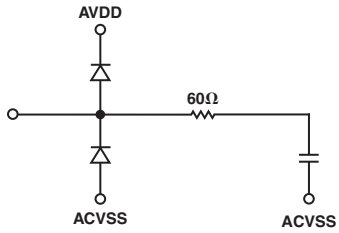


Figure 3. VIN+ and VIN– (Pins 30 and 31)

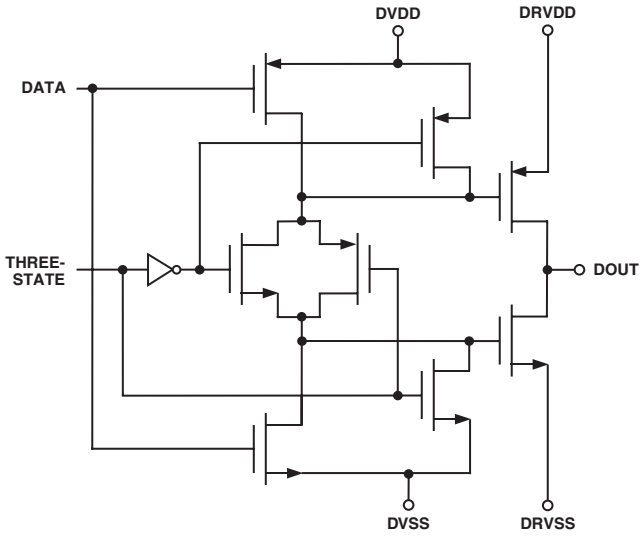


Figure 2. Data Outputs—D0–D11

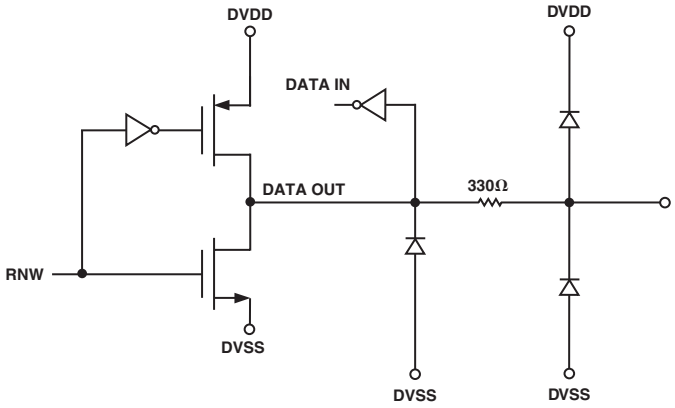
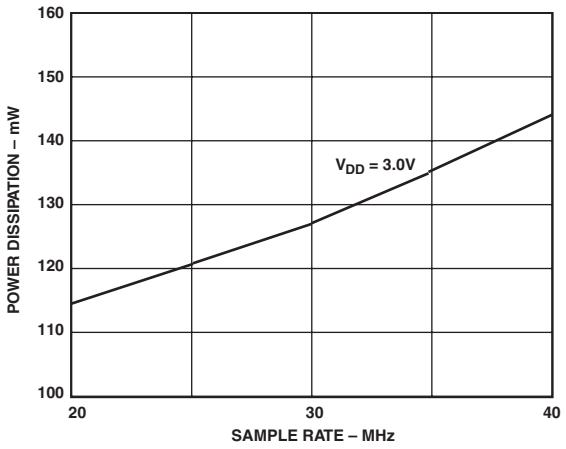
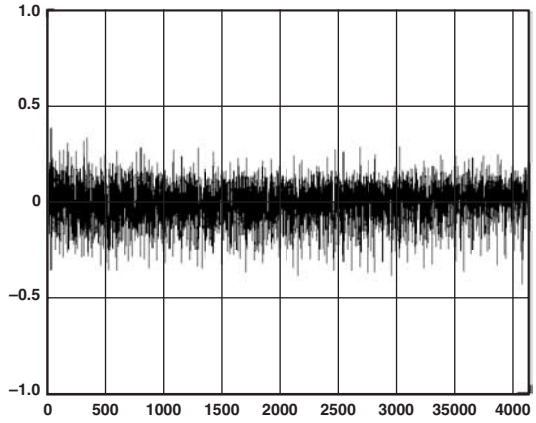


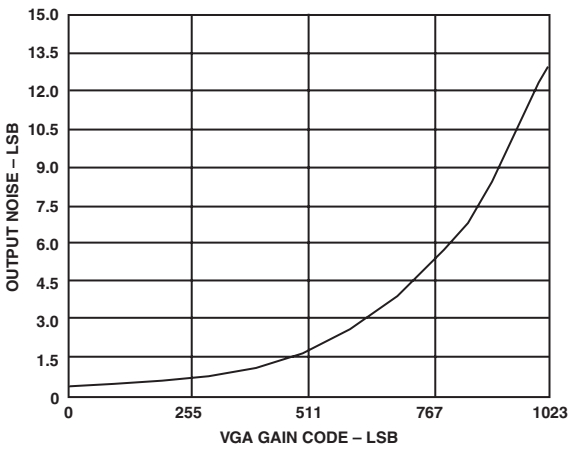
Figure 4. SDATA (Pin 47)



TPC 1. Power vs. Sample Rate

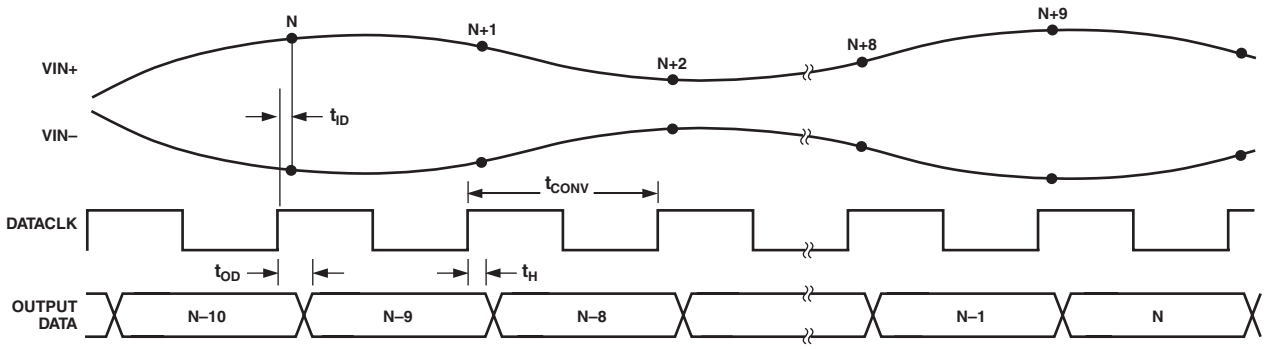


TPC 2. Typical DNL Performance



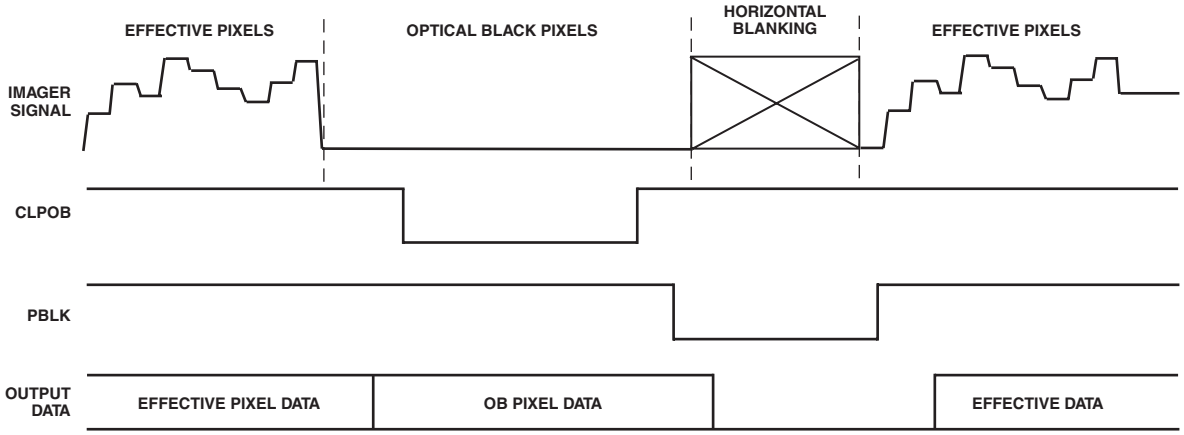
TPC 3. Output Noise vs. VGA Gain

IMAGER MODE AND AUX MODE TIMING



NOTES:
1. VIN+ AND VIN– SIGNALS ARE SAMPLED AT DATACLK RISING EDGES (CAN BE INVERTED USING THE CONTROL REGISTER).
2. INTERNAL SAMPLING DELAY (APERTURE) t_{ID} IS TYPICALLY 3 ns.
3. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

Figure 5. Imager Mode Timing



NOTES:
1. CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING CLPOB.
2. PBLK SIGNAL IS OPTIONAL.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

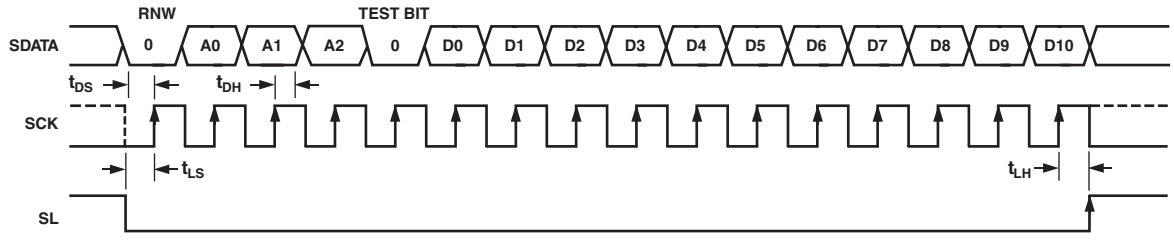
Figure 6. Typical Imager Mode Line Clamp Timing

INTERNAL REGISTER MAP AND SERIAL INTERFACE TIMING

Table I. Internal Register Map

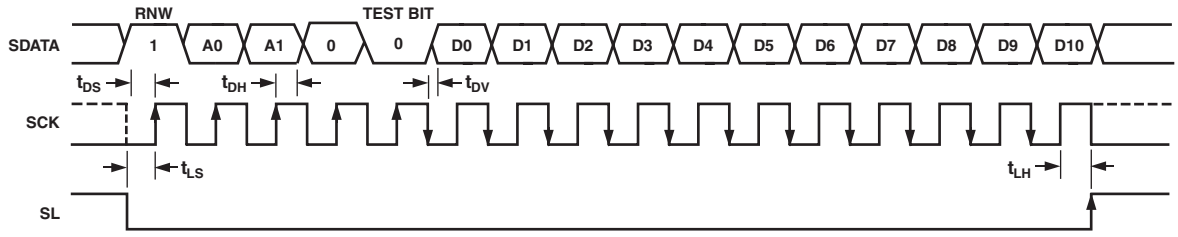
Register Name	Address A0 A1 A2	Data Bits D0 D1 D2	D3 D4	D5	D6	D7	D8	D9	D10	
Operation	0 0 0	Input Mode Selection	Power-Down Modes	Software Reset	OB Clamp On/Off	0[1]	1[2]	0[1]	0[1]	0[1]
VGA Gain	1 0 0	LSB							MSB	X
Clamp Level	0 1 0	LSB					MSB	X	X	X
Control	1 1 0	0[1] 0[1]	0[1] 0[1]	0[1]	Clock Polarity Select for CLP/DATA		0[1]	0[1]	0[1]	X

NOTES
[1]Internal use only. Must be set to 0.
[2]Must be set to 1.



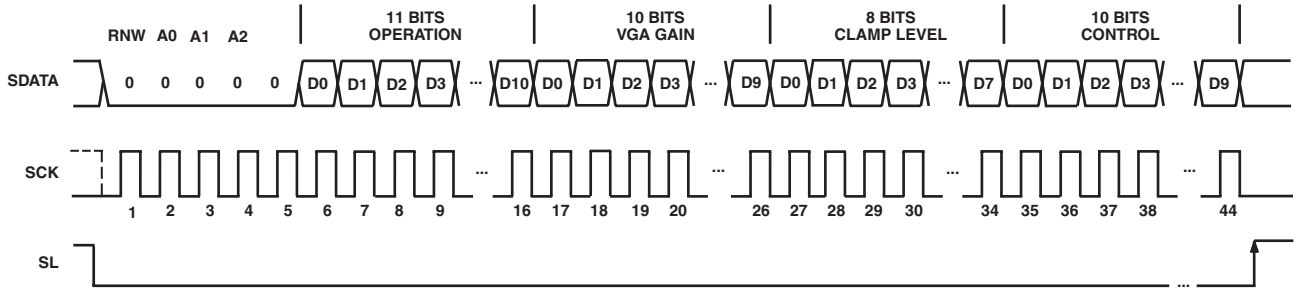
NOTES:
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. RNW = READ-NOT WRITE. SET LOW FOR WRITE OPERATION.
3. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
4. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.

Figure 7. Serial Write Operation



NOTES:
1. RNW = READ-NOT WRITE. SET HIGH FOR READ OPERATION.
2. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
3. SERIAL DATA FROM THE SELECTED REGISTER IS VALID STARTING AFTER THE FIFTH SCK FALLING EDGE, AND IS UPDATED ON SCK FALLING EDGES.

Figure 8. Serial Readback Operation



NOTES:
1. ANY NUMBER OF ADJACENT REGISTERS MAY BE LOADED SEQUENTIALLY, BEGINNING WITH THE LOWEST ADDRESS AND INCREMENTING ONE ADDRESS AT A TIME.
2. WHEN SEQUENTIALLY LOADING MULTIPLE REGISTERS, THE EXACT REGISTER LENGTH (SHOWN ABOVE) MUST BE USED FOR EACH REGISTER.
3. ALL LOADED REGISTERS WILL BE SIMULTANEOUSLY UPDATED WITH THE RISING EDGE OF SL.

Figure 9. Continuous Serial Write Operation to All Registers

REGISTER DETAILS

Table II. Operation Register Contents (Default Value x000)

D10	D9	D8	D7	D6	Optical Black Clamp D5	Reset D4	Power-Down Modes D3 D2	Channel Selection D1 D0
0[1]	0[1]	0[1]	1[2]	0[1]	0 Enable Clamping 1 Disable Clamping	0 Normal 1 Reset All Registers to Default	0 0 Normal Power 0 1 Test Only 1 0 Ref-Standby 1 1 Total Power-Down	0 0 Test Only 0 1 Test Only 1 0 Test Only 1 1 Imager Mode

NOTES
[1]Must be set to 0.
[2]Set to 1.

Table III. VGA Gain Register Contents (Default Value x000)

D10	MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	Gain (dB)
X	0	0	0	0	0	0	0	0	0	0	0.0
					•						•
					•						•
					•						•
	1	1	1	1	1	1	1	1	1	0	35.965
	1	1	1	1	1	1	1	1	1	1	36.0

Table IV. Clamp Level Register Contents (Default Value x080)

D10	D9	D8	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Clamp Level (LSB)
X	X	X	0	0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	1	1
			0	0	0	0	0	0	1	0	2
						•					•
						•					•
						•					•
			1	1	1	1	1	1	1	0	254
			1	1	1	1	1	1	1	1	255

Table V. Control Register Contents (Default Value x000)

D10	D9	D8	D7	DATACLK Polarity D6	CLPOB/PBLK Polarity D5	D4	D3	D2	D1	D0
X	0*	0*	0*	0 Sample on Rising Edge 1 Sample on Falling Edge	0 Active Low 1 Active High	0*	0*	0*	0*	0*

*Must be set to 0.

CIRCUIT DESCRIPTION AND OPERATION

The AD9821 signal processing chain is shown in Figure 10. Each processing step is essential in achieving a high quality image from the raw imager pixel data.

Differential Input SHA

The differential input SHA circuit is designed to accommodate a variety of different image sensor output voltages. The timing shown in Figure 8 illustrates how the DATACLK signal is used to sample both the VIN+ and VIN– signals simultaneously. The imager signal is sampled on the rising edges of DATACLK. Placement of this clock signal is critical in achieving the best performance from the imager. An internal DATACLK delay (t_{ID}) of 3 ns is caused by internal propagation delays.

The differential input can be used in a variety of single-ended and differential configurations, as shown in Table VI. The allowable voltage range for both VIN+ or VIN– is from 0 V to 1.8 V. Signal levels outside this range will result in severely degraded performance. Regardless of the input configuration, the voltage sampled by the SHA is always equal to VIN+ minus VIN–. VIN+ must always be equal to or greater than VIN– or negative clipping will occur. A small amount of offset between the VIN+ and VIN– signals is allowable and can be corrected by the Optical Black Clamp, up to ±30 mV.

Note that the VIN+ and VIN– inputs do not contain any dc restoration or bias circuitry. Therefore, dc-coupling is recommended when driving the AD9821 analog inputs. If ac-coupling is used, external biasing circuitry must be provided for the VIN+ and VIN– inputs to keep them in the acceptable common-mode voltage range of 0 V to 1.8 V.

Table VI. Example Input Voltage Configurations

VIN+ Range (V)		VIN– Range (V)		SHA Output Range (V)	
Black	White	Black	White	Black	White
0	1.0	0	0	0	1.0
0.5	1.5	0.5	0.5	0	1.0
1.0	1.5	1.0	0.5	0	1.0
0.5	1.0	0.5	0	0	1.0
1.0	1.0	1.0	0	0	1.0

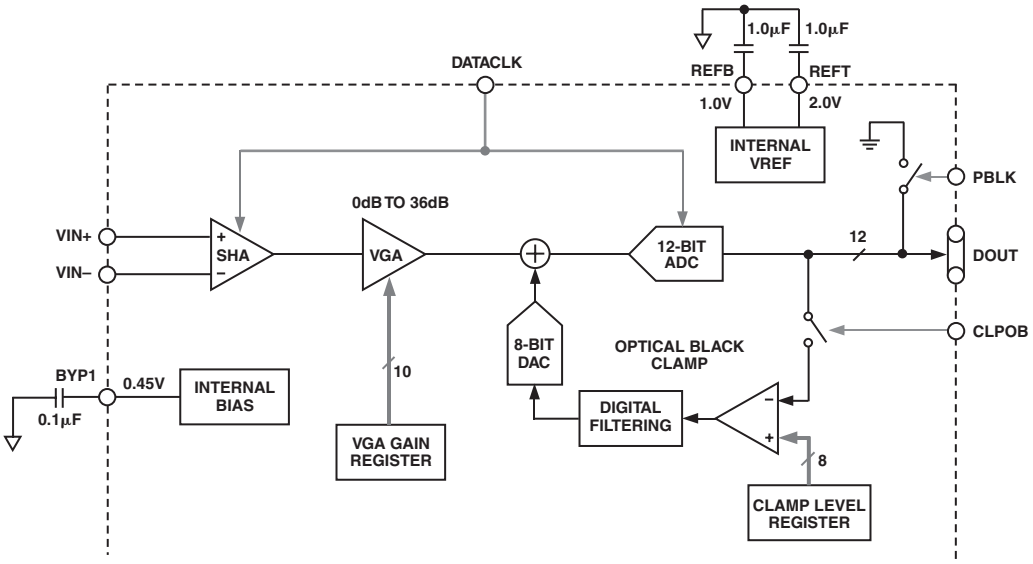


Figure 10. Internal Block Diagram

Variable Gain Amplifier

The VGA stage provides a gain range of 0 dB to 36 dB, programmable with 10-bit resolution through the serial digital interface. A minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is –6 dB to +30 dB.

The VGA gain curve follows a "linear-in-dB" characteristic. The exact VGA gain can be calculated for any Gain Register value by using the equation:

$$Gain(dB) = (0.0351 \times Code)$$

where the code range is 0 to 1023.

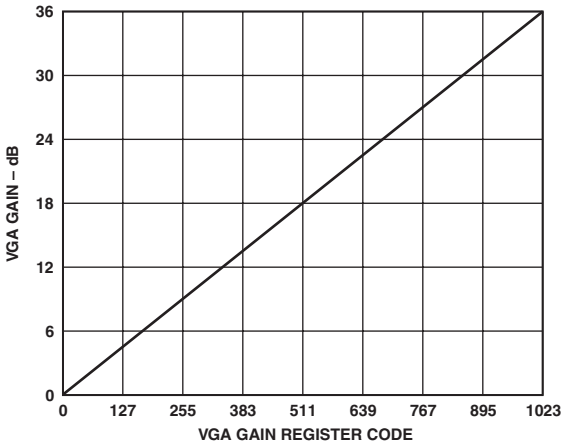


Figure 11. VGA Gain Curve

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference selected by the user in the Clamp Level Register. Any value between 0 LSB and 255 LSB may be programmed using the 8-bit Clamp Level Register. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post-processing, the AD9821 optical black clamping may be disabled using Bit D5 in the Operation Register (see Internal Register Map and Serial Interface Timing section). When the loop is disabled, the Clamp Level Register may still be used to provide programmable offset adjustment.

Horizontal timing is shown in Figure 9. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulsewidths may be used, but the ability to track low frequency variations in the black level will be reduced.

As discussed in the Differential Input SHA section, the CLPOB loop is capable of correcting for an offset difference between the VIN+ and VIN– inputs. Because the clamp is located after the VGA gain stage, the clamp will be most limited when the VGA gain is at its maximum value. Under these conditions, the OB clamp loop correction range is restricted to ±30 mV offset between the VIN+ and VIN– inputs. At minimum VGA gain, the offset correction range increases to ±250 mV of offset. If the OB clamp loop's correction range is exceeded, then the black level at the output of the AD9821 will increase and further correction will be necessary. As mentioned previously, it is also possible to disable the AD9821's OB clamp loop.

A/D Converter (ADC)

The AD9821 uses high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB, as shown in TPC 2. Instead of the 1 V full-scale range used by the earlier AD9801 and AD9803 products from Analog Devices, the AD9821's ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range (see TPC 3).

APPLICATIONS INFORMATION

The AD9821 is a complete Analog Front End (AFE) product for a variety of imager applications using CMOS image sensors and CCDs with on-chip CDS. As shown in Figure 10, the imager output is generally buffered and sent to the AD9821's analog inputs, either as a differential or single-ended signal. The AD9821 performs the sample-and-hold operation, gain adjustment, black level correction, and analog-to-digital conversion. The AD9821's digital output data is then processed by the image processing ASIC. The internal registers of the AD9821—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the imager and the AFE.

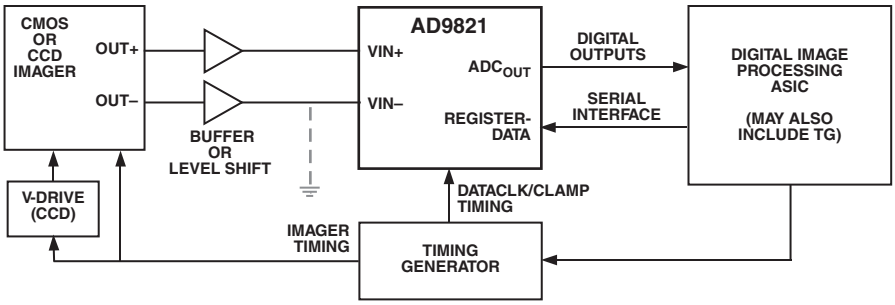


Figure 12. System Applications Diagram

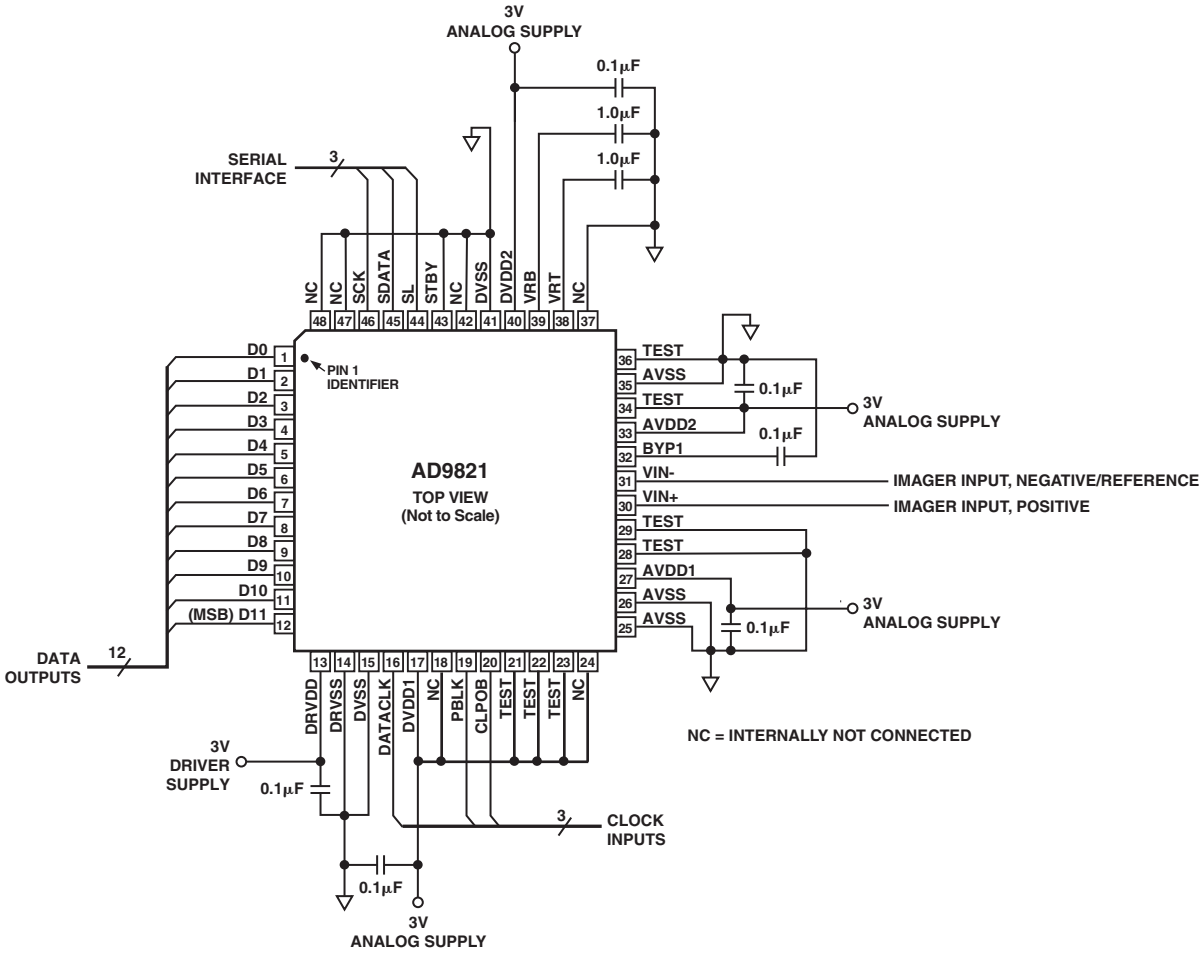


Figure 13. Recommended Circuit Configuration

Internal Power-On Reset Circuitry

After power-on, the AD9821 will automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes will be ignored until the internal reset operation is completed.

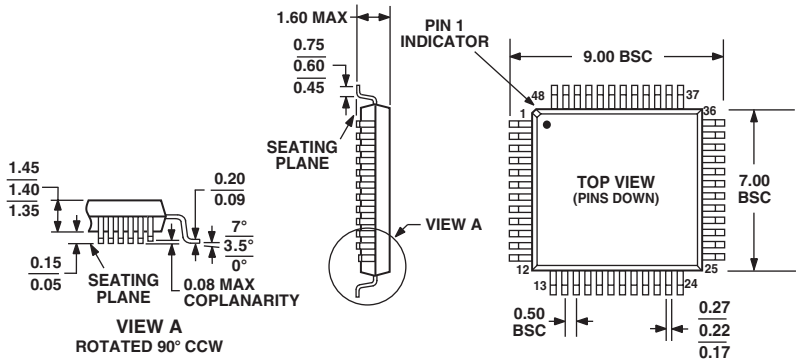
Grounding and Decoupling Recommendations

As shown in Figure 13, a single ground plane is recommended for the AD9821. This ground plane should be as continuous as possible, particularly around Pins 25 through 39. This will ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9821, but a separate digital driver supply may be used for DRVDD (Pin 13). DRVDD should always be decoupled to DRVSS (Pin 14), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, reducing digital power dissipation, and reducing potential noise coupling. If the digital outputs (Pins 1–12) must drive a load larger than 20 pF, buffering is recommended to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

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