25 MHz Direct Digital Synthesizer, Waveform Generator

Data Sheet

AD9832

FEATURES

25 MHz speed
On-chip SIN lookup table
On-chip, 10-bit DAC
Serial loading
Power-down option
Temperature range: −40°C to +85°C
200 mW power consumption
16-Lead TSSOP

APPLICATIONS

Frequency stimulus/waveform generation
Frequency phase tuning and modulation
Low power RF/communications systems
Liquid and gas flow measurement
Sensory applications: proximity, motion, and defect detection
Test and medical equipment

GENERAL DESCRIPTION

The AD9832 is a numerically controlled oscillator employing a phase accumulator, a sine look-up table, and a 10-bit digital-to-analog converter (DAC) integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 25 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the serial interface.

A power-down bit allows the user to power down the AD9832 when it is not in use, the power consumption being reduced to 5 mW (5 V) or 3 mW (3 V). The part is available in a 16-lead TSSOP package.

Similar DDS products can be found at www.analog.com/DDS.

FUNCTIONAL BLOCK DIAGRAM

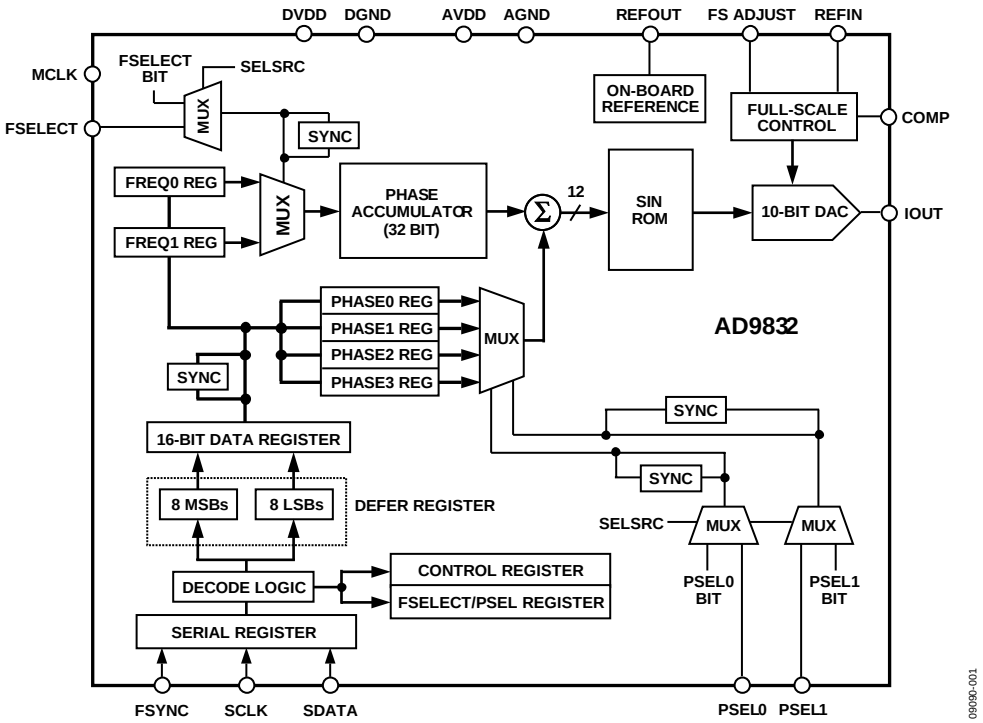


Figure 1.

Rev. E **Document Feedback**

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REVISION HISTORY

2/13—Rev. D to Rev. E

Changes to Table 10 ... 15
Changes to Flowcharts Section ... 16

7/12—Rev. C to Rev. D

Changed On-Chip COS Lookup Table to On-Chip SIN Lookup Table in Features Section ... 1

9/11—Rev. B to Rev. C

Changes to Features and Applications ... 1
Changes to Specification Statement ... 3
Changes to Timing Characteristics Statement ... 5
Replaced Evaluation Board Section; Renumbered Sequentially ... 21
Changes to Ordering Guide ... 26

6/10—Rev. A to Rev. B

Updated Format ... Universal
Changed CMOS Complete DDS to 3 V to 5.0 V Programmable Waveform Generator ... 1
Changes to Serial Interface Section ... 14
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

7/99—Rev 0 to Rev. A

SPECIFICATIONS

V_{DD} = +5 V ± 5%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 3.9 kΩ; R_{LOAD} = 300 Ω for IOUT, unless otherwise noted. Also, see Figure 2.

Table 1.

Parameter[1]	AD9832B	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	25	MSPS nom	
IOUT Full Scale	4	mA nom	
	4.5	mA max	
Output Compliance	1.35	V max	3 V power supply
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS[2]			
Dynamic Specifications			
Signal-to-Noise Ratio	50	dB min	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Total Harmonic Distortion	−53	dBc max	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Spurious-Free Dynamic Range (SFDR)[3]			f_{MCLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Narrow Band (±50 kHz)	−72	dBc min	5 V power supply
	−70	dBc min	3 V power supply
Wideband (±2 MHz)	−50	dBc min	
Clock Feedthrough	−60	dBc typ	
Wake-Up Time[4]	1	ms typ	
Power-Down Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ 25°C	1.21	V typ	
T_{MIN} to T_{MAX}	1.21 ± 7%	V min/V max	
REFIN Input Impedance	10	MΩ typ	
Reference Temperature Coefficient (TC)	100	ppm/°C typ	
REFOUT Output Impedance	300	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	V_{DD} − 0.9	V min	
Input Low Voltage, V_{INL}	0.9	V max	
Input Current, I_{INH}	10	μA max	
Input Capacitance, C_{IN}	10	pF max	
POWER SUPPLIES			
AVDD	2.97/5.5	V min/V max	
DVDD	2.97/5.5	V min/V max	
I_{AA}	5	mA max	5 V power supply
I_{DD}	2.5 + 0.4/MHz	mA typ	5 V power supply
I_{AA} + I_{DD}[5]	15	mA max	3 V power supply
	24	mA max	5 V power supply
Low Power Sleep Mode	350	μA max	

[1] Operating temperature range is −40°C to +85°C.
[2] 100% production tested.
[3] f_{MCLK} = 6.25 MHz, frequency word = 0x5671C71C, and f_{OUT} = 2.11 MHz.
[4] See Figure 13. To reduce the wake-up time at low power supplies and low temperature, the use of an external reference is suggested.
[5] Measured with the digital inputs static and equal to 0 V or DVDD. The AD9832 is tested with a capacitive load of 50 pF. The part can operate with higher capacitive loads, but the magnitude of the analog output will be attenuated. For example, a 5 MHz output signal is attenuated by 3 dB when the load capacitance equals 85 pF.

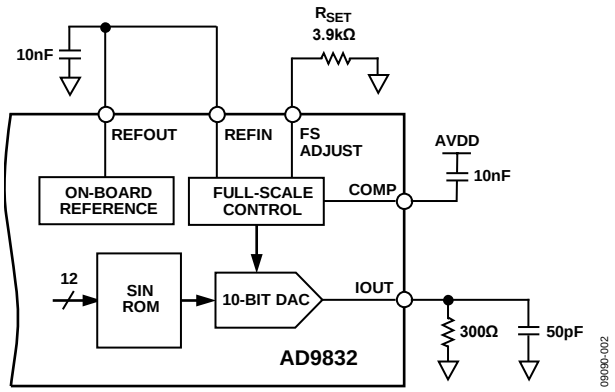


Figure 2. Test Circuit by Which Specifications Were Tested

TIMING CHARACTERISTICS

V_{DD} = +5 V ± 5%; AGND = DGND = 0 V, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	40	ns min	MCLK period
t_2	16	ns min	MCLK high duration
t_3	16	ns min	MCLK low duration
t_4	50	ns min	SCLK period
t_5	20	ns min	SCLK high duration
t_6	20	ns min	SCLK low duration
t_7	15	ns min	FSYNC to SCLK falling edge setup time
t_8	20	ns min	FSYNC to SCLK hold time
	SCLK − 5	ns max	
t_9	15	ns min	Data setup time
t_{10}	5	ns min	Data hold time
t_{11}	8	ns min	FSELECT, PSEL0, PSEL1 setup time before MCLK rising edge
t_{11A}[1]	8	ns min	FSELECT, PSEL0, PSEL1 setup time after MCLK rising edge

[1] See the Pin Configuration and Function Descriptions section.

Timing Diagrams

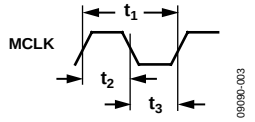


Figure 3. Master Clock

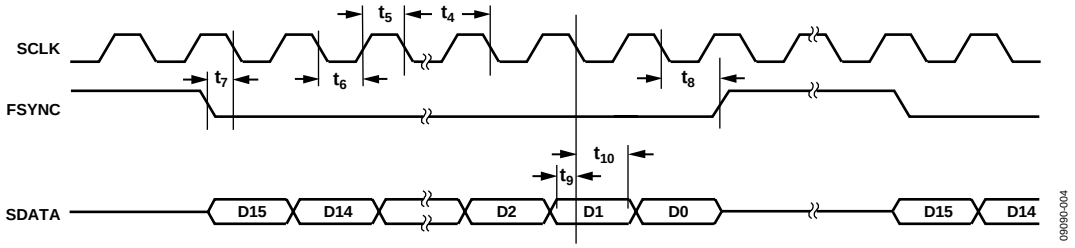


Figure 4. Serial Timing

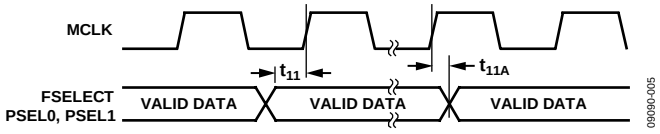


Figure 5. Control Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	−0.3 V to +7 V
DVDD to DGND	−0.3 V to +7 V
AVDD to DVDD	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	158°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	>4500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

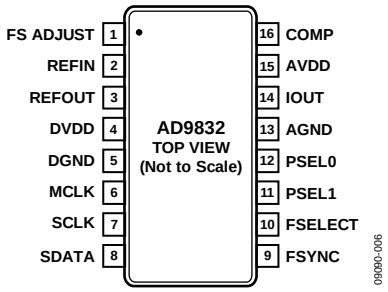


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is $IOUT_{FULL\text{-}SCALE} = 12.5 \times V_{REFIN}/R_{SET}$, where V_{REFIN} = 1.21 V nominal and R_{SET} = 3.9 kΩ typical.
2	REFIN	Voltage Reference Input. The AD9832 can be used with either the on-board reference, which is available from the REFOUT pin, or an external reference. The reference to be used is connected to the REFIN pin. The AD9832 accepts a reference of 1.21 V nominal.
3	REFOUT	Voltage Reference Output. The AD9832 has an on-board reference of value 1.21 V nominal. The reference is available on the REFOUT pin. This reference is used as the reference to the DAC by connecting REFOUT to REFIN. REFOUT should be decoupled with a 10 nF capacitor to AGND.
4	DVDD	Positive Power Supply for the Digital Section. A 0.1 µF decoupling capacitor should be connected between DVDD and DGND. DVDD can have a value of 5 V ± 10% or 3.3 V ± 0%.
5	DGND	Digital Ground.
6	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. This clock determines the output frequency accuracy and phase noise.
7	SCLK	Serial Clock, Logic Input. Data is clocked into the AD9832 on each falling SCLK edge.
8	SDATA	Serial Data In, Logic Input. The 16-bit serial data-word is applied to this input.
9	FSYNC	Data Synchronization Signal, Logic Input. When this input goes low, the internal logic is informed that a new word is being loaded into the device.
10	FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. The frequency register to be used can be selected using the FSELECT pin or the FSELECT bit. FSELECT is sampled on the rising MCLK edge. FSELECT needs to be in steady state when an MCLK rising edge occurs. If FSELECT changes value when a rising edge occurs, there is an uncertainty of one MCLK cycle as to when control is transferred to the other frequency register. To avoid any uncertainty, a change on FSELECT should not coincide with an MCLK rising edge. When the bit is being used to select the frequency register, the FSELECT pin should be tied to DGND.
11, 12	PSEL1, PSEL0	Phase Select Input. The AD9832 has four phase registers. These registers can be used to alter the value being input to the SIN ROM. The contents of the phase register are added to the phase accumulator output, the inputs PSEL0 and PSEL1 selecting the phase register to be used. Alternatively, the phase register to be used can be selected using the PSEL0 and PSEL1 bits. Like the FSELECT input, PSEL0 and PSEL1 are sampled on the rising MCLK edge. Therefore, these inputs need to be in steady state when an MCLK rising edge occurs or there is an uncertainty of one MCLK cycle as to when control is transferred to the selected phase register. When the phase registers are being controlled by the PSEL0 and PSEL1 bits, the pins should be tied to DGND.
13	AGND	Analog Ground.
14	IOUT	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND.
15	AVDD	Positive Power Supply for the Analog Section. A 0.1 µF decoupling capacitor should be connected between AVDD and AGND. AVDD can have a value of 5 V ± 10% or 3.3 V ± 10%.
16	COMP	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 10 nF decoupling ceramic capacitor should be connected between COMP and AVDD.

TYPICAL PERFORMANCE CHARACTERISTICS

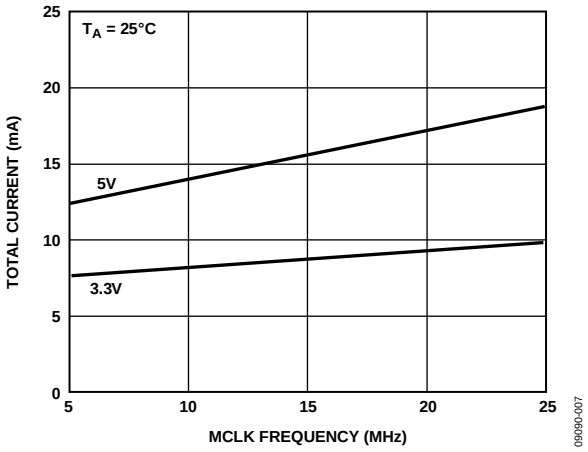


Figure 7. Typical Current Consumption vs. MCLK Frequency

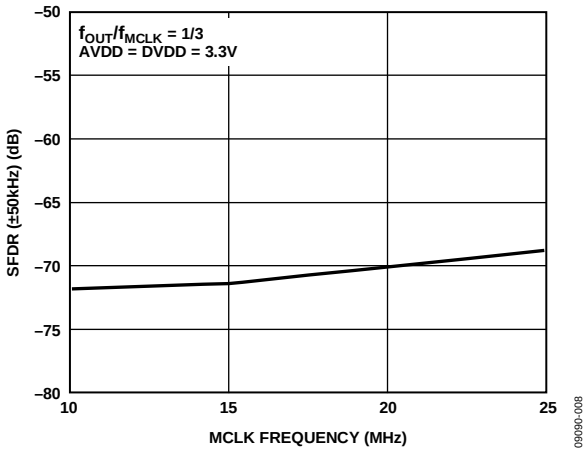


Figure 8. Narrow-Band SFDR vs. MCLK Frequency

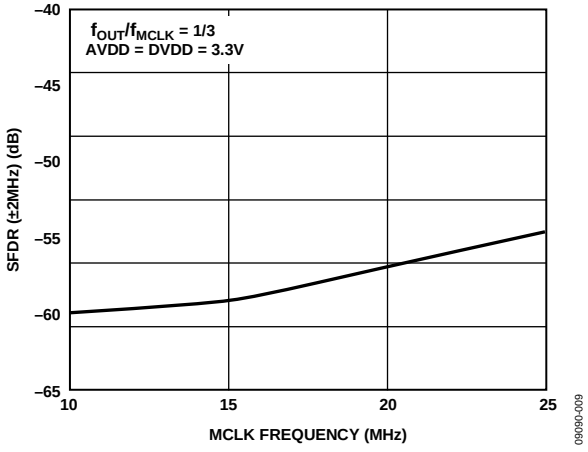


Figure 9. Wideband SFDR vs. MCLK Frequency

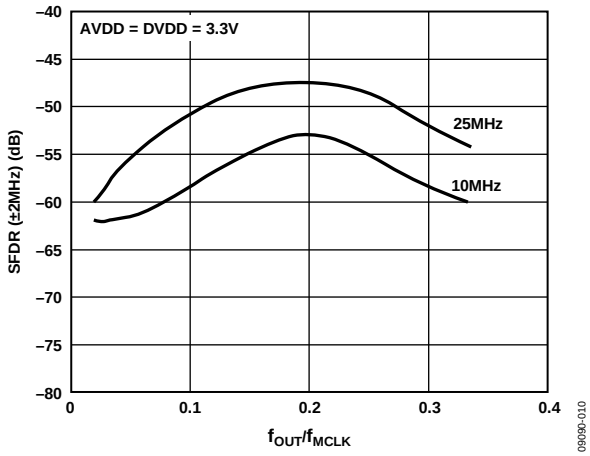


Figure 10. Wideband SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

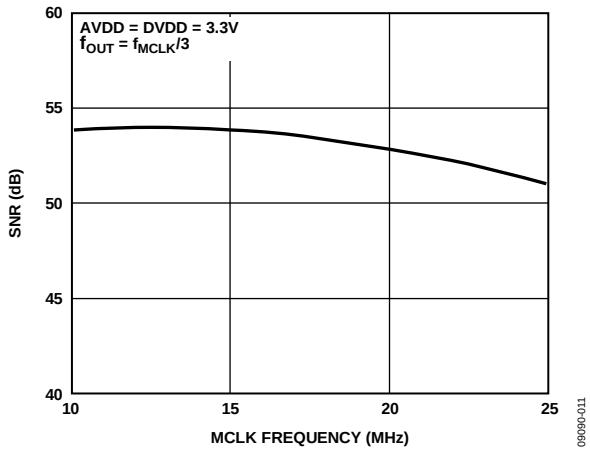


Figure 11. SNR vs. MCLK Frequency

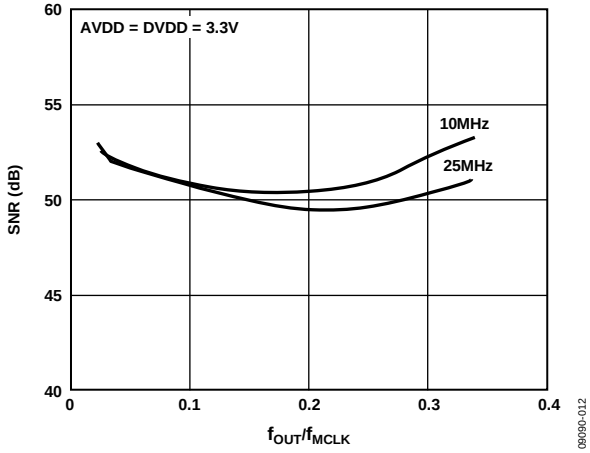


Figure 12. SNR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

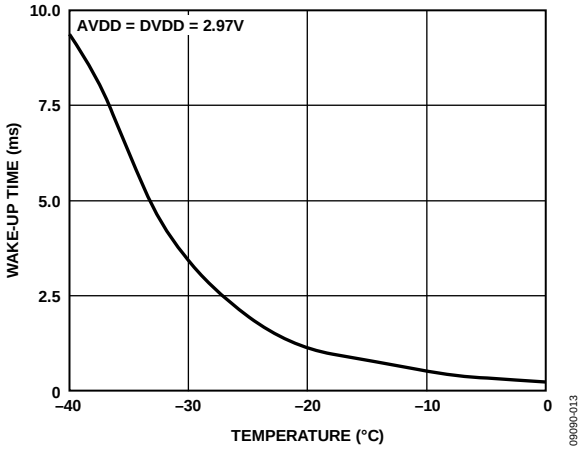


Figure 13. Wake-Up Time vs. Temperature

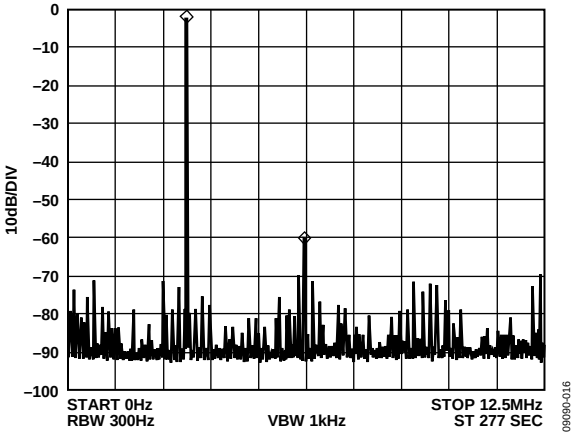


Figure 16. f_{MCLK} = 25 MHz, f_{OUT} = 3.1 MHz, Frequency Word = 0x1FBE76C9

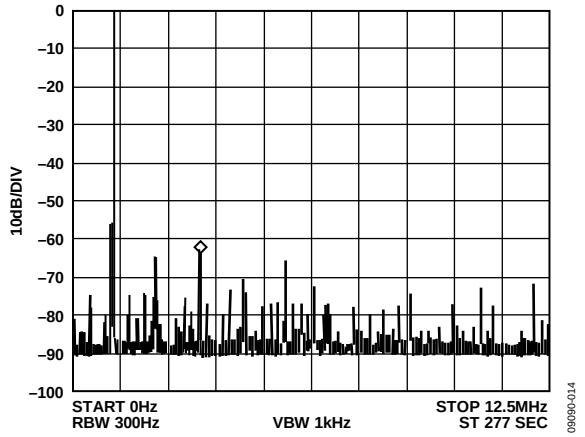


Figure 14. f_{MCLK} = 25 MHz, f_{OUT} = 1.1 MHz, Frequency Word = 0xB439581

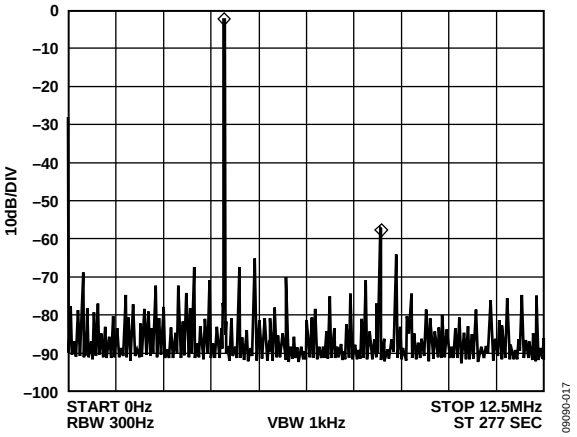


Figure 17. f_{MCLK} = 25 MHz, f_{OUT} = 4.1 MHz, Frequency Word = 0x29FBE76D

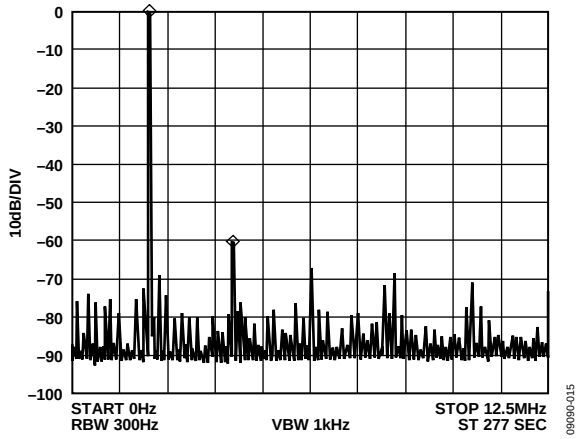


Figure 15. f_{MCLK} = 25 MHz, f_{OUT} = 2.1 MHz, Frequency Word = 0x15810625

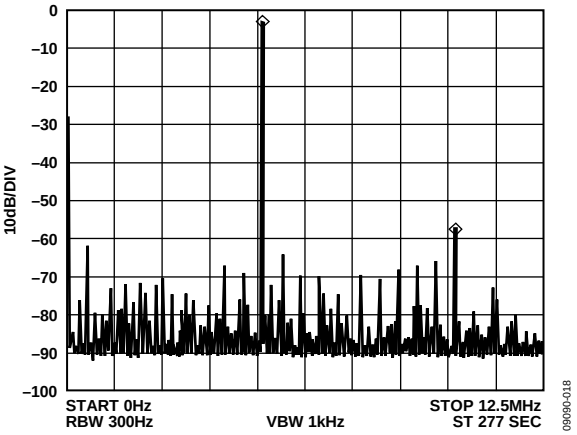


Figure 18. f_{MCLK} = 25 MHz, f_{OUT} = 5.1 MHz, Frequency Word = 0x34395810

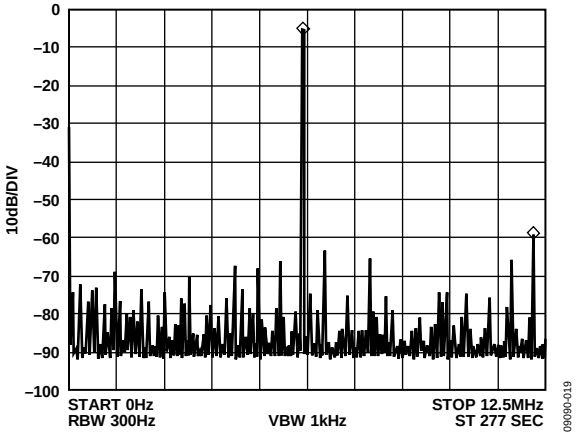


Figure 19. f_{MCLK} = 25 MHz, f_{OUT} = 6.1 MHz, Frequency Word = 0x3E76C8B4

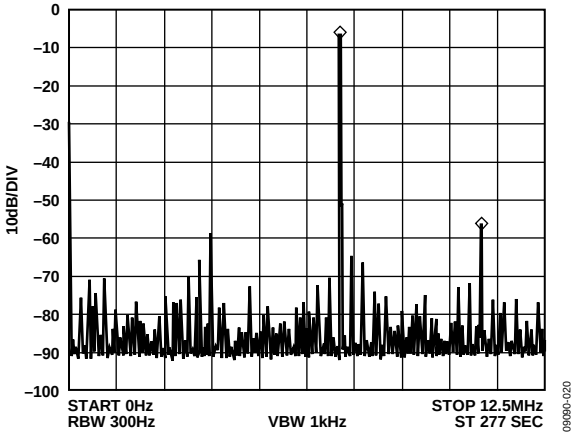


Figure 20. f_{MCLK} = 25 MHz, f_{OUT} = 7.1 MHz, Frequency Word = 0x48B43958

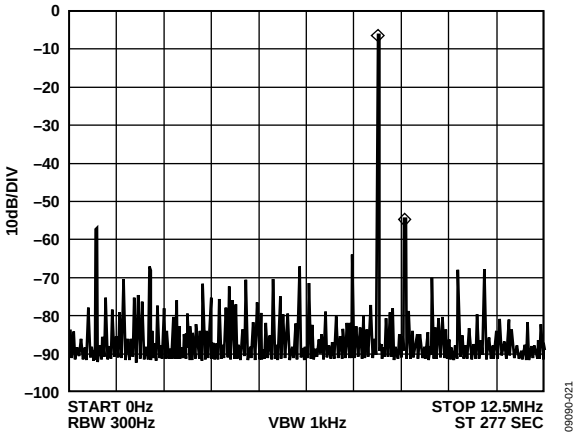


Figure 21. f_{MCLK} = 25 MHz, f_{OUT} = 8.1 MHz, Frequency Word = 0x52F1A9FC

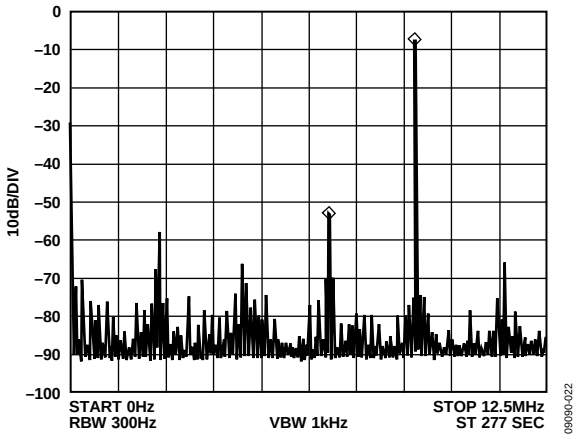


Figure 22. f_{MCLK} = 25 MHz, f_{OUT} = 9.1 MHz, Frequency Word = 0x5D2F1AA0

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC.

Signal-to-Noise-and-Distortion Ratio
It is measured signal to noise at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_{MCLK}/2$) but excluding the dc component. The signal-to-noise-and-distortion ratio is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise-and-distortion ratio for a sine wave input is

$$Signal\text{-}to\text{-}Noise\text{-}and\text{-}Distortion = (6.02N + 1.76)\ \text{dB}$$

where N is the number of bits. Thus, for an ideal 10-bit converter, the signal-to-noise-and-distortion ratio = 61.96 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9832, THD is defined as

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonic.

Output Compliance
The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than those specified for the output compliance are generated, the AD9832 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of the MCLK frequency are present at the output of a DDS device. SFDR refers to the largest spur or harmonic present in the band of interest. The wide-band SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the bandwidth ±2 MHz about the fundamental frequency. The narrowband SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±50 kHz about the fundamental frequency.

Clock Feedthrough
There is feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the output spectrum of the AD9832.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form a(t) = sin (ωt). However, these are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of ω = 2 πf.

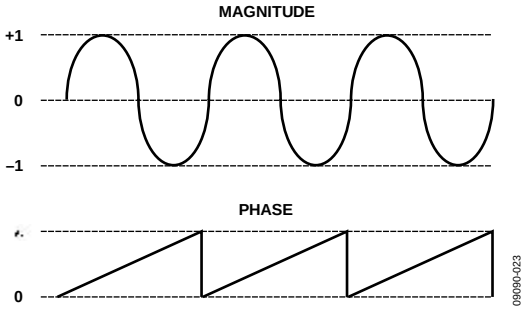


Figure 23. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined by

$$\Delta Phase = \omega\delta t$$

Solving for ω,

$$\omega = \Delta Phase/\delta t = 2\ \pi f$$

Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \delta t$),

$$f = \Delta Phase \times f_{MCLK}/2\ \pi$$

The AD9832 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits.

CIRCUIT DESCRIPTION

The AD9832 provides an exciting new level of integration for the RF/communications system designer. The AD9832 combines the numerical controlled oscillator (NCO), a sine look-up table, frequency and phase modulators, and a DAC on a single integrated circuit.

The internal circuitry of the AD9832 consists of three main sections. They are:

- Numerical controlled oscillator (NCO) and phase modulator
- Sine look-up table
- DAC

The AD9832 is a fully integrated direct digital synthesis (DDS) chip. The chip requires a reference clock, a low precision resistor, and eight decoupling capacitors to provide digitally created sine waves up to 12.5 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain, allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

NUMERICAL CONTROLLED OSCILLATOR AND PHASE MODULATOR

The NCO and phase modulator consists of two frequency select registers, a phase accumulator, and four phase offset registers. The main component of the NCO is a 32-bit phase accumulator that assembles the phase component of the output signal. Continuous time signals have a phase range of 0 to 2 π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9832 is implemented with 32 bits. Therefore, in the AD9832, $2\pi = 2^{32}$. Likewise, the ΔPhase term is scaled into this range of numbers $0 < \Delta Phase < 2^{32} - 1$.

$$f = \Delta Phase \times f_{MCLK}/2^{32}$$

where $0 < \Delta Phase < 2^{32}$.

The input to the phase accumulator (that is, the phase step) can be selected from either the FREQ0 register or the FREQ1 register and can be controlled by the FSELECT pin or the FSELECT bit. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASEx registers. The contents of these registers are added to the most significant bits of the NCO. The AD9832 has four PHASEx registers, the resolution of these registers being 2 π/4096.

SINE LOOK-UP TABLE (LUT)

To make the output useful, the signal must be converted from phase information into a sinusoidal value. Because phase information maps directly into amplitude, a ROM LUT converts the phase information into amplitude. To do this, the digital phase information is used to address a sine ROM LUT. Although the NCO contains a 32-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary because this would require a look-up table of 2^{32} entries.

It is only necessary to have sufficient phase resolution in the LUTs so that the dc error of the output waveform is dominated by the quantization error in the DAC. This requires the look-up table to have two more bits of phase resolution than the 10-bit DAC.

DIGITAL-TO-ANALOG CONVERTER

The AD9832 includes a high impedance current source 10-bit DAC, capable of driving a wide range of loads at different speeds. Full-scale output current can be adjusted for optimum power and external load requirements by using a single external resistor (R_{SET}).

The DAC is configured for single-ended operation. The load resistor can be any value required, as long as the full-scale voltage developed across it does not exceed the voltage compliance range. Because full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistor. However, if the DAC full-scale output current is significantly less than 4 mA, the linearity of the DAC may degrade.

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The AD9832 has a serial interface, with 16 bits being loaded during each write cycle. SCLK, SDATA, and FSYNC are used to load the word into the AD9832.

When FSYNC is taken low, the AD9832 is informed that a word is being written to the device. The first bit is read into the device on the next SCLK falling edge with the remaining bits being read into the device on the subsequent SCLK falling edges. FSYNC frames the 16 bits; therefore, when 16 SCLK falling edges have occurred, FSYNC should be taken high again. The SCLK can be continuous, or alternatively, the SCLK can idle high or low between write operations.

Table 5. Control Registers

Register	Size	Description
FREQ0 REG	32 bits	Frequency Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the MCLK frequency.
FREQ1 REG	32 bits	Frequency Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the MCLK frequency.
PHASE0 REG	12 bits	Phase Offset Register 0. When PSEL0 = PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1 REG	12 bits	Phase Offset Register 1. When PSEL0 = 1 and PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE2 REG	12 bits	Phase Offset Register 2. When PSEL0 = 0 and PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.
PHASE3 REG	12 bits	Phase Offset Register 3. When PSEL0 = PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.

When writing to a frequency/phase register, the first four bits identify whether a frequency or phase register is being written to, the next four bits contain the address of the destination register, while the 8 LSBs contain the data. Table 6 lists the addresses for the phase/frequency registers, and Table 7 and Table 8 list the data structure for each.

For an example on programming the AD9832, see the AN-621 application note, *Programming the AD9832/AD9835*, at www.analog.com.

Table 6. Addressing the Registers

A3	A2	A1	A0	Destination Register
0	0	0	0	FREQ0 REG 8 L LSBs
0	0	0	1	FREQ0 REG 8 H LSBs
0	0	1	0	FREQ0 REG 8 L MSBs
0	0	1	1	FREQ0 REG 8 H MSBs
0	1	0	0	FREQ1 REG 8 L LSBs
0	1	0	1	FREQ1 REG 8 H LSBs
0	1	1	0	FREQ1 REG 8 L MSBs
0	1	1	1	FREQ1 REG 8 H MSBs
1	0	0	0	PHASE0 REG 8 LSBs
1	0	0	1	PHASE0 REG 8 MSBs
1	0	1	0	PHASE1 REG 8 LSBs
1	0	1	1	PHASE1 REG 8 MSBs
1	1	0	0	PHASE2 REG 8 LSBs
1	1	0	1	PHASE2 REG 8 MSBs
1	1	1	0	PHASE3 REG 8 LSBs
1	1	1	1	PHASE3 REG 8 MSBs

Table 7. 32-Bit Frequency Word

16 MSBs		16 LSBs	
8 H MSBs	8 L MSBs	8 H LSBs	8 L LSBs

Table 8. 12-Bit Frequency Word

4 MSBs (The 4 MSBs of the 8-Bit Word Loaded = 0)	8 LSBs

DIRECT DATA TRANSFER AND DEFERRED DATA TRANSFER

Within the AD9832, 16-bit transfers are used when loading the destination frequency/phase register. There are two modes for loading a register, direct data transfer and a deferred data transfer. With a deferred data transfer, the 8-bit word is loaded into the defer register (8 LSBs or 8 MSBs). However, this data is not loaded into the 16-bit data register; therefore, the destination register is not updated. With a direct data transfer, the 8-bit word is loaded into the appropriate defer register (8 LSBs or 8 MSBs).

Immediately following the loading of the defer register, the contents of the complete defer register are loaded into the 16-bit data register and the destination register is loaded on the next MCLK rising edge. When a destination register is addressed, a deferred transfer is needed first followed by a direct transfer. When all 16 bits of the defer register contain relevant data, the destination register can then be updated using 8-bit loading rather than 16-bit loading, that is, direct data transfers can be used. For example, after a new 16-bit word has been loaded to a destination register, the defer register will also contain this word. If the next write instruction is to the same destination register, the user can use direct data transfers immediately.

When writing to a phase register, the 4 MSBs of the 16-bit word loaded into the data register should be zero (the phase registers are 12 bits wide).

To alter the entire contents of a frequency register, four write operations are needed. However, the 16 MSBs of a frequency word are contained in a separate register to the 16 LSBs. Therefore, the 16 MSBs of the frequency word can be altered independent of the 16 LSBs.

Table 9. Commands

C3	C2	C1	C0	Command
0	0	0	0	Write 16 phase bits (present 8 bits + 8 bits in the defer register) to selected PHASEx REG.
0	0	0	1	Write 8 phase bits to the defer register.
0	0	1	0	Write 16 frequency bits (present 8 bits + 8 bits in the defer register) to selected the FREQx REG.
0	0	1	1	Write 8 frequency bits to the defer register.
0	1	0	0	Bit D9 (PSEL0) and Bit D10 (PSEL1) are used to select the PHASEx REG when SELSRC = 1. When SELSRC = 0, the PHASEx REG is selected using the PSEL0 and PSEL1 pins.
0	1	0	1	Bit D11 is used to select the FREQx REG when SELSRC = 1. When SELSRC = 0, the FREQx REG is selected using the FSELECT pin.
0	1	1	0	To control the PSEL0, PSEL1, and FSELECT bits using only one write, this command is used. Bit D9 and Bit D10 are used to select the PHASEx REG, and Bit 11 is used to select the FREQx REG when SELSRC = 1. When SELSRC = 0, the PHASEx REG is selected using the PSEL0 and PSEL1 pins and the FREQx REG is selected using the FSELECT pin.
0	1	1	1	Reserved. It configures the AD9832 for test purposes.

The phase and frequency registers to be used are selected using the FSELECT, PSEL0, and PSEL1 pins, or the corresponding bits can be used. Bit SELSRC determines whether the bits or the pins are used. When SELSRC = 0, the pins are used, and when SELSRC = 1, the bits are used. When CLR is taken high, SELSRC is set to 0 so that the pins are the default source. Data transfers from the serial (defer) register to the 16-bit data register, and the FSELECT and PSEL registers, occur following the 16th falling SCLK edge.

Table 10. Controlling the AD9832

D15	D14	Command
1	0	Selects source of control for the PHASEx and FREQx registers and enables synchronization. Bit D13 is the SYNC bit. When this bit is high, reading of the FSELECT, PSEL0, and PSEL1 bits/ pins and the loading of the destination register with data is synchronized with the rising edge of MCLK. The latency is increased by 2 MCLK cycles when SYNC = 1. When SYNC = 0, the loading of the data and the sampling of FSELECT/PSEL0/PSEL1 occurs asynchronously. Bit D12 is the select source bit (SELSRC). When this bit equals 1, the PHASEx/FREQx REG is selected using the FSELECT, PSEL0, and PSEL1 bits. When SELSRC = 0, the PHASEx/FREQx REG is selected using the FSELECT, PSEL0, and PSEL1 pins.
1	1	SLEEP, RESET, and CLR (clear). D13 is the SLEEP bit. When this bit equals 1, the AD9832 is powered down, internal clocks are disabled, and the current sources and REFOUT of the DAC are turned off. When SLEEP = 0, the AD9832 is powered up. When RESET (D12) = 1, the phase accumulator is set to zero phase that corresponds to a full-scale output. When CLR (D11) = 1, SYNC and SELSRC are set to zero. CLR resets to 0 automatically.

Transfer of the data from the 16-bit data register to the destination register or from the FSELECT/PSEL register to the respective multiplexer occurs on the next MCLK rising edge. Because SCLK and MCLK are asynchronous, an MCLK rising edge may occur while the data bits are in a transitional state. This can cause a brief spurious DAC output if the register being written to is generating the DAC output. To avoid such spurious outputs, the AD9832 contains synchronizing circuitry.

When the SYNC bit is set to 1, the synchronizer is enabled and data transfers from the serial register (defer register) to the 16-bit data register, and the FSELECT/PSEL registers occur following a two-stage pipeline delay that is triggered on the MCLK falling edge. The pipeline delay ensures that the data is valid when the transfer occurs. Similarly, selection of the frequency/phase registers using the FSELECT/PSELx pins is synchronized with the MCLK rising edge when SYNC = 1. When SYNC = 0, the synchronizer is bypassed.

Selecting the frequency/phase registers using the pins is synchronized with MCLK internally also when SYNC = 1 to ensure that these inputs are valid at the MCLK rising edge. If times t_{11} and t_{11A} are met, then the inputs will be at steady state at the MCLK rising edge. However, if times t_{11} and t_{11A} are violated, the internal synchronizing circuitry will delay the instant at which the pins are sampled, ensuring that the inputs are valid at the sampling instant (see Figure 5).

Table 11. Writing to the AD9832 Data Registers

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C3	C2	C1	C0	A3	A2	A1	A0	MSB	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	LSB

[1] X = don't care.

Table 12. Setting SYNC and SELSRC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	SYNC	SELSRC	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]

[1] X = don't care.

Table 13. Power-Down, Resetting and Clearing the AD9832

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	SLEEP	RESET	CLR	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]

[1] X = don't care.

LATENCY

Associated with each operation is a latency. When inputs FSELECT/PSEL change value, there is a pipeline delay before control is transferred to the selected register; there is a pipeline delay before the analog output is controlled by the selected register. When times t_{11} and t_{11A} are met, PSEL0, PSEL1, and FSELECT have latencies of six MCLK cycles when SYNC = 0. When SYNC = 1, the latency is increased to 8 MCLK cycles. When times t_{11} and t_{11A} are not met, the latency can increase by one MCLK cycle. Similarly, there is a latency associated with each write operation. If a selected frequency/phase register is loaded with a new word, there is a delay of 6 to 7 MCLK cycles before the analog output will change (there is an uncertainty of one MCLK cycle regarding the MCLK rising edge at which the data is loaded into the destination register). When SYNC = 1, the latency is 8 or 9 MCLK cycles.

FLOWCHARTS

The flowchart in Figure 24 shows the operating routine for the AD9832. When the AD9832 is powered up, the part should be reset, which resets the phase accumulator to zero so that the analog output is at full scale. To avoid spurious DAC outputs while the AD9832 is being initialized, the RESET bit should be set to 1 until the part is ready to begin generating an output. Taking CLR high sets SYNC and SELSRC to 0 so that the FSELECT/PSELx pins are used to select the frequency/phase registers, and the synchronization circuitry is bypassed. A write operation is needed to the SYNC/SELSRC register to enable the synchronization circuitry or to change control to the FSELECT/PSEL bits. RESET does not reset the phase and frequency registers. These registers will contain invalid data and, therefore, should be set to a known value by the user. The RESET bit is then set to 0 to begin generating an output. A signal will appear at the DAC output 6 MCLK cycles after RESET is set to 0.

The analog output is $f_{MCLK}/2^{32} \times$ FREG, where FREG is the value loaded into the selected frequency register. This signal is phase shifted by the amount specified in the selected phase register ($2\pi/4096 \times$ PHASEx REG, where PHASEx REG is the value contained in the selected phase register).

Control of the frequency/phase registers can be interchanged from the pins to the bits.

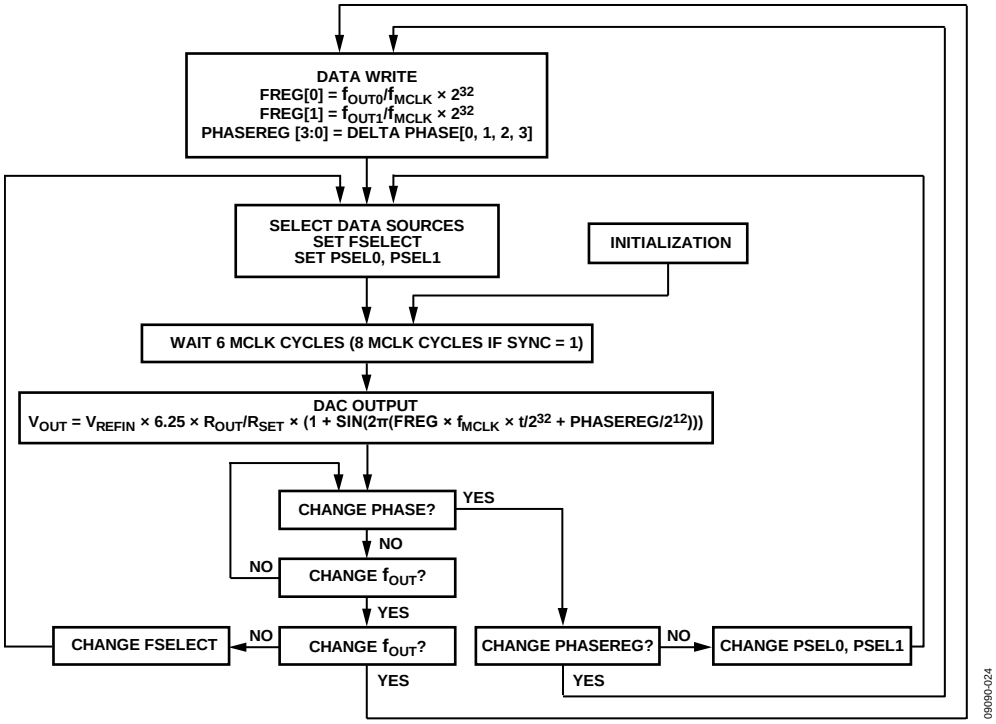


Figure 24. Flowchart for the AD9832 Initialization and Operation

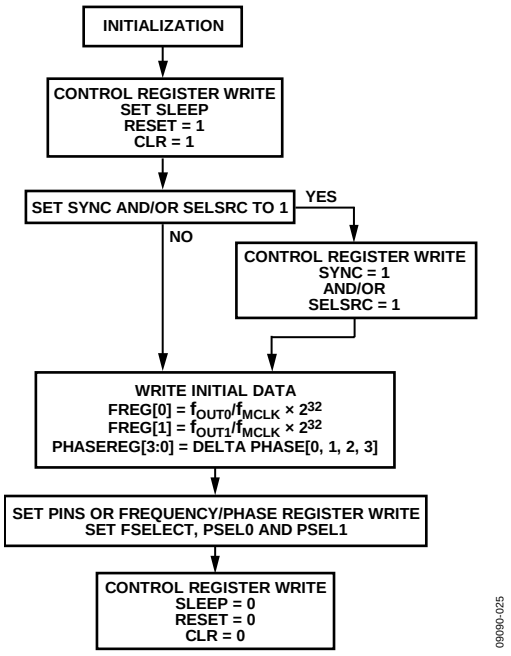


Figure 25. Initialization

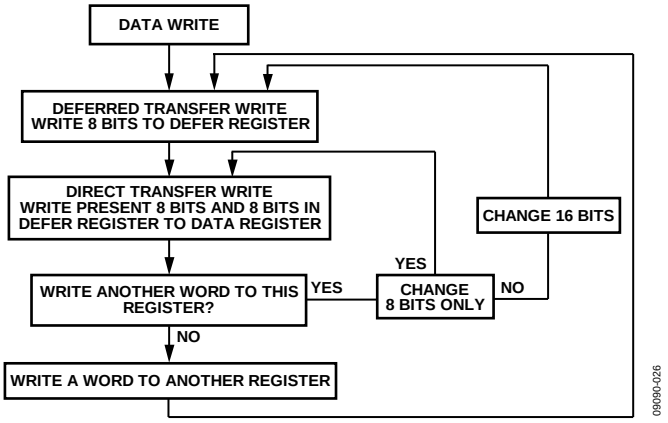


Figure 26. Data Writes

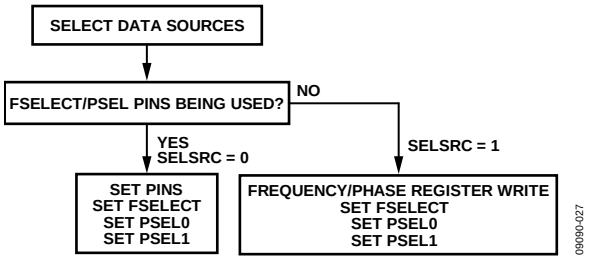


Figure 27. Selecting Data Sources

APPLICATIONS INFORMATION

The AD9832 contains functions that make it suitable for modulation applications. The part can be used to perform simple modulation, such as FSK, and more complex modulation schemes, such as GMSK and QPSK, can also be implemented using the AD9832. In an FSK application, the two frequency registers of the AD9832 are loaded with different values; one frequency represents the space frequency while the other represents the mark frequency. The digital data stream is fed to the FSELECT pin, which causes the AD9832 to modulate the carrier frequency between the two values.

The AD9832 has four phase registers; this enables the part to perform PSK. With phase shift keying, the carrier frequency is phase shifted, the phase being altered by an amount which is related to the bit stream being input to the modulator. The presence of four shift registers eases the interaction needed between the DSP and the AD9832.

The AD9832 is also suitable for signal generator applications. With its low current consumption, the part is suitable for applications where it can be used as a local oscillator. In addition, the part is fully specified for operation with a 3.3 V ± 10% power supply. Therefore, in portable applications where current consumption is an important issue, the AD9832 is perfect.

GROUNDING AND LAYOUT

The printed circuit board (PCB) that houses the AD9832 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD9832 is the only device requiring an AGND-to-DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD9832. If the AD9832 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9832.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD9832 to avoid noise coupling. The power supply lines to the AD9832 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, which reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD9832 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the AD9832, it is recommended that the AVDD supply of the system be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD9832 and AGND and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

INTERFACING THE AD9832 TO MICROPROCESSORS

The AD9832 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data/control information into the device. The serial clock can have a frequency of 20 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data/control information is being written to the AD9832, FSYNC is taken low and held low while the 16 bits of data are being written into the AD9832. The FSYNC signal frames the 16 bits of information being loaded into the AD9832.

AD9832 TO ADSP-2101 INTERFACE

Figure 28 shows the serial interface between the AD9832 and the ADSP-2101. The ADSP-2101 should be set up to operate in SPORT transmit alternate framing mode (TFSW = 1). The ADSP-2101 is programmed through the SPORT control register and should be configured as follows: internal clock operation (ISCLK = 1), active low framing (INVTFS = 1), 16-bit word length (SLEN = 15), internal frame sync signal (ITFS = 1), and a frame sync for each write operation (TFSR = 1) must be generated. Transmission is initiated by writing a word to the Tx register after SPORT is enabled. The data is clocked out on each rising edge of the serial clock and clocked into the AD9832 on the SCLK falling edge.

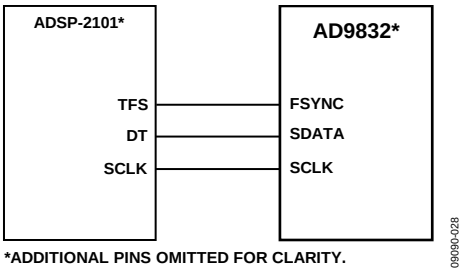


Figure 28. ADSP-2101 to AD9832 Interface

AD9832 TO 68HC11/68L11 INTERFACE

Figure 29 shows the serial interface between the AD9832 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting bit MSTR in the SPCR to 1, which provides a serial clock on SCK while the MOSI output drives the serial data line SDATA. Because the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows: SCK idles high between write operations (CPOL = 0), and data is valid on SCK falling edge (CPHA = 1). When data is transmitted to the AD9832, the FSYNC line is taken low (PC7). Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data into the AD9832, PC7 is held low after the first 8 bits are transferred and a second serial write operation is performed to the AD9832. Only after the second 8 bits have been transferred should FSYNC be taken high again.

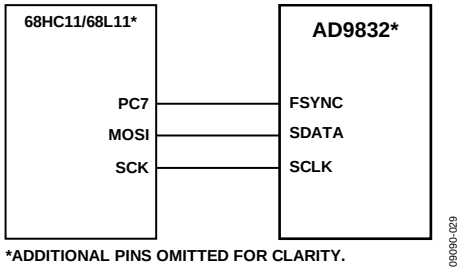


Figure 29. 68HC11/68L11 to AD9832 Interface

AD9832 TO 80C51/80L51 INTERFACE

Figure 30 shows the serial interface between the AD9832 and the 80C51/80L51 microcontroller. The microcontroller operates in Mode 0 so that TXD of the 80C51/80L51 drives SCLK of the AD9832, while RXD drives the serial data line SDATA. The FSYNC signal is again derived from a bit programmable pin on the port (P3.3 being used in the diagram). When data is transmitted to the AD9832, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes; therefore, only 8 falling SCLK edges occur in each cycle. To load the remaining 8 bits to the AD9832, P3.3 is held low after the first 8 bits have been transmitted and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations. The 80C51/80L51 outputs the serial data in a format that has LSB first. The AD9832 accepts MSB first (the 4 MSBs being the control information, the next 4 bits being the address, while the 8 LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must consider this format and rearrange the bits so that the MSB is output first.

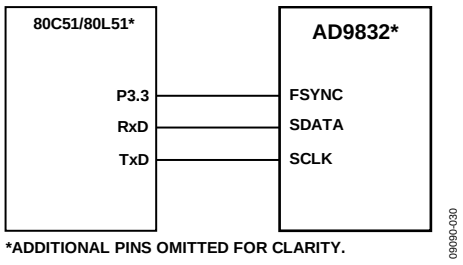


Figure 30. 80C51/80L51 to AD9832 Interface

AD9832 TO DSP56002 INTERFACE

Figure 31 shows the interface between the AD9832 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16-bits wide (WL1 = 1, WL0 = 0), and the frame sync signal frames the 16 bits (FSL = 0). The frame sync signal is available on Pin SC2, but it needs to be inverted before being applied to the AD9832. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

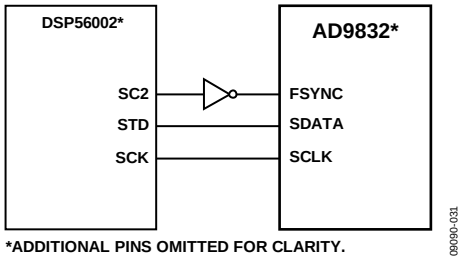


Figure 31. AD9832 to DSP56002 Interface

EVALUATION BOARD

SYSTEM DEMONSTRATION PLATFORM

The system demonstration platform (SDP) is a hardware and software evaluation tool for use in conjunction with product evaluation boards. The SDP board is based on the Blackfin® BF527 processor with USB connectivity to the PC through a USB 2.0 high speed port.

Note that the SDP board is sold separately from the AD9832 evaluation board.

AD9832 TO SPORT INTERFACE

The Analog Devices SDP board has a SPORT serial port that is used to control the serial inputs to the AD9832. The connections are shown in Figure 32.

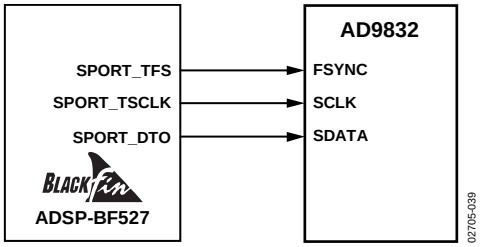


Figure 32. SDP to AD9832 Interface

The AD9832 evaluation board allows designers to evaluate the high performance AD9832 DDS modulator with a minimum of effort. The GUI interface for the AD9832 evaluation board is shown in Figure 33.

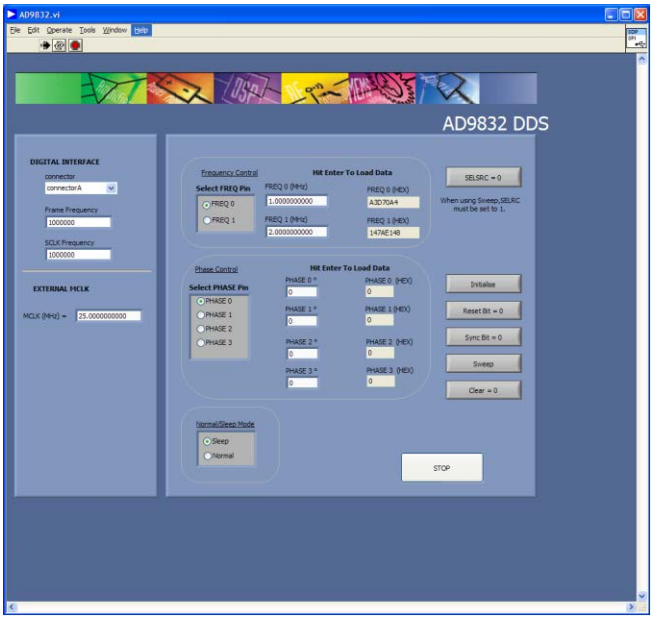


Figure 33. AD9832 Evaluation Software

The DDS evaluation kit includes a populated, tested AD9832 PCB. Software is available with the evaluation board that allows the user to easily program the AD9832. The schematics of the AD9832 evaluation board are shown in Figure 34 and Figure 35. The software runs on any IBM-compatible PC that has Microsoft® Windows® 95, Windows 98, Windows ME, Windows 2000 NT®, or Windows 7 installed.

Additional details can be found in the EVAL-AD9832SDZ data sheet that is available on the software CD and on the AD9832 product page.

XO vs. EXTERNAL CLOCK

The AD9832 can operate with master clocks up to 25 MHz. A 25 MHz general oscillator is included on the evaluation board. However, this oscillator can be removed and, if required, an external CMOS clock can be connected to the part.

Two options for the general oscillator are

- AEL 301 series crystals oscillators (AEL Crystals, Ltd.)
- SG-310SCN oscillators (Epson Toyocom Corporation)

POWER SUPPLY

Power to the AD9832 evaluation board can be provided from a USB connector or externally through pin connections. The power leads should be twisted to reduce ground loops.

EVALUATION BOARD SCHEMATICS

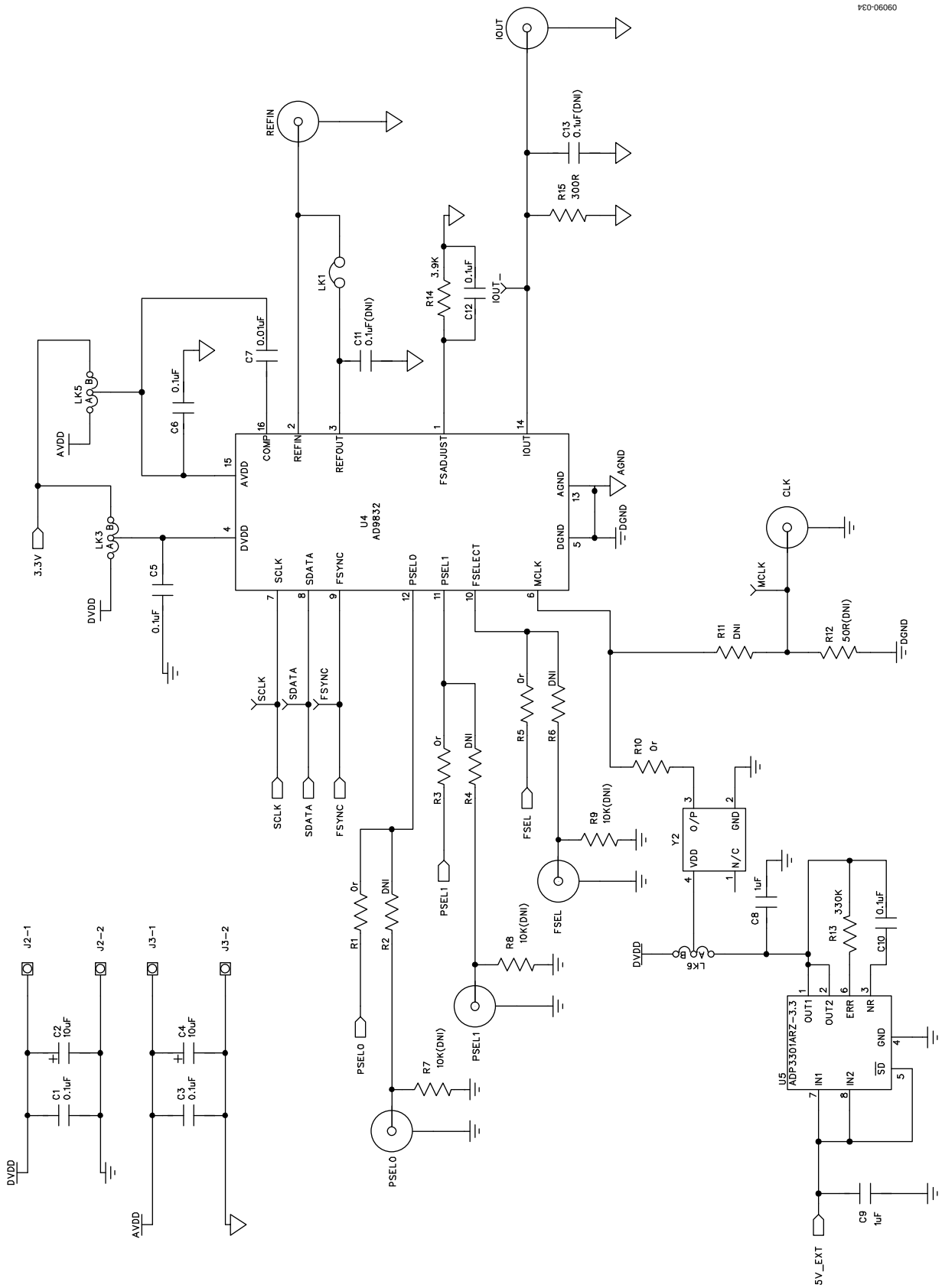


Figure 34. AD9832 Evaluation Board Schematic, Part A

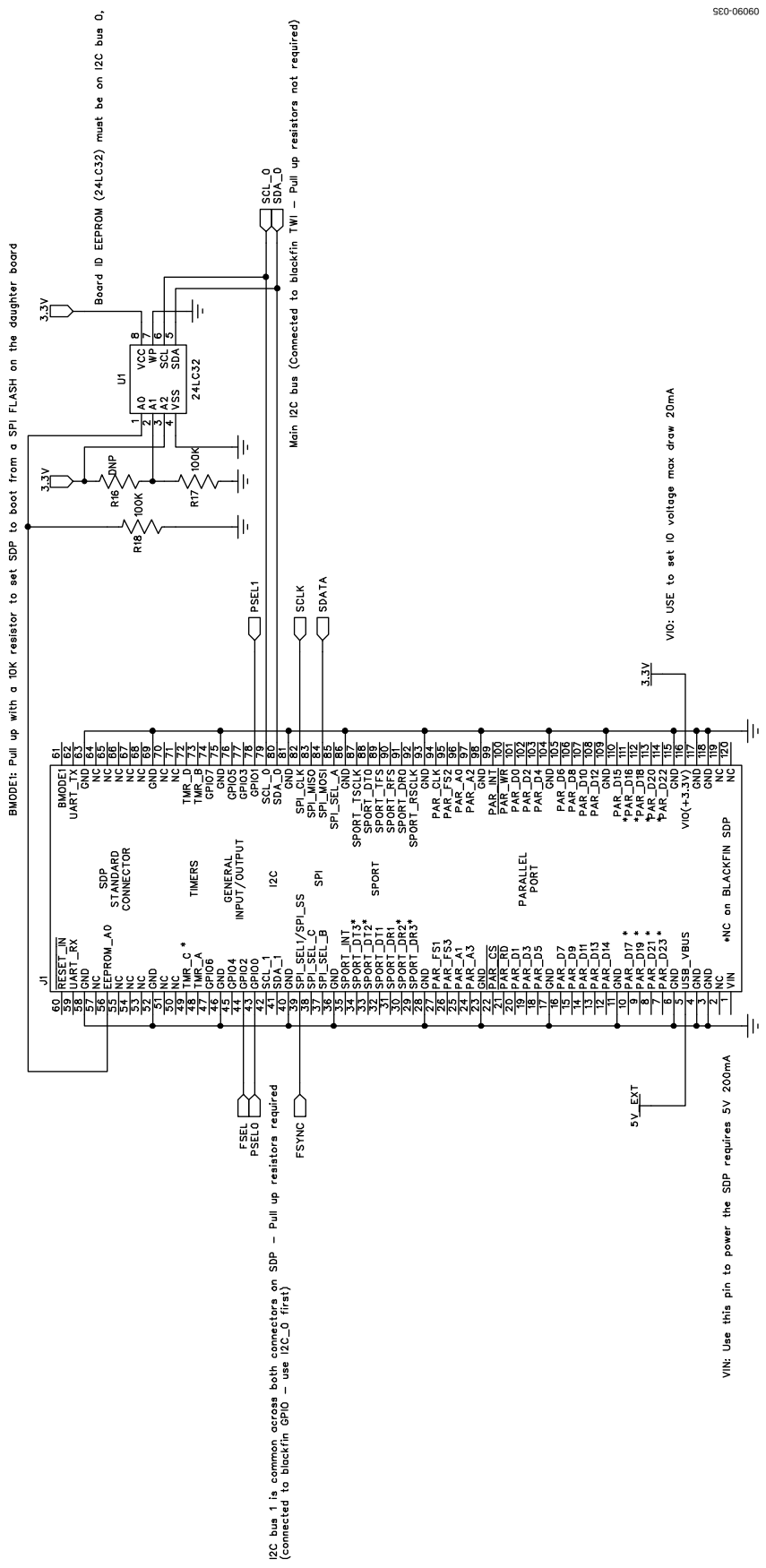


Figure 35. AD9832 Evaluation Board Schematic, Part B—J1 Header Connector

EVALUATION BOARD LAYOUT

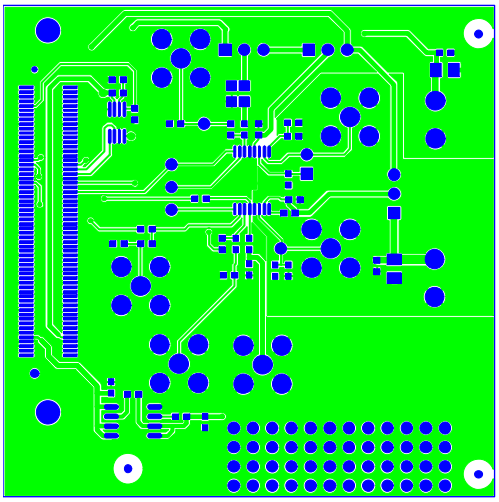


Figure 36. AD9832 Evaluation Board Component Side

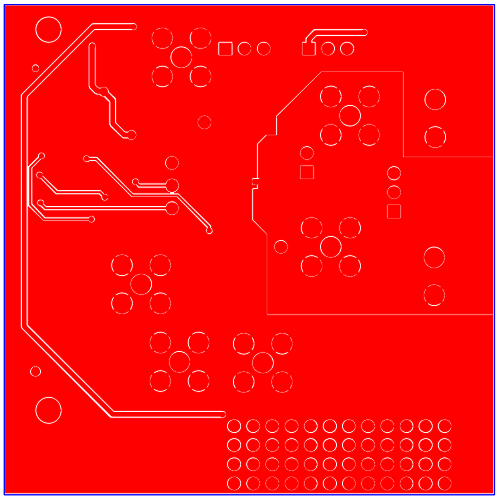


Figure 37. AD9832 Evaluation Board Silkscreen

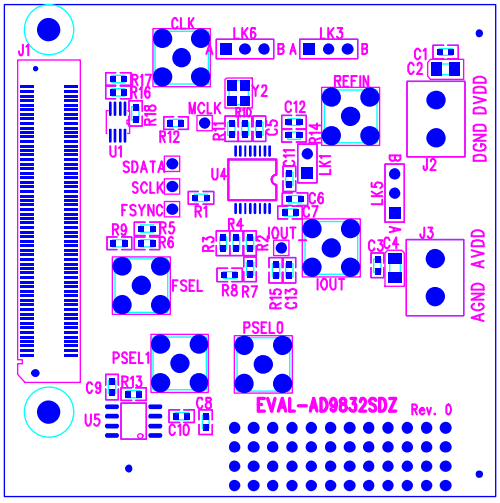


Figure 38. AD9832 Evaluation Board Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 14.

Reference Designator	Description	Manufacturer	Part Number
C1, C3, C5, C6, C11, C12, C13	0.1 µF, ±10%, 50 V, X7R, ceramic capacitor	Murata	GRM188R71H104KA93D
C7	0.01 µF, ±10%, 10 V, 0603, X5R, capacitor	Kemet	C0603C103K5RACTU
C2, C4	10 µF, ±10%,10 V, SMD tantalum capacitor	AVX	TAJA106K010R
C8,C9	1 µF, ±10%,10 V,Y5V, 0603, ceramic capacitor	Yageo	CC0603ZRY5V6BB105
C10	0.1 µF, ±10%, 16 V, X7R, 0603, capacitor	Multicomp	B0603R104KCT
CLK[1], FSEL[1], IOUT, PSEL1[1], REFIN, PSEL0[1]	Straight PCB mount SMB jack, 50 Ω	Tyco	1-1337482-0
FSYNC, IOUT_, MCLK , SCLK, SDATA	Red test point	Vero	20-313137
G2	Copper short	Not applicable	Not applicable
J1	120-way connector, 0.6 mm pitch receptacle	HRS (Hirose)	FX8-120S-SV(21)
J2, J3	2-pin terminal block (5 mm pitch)	Campden	CTB5000/2
LK3, LK5, LK6	3-pin SIL header and shorting link	Harwin	M20-9990345 and M7567-05
LK1	2-pin SIL header and shorting link	Harwin	M20-9990246
R7[1], R8[1], R9[1]	10 kΩ, ±1%, 0603, SMD resistor	Multicomp	MC 0.063W 0603 10K
R12[1]	50 Ω, ±1%, 0603, SMD resistor	Multicomp	MC 0.063W 0603 50r
R14	3.9 kΩ, ±1%, SMD resistor	Multicomp	MC 0.063W 0603 6K8
R15	300 Ω, ±1%, SMD resistor	Multicomp	MC 0.063W 0603 200r
R17,R18	100 KΩ, ±1%, SMD resistor	Multicomp	MC 0.063W 0603 1% 100K
R1, R2[1], R3, R4[1], R6[1], R5, R11[1], R10,R16[2]	0 Ω, ±1%, 0603, SMD resistor	Multicomp	MC 0.063W 0603 0r
R13	330 kΩ, ±5%, SMD resistor	Multicomp	MC 0.063W 0603 330KR
U4	45 mW power, 3 V to 5.5 V, 25 MHz complete DDS	Analog Devices	AD9832BRUZ
U1	32K I²C serial EEPROM 8-lead MSOP	Micro Chip	24LC32A-I/MS
U5	High accuracy anyCAP® 100 mA low dropout linear regulator	Analog Devices	ADP3301ARZ-3.3
Y2	25 MHz, 3 mm × 2 mm SMD clock oscillator	AEL Crystals	AEL301 series

[1] Do not install.
[2]DNP

OUTLINE DIMENSIONS

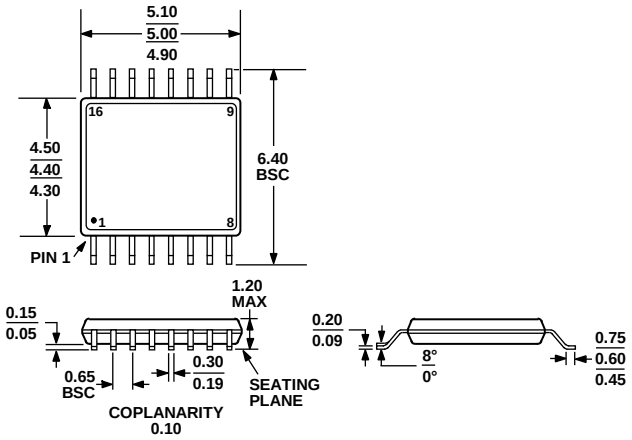


Figure 39. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9832BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD9832BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD9832BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD9832BRUZ-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD9832BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD9832SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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