Low Power, 8.5 mW, 2.3 V to 5.5 V, Programmable Waveform Generator

Data Sheet

AD9837

FEATURES

Digitally programmable frequency and phase
8.5 mW power consumption at 2.3 V
MCLK speed: 16 MHz (B grade), 5 MHz (A grade)
28-bit resolution: 0.06 Hz at 16 MHz reference clock
Sinusoidal, triangular, and square wave outputs
2.3 V to 5.5 V power supply
3-wire SPI interface
Extended temperature range: −40°C to +125°C
Power-down option
10-lead LFCSP

APPLICATIONS

Frequency stimulus/waveform generation
Liquid and gas flow measurement
Sensory applications: proximity, motion, and defect detection
Line loss/attenuation
Test and medical equipment
Sweep/clock generators
Time domain reflectometry (TDR) applications

GENERAL DESCRIPTION

The AD9837 is a low power, programmable waveform generator capable of producing sine, triangular, and square wave outputs. Waveform generation is required in various types of sensing, actuation, and time domain reflectometry (TDR) applications. The output frequency and phase are software programmable, allowing easy tuning. The frequency registers are 28 bits wide: with a 16 MHz clock rate, resolution of 0.06 Hz can be achieved; with a 5 MHz clock rate, the AD9837 can be tuned to 0.02 Hz resolution.

The AD9837 is written to via a 3-wire serial interface. This serial interface operates at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards. The device operates with a power supply from 2.3 V to 5.5 V.

The AD9837 has a power-down (sleep) function. Sections of the device that are not being used can be powered down to minimize the current consumption of the part. For example, the DAC can be powered down when a clock output is being generated.

The AD9837 is available in a 10-lead LFCSP_WD package.

FUNCTIONAL BLOCK DIAGRAM

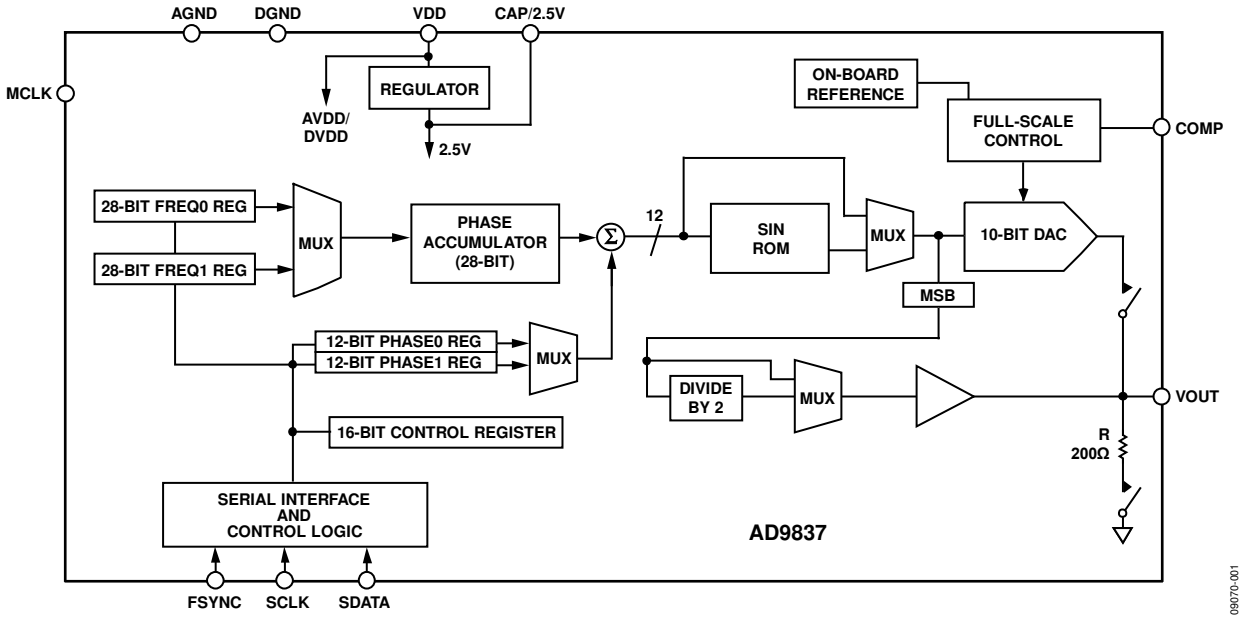


Figure 1.

Rev. A Document Feedback
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REVISION HISTORY

12/12—Rev. 0 to Rev. A

Changed Input Current, I_{INH}/I_{INL} from 10 mA to 10 μA ... 3
Updated Outline Dimensions ... 25

4/11—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate					
A Grade			5	MSPS	
B Grade			16	MSPS	
V_{OUT} Maximum		0.645		V	
V_{OUT} Minimum		37		mV	
V_{p-p}		0.610		V	
V_{OUT} TC		200		ppm/°C	
DC Accuracy					
Integral Nonlinearity (INL)		±1.0		LSB	
Differential Nonlinearity (DNL)		±0.5		LSB	
DDS SPECIFICATIONS					
Dynamic Specifications					
Signal-to-Noise Ratio (SNR)					
A Grade		−64		dB	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/4096$
B Grade		−64		dB	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
Total Harmonic Distortion (THD)					
A Grade		−68		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/4096$
B Grade		−68		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)					
A Grade		−65		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/50$
B Grade		−65		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/50$
Narrow-Band (±200 kHz)					
A Grade		−94		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/50$
B Grade		−97		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/50$
Clock Feedthrough		−67		dBc	
Wake-Up Time		1		ms	
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.7			V	2.3 V to 2.7 V power supply
	2.0			V	2.7 V to 3.6 V power supply
	2.8			V	4.5 V to 5.5 V power supply
Input Low Voltage, V_{INL}			0.5	V	2.3 V to 2.7 V power supply
			0.7	V	2.7 V to 3.6 V power supply
			0.8	V	4.5 V to 5.5 V power supply
Input Current, I_{INH}/I_{INL}			10	µA	
Input Capacitance, C_{IN}		3		pF	
POWER SUPPLIES					f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
VDD	2.3		5.5	V	
I_{DD}					
A Grade		3.7	5.0	mA	I_{DD} code dependent; see Figure 6
B Grade		4.5	5.5	mA	I_{DD} code dependent; see Figure 7
Low Power Sleep Mode		0.5	0.8	mA	DAC powered down (SLEEP1 and SLEEP12 bits = 11; see Table 15)

[1] Operating temperature range is −40°C to +125°C; typical specifications are at 25°C.

TIMING CHARACTERISTICS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	62.5	ns min	MCLK period (f_{MCLK} = 16 MHz)
t_2	25	ns min	MCLK high duration (f_{MCLK} = 16 MHz)
t_3	25	ns min	MCLK low duration (f_{MCLK} = 16 MHz)
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high duration
t_6	10	ns min	SCLK low duration
t_7	5	ns min	FSYNC to SCLK falling edge setup time
t_8	10	ns min	SCLK falling edge to FSYNC rising edge time
	$t_4 - 5$	ns max	
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	5	ns min	SCLK high to FSYNC falling edge setup time

[1] Guaranteed by design; not production tested.

Timing Diagrams

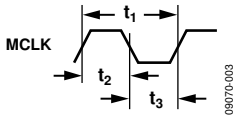


Figure 2. Master Clock

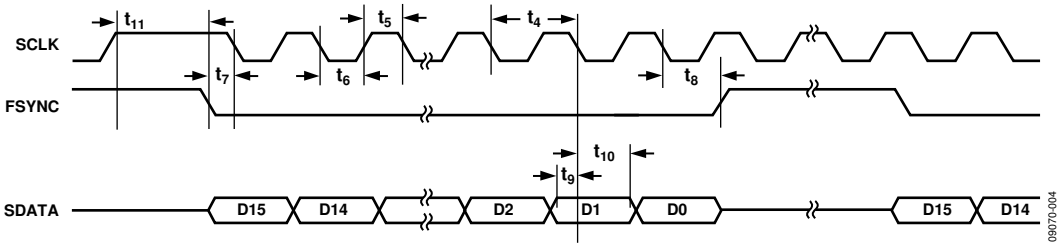


Figure 3. Serial Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to AGND	−0.3 V to +6 V
VDD to DGND	−0.3 V to +6 V
AGND to DGND	−0.3 V to +0.3 V
CAP/2.5V	2.75 V
Digital I/O Voltage to DGND	−0.3 V to VDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP_WD (CP-10-9)	206	44	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

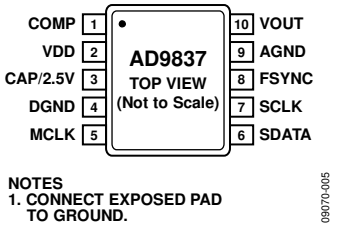


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage.
2	VDD	Positive Power Supply for the Analog and Digital Interface Sections. The on-board 2.5 V regulator is also supplied from VDD. VDD can have a value from 2.3 V to 5.5 V. A 0.1 µF and a 10 µF decoupling capacitor should be connected between VDD and AGND.
3	CAP/2.5V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from VDD using an on-board regulator when VDD exceeds 2.7 V. The regulator requires a decoupling capacitor of 100 nF typical, which is connected from CAP/2.5V to DGND. If VDD is less than or equal to 2.7 V, CAP/2.5V should be tied directly to VDD to bypass the on-board regulator.
4	DGND	Digital Ground.
5	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
6	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input.
7	SCLK	Serial Clock Input. Data is clocked into the AD9837 on each falling edge of SCLK.
8	FSYNC	Active Low Control Input. FSYNC is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
9	AGND	Analog Ground.
10	VOUT	Voltage Output. The analog and digital output from the AD9837 is available at this pin. An external load resistor is not required because the device has a 200 Ω resistor on board.
	EP	Exposed Pad. Connect the exposed pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

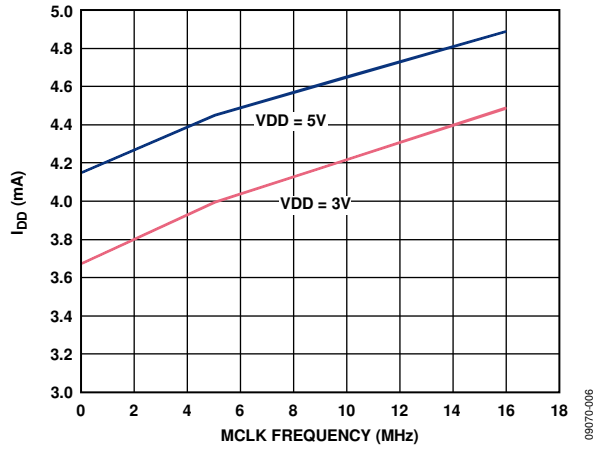


Figure 5. Typical Current Consumption (I_{DD}) vs. MCLK Frequency for f_{OUT} = MCLK/10

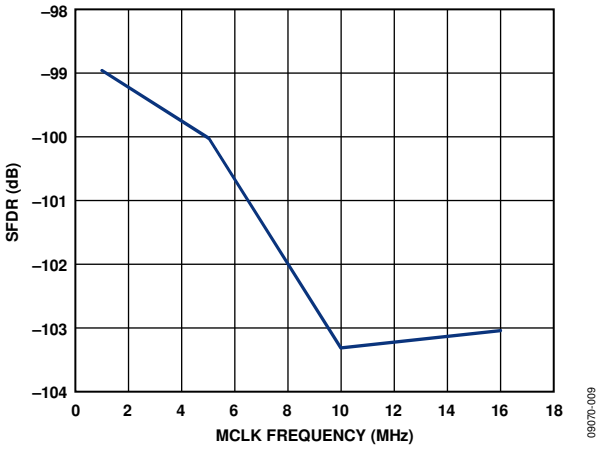


Figure 8. Narrow-Band SFDR vs. MCLK Frequency, f_{OUT} = MCLK/50 to ±200 kHz

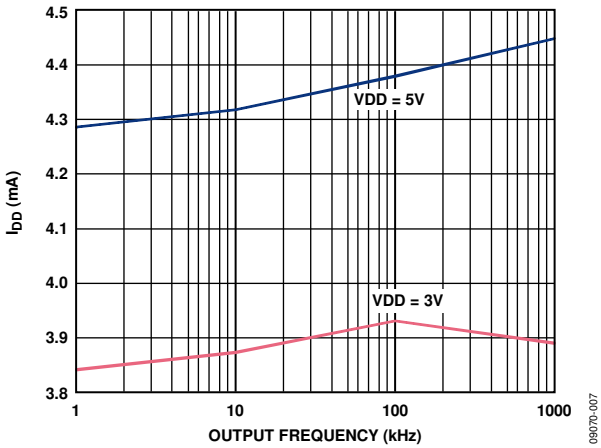


Figure 6. Typical I_{DD} vs. Output Frequency for f_{MCLK} = 5 MHz

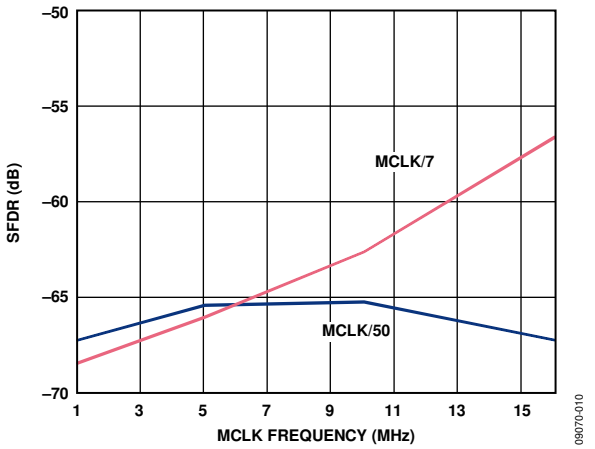


Figure 9. Wideband SFDR vs. MCLK Frequency

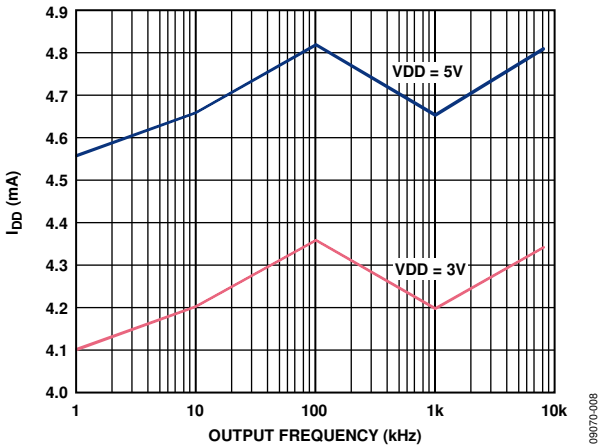


Figure 7. Typical I_{DD} vs. Output Frequency for f_{MCLK} = 16 MHz

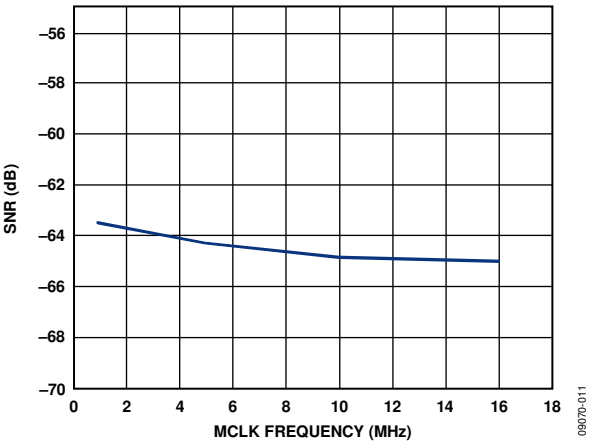


Figure 10. SNR vs. MCLK Frequency

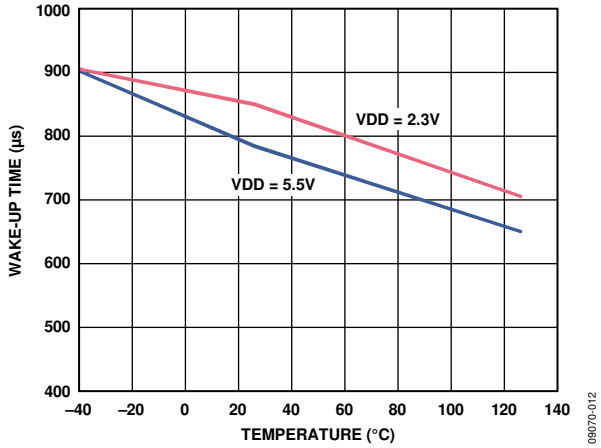


Figure 11. Wake-Up Time vs. Temperature

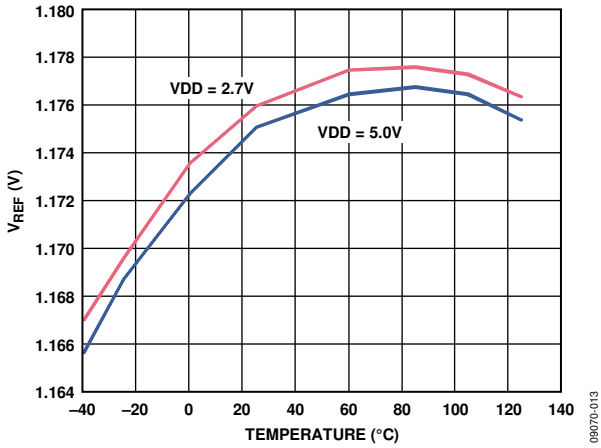


Figure 12. V_{REF} vs. Temperature

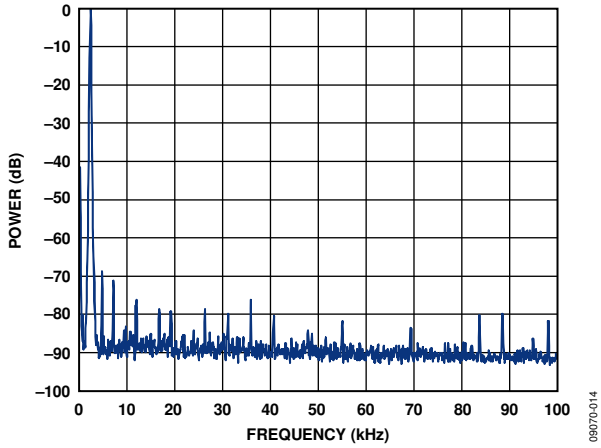


Figure 13. Power vs. Frequency, f_{MCLK} = 5 MHz, f_{OUT} = 2.4 kHz, Frequency Word = 0x1F751

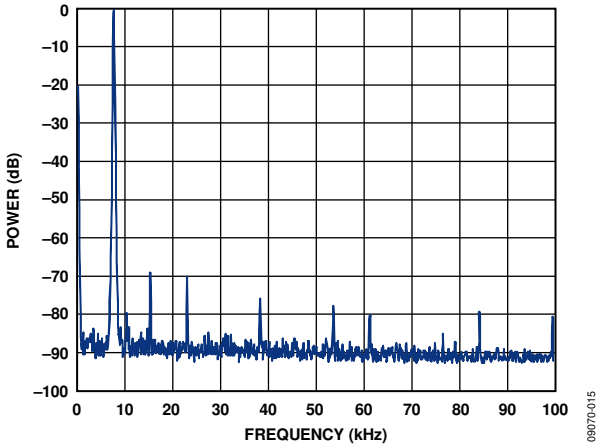


Figure 14. Power vs. Frequency, f_{MCLK} = 16 MHz, f_{OUT} = 7.692 kHz, Frequency Word = 0x1F81A

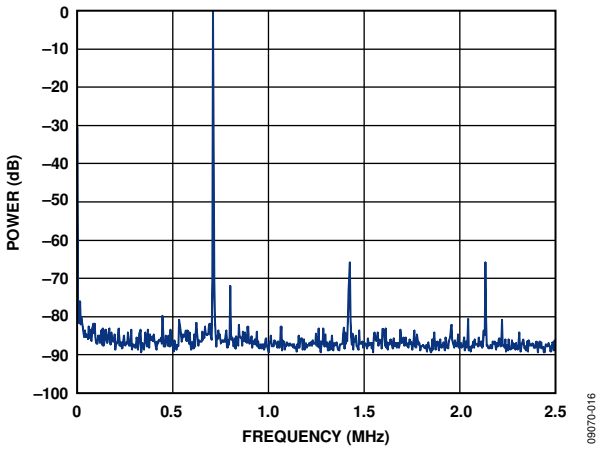


Figure 15. Power vs. Frequency, f_{MCLK} = 5 MHz, f_{OUT} = 0.714285 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

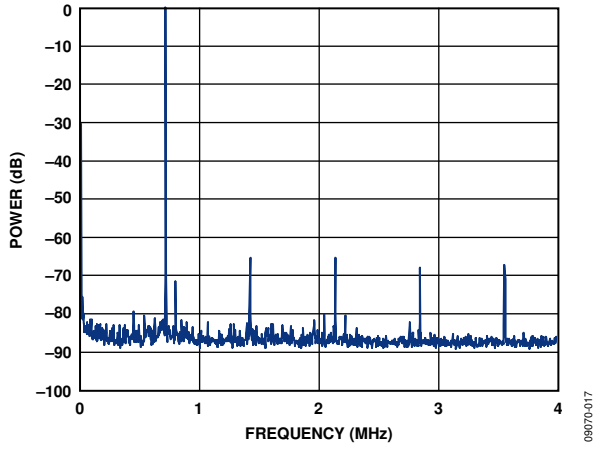


Figure 16. Power vs. Frequency, f_{MCLK} = 16 MHz, f_{OUT} = 2.285714 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

TEST CIRCUIT

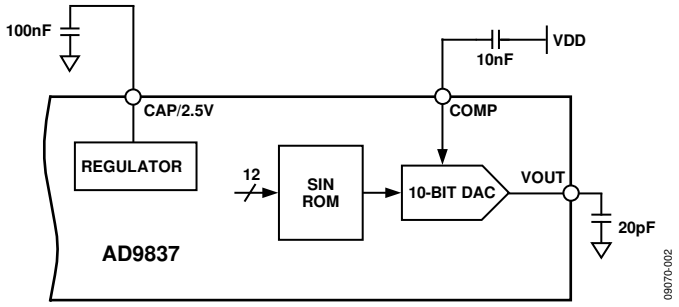


Figure 17. Test Circuit Used to Test Specifications

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 … 00 to 000 … 01), and full scale, a point 0.5 LSB above the last code transition (111 … 10 to 111 … 11). The error is expressed in LSBs.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified DNL of ±1 LSB maximum ensures monotonicity.

Output Compliance
Output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9837 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range (SFDR) refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest spur or harmonic relative to the magnitude of the fundamental frequency in the 0 to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion (THD)
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9837, THD is defined as

$$THD = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1}}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There is feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the output spectrum of the AD9837.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form: a(t) = sin(ωt). However, sine waves are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature; that is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

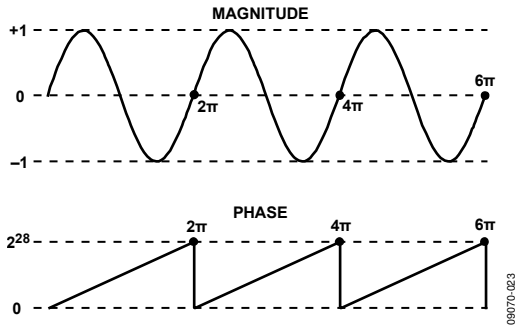


Figure 18. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined as follows:

$$\Delta Phase = \omega \Delta t \quad (1)$$

Solving for ω,

$$\omega = \Delta Phase/\Delta t = 2\pi f \quad (2)$$

Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \Delta t$),

$$f = \Delta Phase \times f_{MCLK}/2\pi \quad (3)$$

The AD9837 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits: numerically controlled oscillator (NCO) plus phase modulator, SIN ROM, and digital-to-analog converter (DAC). Each subcircuit is described in the Circuit Description section.

The AD9837 provides a sampled signal with its output following the Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental plus aliased signals (images) that occur at multiples of the reference clock frequency and the selected output frequency. A graphical representation of the sampled spectrum with aliased images is shown in Figure 19.

The prominence of the aliased images depends on the ratio of f_{OUT} to MCLK. If the ratio is small, the aliased images are very prominent and of a relatively high energy level as determined by the sin(x)/x roll-off of the quantized DAC output. In fact, depending on the f_{OUT}/reference clock ratio, the first aliased image can be on the order of −3 dB below the fundamental.

External filtering is required if the aliased image is within the output band of interest.

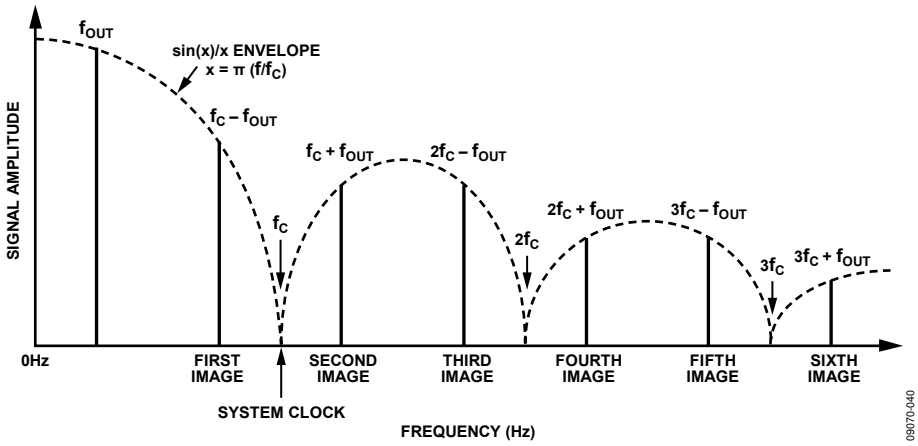


Figure 19. DAC Output Spectrum

CIRCUIT DESCRIPTION

The AD9837 is a fully integrated direct digital synthesis (DDS) chip. The chip requires a reference clock and decoupling capacitors to provide digitally created sine waves up to 8 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain, allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

The internal circuitry of the AD9837 consists of the following main sections: a numerically controlled oscillator (NCO), frequency and phase modulators, SIN ROM, a digital-to-analog converter, and a regulator.

NUMERICALLY CONTROLLED OSCILLATOR PLUS PHASE MODULATOR

The AD9837 consists of two frequency select registers, a phase accumulator, two phase offset registers, and a phase offset adder. The main component of the NCO is a 28-bit phase accumulator. Continuous time signals have a phase range of 0 to 2π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9837 is implemented with 28 bits. Therefore, in the AD9837, $2\pi = 2^{28}$. Likewise, the ΔPhase term is scaled into this range of numbers:

$$0 < \Delta Phase < 2^{28} - 1$$

With these substitutions, Equation 3 becomes

$$f = \Delta Phase \times f_{MCLK}/2^{28} \quad (4)$$

where $0 < \Delta Phase < 2^{28} - 1$.

The input to the phase accumulator can be selected from either the FREQ0 register or the FREQ1 register and is controlled by the FSEL bit in the control register. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit phase registers. The contents of one of these phase registers is added to the MSBs of the NCO. The AD9837 has two phase registers; their resolution is 2π/4096.

SIN ROM

To make the output from the NCO useful, it must be converted from phase information into a sinusoidal value. Because phase information maps directly to amplitude, the SIN ROM uses the digital phase information as an address to a lookup table and converts the phase information into amplitude.

Although the NCO contains a 28-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary because a lookup table of 2^{28} entries would be required. It is only necessary to have sufficient phase resolution such that the errors due to truncation are smaller than the resolution of the 10-bit DAC. Therefore, the SIN ROM must have two bits of phase resolution more than the 10-bit DAC.

The SIN ROM is enabled using the MODE bit (Bit D1) in the control register (see Table 16).

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD9837 includes a high impedance, current source, 10-bit DAC. The DAC receives the digital words from the SIN ROM and converts them into the corresponding analog voltages.

The DAC is configured for single-ended operation. An external load resistor is not required because the device has an on-board 200 Ω resistor. The DAC generates an output voltage of 0.6 V p-p typical.

REGULATOR

VDD provides the power supply required for the analog section and the digital section of the AD9837. This supply can have a value of 2.3 V to 5.5 V.

The internal digital section of the AD9837 is operated at 2.5 V. An on-board regulator steps down the voltage applied at VDD to 2.5 V. When the applied voltage at the VDD pin of the AD9837 is less than or equal to 2.7 V, the CAP/2.5V and VDD pins should be tied together to bypass the on-board regulator.

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The AD9837 has a standard 3-wire serial interface that is compatible with the SPI, QSPI™, MICROWIRE®, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 3.

FSYNC is a level triggered input that acts as a frame synchronization and chip enable input. Data can be transferred into the device only when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC to SCLK falling edge setup time, t_7 (see Table 2). After FSYNC goes low, serial data is shifted into the input shift register of the device on the falling edges of SCLK for 16 clock pulses. FSYNC can be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low; FSYNC goes high only after the 16th SCLK falling edge of the last word loaded.

The SCLK can be continuous, or it can idle high or low between write operations. In either case, it must be high when FSYNC goes low (t_{11}).

For an example of how to program the AD9837, see the AN-1070 Application Note on the Analog Devices, Inc., website. The AD9837 has the same register settings as the AD9833/AD9834.

LATENCY PERIOD

A latency period is associated with each asynchronous write operation in the AD9837. If a selected frequency or phase register is loaded with a new word, there is a delay of seven or eight MCLK cycles before the analog output changes. The delay can be seven or eight cycles, depending on the position of the MCLK rising edge when the data is loaded into the destination register.

CONTROL REGISTER

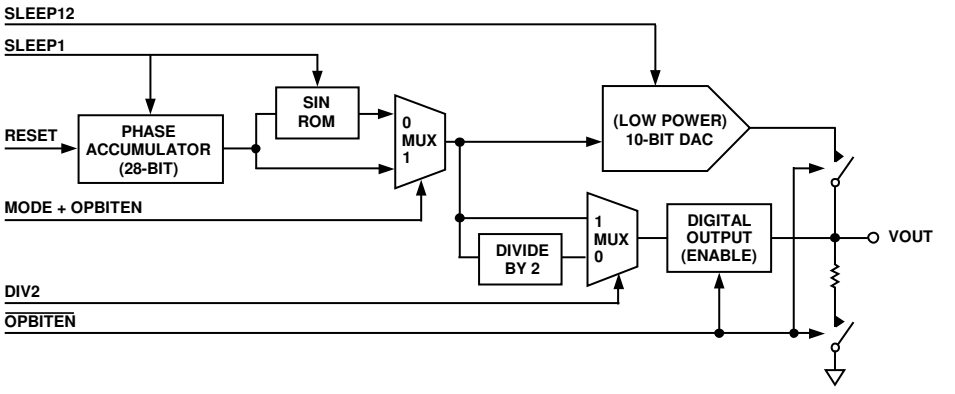
The AD9837 contains a 16-bit control register that allows the user to configure the operation of the AD9837. All control bits other than the MODE bit are sampled on the internal falling edge of MCLK.

Figure 20 illustrates the functions of the control bits. Table 7 describes the individual bits of the control register. The different functions and the various output options of the AD9837 are described in more detail in the following sections.

To inform the AD9837 that the contents of the control register will be altered, Bit D15 and Bit D14 must be set to 0, as shown in Table 6.

Table 6. Control Register Bits

D15	D14	D13 to D0
0	0	Control bits



D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	B28	HLB	FSEL	PSEL	0	RESET	SLEEP1	SLEEP12	OPBITEN	0	DIV2	0	MODE	0

Figure 20. Function of Control Bits

Table 7. Control Register Bit Descriptions

Bit	Bit Name	Description
D13	B28	Two write operations are required to load a complete word into either of the frequency registers. B28 = 1 allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 14 LSBs of the frequency word, and the second write contains the 14 MSBs. The first two bits of each 16-bit word define the frequency register to which the word is loaded and should, therefore, be the same for both consecutive writes. See Table 9 for the appropriate addresses. The write to the frequency register occurs after both words have been loaded, so the register never holds an intermediate value. An example of a complete 28-bit write is shown in Table 10. Note, however, that consecutive 28-bit writes to the same frequency register are not allowed; to execute consecutive 28-bit writes, you must alternate between the frequency registers. B28 = 0 configures the 28-bit frequency register to operate as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. In this way, the 14 MSBs of the frequency word can be altered independently of the 14 LSBs, and vice versa. To alter the 14 MSBs or the 14 LSBs, a single write is made to the appropriate frequency address. Bit D12 (HLB) informs the AD9837 whether the bits to be altered are the 14 MSBs or the 14 LSBs.
D12	HLB	This control bit allows the user to continuously load the MSBs or LSBs of a frequency register while ignoring the remaining 14 bits. This is useful if the complete 28-bit resolution is not required. The HLB bit is used in conjunction with the B28 bit (Bit D13). The HLB bit indicates whether the 14 bits to be loaded are transferred to the 14 MSBs or the 14 LSBs of the addressed frequency register. Bit D13 (B28) must be set to 0 to change the MSBs or LSBs of a frequency word separately. When Bit D13 (B28) is set to 1, the HLB bit is ignored. HLB = 1 allows a write to the 14 MSBs of the addressed frequency register. HLB = 0 allows a write to the 14 LSBs of the addressed frequency register.
D11	FSEL	The FSEL bit defines whether the FREQ0 register or the FREQ1 register is used in the phase accumulator (see Table 8).
D10	PSEL	The PSEL bit defines whether the PHASE0 register data or the PHASE1 register data is added to the output of the phase accumulator (see Table 8).
D9	Reserved	This bit should be set to 0.
D8	RESET	This bit controls the reset function. RESET = 1 resets internal registers to 0, which corresponds to an analog output of midscale. RESET = 0 disables the reset function (see the Reset Function section).
D7	SLEEP1	This bit enables or disables the internal MCLK. SLEEP1 = 1 disables the internal MCLK. The DAC output remains at its present value because the NCO is no longer accumulating. SLEEP1 = 0 enables the internal MCLK (see the Sleep Function section).
D6	SLEEP12	This bit powers down the on-chip DAC. SLEEP12 = 1 powers down the on-chip DAC. This is useful when the AD9837 is used to output the MSB of the DAC data. SLEEP12 = 0 implies that the DAC is active (see the Sleep Function section).
D5	OPBITEN	This bit, in association with the MODE bit (Bit D1), controls the output at the VOUT pin (see Table 16). OPBITEN = 1 causes the output of the DAC to no longer be available at the VOUT pin. Instead, the MSB (or MSB/2) of the DAC data is connected to the VOUT pin. This output is useful as a coarse clock source. The DIV2 bit (Bit D3) controls whether the VOUT pin outputs the MSB or the MSB/2. OPBITEN = 0 connects the output of the DAC to VOUT. The MODE bit (Bit D1) determines whether the output is sinusoidal or triangular.
D4	Reserved	This bit must be set to 0.
D3	DIV2	DIV2 is used in association with Bit D5 (OPBITEN). See Table 16. DIV2 = 1 causes the MSB of the DAC data to be output at the VOUT pin. DIV2 = 0 causes the MSB/2 of the DAC data to be output at the VOUT pin.
D2	Reserved	This bit must be set to 0.
D1	MODE	This bit, in association with the OPBITEN bit (Bit D5), controls the output at the VOUT pin when the on-chip DAC is connected to VOUT. This bit should be set to 0 if the OPBITEN bit is set to 1 (see Table 16). MODE = 1 bypasses the SIN ROM, resulting in a triangle output from the DAC. MODE = 0 uses the SIN ROM to convert the phase information into amplitude information, resulting in a sinusoidal signal at the output. (The OPBITEN bit (Bit D5) must also be set to 0 for sinusoidal output.)
D0	Reserved	This bit must be set to 0.

FREQUENCY AND PHASE REGISTERS

The AD9837 contains two frequency registers and two phase registers, which are described in Table 8.

Table 8. Frequency and Phase Registers

Register	Size	Description
FREQ0	28 bits	Frequency Register 0. When the FSEL bit = 0, the FREQ0 register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 bits	Frequency Register 1. When the FSEL bit = 1, the FREQ1 register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 bits	Phase Offset Register 0. When the PSEL bit = 0, the contents of the PHASE0 register are added to the output of the phase accumulator.
PHASE1	12 bits	Phase Offset Register 1. When the PSEL bit = 1, the contents of the PHASE1 register are added to the output of the phase accumulator.

The analog output from the AD9837 is

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency register.

This signal is phase shifted by

$$2\pi/4096 \times PHASEREG$$

where *PHASEREG* is the value contained in the selected phase register.

The relationship of the selected output frequency and the reference clock frequency must be considered to avoid unwanted output anomalies.

The flowchart in Figure 24 shows the routine for writing to the frequency and phase registers of the AD9837.

Writing to a Frequency Register

When writing to a frequency register, Bit D15 and Bit D14 of the control register give the address of the frequency register (see Table 9).

Table 9. Frequency Register Bits

D15	D14	D13 to D0
0	1	14 FREQ0 register bits
1	0	14 FREQ1 register bits

To change the entire contents of a frequency register, two consecutive writes to the same address must be performed because the frequency registers are 28 bits wide. The first write contains the 14 LSBs, and the second write contains the 14 MSBs. For this mode of operation, the B28 control bit (Bit D13) must be set to 1. An example of a 28-bit write is shown in Table 10.

Table 10. Writing 0xFFFC000 to the FREQ0 Register

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 register write (D15, D14 = 01), 14 LSBs = 0x0000
0111 1111 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x3FFF

Note, however, that continuous writes to the same frequency register may result in intermediate updates during the writes. If a frequency sweep, or something similar, is required, it is recommended that users alternate between the two frequency registers.

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered; with fine tuning, only the 14 LSBs are altered. By setting the B28 control bit (Bit D13) to 0, the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. In this way, the 14 MSBs of the frequency word can be altered independently of the 14 LSBs, and vice versa. The HLB bit (Bit D12) in the control register identifies which 14 bits are being altered (see Table 11 and Table 12).

Table 11. Writing 0x3FFF to the 14 LSBs of the FREQ1 Register

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 0, that is, LSBs
1011 1111 1111 1111	FREQ1 register write (D15, D14 = 10), 14 LSBs = 0x3FFF

Table 12. Writing 0x00FF to the 14 MSBs of the FREQ0 Register

SDATA Input	Result of Input Word
0001 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 1, that is, MSBs
0100 0000 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x00FF

Writing to a Phase Register

When writing to a phase register, Bit D15 and Bit D14 are set to 11. Bit D13 identifies the phase register that is being loaded.

Table 13. Phase Register Bits

D15	D14	D13	D12	D11 to D0
1	1	0	X	12 PHASE0 register bits
1	1	1	X	12 PHASE1 register bits

RESET FUNCTION

The reset function resets the appropriate internal registers to 0 to provide an analog output of midscale. A reset does not reset the phase, frequency, or control registers. When the AD9837 is powered up, the part should be reset (see the Powering Up the AD9837 section). To reset the AD9837, set the RESET bit to 1. To take the part out of reset, set the bit to 0. A signal appears at the DAC output seven or eight MCLK cycles after the RESET bit is set to 0.

Table 14. Applying the Reset Function

RESET Bit	Result
0	No reset applied
1	Internal registers reset

SLEEP FUNCTION

Sections of the AD9837 that are not in use can be powered down to minimize power consumption by using the sleep function. The parts of the chip that can be powered down are the internal clock and the DAC. The bits required for the sleep function are shown in Table 15.

Table 15. Applying the Sleep Function

SLEEP1 Bit	SLEEP12 Bit	Result
0	0	No power-down
0	1	DAC powered down
1	0	Internal clock disabled
1	1	DAC powered down and internal clock disabled

DAC Powered Down

When the AD9837 is used to output the MSB of the DAC data only, the DAC is not required. The DAC can be powered down using the SLEEP12 bit to reduce power consumption.

Internal Clock Disabled

When the internal clock of the AD9837 is disabled, the DAC output remains at its present value because the NCO is no longer accumulating. New frequency, phase, and control words can be written to the part when the SLEEP1 control bit is active. Because the synchronizing clock (FSYNC) remains active, the selected frequency and phase registers can also be changed using the control bits. Setting the SLEEP1 bit to 0 enables the MCLK. Any changes made to the registers while SLEEP1 was active are observed at the output after a latency period (see the Latency Period section).

VOUT PIN

The AD9837 offers a variety of outputs from the chip, all of which are available from the VOUT pin. The available outputs are the MSB of the DAC data, a sinusoidal output, or a triangle output.

The OPBITEN and MODE bits (Bit D5 and Bit D1 in the control register) are used to determine the output that is available from the AD9837 (see Table 16).

Table 16. Outputs from the VOUT Pin

OPBITEN Bit	MODE Bit	DIV2 Bit	VOUT Pin Output
0	0	X	Sinusoid
0	1	X	Triangle
1	0	0	DAC data MSB/2
1	0	1	DAC data MSB
1	1	X	Reserved

MSB of the DAC Data

The MSB of the DAC data can be output from the AD9837. By setting the OPBITEN bit (Bit D5) to 1, the MSB of the DAC data is available at the VOUT pin. This is useful as a coarse clock source. This square wave can also be divided by 2 before being output. The DIV2 bit (Bit D3) in the control register controls the frequency of this output from the VOUT pin.

Sinusoidal Output

The SIN ROM converts the phase information from the frequency and phase registers into amplitude information, resulting in a sinusoidal signal at the output. To obtain a sinusoidal output from the VOUT pin, set the MODE bit (Bit D1) to 0 and the OPBITEN bit (Bit D5) to 0.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC produces a 10-bit linear triangular function (see Figure 21). To obtain a triangle output from the VOUT pin, set the MODE bit (Bit D1) to 1 and the OPBITEN bit (Bit D5) to 0.

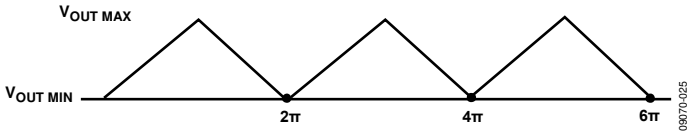


Figure 21. Triangle Output

POWERING UP THE AD9837

The flowchart in Figure 22 shows the operating routine for the AD9837. When the AD9837 is powered up, the part should be reset. This resets the appropriate internal registers to 0 to provide an analog output of midscale. To avoid spurious DAC outputs during AD9837 initialization, the RESET bit should be set to 1 until the part is ready to begin generating an output.

A reset does not reset the phase, frequency, or control registers. These registers will contain invalid data and, therefore, should be set to known values by the user. The RESET bit should then be set to 0 to begin generating an output. The data appears on the DAC output seven or eight MCLK cycles after the RESET bit is set to 0.

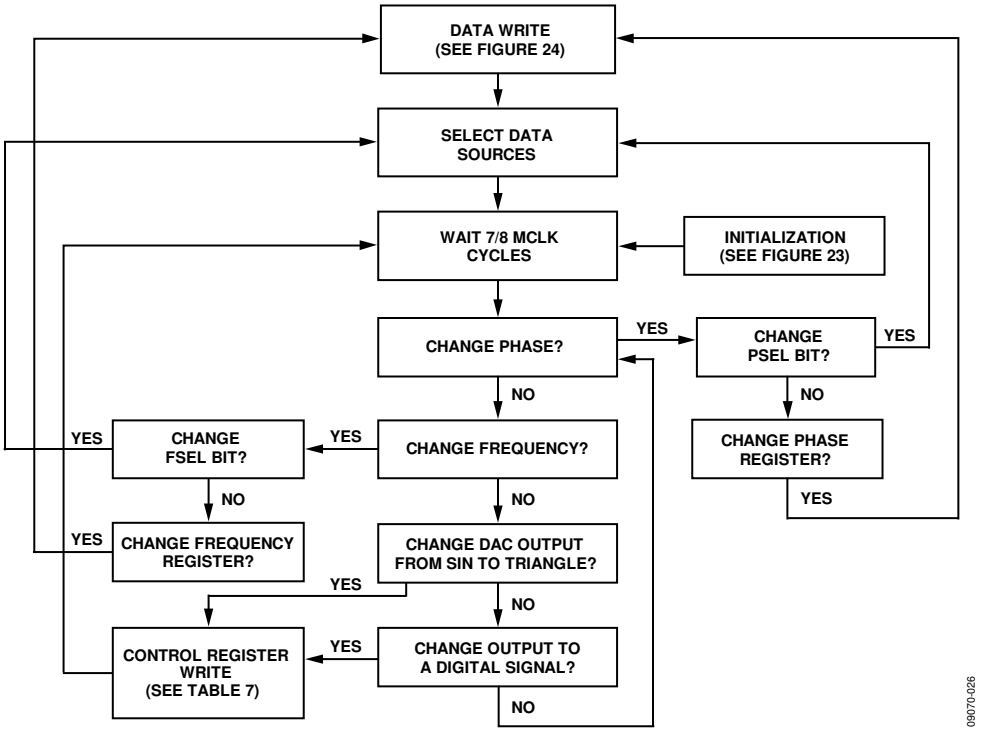


Figure 22. Flowchart for AD9837 Initialization and Operation

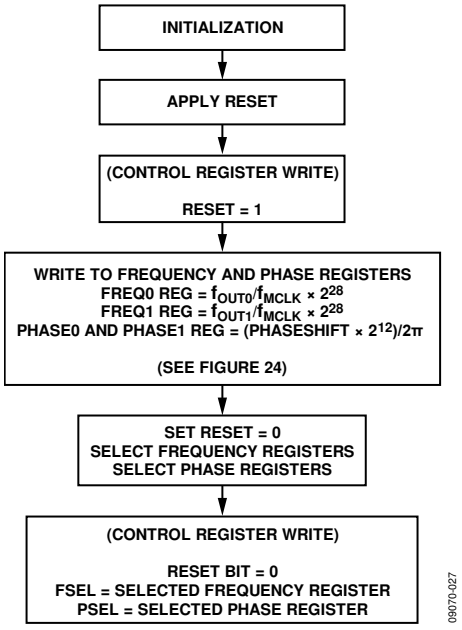


Figure 23. Flowchart for Initialization

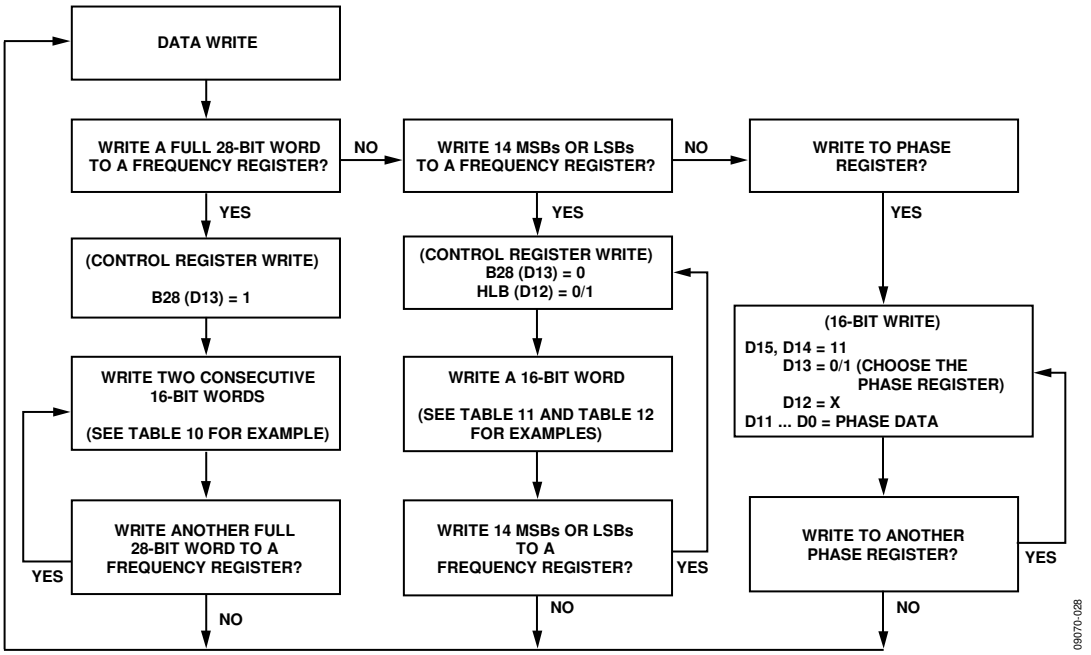


Figure 24. Flowchart for Data Writes

APPLICATIONS INFORMATION

The various output options available from the AD9837 make the part suitable for a wide variety of applications, including modulation applications. The AD9837 can be used to perform simple modulation, such as frequency shift keying (FSK). More complex modulation schemes, such as Gaussian minimum shift keying (GMSK) and quadrature phase shift keying (QPSK), can also be implemented using the AD9837.

In an FSK application, the two frequency registers of the AD9837 are loaded with different values. One frequency represents the space frequency, and the other represents the mark frequency. Using the FSEL bit in the control register of the AD9837, the user can modulate the carrier frequency between the two values.

The AD9837 has two phase registers, enabling the part to perform phase shift keying (PSK). With PSK, the carrier frequency is phase shifted, that is, the phase is altered by an amount that is related to the bit stream input to the modulator.

The AD9837 is also suitable for signal generator applications. Because the MSB of the DAC data is available at the VOUT pin, the device can be used to generate a square wave.

With its low current consumption, the part is also suitable for applications in which it can be used as a local oscillator.

GROUNDING AND LAYOUT

The printed circuit board that houses the AD9837 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it provides the best shielding. Digital and analog ground planes should be joined in one place only. If the AD9837 is the only device that requires an AGND to DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD9837. If the AD9837 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9837.

Avoid running digital lines under the device; these lines couple noise onto the die. The analog ground plane should be allowed to run under the AD9837 to avoid noise coupling. The power supply lines to the AD9837 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes and signals are placed on the other side.

Good decoupling is important. The AD9837 should have supply bypassing of 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best performance from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device.

INTERFACING TO MICROPROCESSORS

The AD9837 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data or control information into the device. The serial clock can have a frequency of 40 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data or control information is written to the AD9837, FSYNC is taken low and is held low until the 16 bits of data are written into the AD9837. The FSYNC signal frames the 16 bits of information that are loaded into the AD9837.

AD9837 to 68HC11/68L11 Interface

Figure 25 shows the serial interface between the AD9837 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting the MSTR bit in the SPCR to 1. This setting provides a serial clock on SCK; the MOSI output drives the serial data line, SDATA. Because the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows:

- SCK idles high between write operations (CPOL = 0)
- Data is valid on the SCK falling edge (CPHA = 1)

When data is to be transmitted to the AD9837, the FSYNC line (PC7) is taken low. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data into the AD9837, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the AD9837. Only after the second eight bits are transferred should FSYNC be taken high again.

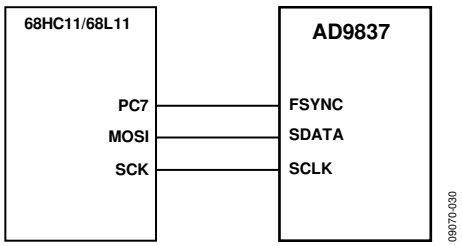


Figure 25. 68HC11/68L11 to AD9837 Interface

AD9837 to 80C51/80L51 Interface

Figure 26 shows the serial interface between the AD9837 and the 80C51/80L51 microcontroller. The microcontroller is operated in Mode 0 so that TxD of the 80C51/80L51 drives SCLK of the AD9837, and RxD drives the serial data line, SDATA. The FSYNC signal is derived from a bit programmable pin on the port (P3.3 is shown in Figure 26).

When data is to be transmitted to the AD9837, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes with only eight falling SCLK edges occurring in each cycle. To load the remaining eight bits to the AD9837, P3.3 is held low after the first eight bits are transmitted, and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations.

The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD9837 accepts the MSB first (the four MSBs are the control information, the next four bits are the address, and the eight LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

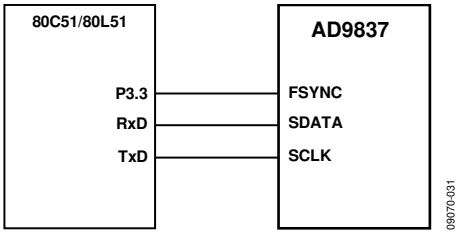


Figure 26. 80C51/80L51 to AD9837 Interface

AD9837 to DSP56002 Interface

Figure 27 shows the interface between the AD9837 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0), and the frame sync signal frames the 16 bits (FSL = 0). The frame sync signal is available on the SC2 pin, but it must be inverted before it is applied to the AD9837. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

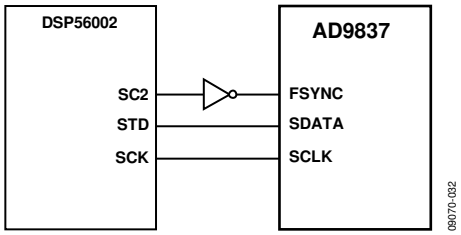


Figure 27. DSP56002 to AD9837 Interface

EVALUATION BOARD

The AD9837 evaluation board allows designers to evaluate the high performance AD9837 DDS modulator with a minimum of effort.

SYSTEM DEMONSTRATION PLATFORM

The system demonstration platform (SDP) is a hardware and software evaluation tool for use in conjunction with product evaluation boards. The SDP board is based on the Blackfin® ADSP-BF527 processor with USB connectivity to the PC through a USB 2.0 high speed port. For more information, see the SDP board product page.

Note that the SDP board is sold separately from the AD9837 evaluation board.

AD9837 TO SPORT INTERFACE

The Analog Devices SDP board has a SPORT serial port that is used to control the serial inputs to the AD9837. The connections are shown in Figure 28.

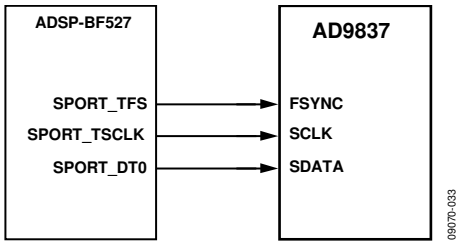


Figure 28. SDP to AD9837 Interface

EVALUATION KIT

The DDS evaluation kit includes a populated, tested AD9837 printed circuit board (PCB). The schematics of the evaluation board are shown in Figure 30 and Figure 31.

The software provided in the evaluation kit allows the user to easily program the AD9837 (see Figure 29). The evaluation software runs on any IBM-compatible PC with Microsoft® Windows® software installed (including Windows 7). The software is compatible with both 32-bit and 64-bit operating systems.

More information about the evaluation software is available on the software CD and on the AD9837 product page.



Figure 29. AD9837 Evaluation Software Interface

CRYSTAL OSCILLATOR VS. EXTERNAL CLOCK

The AD9837 can operate with master clocks up to 16 MHz. A 16 MHz oscillator is included on the evaluation board. This oscillator can be removed and, if required, an external CMOS clock can be connected to the part. Options for the general oscillator include the following:

- AEL 301-Series oscillators, AEL Crystals
- SG-310SCN oscillators, Epson Electronics

POWER SUPPLY

Power to the AD9837 evaluation board can be provided from the USB connector or externally through pin connections. The power leads should be twisted to reduce ground loops.

EVALUATION BOARD SCHEMATICS

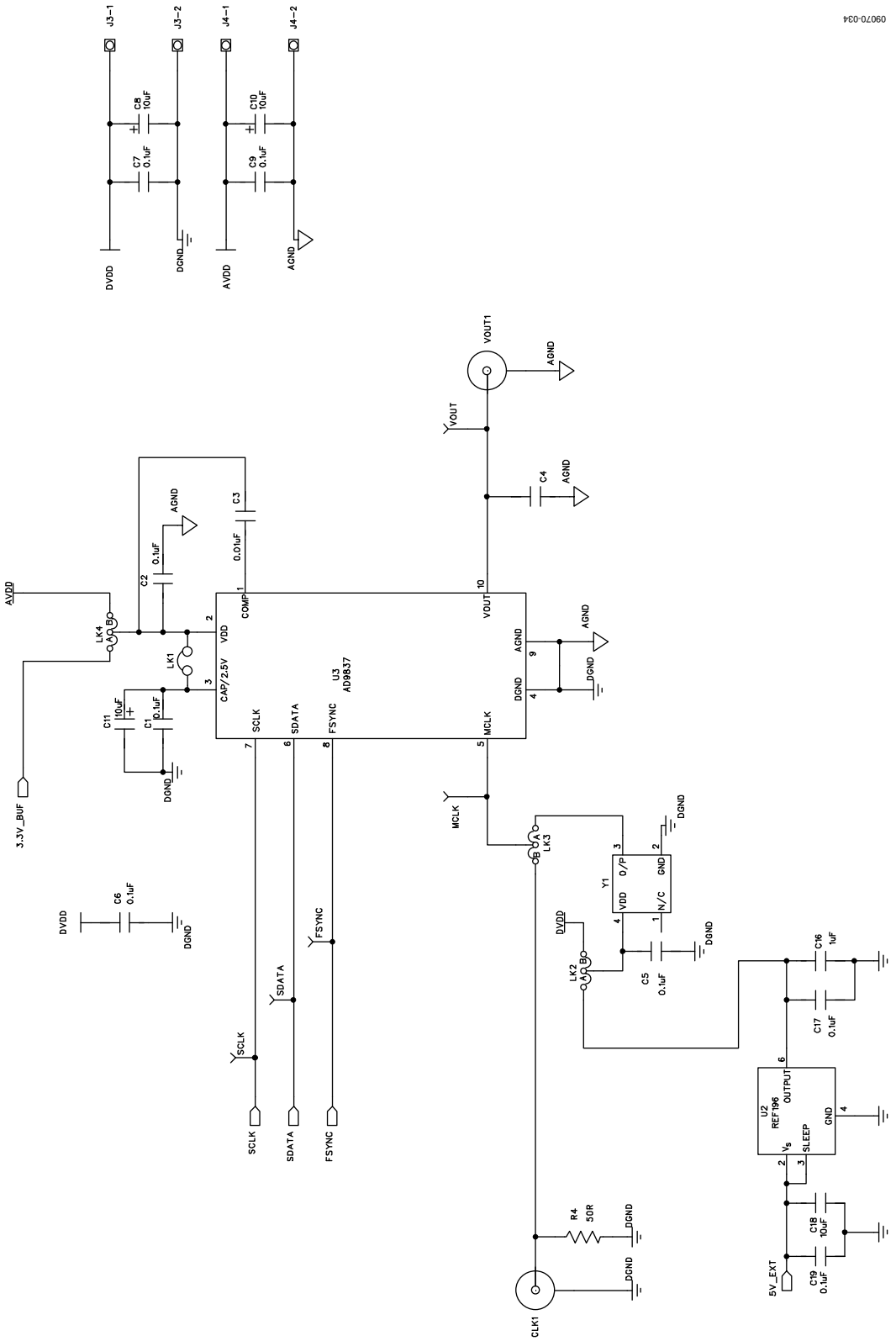


Figure 30. Evaluation Board Schematic

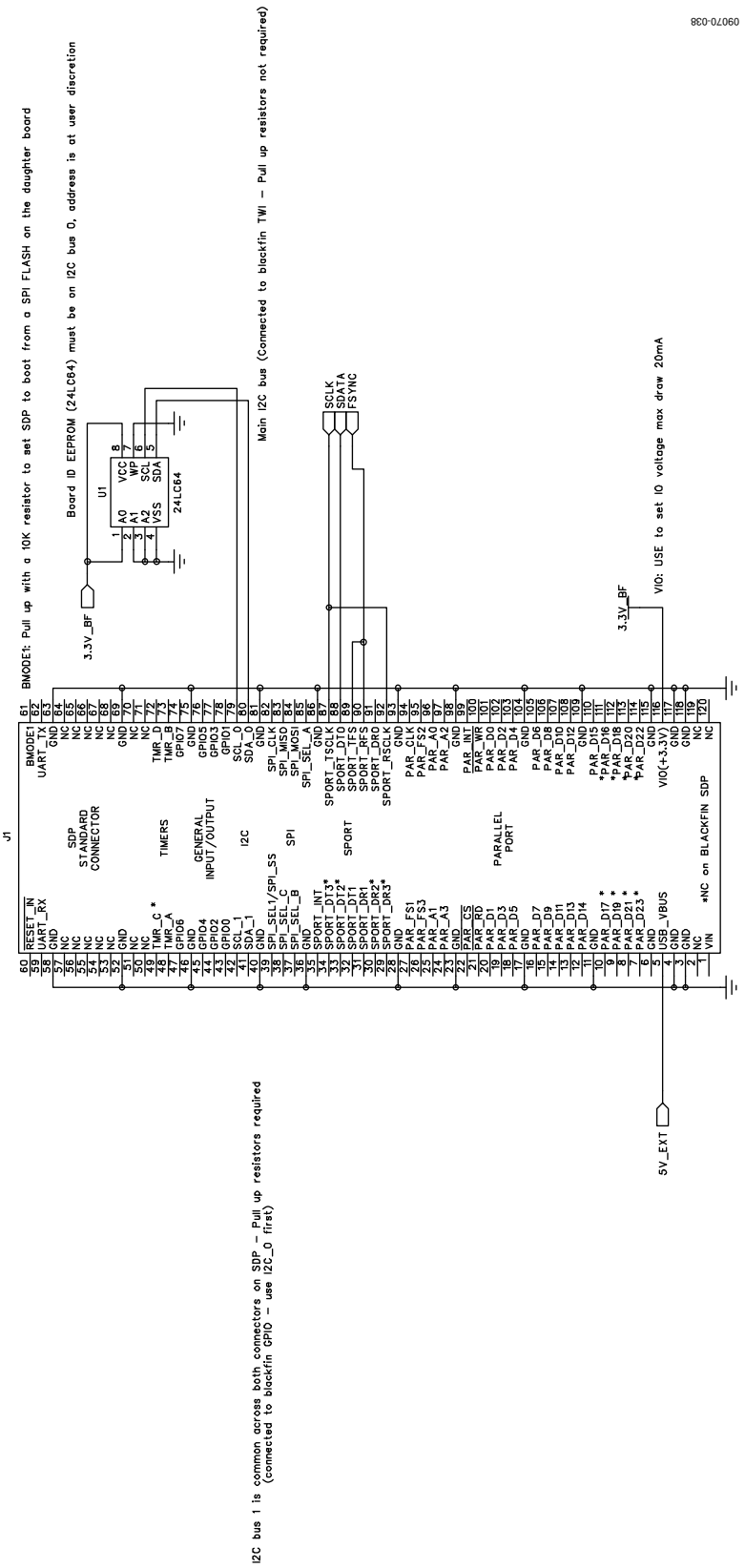


Figure 31. SDP Connector Schematic

EVALUATION BOARD LAYOUT

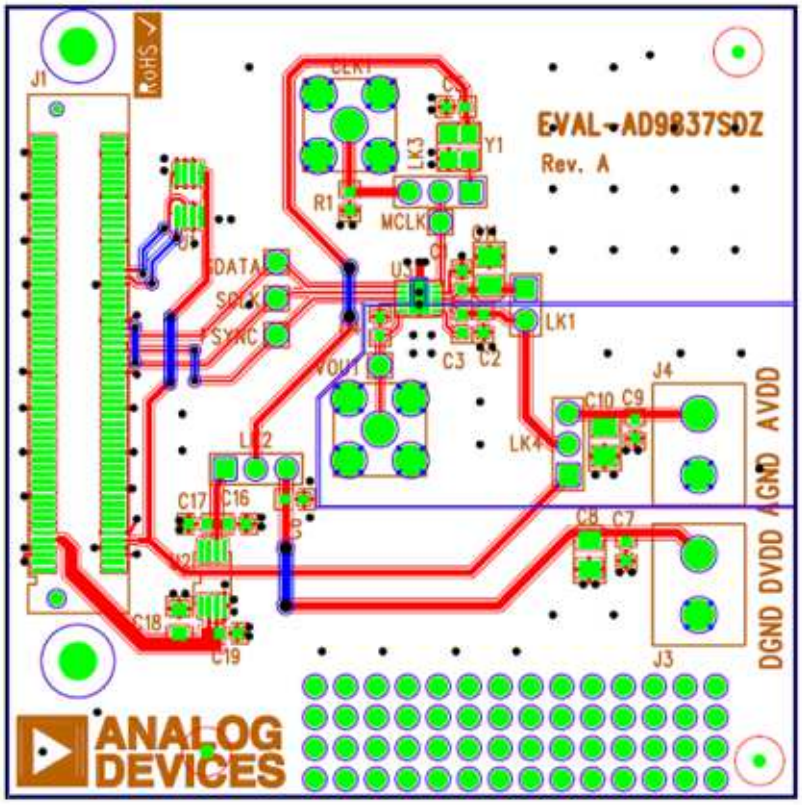


Figure 32. Evaluation Board Layout

OUTLINE DIMENSIONS

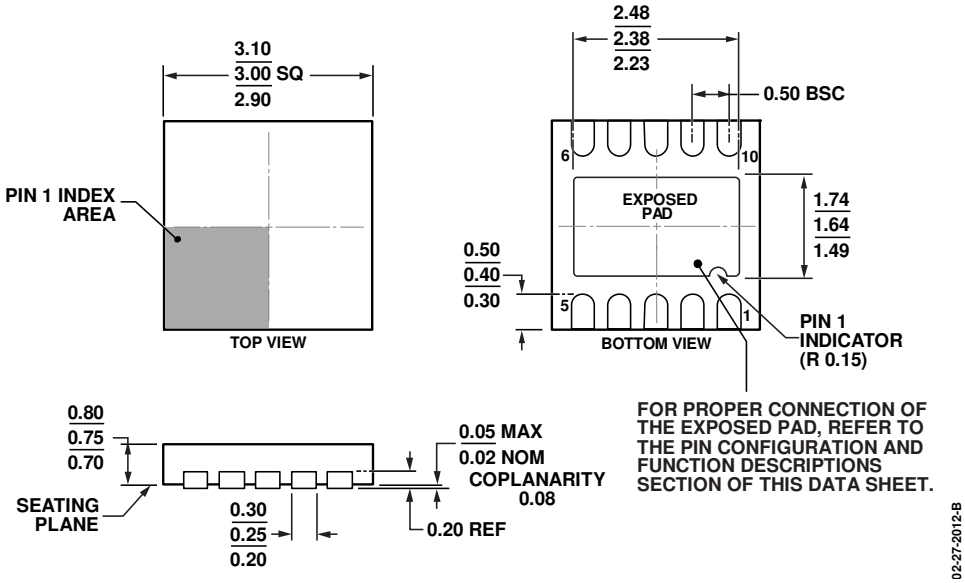


Figure 33. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Max MCLK	Package Description	Package Option	Branding
AD9837BCPZ-RL	−40°C to +125°C	16 MHz	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	DGH
AD9837BCPZ-RL7	−40°C to +125°C	16 MHz	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	DGH
AD9837ACPZ-RL	−40°C to +125°C	5 MHz	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	DGG
AD9837ACPZ-RL7	−40°C to +125°C	5 MHz	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	DGG
EVAL-AD9837SDZ			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The evaluation board for the AD9837 requires the system demonstration platform (SDP) board, which is sold separately.

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