CMOS 180 MHz DDS/DAC Synthesizer

AD9851

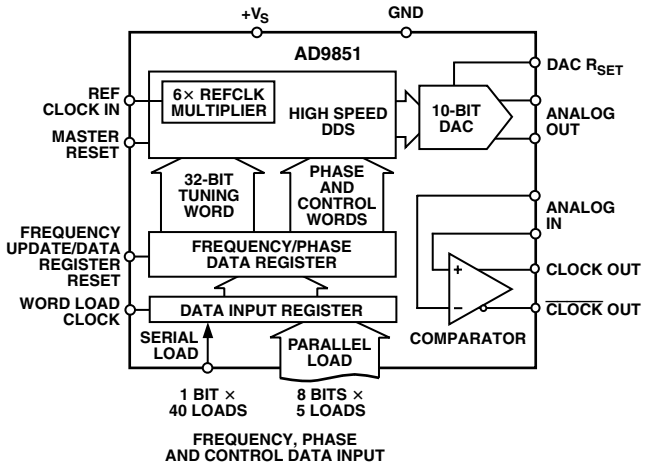
FEATURES

180 MHz Clock Rate with Selectable 6× Reference Clock Multiplier
On-Chip High Performance 10-Bit DAC and High Speed Comparator with Hysteresis
SFDR >43 dB @ 70 MHz A_{OUT}
32-Bit Frequency Tuning Word
Simplified Control Interface: Parallel or Serial Asynchronous Loading Format
5-Bit Phase Modulation and Offset Capability
Comparator Jitter <80 ps p-p @ 20 MHz
2.7 V to 5.25 V Single-Supply Operation
Low Power: 555 mW @ 180 MHz
Power-Down Function, 4 mW @ 2.7 V
Ultrasmall 28-Lead SSOP Packaging

APPLICATIONS

Frequency/Phase-Agile Sine Wave Synthesis
Clock Recovery and Locking Circuitry for Digital Communications
Digitally Controlled ADC Encode Generator
Agile Local Oscillator Applications in Communications
Quadrature Oscillator
CW, AM, FM, FSK, MSK Mode Transmitter

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9851 is a highly integrated device that uses advanced DDS technology, coupled with an internal high speed, high performance D/A converter, and comparator, to form a digitally programmable frequency synthesizer and clock generator function. When referenced to an accurate clock source, the AD9851 generates a stable frequency and phase-programmable digitized analog output sine wave. This sine wave can be used directly as a frequency source, or internally converted to a square wave for agile-clock generator applications. The AD9851's innovative high speed DDS core accepts a 32-bit frequency tuning word, which results in an output tuning resolution of approximately 0.04 Hz with a 180 MHz system clock. The AD9851 contains a unique 6× REFCLK Multiplier circuit that eliminates the need for a high speed reference oscillator. The 6× REFCLK Multiplier has minimal impact on SFDR and phase noise characteristics. The AD9851 provides five bits of programmable phase modulation resolution to enable phase shifting of its output in increments of 11.25°.

The AD9851 contains an internal high speed comparator that can be configured to accept the (externally) filtered output of the DAC to generate a low jitter output pulse.

The frequency tuning, control, and phase modulation words are asynchronously loaded into the AD9851 via a parallel or serial loading format. The parallel load format consists of five iterative loads of an 8-bit control word (byte). The first 8-bit byte controls output phase, 6× REFCLK Multiplier, power-down enable and loading format; the remaining bytes comprise the 32-bit frequency tuning word. Serial loading is accomplished via a 40-bit serial data stream entering through one of the parallel input bus lines. The AD9851 uses advanced CMOS technology to provide this breakthrough level of functionality on just 555 mW of power dissipation (5 V supply), at the maximum clock rate of 180 MHz.

The AD9851 is available in a space-saving 28-lead SSOP, surface-mount package that is pin-for-pin compatible with the popular AD9850 125 MHz DDS. It is specified to operate over the extended industrial temperature range of –40°C to +85°C at >3.0 V supply voltage. Below 3.0 V, the specifications apply over the commercial temperature range of 0°C to 85°C.

REV. D

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AD9851–SPECIFICATIONS

(V_S[1] = 5 V ± 5%, R_{SET} = 3.9 kΩ, 6× REFCLK Multiplier Disabled, External Reference Clock = 180 MHz, except as noted.)

Parameter	Temp	Test Level	AD9851BRS Min	Typ	Max	Unit
CLOCK INPUT CHARACTERISTICS						
Frequency Range (6× REFCLK Multiplier Disabled)						
5.0 V Supply	Full	IV	1		180	MHz
3.3 V Supply	Full	IV	1		125	MHz
2.7 V Supply	0°C to 85°C	IV	1		100	MHz
Frequency Range (6× REFCLK Multiplier Enabled)						
5.0 V Supply	Full	IV	5		30	MHz
3.3 V Supply	Full	IV	5		20.83	MHz
2.7 V Supply	0°C to 85°C	IV	5		16.66	MHz
Duty Cycle	Full	IV	45		60	%
Duty Cycle (6× REFCLK Multiplier Enabled)	Full	IV	35		65	%
Input Resistance	25°C	V		1		MΩ
Minimum Switching Thresholds[2]						
Logic 1, 5.0 V Supply	25°C	IV	3.5			V
Logic 1, 3.3 V Supply	25°C	IV	2.3			V
Logic 0, 5.0 V Supply	25°C	IV			1.5	V
Logic 0, 3.3 V Supply	25°C	IV			1	V
DAC OUTPUT CHARACTERISTICS						
Full-Scale Output Current	25°C	IV	5	10	20	mA
Gain Error	25°C	I	–10		+10	% FS
Output Offset	25°C	I			10	µA
Differential Nonlinearity	25°C	I			0.75	LSB
Integral Nonlinearity	25°C	I			1	LSB
Residual Phase Noise, 5.2 MHz, 1 kHz Offset						
PLL On	25°C	V		–125		dBc/Hz
PLL Off	25°C	V		–132		dBc/Hz
Output Impedance	25°C	V		120		kΩ
Voltage Compliance Range	25°C	I	–0.5		+1.5	V
Wideband Spurious-Free Dynamic Range						
1.1 MHz Analog Out (DC to 72 MHz)	25°C	IV	60	64		dBc
20.1 MHz Analog Out (DC to 72 MHz)	25°C	IV	51	53		dBc
40.1 MHz Analog Out (DC to 72 MHz)	25°C	IV	51	55		dBc
50.1 MHz Analog Out (DC to 72 MHz)	25°C	IV	46	53		dBc
70.1 MHz Analog Out (DC to 72 MHz)	25°C	IV	42	43		dBc
Narrowband Spurious-Free Dynamic Range						
1.1 MHz (±50 kHz)	25°C	V		85		dBc
1.1 MHz (±200 kHz)	25°C	V		80		dBc
40.1 MHz (±50 kHz)	25°C	V		85		dBc
40.1 MHz (±200 kHz)	25°C	V		80		dBc
70.1 MHz (±50 kHz)	25°C	V		85		dBc
70.1 MHz (±200 kHz)	25°C	V		73		dBc
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	25°C	V		3		pF
Input Resistance	25°C	IV		500		kΩ
Input Bias Current	25°C	I		12		µA
Input Voltage Range	25°C	IV	0		5	V
COMPARATOR OUTPUT CHARACTERISTICS						
Logic 1 Voltage 5 V Supply	25°C	VI	4.8			V
Logic 1 Voltage 3.3 V Supply	25°C	VI	3.1			V
Logic 1 Voltage 2.7 V Supply	25°C	VI	2.3			V
Logic 0 Voltage	25°C	VI			+0.4	V
Continuous Output Current	25°C	IV			20	mA
Hysteresis	25°C	IV	10			mV
Propagation Delay	25°C	IV			7	ns
Toggle Frequency (1 V p-p Input Sine Wave)	25°C	IV			200	MHz
Rise/Fall Time, 15 pF Output Load	25°C	IV			7	ns
Output Jitter (p-p)[3]	25°C	IV		80		ps (p-p)
CLOCK OUTPUT CHARACTERISTICS						
Output Jitter (Clock Generator Configuration, 40 MHz 1 V p-p Input Sine Wave)	25°C	V		250		ps (p-p)
Clock Output Duty Cycle	Full	IV		50 ± 10		%

Parameter	Temp	Test Level	AD9851BRS Min	Typ	Max	Unit
TIMING CHARACTERISTICS[4]						
t_{WH}, t_{WL} (W_CLK Min Pulse Width High/Low)	Full	IV	3.5			ns
t_{DS}, t_{DH} (Data to W_CLK Setup and Hold Times)	Full	IV	3.5			ns
t_{FH}, t_{FL} (FQ_UD Min Pulse Width High/Low)	Full	IV	7			ns
t_{CD} (REFCLK Delay After FQ_UD)[5]	Full	IV	3.5			ns
t_{FD} (FQ_UD Min Delay After W_CLK)	Full	IV	7			ns
t_{CF} (Output Latency from FQ_UD)						
Frequency Change	Full	IV	18			SYSCLK Cycles
Phase Change	Full	IV	13			SYSCLK Cycles
t_{RH} (CLKIN Delay After RESET Rising Edge)	Full	IV	3.5			ns
t_{RL} (RESET Falling Edge After CLKIN)	Full	IV	3.5			ns
t_{RR} (Recovery from RESET)	Full	IV	2			SYSCLK Cycles
t_{RS} (Minimum RESET Width)	Full	IV	5			SYSCLK Cycles
t_{OL} (RESET Output Latency)	Full	IV	13			SYSCLK Cycles
Wake-Up Time from Power-Down Mode[6]	25°C	V		5		µs
CMOS LOGIC INPUTS						
Logic 1 Voltage, 5 V Supply	25°C	I	3.5			V
Logic 1 Voltage, 3.3 V Supply	25°C	IV	2.4			V
Logic 1 Voltage, 2.7 V Supply	25°C	IV	2.0			V
Logic 0 Voltage	25°C	IV			0.8	V
Logic 1 Current	25°C	I			12	µA
Logic 0 Current	25°C	I			12	µA
Rise/Fall Time	25°C	IV			100	ns
Input Capacitance	25°C	V		3		pF
POWER SUPPLY						
V_S[6] Current @:						
62.5 MHz Clock, 2.7 V Supply	25°C	VI		30	35	mA
100 MHz Clock, 2.7 V Supply	25°C	VI		40	50	mA
62.5 MHz Clock, 3.3 V Supply	25°C	VI		35	45	mA
125 MHz Clock, 3.3 V Supply	25°C	VI		55	70	mA
62.5 MHz Clock, 5 V Supply	25°C	VI		50	65	mA
125 MHz Clock, 5 V Supply	25°C	VI		70	90	mA
180 MHz Clock, 5 V Supply	25°C	VI		110	130	mA
Power Dissipation @ :						
62.5 MHz Clock, 5 V Supply	25°C	VI		250	325	mW
62.5 MHz Clock, 3.3 V Supply	25°C	VI		115	150	mW
62.5 MHz Clock, 2.7 V Supply	25°C	VI		85	95	mW
100 MHz Clock, 2.7 V Supply	25°C	VI		110	135	mW
125 MHz Clock, 5 V Supply	25°C	VI		365	450	mW
125 MHz Clock, 3.3 V Supply	25°C	VI		180	230	mW
180 MHz Clock, 5 V Supply	25°C	VI		555	650	mW
P_{DISS} Power-Down Mode @:						
5 V Supply	25°C	VI		17	55	mW
2.7 V Supply	25°C	VI		4	20	mW

NOTES

[1]+V_S collectively refers to the positive voltages applied to DVDD, PVCC, and AVDD. Voltages applied to these pins should be of the same potential.

[2]Indicates the minimum signal levels required to reliably clock the device at the indicated supply voltages. This specifies the p-p signal level and dc offset needed when the clocking signal is not of CMOS/TTL origin, i.e., a sine wave with 0 V dc offset.

[3]The comparator's jitter contribution to any input signal. This is the minimum jitter on the outputs that can be expected from an ideal input. Considerably more output jitter is seen when nonideal input signals are presented to the comparator inputs. Nonideal characteristics include the presence of extraneous, nonharmonic signals (spur's, noise), slower slew rate, and low comparator overdrive.

[4]Timing of input signals FQ_UD, WCLK, RESET are asynchronous to the reference clock; however, the presence of a reference clock is required to implement those functions. In the absence of a reference clock, the AD9851 automatically enters power-down mode rendering the IC, including the comparator, inoperable until a reference clock is restored. Very high speed updates of frequency/phase word will require FQ_UD and WCLK to be externally synchronized with the external reference clock to ensure proper timing.

[5]Not applicable when 6× REFCLK Multiplier is engaged.

[6]Assumes no capacitive load on DACBP (Pin 17).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
V_S . . . . . 6 V
Operating Temperature . . . . . –40°C to +85°C
Digital Inputs . . . . . –0.7 V to $+V_S$ + 0.7 V
Lead Temperature (10 sec) Soldering . . . . . 300°C
Digital Output Current . . . . . 30 mA
SSOP θ_{JA} Thermal Impedance . . . . . 82°C/W
DAC Output Current . . . . . 30 mA

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% Production Tested.
III – Sample Tested Only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9851BRS	–40°C to +85°C	Shrink Small Outline (SSOP)	RS-28
AD9851BRSRL	–40°C to +85°C	Shrink Small Outline (SSOP)	RS-28
AD9851/CGPCB		Evaluation Board Clock Generator	
AD9851/FSPCB		Evaluation Board Frequency Synthesizer	

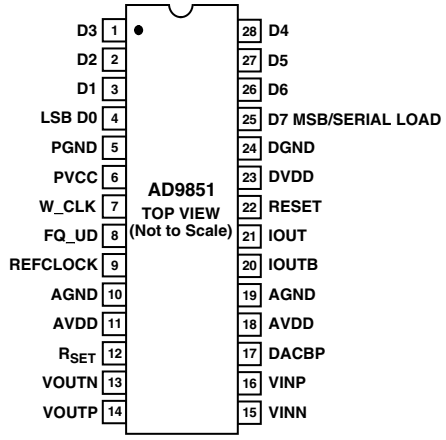
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9851 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Application Note: Users are cautioned not to apply digital input signals prior to power-up of this device. Doing so may result in a latch-up condition.



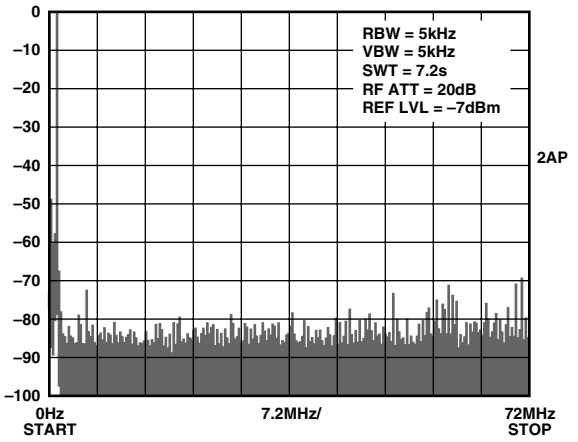
PIN CONFIGURATION



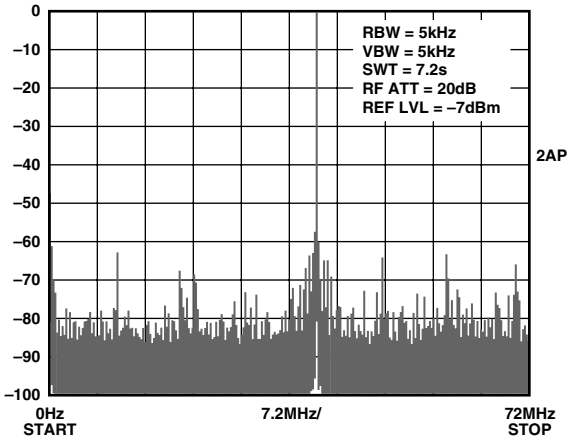
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
4–1, 28–25	D0–D7	8-Bit Data Input. The data port for loading the 32-bit frequency and 8-bit phase/control words. D7 = MSB; D0 = LSB. D7, Pin 25, also serves as the input pin for 40-bit serial data word.
5	PGND	6× REFCLK Multiplier Ground Connection.
6	PVCC	6× REFCLK Multiplier Positive Supply Voltage Pin.
7	W_CLK	Word Load Clock. Rising edge loads the parallel or serial frequency/phase/control words asynchronously into the 40-bit input register.
8	FQ_UD	Frequency Update. A rising edge asynchronously transfers the contents of the 40-bit input register to be acted upon by the DDS core. FQ_UD should be issued when the contents of the input register are known to contain only valid, allowable data.
9	REFCLOCK	Reference Clock Input. CMOS/TTL-level pulse train, direct or via the 6× REFCLK Multiplier. In direct mode, this is also the SYSTEM CLOCK. If the 6× REFCLK Multiplier is engaged, then the output of the multiplier is the SYSTEM CLOCK. The rising edge of the SYSTEM CLOCK initiates operations.
10, 19	AGND	Analog Ground. The ground return for the analog circuitry (DAC and Comparator).
11, 18	AVDD	Positive supply voltage for analog circuitry (DAC and Comparator, Pin 18) and bandgap voltage reference, Pin 11.
12	R_{SET}	The DAC's external R_{SET} connection—nominally a 3.92 kΩ resistor to ground for 10 mA out. This sets the DAC full-scale output current available from IOUT and IOUTB. R_{SET} = 39.93/IOUT.
13	VOUTN	Voltage Output Negative. The comparator's complementary CMOS logic level output.
14	VOUTP	Voltage Output Positive. The comparator's true CMOS logic level output.
15	VINN	Voltage Input Negative. The comparator's inverting input.
16	VINP	Voltage Input Positive. The comparator's noninverting input.
17	DACBP	DAC Bypass Connection. This is the DAC voltage reference bypass connection normally NC (NO CONNECT) for optimum SFDR performance.
20	IOUTB	The complementary DAC output with same characteristics as IOUT except that *IOUTB = (full-scale output–IOUT)*. Output load should equal that of IOUT for best SFDR performance.
21	IOUT	The true output of the balanced DAC. Current is sourcing and requires current-to-voltage conversion, usually a resistor or transformer referenced to GND. *IOUT = (full-scale output–IOUTB)*.
22	RESET	Master Reset pin; active high; clears DDS accumulator and phase offset register to achieve 0 Hz and 0° output phase. Sets programming to parallel mode and disengages the 6× REFCLK Multiplier. Reset does not clear the 40-bit input register. On power-up, asserting RESET should be the first priority before programming commences.
23	DVDD	Positive supply voltage pin for digital circuitry.
24	DGND	Digital Ground. The ground return pin for the digital circuitry.

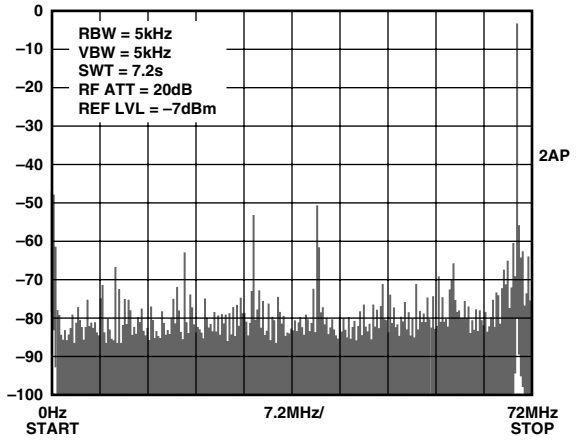
AD9851–Typical Performance Characteristics



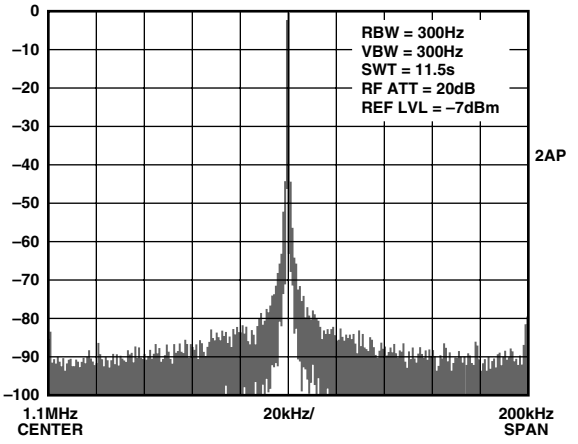
TPC 1. Wideband (dc to 72 MHz) output SFDR for a 1.1 MHz fundamental output signal. System clock = 180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



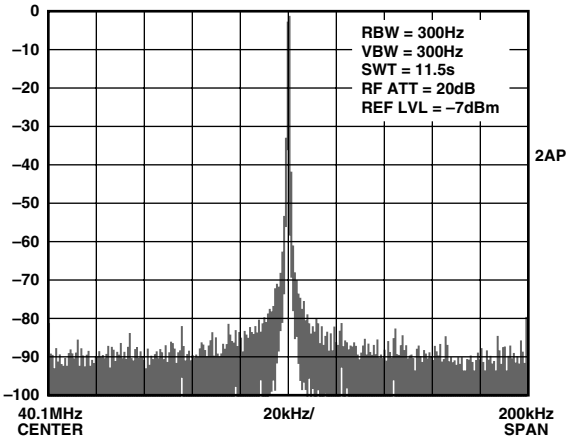
TPC 2. Wideband (dc to 72 MHz) output SFDR for a 40.1 MHz fundamental output signal. System clock = 180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



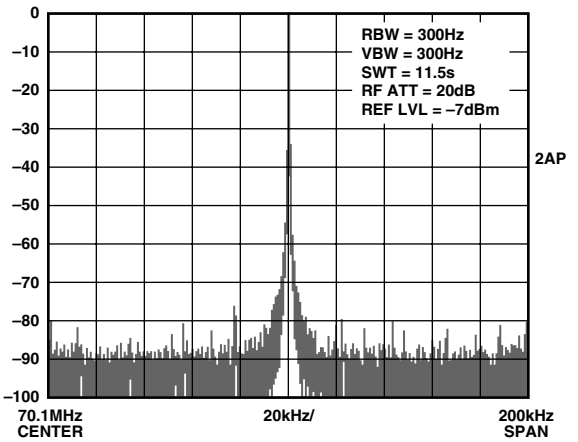
TPC 3. Wideband (dc to 72 MHz) output SFDR for a 70.1 MHz fundamental output signal. System clock = 180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



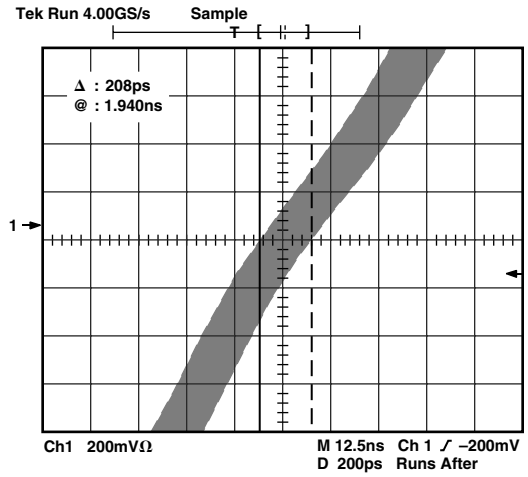
TPC 4. Narrowband (1.1 ± 0.1 MHz) output SFDR for a 1.1 MHz fundamental output signal. System clock =180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



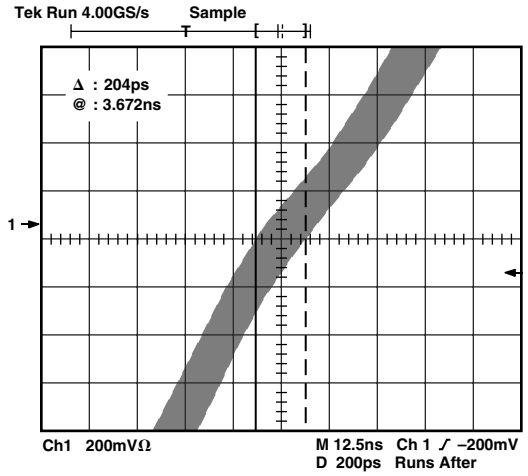
TPC 5. Narrowband (40.1 ± 0.1 MHz) output SFDR for a 40.1 MHz fundamental output signal. System clock = 180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



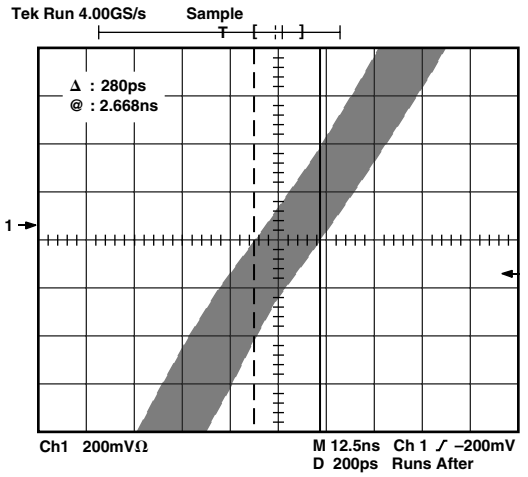
TPC 6. Narrowband (70.1 ± 0.1 MHz) output SFDR for a 70.1 MHz fundamental output signal. System clock = 180 MHz (6× REFCLK multiplier engaged), V_S = 5 V.



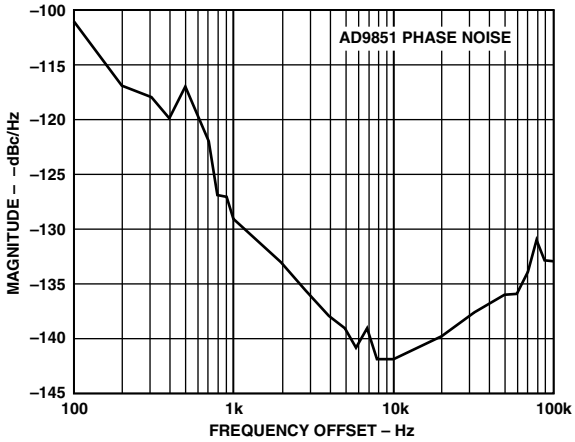
TPC 7. Typical CMOS comparator p-p output jitter with the AD9851 configured as a clock generator, DDS f_{OUT} = 10.1 MHz, V_S = 5 V, system clock = 180 MHz, 70 MHz LPF. Graph details the center portion of a rising edge with scope in delayed trigger mode, 200 ps/div. Cursors show 208 ps p-p jitter.



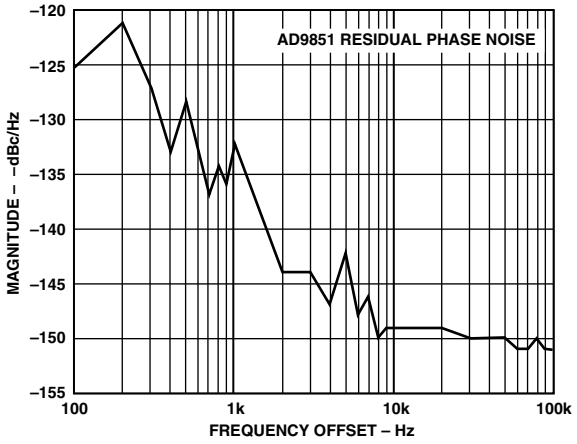
TPC 8. Typical CMOS comparator p-p output jitter with the AD9851 configured as a clock generator, DDS f_{OUT} = 40.1 MHz, V_S = 5 V, system clock = 180 MHz, 70 MHz LPF. Graph details the center portion of a rising edge with scope in delayed trigger mode, 200 ps/div. Cursors show 204 ps p-p jitter.



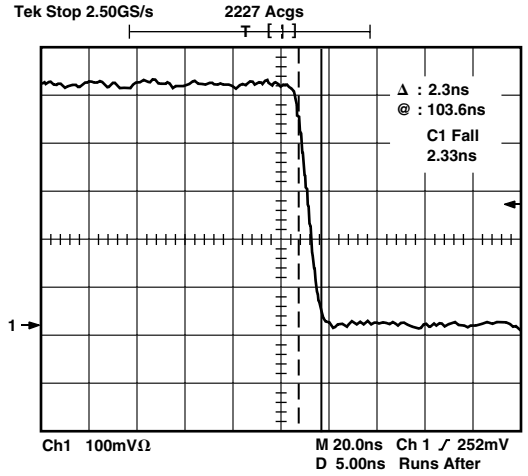
TPC 9. Typical CMOS comparator p-p output jitter with the AD9851 configured as a clock generator, DDS f_{OUT} = 70.1 MHz, V_S = 5 V, system clock = 180 MHz, 70 MHz LPF. Graph details the center portion of a rising edge with scope in delayed trigger mode, 200 ps/div. Cursors show 280 ps p-p jitter.



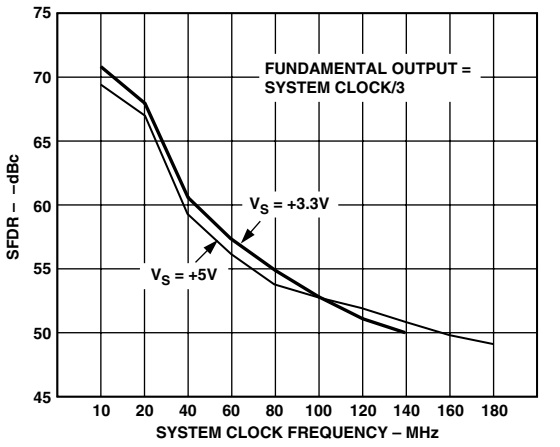
TPC 10. Output Phase Noise (5.2 MHz A_{OUT}), 6× REFCLK Multiplier Enabled, System Clock = 180 MHz, Reference Clock = 30 MHz



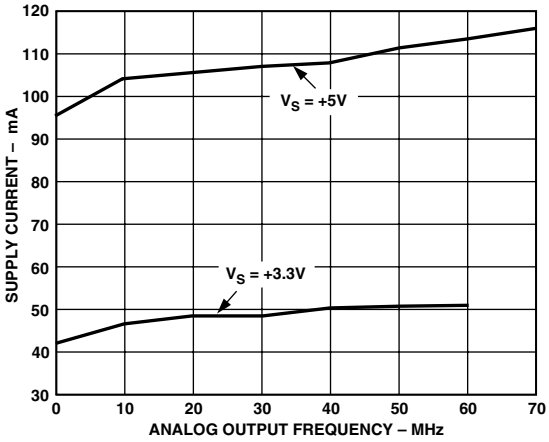
TPC 11. Output Residual Phase Noise (5.2 MHz A_{OUT}), 6× REFCLK Multiplier Disabled, System Clock = 180 MHz, Reference Clock = 180 MHz



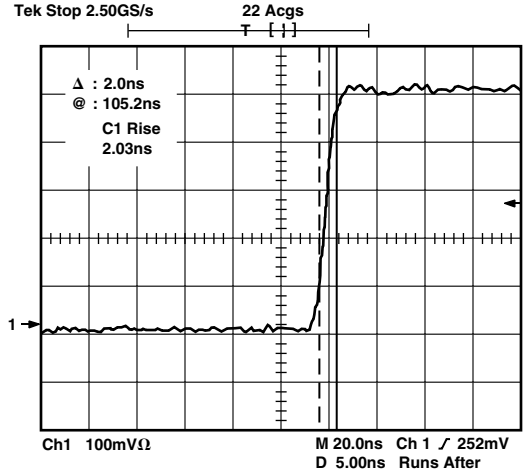
TPC 14. Comparator Fall Time, 15 pF Load



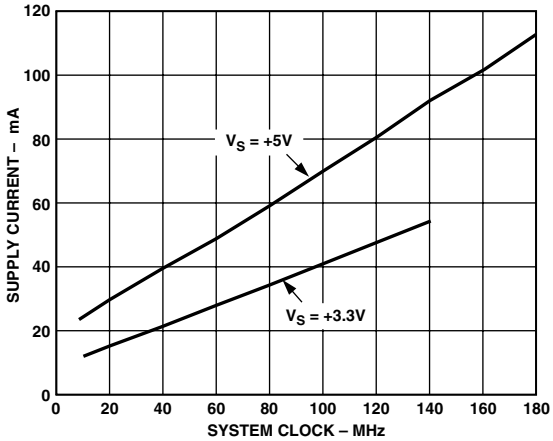
TPC 12. Spurious-free dynamic range (SFDR) is generally a function of the DAC analog output frequency. Analog output frequencies of 1/3 the system clock rate are considered worst case. Plotted below are typical worst case SFDR numbers for various system clock rates.



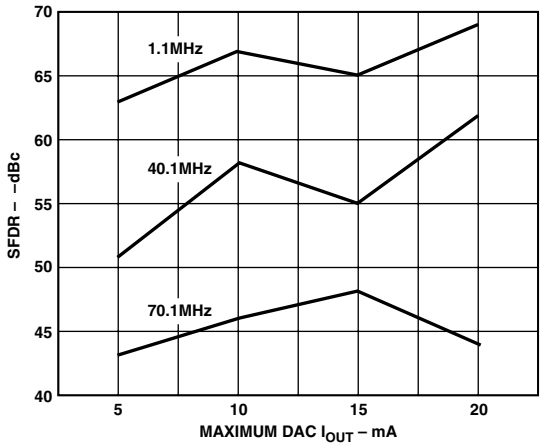
TPC 15. Supply current variation with analog output frequency at 180 MHz system clock (upper trace) and 125 MHz system clock (lower trace)



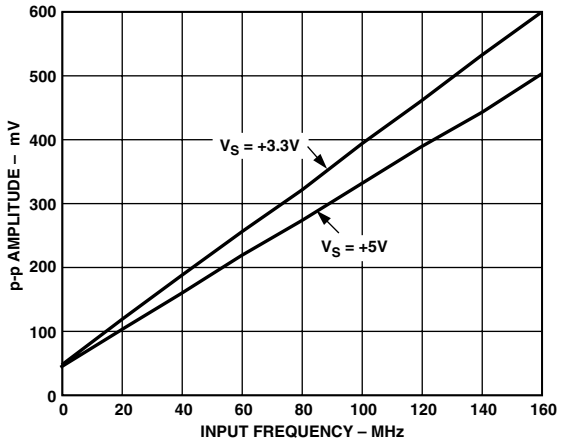
TPC 13. Comparator Rise Time, 15 pF Load



TPC 16. Supply current variation with system clock frequency



TPC 17. Effect of DAC maximum output current on wideband (0 to 72 MHz) SFDR at three representative DAC output frequencies: 1.1 MHz, 40.1 MHz, and 70.1 MHz. V_S = 5 V, 180 MHz system clock (6× REFCLK multiplier disabled). Currents are set using appropriate values of R_{SET}.



TPC 18. Minimum p-p input signal needed to toggle the AD9851 comparator output. Comparator input is a sine wave compared with a fixed voltage threshold. Use this data in addition to sin(x)/x rolloff and any filter losses to determine whether adequate signal is being presented to the AD9851 comparator.

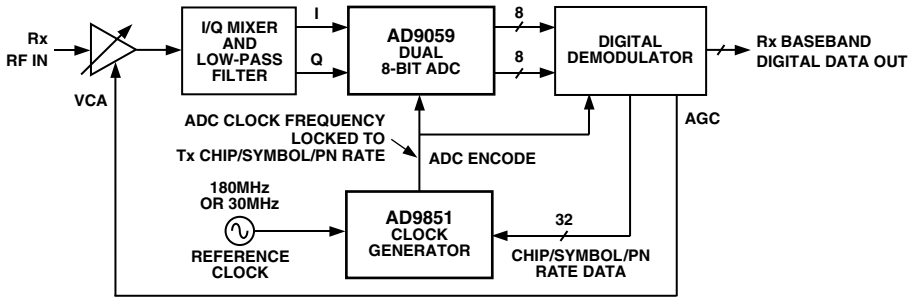


Figure 1. Chip Rate Clock Generator Application in a Spread Spectrum Receiver

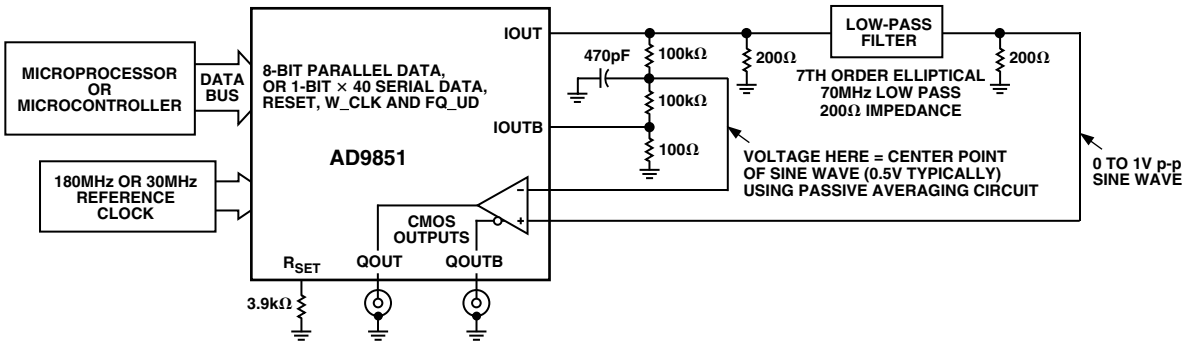


Figure 2. Basic Clock Generator Configuration

IOUT and IOUTB are equally loaded with 100 Ω. Two 100 kΩ resistors sample each output and average the two voltages. The result is filtered with the 470 pF capacitor and applied to one comparator input as a dc switching threshold. The filtered DAC sine wave output is applied to the other comparator input. The comparator will toggle with nearly 50% duty cycle as the sine wave alternately traverses the center point threshold.

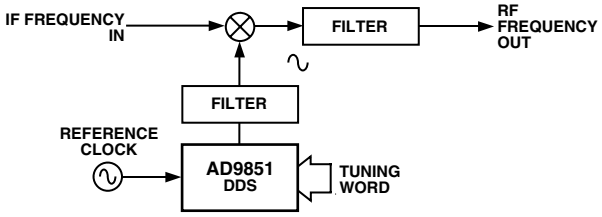


Figure 3. Frequency/Phase-Agile Local Oscillator for Frequency Mixing/Multiplying

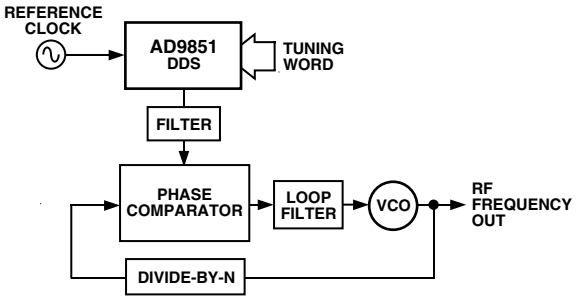


Figure 4. Frequency/Phase-Agile Reference for PLL

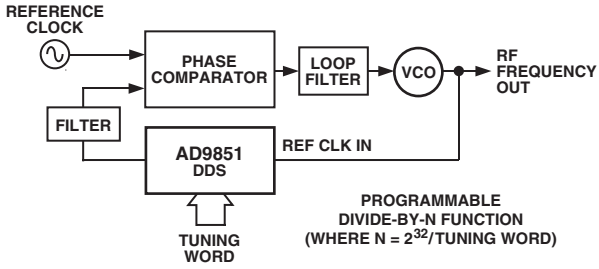


Figure 5. Digitally Programmable Divide-by-N Function in PLL

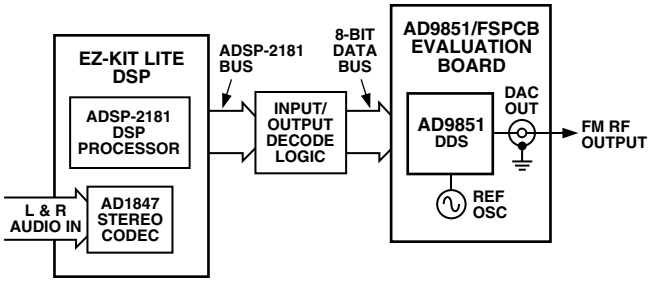


Figure 6. High Quality, All Digital RF Frequency Modulation

High quality, all digital RF frequency modulation generation with the ADSP-2181 DSP and the AD9851 DDS is well documented in Analog Devices' application note AN-543. It uses an image of the DDS output as illustrated in Figure 8.

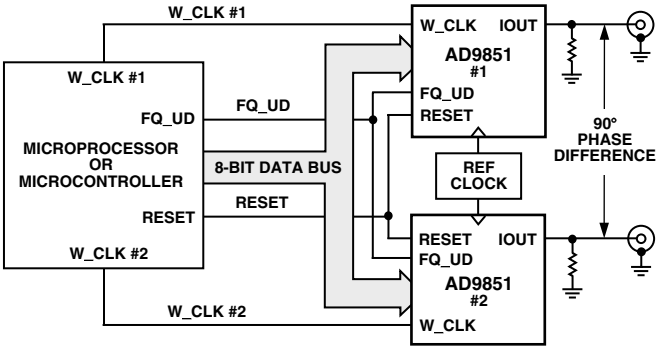


Figure 7. Application Showing Synchronization of Two AD9851 DDSs to Form a Quadrature Oscillator

After a common RESET command is issued, separate W_CLKs allow independent programming of each AD9851 40-bit input register via the 8-bit data bus or serial input pin. A common FQ_UD pulse is issued after programming is completed to simultaneously engage both oscillators at their specified frequency and phase.

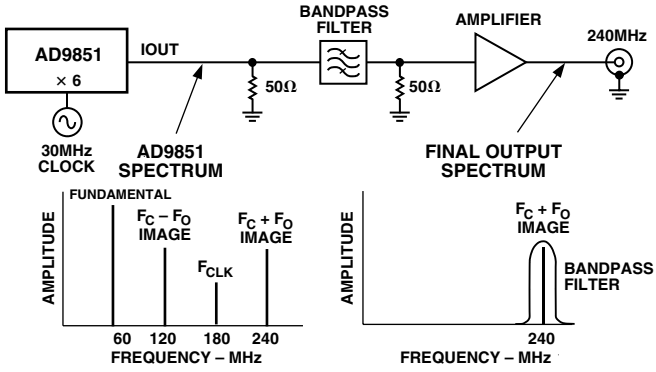


Figure 8. Deriving a High Frequency Output Signal from the AD9851 by Using an Alias or Image Signal

The differential DAC output connection in Figure 9 enables reduction of common-mode signals and allows highly reactive filters to be driven without a filter input termination resistor (see above single-ended example, Figure 8). A 6 dB power advantage is obtained at the filter output as compared with the single-ended example, since the filter need not be doubly terminated.

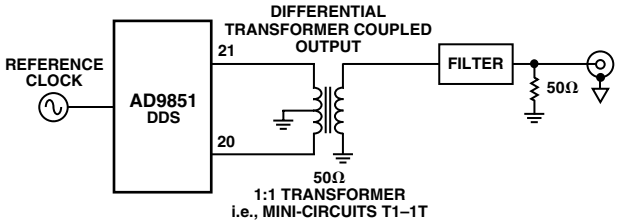


Figure 9. Differential DAC Output Connection for Reduction of Common-Mode Signals

The AD9851 R_{SET} input is driven by an external DAC (Figure 10) to provide amplitude modulation or fixed, digital amplitude control of the DAC output current. Full description of this application is found as a Technical Note in the AD9851 data sheet under Related Information. An Analog Devices' application note for the AD9850, AN-423, describes another method of amplitude control using an enhancement mode MOSFET that is equally applicable to the AD9851.

NOTE: If the 6× REFCLK multiplier of the AD9851 is engaged, the 125 MHz clocking source shown in Figure 10 can be reduced by a factor of six.

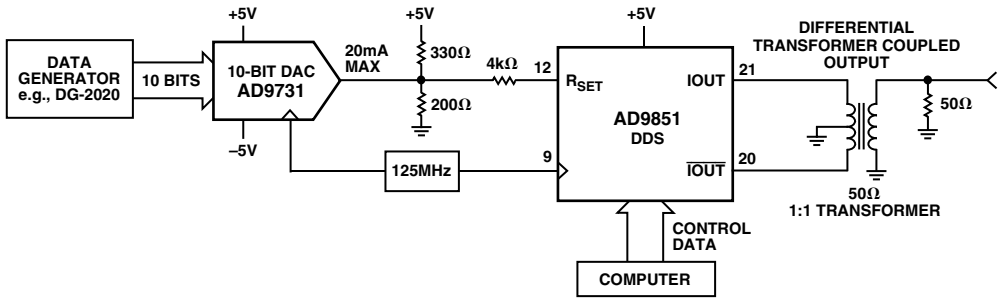


Figure 10. The AD9851 RSET Input Being Driven by an External DAC

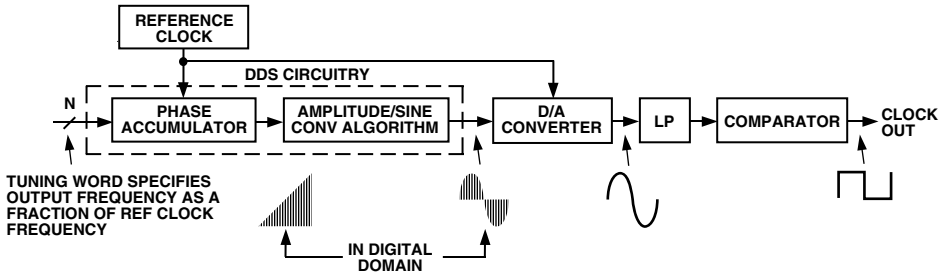


Figure 11. Basic DDS Block Diagram and Signal Flow of AD9851

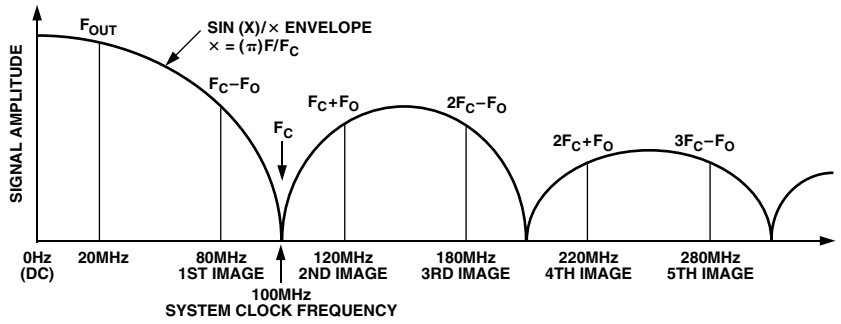


Figure 12. Output Spectrum of a Sampled Sin(x)/x Signal

THEORY OF OPERATION AND APPLICATION

The AD9851 uses direct digital synthesis (DDS) technology, in the form of a numerically controlled oscillator (NCO), to generate a frequency/phase-agile sine wave. The digital sine wave is converted to analog form via an internal 10-bit high speed D/A converter. An on-board high speed comparator is provided to translate the analog sine wave into a low-jitter TTL/CMOS-compatible output square wave. DDS technology is an innovative circuit architecture that allows fast and precise manipulation of its output word, under full digital control. DDS also enables very high resolution in the incremental selection of output frequency. The AD9851 allows an output frequency resolution of approximately 0.04 Hz at an 180 MSPS clock rate with the option of directly using the reference clock or by engaging the 6× REFCLK multiplier. The AD9851's output waveform is phase-continuous from one output frequency change to another.

The basic functional block diagram and signal flow of the AD9851 configured as a clock generator is shown in Figure 11.

The DDS circuitry is basically a digital frequency divider function whose incremental resolution is determined by the frequency of the system clock, and N (number of bits in the tuning word). The phase accumulator is a variable-modulus counter that increments the number stored in it each time it receives a clock pulse. When the counter reaches full-scale it wraps around, making the phase accumulator's output phase-continuous. The frequency tuning word sets the modulus of the counter, which effectively determines the size of the increment (Δ Phase) that will be added to the value in the phase accumulator on the next clock pulse. The larger the added increment, the faster the accumulator wraps around, which results in a higher output frequency.

The AD9851 uses an innovative and proprietary angle rotation algorithm that mathematically converts the 14-bit truncated value of the 32-bit phase accumulator to the 10-bit quantized amplitude that is passed to the DAC. This unique algorithm uses a much-reduced ROM look-up table and DSP to perform this function. This contributes to the small size and low power dissipation of the AD9851.

The relationship between the output frequency, system clock, and tuning word of the AD9851 is determined by the expression:

$$f_{OUT} = (\Delta\ Phase \times System\ Clock)/2^{32}$$

where

$\Delta Phase$ = decimal value of 32-bit frequency tuning word.

System Clock = direct input reference clock (in MHz) or 6× the input clock (in MHz) if the 6× REFCLK multiplier is engaged.

f_{OUT} = frequency of the output signal in MHz.

The digital sine wave output of the DDS core drives the internal high speed 10-bit D/A converter that will construct the sine wave in analog form. This DAC has been optimized for dynamic performance and low glitch energy, which results in the low spurious and jitter performance of the AD9851. The DAC can be operated in either the single-ended (Figures 2 and 8) or differential output configuration (Figures 9 and 10). DAC output current and R_{SET} values are determined using the following expressions:

$$I_{OUT} = 39.93/R_{SET}$$
$$R_{SET} = 39.93/I_{OUT}$$

Since the output of the AD9851 is a sampled signal, its output spectrum follows the Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental plus aliased signals (images) that occur at integer multiples of the system clock frequency ± the selected output frequency. A graphical representation of the sampled spectrum, with aliased images, is shown in Figure 12. Normal usable bandwidth is considered to extend from dc to 1/2 the system clock.

In the example shown in Figure 12, the system clock is 100 MHz and the output frequency is set to 20 MHz. As can be seen, the aliased images are very prominent and of a relatively high energy level as determined by the sin(x)/x rolloff of the quantized D/A converter output. In fact, depending on the f/system clock relationship, the first aliased image can equal the fundamental amplitude (when f_{OUT} = 1/2 system clock). A low-pass filter is generally placed between the output of the D/A converter and the input of the comparator to suppress the jitter-producing effects of nonharmonically related aliased images and other spurious signals. Consideration must be given to the relationship of the selected output frequency, the system clock frequency, and alias frequencies to avoid unwanted output anomalies.

Images need not be thought of as useless by-products of a DAC. In fact, with bandpass filtering around an image and some amount of post-filter amplification, the image can become the primary output signal (see Figure 8). Since images are not harmonics, they retain a 1:1 Δfrequency relationship to the fundamental output. That is, if the fundamental is shifted 1 kHz, then the image is also shifted 1 kHz. This relationship accounts for the frequency stability of an image, which is identical to that of the fundamental. Users should recognize that the lower image of an image pair surrounding an integer multiple of the system clock will move in a direction opposite to that of the fundamental. Images of an image pair located above an integer multiple of the system clock will move in the same direction as a fundamental movement.

The frequency band where images exist is much richer in spurious signals and, therefore, more hostile in terms of SFDR. Users of this technique should empirically determine what frequencies are usable if their SFDR requirements are demanding.

A good rule-of-thumb for applying the AD9851 as a clock generator is to limit the fundamental output frequency to 40% of reference clock frequency to avoid generating aliased signals that are too close to the output band of interest (generally dc—highest selected output frequency) to be filtered. This practice will ease the complexity and cost of the external filter requirement for the clock generator application.

The reference clock input of the AD9851 has a minimum limitation of 1 MHz without 6× REFCLK multiplier engaged and 5 MHz with multiplier engaged. The device has internal circuitry that senses when the clock rate has dropped below the minimum and automatically places itself in the power-down mode. In this mode, the on-chip comparator is also disabled. This is important information for those who may wish to use the on-chip comparator for purposes other than squaring the DDS sine wave output. When the clock frequency returns above the minimum threshold, the device resumes normal operation after 5 µs (typically). This shutdown mode prevents excessive current leakage in the dynamic registers of the device.

The impact of reference clock phase noise in DDS systems is actually reduced, since the DDS output is the result of a division of the input frequency. The amount of apparent phase noise reduction, expressed in dB, is found using 20 log f_{OUT}/f_{CLK}, where f_{OUT} is the fundamental DDS output frequency and f_{CLK} is the system clock frequency. From this standpoint, using the highest system clock input frequency makes good sense in reducing the effects of reference clock phase noise contribution to the output signals' overall phase noise. As an example, an oscillator with –100 dBc phase noise operating at 180 MHz would appear as a –125 dB contribution to DDS overall phase noise for a 10 MHz output. Engaging the 6× REFCLK multiplier has generally been found to increase overall output phase noise. This increase is due to the inherent 6× (15.5 dB) phase gain transfer function of the 6× REFCLK multiplier, as well as noise generated internally by the clock multiplier circuit. By using a low phase noise reference clock input to the AD9851, users can be assured of better than –100 dBc/Hz phase noise performance for output frequencies up to 50 MHz at offsets from 1 kHz to 100 kHz.

Programming the AD9851

The AD9851 contains a 40-bit register that stores the 32-bit frequency control word, the 5-bit phase modulation word, 6× REFCLK multiplier, enable, and the power-down function. This register can be loaded in parallel or serial mode. A logic high engages functions; for example, to power-down the IC (sleep mode), a logic high must be programmed in that bit location. Those users who are familiar with the AD9850 DDS will find only a slight change in programming the AD9851, specifically, data[0] of W0 (parallel load) and W32 (serial load) now contains a 6× REFCLK multiplier enable bit that needs to be set high to enable or low to disable the internal reference clock multiplier.

Note: setting data[1] high in programming word W0 (parallel mode) or word W33 high in serial mode is not allowed (see Tables I and III). This bit controls a factory test mode that will cause abnormal operation in the AD9851 if set high. If erroneously entered (as evidenced by Pin 2 changing from an input pin to an output signal), an exit is provided by asserting RESET. Unintentional entry to the factory test mode can occur if an FQ_UD pulse is sent after initial power-up and RESET of the AD9851. Since RESET does not clear the 40-bit input register, this will transfer the random power-up values of the input register to the DDS core. The random values may invoke the factory test mode or power-down mode. Never issue an FQ_UD command if the 40-bit input register contents are unknown.

In the default parallel load mode, the 40-bit input register is loaded using an 8-bit bus. W_CLK is used to load the register in five iterations of eight bytes. The rising edge of FQ_UD transfers the contents of the register into the device to be acted upon and resets the word address pointer to W0. Subsequent W_CLK rising edges load 8-bit data, starting at W0 and then move the word pointer to the next word. After W0 through W4 are loaded, additional W_CLK edges are ignored until either a RESET is asserted or an FQ_UD rising edge resets the address pointer to W0 in preparation for the next 8-bit load. See Figure 13.

In serial load mode, forty subsequent rising edges of W_CLK will shift and load the 1-bit data on Pin 25 (D7) through the 40-bit register in shift-register fashion. Any further W_CLK rising edges after the register is full will shift data out causing data that is left in the register to be out-of-sequence and corrupted. The serial mode must be entered from the default parallel mode (see Figure 17). Data is loaded beginning with W0 and ending with W39. One note of caution: the 8-bit *parallel* word (W0)—xxxxx011—that invokes the serial mode should be overwritten with a valid 40-bit serial word immediately after entering the serial mode to prevent unintended engaging of the 6× REFCLK multiplier or entry into

the factory test mode. Exit from serial mode to parallel mode is only possible using the RESET command.

The function assignments of the data and control words are shown in Tables I and III; the detailed timing sequence for updating the output frequency and/or phase, resetting the device, engaging the 6× REFCLK multiplier, and powering up/down, are shown in the timing diagrams of Figures 13 through 20. As a programming example for the following DDS characteristics:

1. Phase set to 11.25°
2. 6× REFCLK multiplier engaged
3. Powered-up mode selected
4. Output = 10 MHz (for 180 MHz system clock)

In parallel mode, user would program the 40-bit control word (composed of five 8-bit loads) as follows:

W0 = 00001001
W1 = 00001110
W2 = 00111000
W3 = 11100011
W4 = 10001110

If in serial mode, load the 40 bits starting from the LSB location of W4 in the above array, loading from right to left, and ending with the MSB of W0.

Table I. 8-Bit Parallel-Load Data/Control Word Functional Assignment

Word	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]
W0	Phase–b4 (MSB)	Phase–b3	Phase–b2	Phase–b1	Phase–b0 (LSB)	Power-Down	Logic 0*	6× REFCLK Multiplier Enable
W1	Freq–b31 (MSB)	Freq–b30	Freq–b29	Freq–b28	Freq–b27	Freq–b26	Freq–b25	Freq–b24
W2	Freq–b23	Freq–b22	Freq–b21	Freq–b20	Freq–b19	Freq–b18	Freq–b17	Freq–b16
W3	Freq–b15	Freq–b14	Freq–b13	Freq–b12	Freq–b11	Freq–b10	Freq–b9	Freq–b8
W4	Freq–b7	Freq–b6	Freq–b5	Freq–b4	Freq–b3	Freq–b2	Freq–b1	Freq–b0 (LSB)

*This bit is always Logic 0 unless invoking the serial mode (see Figure 17). After serial mode is entered, this data bit must be set back to Logic 0 for proper operation.

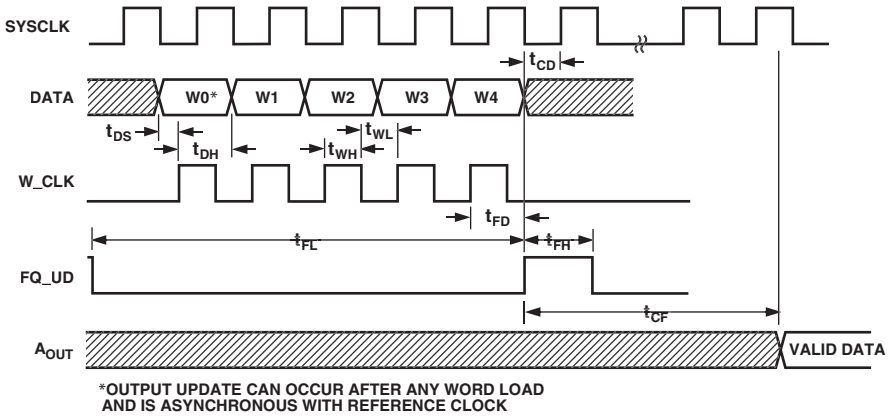


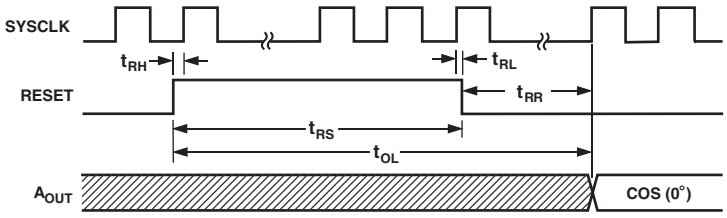
Figure 13. Parallel Load Frequency/Phase Update Timing Sequence

Note: To update W0 it is not necessary to load W1 through W4. Simply load W0 and assert FQ_UD. To update W1, reload W0 then W1—users do not have random access to programming words.

Table II. Timing Specifications

Symbol	Definition	Min
t_{DS}	Data Setup Time	3.5 ns
t_{DH}	Data Hold Time	3.5 ns
t_{WH}	W_CLK High	3.5 ns
t_{WL}	W_CLK Low	3.5 ns
t_{CD}	REFCLK Delay after FQ_UD	3.5 ns*
t_{FH}	FQ_UD High	7.0 ns
t_{FL}	FQ_UD Low	7.0 ns
t_{FD}	FQ_UD Delay after W_CLK	7.0 ns
t_{CF}	Output Latency from FQ_UD	
	Frequency Change	18 SYSCLK Cycles
	Phase Change	13 SYSCLK Cycles

*Specification does not apply when the 6× REFCLK multiplier is engaged.



SYMBOL	DEFINITION	MIN SPEC
t_{RH}	CLK DELAY AFTER RESET RISING EDGE	3.5ns*
t_{RL}	RESET FALLING EDGE AFTER CLK	3.5ns*
t_{RR}	RECOVERY FROM RESET	2 SYSCLK CYCLES
t_{RS}	MINIMUM RESET WIDTH	5 SYSCLK CYCLES
t_{OL}	RESET OUTPUT LATENCY	13 SYSCLK CYCLES

*SPECIFICATIONS DO NOT APPLY WHEN THE REF CLOCK MULTIPLIER IS ENGAGED

Figure 14. Master Reset Timing Sequence

Note: The timing diagram above shows the minimal amount of reset time needed before writing to the device. However, the master reset does not have to be synchronous to the SYSCLK if the minimal time is not required.

Results of Reset, Figure 14

– Phase accumulator zeroed such that the output = 0 Hz (dc)
– Phase offset register set to 0 such that DAC IOUT = full-scale output and IOUTB = zero mA output
– Internal programming address pointer reset to W0
– Power-down bit reset to 0 (power-down disabled)
– 40-bit data input register is NOT cleared
– 6× reference clock multiplier is disabled
– Parallel programming mode selected by default

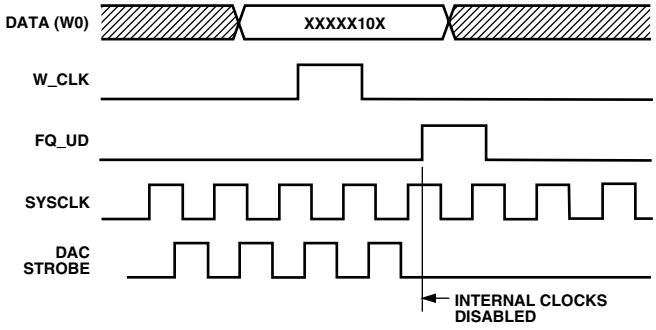


Figure 15. Parallel Load Power-Down Sequence/ Internal Operation

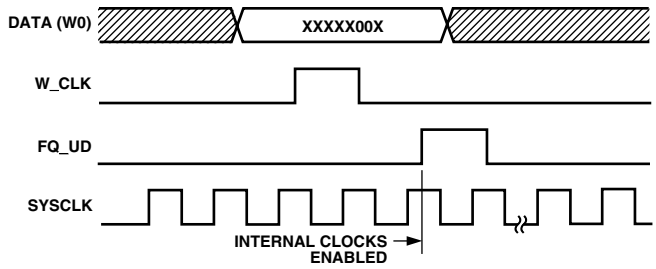


Figure 16. Parallel Load Power-Up Sequence (to Recover from Power-Down)/Internal Operation

Entry to the serial mode, see Figure 17, is via the parallel mode, which is selected by default after a RESET is asserted. One needs only to program the first eight bits (word W0) with the sequence xxxxx011 as shown in Figure 17 to change from parallel to serial mode. The W0 programming word may be sent over the 8-bit data bus or hardwired as shown in Figure 18. After serial mode is achieved, the user must follow the programming sequence of Figure 19.

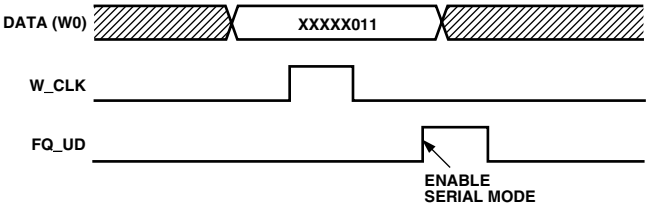


Figure 17. Serial Load Enable Sequence

Note: After serial mode is invoked, it is best to immediately write a valid 40-bit serial word (see Figure 19), even if it is all zeros, followed by a FQ_UD rising edge to flush the residual data left in the DDS core. A valid 40-bit serial word is any word where W33 is Logic 0.

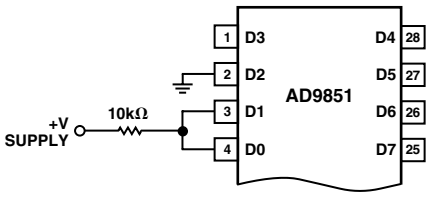


Figure 18. Hardwired xxxxx011 Configuration for Serial Load Enable Word W0 in Figure 17

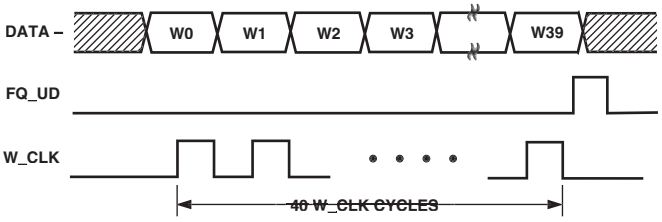


Figure 19. Serial Load Frequency/Phase Update Sequence

Table III. 40-Bit Serial Load Word Functional Assignment

W0	Freq–b0 (LSB)
W1	Freq–b1
W2	Freq–b2
W3	Freq–b3
W4	Freq–b4
W5	Freq–b5
W6	Freq–b6
W7	Freq–b7
W8	Freq–b8
W9	Freq–b9
W10	Freq–b10
W11	Freq–b11
W12	Freq–b12
W13	Freq–b13
W14	Freq–b14
W15	Freq–b15
W16	Freq–b16
W17	Freq–b17
W18	Freq–b18
W19	Freq–b19
W20	Freq–b20
W21	Freq–b21
W22	Freq–b22
W23	Freq–b23
W24	Freq–b24
W25	Freq–b25
W26	Freq–b26
W27	Freq–b27
W28	Freq–b28
W29	Freq–b29
W30	Freq–b30
W31	Freq–b31 (MSB)
W32	6× REFCLK Multiplier Enable
W33	Logic 0*
W34	Power-Down
W35	Phase–b0 (LSB)
W36	Phase–b1
W37	Phase–b2
W38	Phase–b3
W39	Phase–b4 (MSB)

*This bit is always Logic 0.

Figure 20 shows a normal 40-bit serial word load sequence with W33 always set to Logic 0 and W34 set to Logic 1 or Logic 0 to control the power-down function. The logic states of the remaining 38 bits are unimportant and are marked with an X, indicating "don't care" status. To power down, set W34 = 1. To power up from a powered down state, change W34 to Logic 0. Wake-up from power-down mode requires approximately 5 µs.

Note: The 40-bit input register of the AD9851 is fully programmable while in the power-down mode.

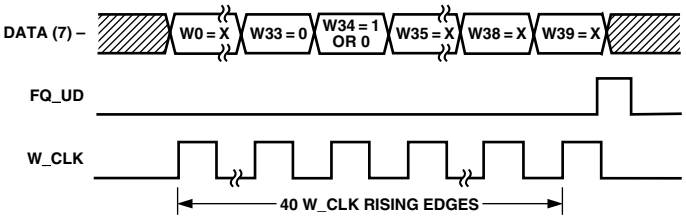
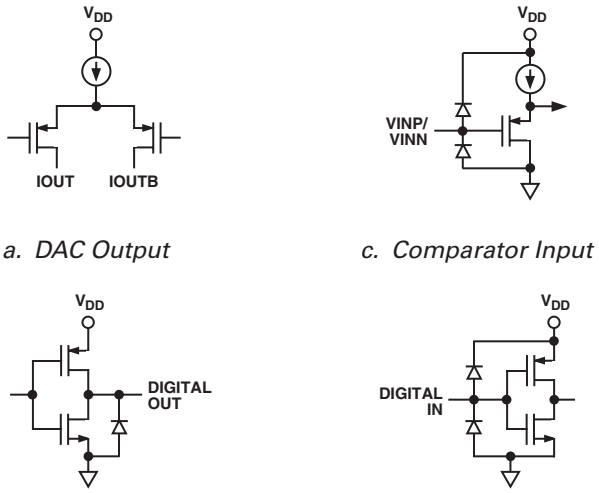


Figure 20. Serial Load Power-Down\Power-Up Sequence



a. DAC Output

c. Comparator Input

b. Comparator Output

d. Digital Input

Figure 21. I/O Equivalent Circuits

PCB LAYOUT INFORMATION

The AD9851/CGPCB and AD9851/FSPCB evaluation boards (Figures 22 through 25 and TPCs 1 and 2) represent typical implementations of the AD9851 and exemplify the use of high frequency/high resolution design and layout practices. The printed circuit board that contains the AD9851 should be a multilayer board that allows dedicated power and ground planes. The power and ground planes should (as much as possible) be free of etched traces that cause discontinuities in the planes. It is recommended that the top layer of the board also contain an interspatial ground plane that makes ground available without vias for the surface-mount devices. If separate analog and digital system ground planes exist, they should be connected together at the AD9851 evaluation board for optimum performance.

Avoid running digital lines under the device as these will couple unnecessary noise onto the die. The power supply lines to the AD9851 should use as large a trace as possible to provide a low-impedance path and reduce the effects of switching currents on the power supply line. Fast switching signals like clocks should use microstrip, controlled impedance techniques where possible. Avoid crossover of digital and analog signal paths. Traces on opposite sides of the board should run at right angles to each other. This will reduce crosstalk between the lines.

Good power supply decoupling is also an important consideration. The analog (AVDD) and digital (DVDD) supplies to the AD9851 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supply pins should be decoupled to AGND and DGND, respectively, with high quality ceramic chip capacitors. To achieve best performance from the decoupling capacitors, they should be placed as close as possible to the device. In systems where a common supply is used to drive both the AVDD and DVDD supplies of the AD9851, it is recommended that the system's AVDD supply be used.

Analog Devices applications engineering support is available to answer additional questions on grounding and PCB layout. Call 1-800-ANALOGD.

EVALUATION BOARDS

Two versions of the AD9851 evaluation board are available. The evaluation boards facilitate easy implementation of the device for bench-top analysis and serve as a reference for PCB layout.

The AD9851/FSPCB is intended for applications where the device will primarily be used as a frequency synthesizer. This version is optimized for connection of the AD9851 internal D/A converter output to a 50 Ω spectrum analyzer input. The internal comparator of the AD9851 is made available for use via wire hole access. The comparator inputs are externally pulled to opposing voltages to prevent comparator chatter due to floating inputs. The DDS DAC output is unfiltered and no reference oscillator is provided. This is done in recognition of the fact that many users may find an oscillator to be a liability rather than an asset. See Figure 22 for an electrical schematic.

The AD9851/CGPCB is intended for applications using the device as a CMOS output clock generator. It connects the AD9851 DAC output to the internal comparator input via a single-ended, 70 MHz low pass, 7th order, elliptic filter. To minimize output jitter of the comparator, special attention has been given to the low-pass filter design. Primary considerations were input and output impedances (200 Ω) and a very steep roll-off characteristic to attenuate unwanted, nearby alias signals. The high impedance of the filter allows the DAC to develop 1 V p-p (with 10 mA) across the two 200 Ω resistors at the input and output of the filter. This voltage is entirely sufficient to optimally drive the AD9851 comparator. This filter was designed with the assumption that the AD9851 DDS is at full clock speed (180 MHz). If this is not the case, filter specifications may need to change to achieve proper attenuation of anticipated alias signals. BNC connectors allow convenient observation of the comparator CMOS output and input, as well as that of the DAC. No reference oscillator is provided for reasons stated above. This model allows easy evaluation of the AD9851 as a frequency and phase-agile CMOS output clock source (see Figure 24 for electrical schematic).

Jitter Reduction Note

The AD9851/CGPCB has a wideband DDS fundamental output, dc to 70 MHz, and the on-chip comparator has even more bandwidth. To optimize low jitter performance users should consider bandpass filtering of the DAC output if only a narrow bandwidth is required. This will reduce jitter caused by spurious, nonharmonic signals above and below the desired signal. Lowering the applied V_{DD} helps in reducing comparator switching noise by reducing $\Delta V/\Delta T$ of the comparator outputs. For optimum jitter performance, users should avoid the very busy digital environment of the on-chip comparator and opt for an external, high speed comparator.

Both versions of the AD9851 evaluation boards are designed to interface to the parallel printer port of a PC. The operating software (C++) runs under Microsoft® Windows® (Windows 3.1 and Windows 95); Windows NT® not supported and provides a user-friendly and intuitive format for controlling the functionality and observing the performance of the device. The 3.5-in disk provided with the evaluation board contains an executable file that displays the AD9851 function-selection screen. The evaluation board may be operated with 3.0 V or 5 V supplies. Evaluation boards are configured at the factory for an external clock input. If the optional on-board crystal clock source is installed, resistor R2 (50 Ω) must be removed.

EVALUATION BOARD INSTRUCTIONS

Required Hardware/Software

Personal computer operating in Windows 3.1 or 95 environment (does not support Windows NT)

Printer port, 3.5-in floppy drive, mouse, and Centronics compatible printer cable, 3 V to 5 V voltage supply

Crystal clock oscillator or high frequency signal generator (sine wave output) with dc offset capability

AD9851 Evaluation Board Software disk and AD9851/FSPCB or AD9851/CGPCB Evaluation Board

Setup

Copy the contents of the AD9851 disk onto the host PCs hard drive. (There are two files, WIN9851.EXE version 1.x and Bwcc.dll.) Connect the printer cable from the computer to the evaluation board. Use a good quality cable as some cables do not connect every wire that the printer port supports.

Apply power to AD9851 evaluation board. The AD9851 is powered separately from the other active components on the board via connector marked DUT +V. The connector marked 5 V is used to power the CMOS latches, optional crystal oscillator and pull-up resistors. Both 5 V and DUT +V may be tied together for ease of operation without adverse affects. The AD9851 may be powered with 2.7 V to 5.25 V.

Connect an external 50 Ω Z clock source or remove R2 and install a suitable crystal clock oscillator with CMOS output levels at Y1. A sine wave signal generator may be used as a clock source at frequencies >50 MHz by dc offsetting the output signal to 1/2 the supply voltage to the AD9851. This method requires a minimum of 2 V p-p signal and disabling of the 6× REFCLK Multiplier function.

Locate the file called WIN9851.EXE and execute that program. The computer monitor should show a control panel that allows operation of the AD9851 evaluation board by use of a mouse.

Operation

On the control panel locate the box labeled COMPUTER I/O. Click the correct parallel printer port for the host computer and then click the TEST box. A message will appear indicating whether the selection of output port is correct. Choose other ports as necessary to achieve a correct port setting.

Click the MASTER RESET button. This will reset the part to 0 Hz, 0° phase, parallel programming mode. The output from the DAC IOUT should be a dc voltage equal to the full-scale output of the AD9851 (1 V for the AD9851/CGPCB and 0.5 V for the AD9851/FSPCB), while the DAC IOUTB should be 0 V for both evaluation boards. *RESET should always be the first command to the AD9851 following power-up*.

Locate the CLOCK SECTION and place the cursor in the FREQUENCY box. Enter the clock frequency (in MHz) that will be applied to the reference clock input of the AD9851. Click the PLL box in the CONTROL FUNCTION menu if the 6× reference clock multiplier is to be engaged—a check mark will appear when engaged. When the reference clock multiplier is engaged, software will multiply the value entered in the frequency box by 6; otherwise, the value entered is the value used. Click the LOAD button or press the enter key.

Move the cursor to the OUTPUT FREQUENCY box and type in the desired frequency (in MHz). Click the LOAD button or press the enter key. The BUS MONITOR section of the control panel will show the 32-bit frequency word and 8-bit phase/control word. Upon completion of this step, the AD9851 output should be active at the programmed frequency/phase.

Changing the output phase is accomplished by clicking the down arrow in the OUTPUT PHASE DELAY box to make a selection and then clicking the LOAD button. Note: clicking the load buttons of the clock frequency box, the output frequency box, or the phase box will *automatically* initiate a reloading of all three boxes and issuance of a FQ_UD (frequency update) pulse. To bypass this automatic reloading and frequency update sequence, refer to the note below.

Other operational modes (Frequency Sweeping, Sleep, Serial Input) are available. Frequency sweeping allows the user to enter a start and stop frequency and to specify the frequency step size. Sweeping begins at the start frequency, proceeds to the stop frequency in a linear manner, reverses direction, and sweeps back to the start frequency repeatedly.

Note: For those who may be operating multiple AD9851 evaluation boards from one computer, a MANUAL FREQUENCY UPDATE option exists. By eliminating the automatic issuance of an FQ_UD, the user can load the 40-bit input registers of multiple AD9851s without transferring that data to the internal accumulators. When all input registers are loaded, a single FREQUENCY UPDATE pulse can be issued to all AD9851s. A block diagram of this technique is shown in the AD9851 data sheet as a quadrature oscillator application. This single pulse synchronizes all the units so that their particular phases and frequencies take effect simultaneously. Proper synchronization requires that each AD9851 be clocked by the same reference clock source and that each oscillator be in an identical state while being programmed. RESET command ensures identical states. When manual frequency update is selected, a new box labeled FREQUENCY UPDATE will appear just above the frequency sweeping menu. Clicking the box initiates a single FQ_UD pulse.

Note: RESET can be used to synchronize multiple oscillators. If several oscillators have already been programmed at various phases or frequencies, issuance of a RESET pulse will set their outputs to 0 Hz and 0 phase. By issuing a common FQ_UD, the previously programmed information in the 40-bit input registers will transfer once again to the DDS core and take effect in 18 clock cycles. This is due to the fact that RESET does not affect the contents of the 40-bit input register in any way.

The AD9851/FSPCB provides access into and out of the on-chip comparator via test point pairs (each pair has an active input and a ground connection). The two active inputs are labeled TP1 and TP2. The unmarked hole next to each labeled test point is a ground connection. The two active outputs are labeled TP5 and TP6. Adjacent to those test points are unmarked ground connections. To prevent unwanted comparator chatter when not in use, the two inputs are pulled either to ground or +V via 1 kΩ resistors.

The AD9851/CGPCB provides BNC inputs and outputs associated with the on-chip comparator and an onboard, 7th order, 200 Ω input /output Z, elliptic 70 MHz low-pass filter. Jumpering (soldering a wire) E1 to E2, E3 to E4, and E5 to E6 connects the onboard filter and the midpoint switching voltage to the comparator. Users may elect to insert their own filter and comparator threshold voltage by removing the jumpers and inserting a filter between J7 and J6 and providing a comparator threshold voltage at E1.

Use of the XTAL oscillator socket on the evaluation board to supply the clock to the AD9851 requires the removal R2 (a 50 Ω chip resistor) unless the oscillator can drive a 50 Ω load. The crystal oscillator should be either TTL or CMOS (preferably) compatible.

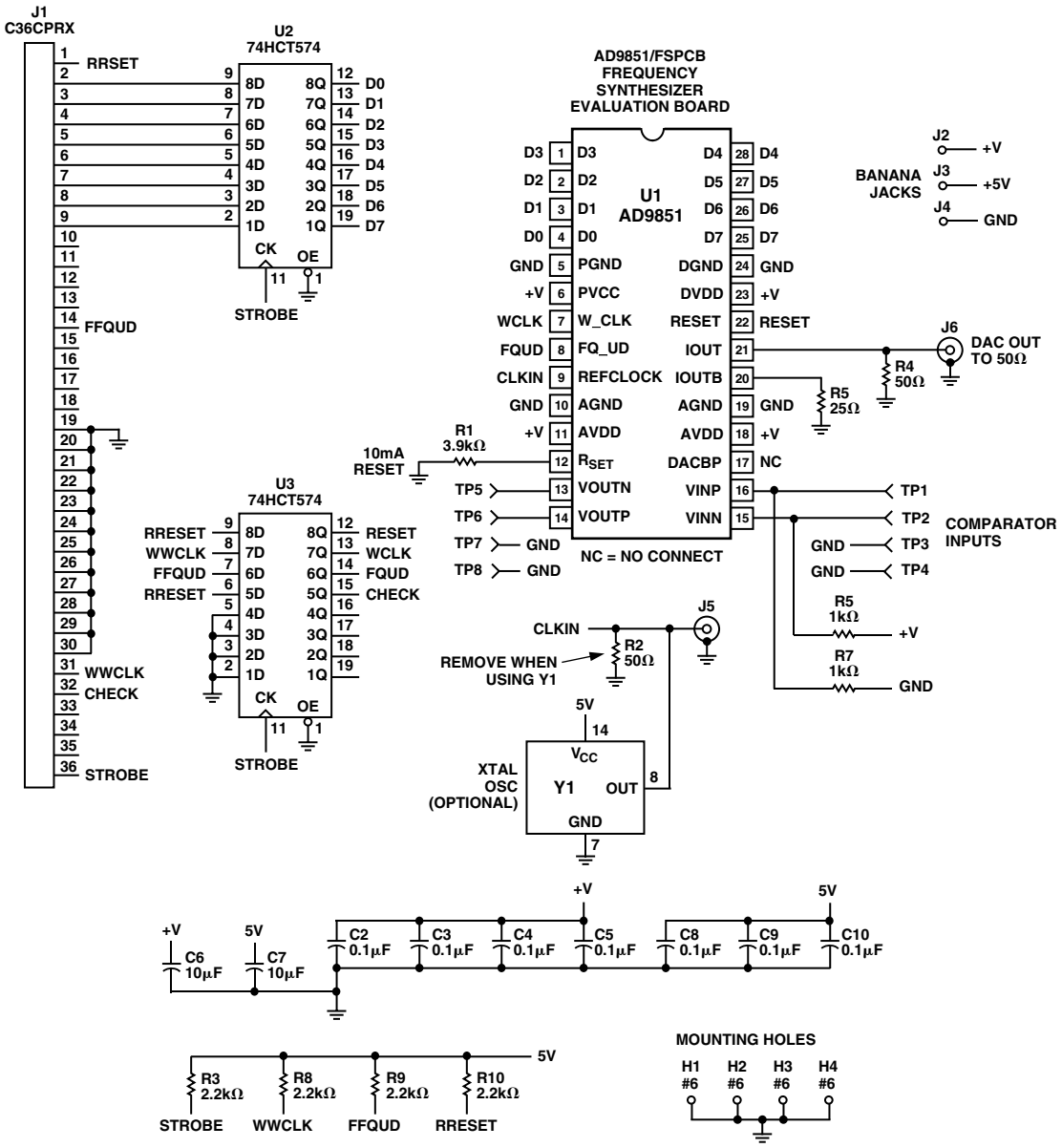
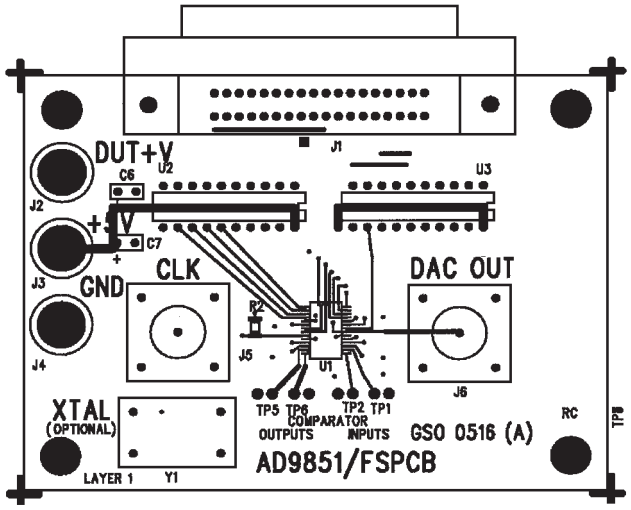
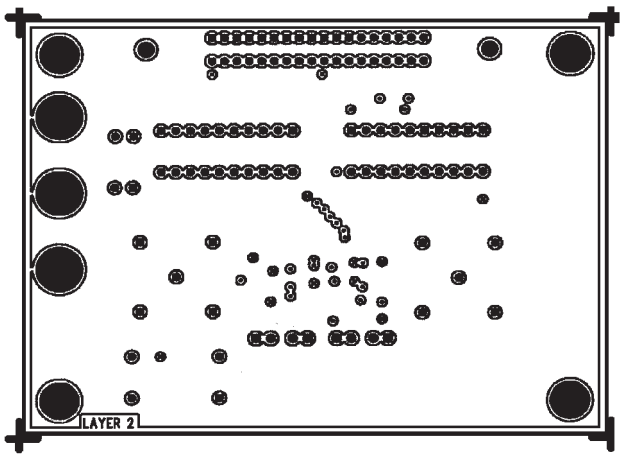


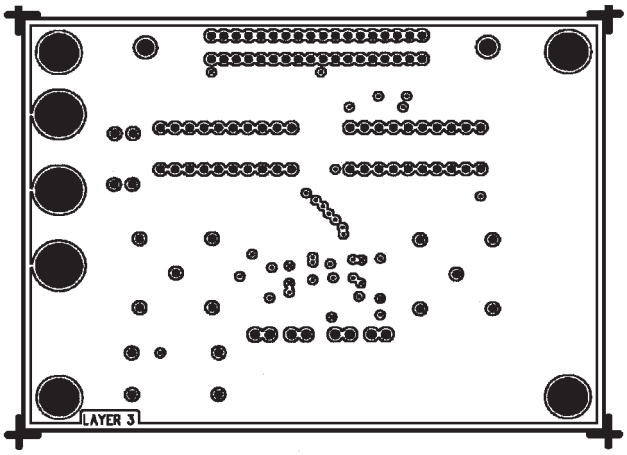
Figure 22. FSPCB Electrical Schematic



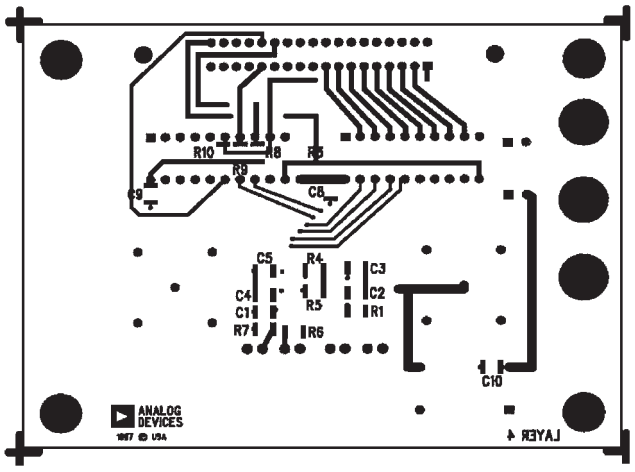
23a. FSPCB Top Layer



23c. FSPCB Ground Plane



23b. FSPCB Power Plane



23d. FSPCB Bottom Layer

Figure 23. FSPCB Evaluation Board 4-Layer PCB Layout Patterns

AD9851/FSPCB Evaluation Board Parts List—GSO 0516(A)

Miscellaneous Hardware	Ref. Des.
1 Amp 552742-1, 36-Pin Plastic, Right Angle, PC Mount, Female	J1
1 Banana Jack–Color Not Important	J2
1 Yellow Banana Jack	J3
1 Black Banana Jack	J4
2 BNC Coax. Connector, PC Mount	J5, J6
1 AD9851/FSPCB Evaluation Board GSO 0516(A)	None
4 AMP 5-330808-6, Open-Ended Pin Socket	None
2 #2-56 Hex Nut (to Fasten J1)	None
2 #2-56 × 3/8 Binder Head Machine Screw (to Fasten J1)	None
4 #4-40 Hex Nut (to Fasten Standoffs to Board)	None
4 #4 1-In Metal Stand-Off	None

Miscellaneous Hardware	Ref. Des.
Decoupling Capacitors	
7 Size 1206 Chip Capacitor, 0.1 μF	C2–C5, C8–C10
2 Tantalum Capacitors, 10 μF	C6, C7
Resistors	
1 25 Ω Chip Resistor, Size 1206	R5
2 50 Ω Chip Resistor, Size 1206	R2, R4
1 3.9 kΩ Chip Resistor, Size 1206	R1
4 2 kΩ or 2.2 kΩ Chip Resistor, Size 1206	R3, R8, R9, R10
2 1 kΩ Chip Resistor, Size 1206	R6, R7
Integrated Circuits	
1 AD9851 Direct Digital Synthesizer, Surface-mount	U1
2 74HCT574AN HCMOS Octal Flip-Flop, Through-Hole Mount	U2, U3

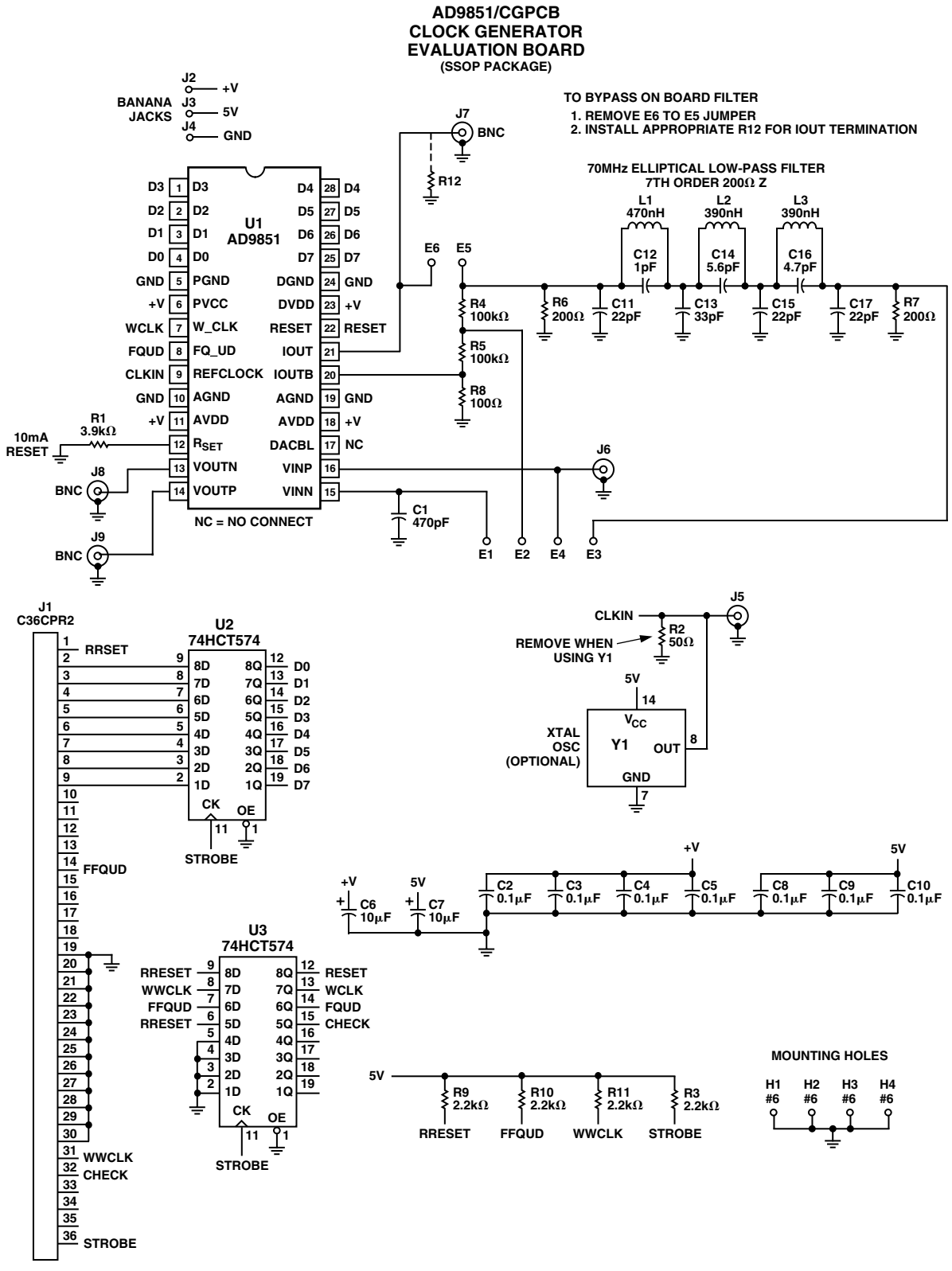
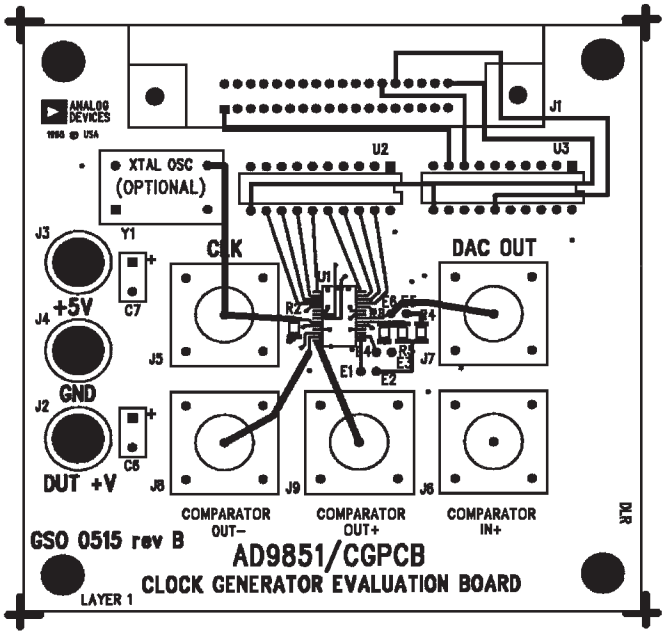
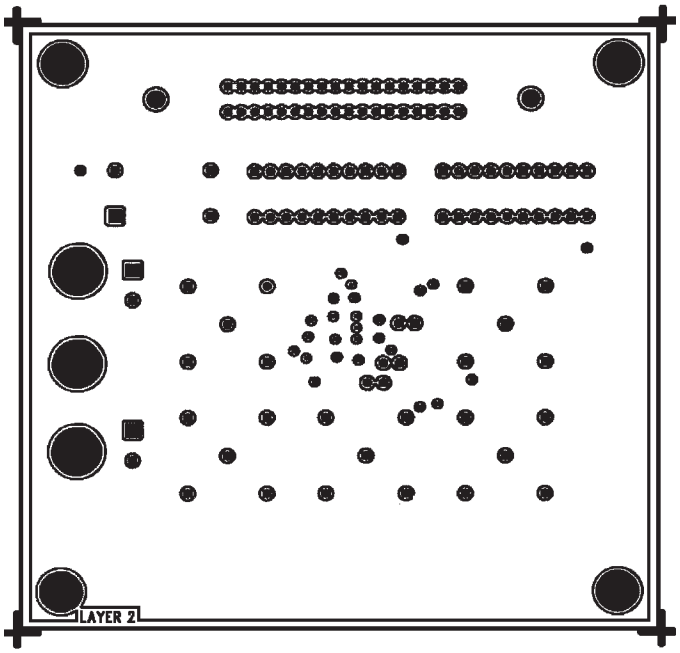


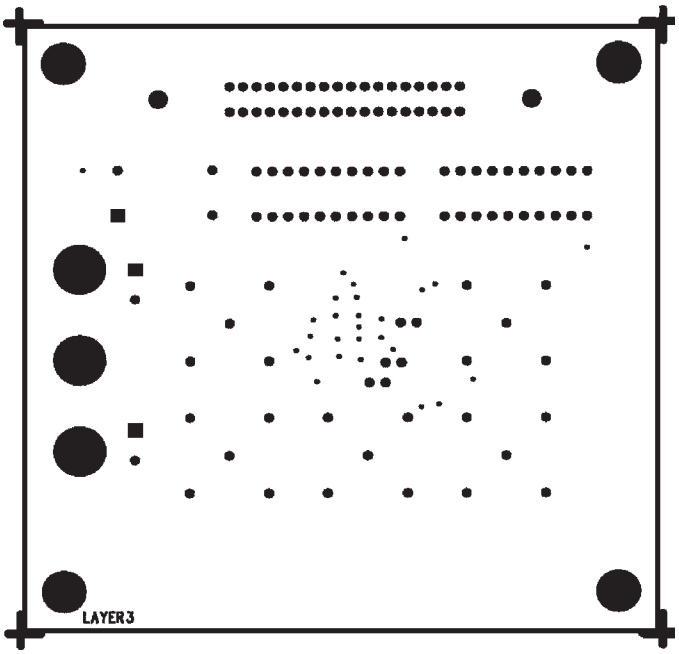
Figure 24. CGPCB Electrical Schematic



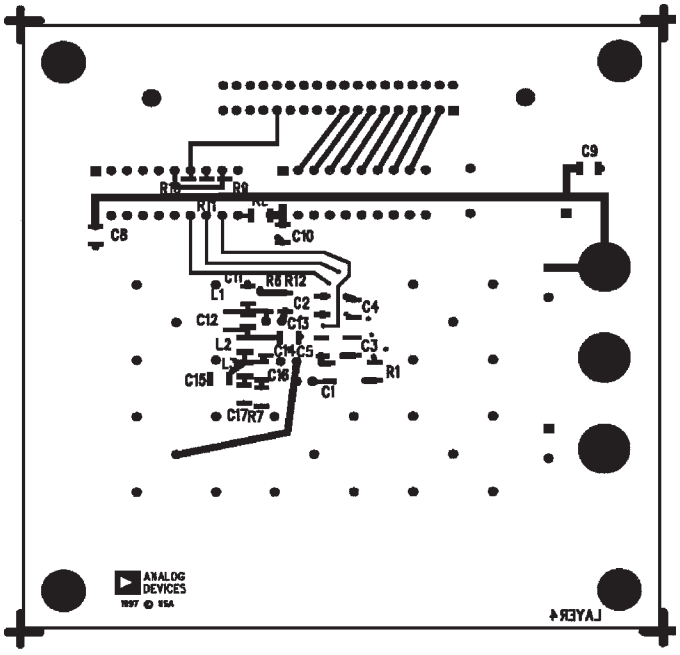
25a. CGPCB Top Layer



25c. CGPCB Power Plane



25b. CGPCB Ground Plane



25d. CGPCB Bottom Layer

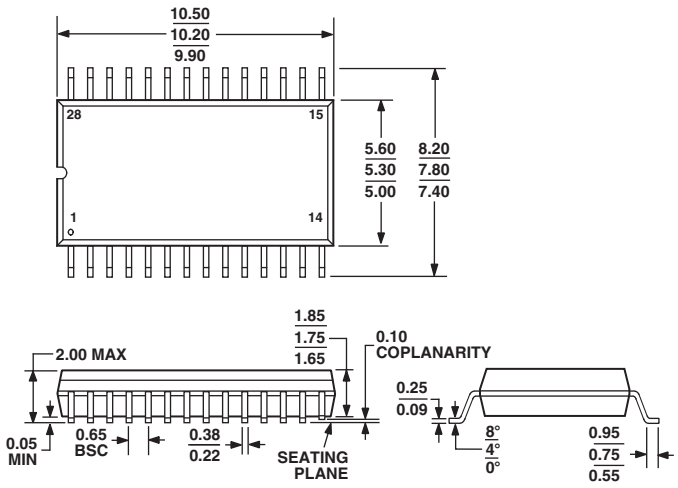
Figure 25. FSPCB Evaluation Board 4-Layer PCB Layout Patterns

CGPCB Evaluation Board Parts List—GSO 0515(B)

Miscellaneous Hardware	Ref. Des.
1 Amp 552742-1, 36-Pin Plastic, Right Angle, PC Mount, Female	J1
1 Banana Jack—Color Not Important	J2
1 Yellow Banana Jack	J3
1 Black Banana Jack	J4
5 BNC Coax. Connector, PC Mount	J5, J6, J7, J8, J9
1 AD9851/CGPCB Evaluation Board GSO 0515(B)	None
4 AMP 5-330808-6, Open-Ended Pin Socket	None
2 #2-56 Hex Nut (to Fasten J1)	None
2 #2-56 × 3/8 Binder Head Machine Screw (to Fasten J1)	None
4 #4-40 Hex Nut (to Fasten Stand-Offs to Board)	None
4 #4 1-In Metal Stand-Off	None
Decoupling Capacitors	
1 Size 1206 Chip Capacitor, 470 pF	C1
7 Size 1206 Chip Capacitor, 0.1 μF	C2–C5, C8–C10
2 Tantalum Capacitors, 10 μF	C6, C7
Resistors	
1 3.9 kΩ Chip Resistor, Size 1206	R1
1 50 Ω Chip Resistor, Size 1206	R2
4 2 kΩ or 2.2 kΩ Chip Resistor, Size 1206	R3, R9, R10, R11
2 100 kΩ Chip Resistor, Size 1206	R4, R5
2 200 Ω Chip Resistor, Size 1206	R6, R7
1 100 Ω Chip Resistor, Size 1206	R8
1 Dummy Resistor (for Optional Installation)	R12
Filter Capacitors (70 MHz 7-Pole Elliptic Filter)	
3 22 pF Chip Capacitor, Size 1206	C11, C15, C17
1 1 pF Chip Capacitor, Size 1206	C12
1 33 pF Chip Capacitor, Size 1206	C13
1 5.6 pF Chip Capacitor, Size 1206	C14
1 4.7 pF Chip Capacitor, Size 1206	C16
Inductors (70 MHz 7-Pole Elliptic Filter)	
1 470 nH Chip Inductor, Coil Craft 1008CS	L1
2 390 nH Chip Inductor, Coil Craft 1008CS	L2, L3
Integrated Circuits	
1 AD9851 Direct Digital Synthesizer, Surface-mount	U1
2 74HCT574AN HCMOS Octal Flip-Flop, Through-Hole Mount	U2, U3

OUTLINE DIMENSIONS

28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AH

C00633–0–1/04(D)

Revision History

Location	Page
1/04—Data Sheet changed from REV. C to REV. D	
Renumbered figures and TPCs	Universal
Changes to SPECIFICATIONS	2
Updated ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	23