Programmable Digital QPSK/16-QAM Modulator

AD9853

OBSOLETE

FEATURES

Universal Low Cost Solution for HFC Network
Return-Channel T_X Function: 5 MHz–42 MHz/ 5 MHz–65 MHz
165 MHz Internal Reference Clock Capability
Includes Programmable Pulse-Shaping FIR Filters and Programmable Interpolating Filters
FSK/QPSK/DQPSK/16-QAM/D16-QAM Modulation Formats
6× Internal Reference Clock Multiplier
Integrated Reed-Solomon FEC Function
Programmable Randomizer/Preamble Function
Supports Interoperable Cable Modem Standards
Internal SINx/x Compensation
>50 dB SFDR @ 42 MHz Output Frequency (Single Tone)
Controlled Burst Mode Operation
+3.3 V to +5 V Single Supply Operation
Low Power: 750 mW @ Full Clock Speed (3.3 V Supply)
Space Saving Surface Mount Packaging

APPLICATIONS

HFC Data, Telephony and Video Modems
Wireless LAN

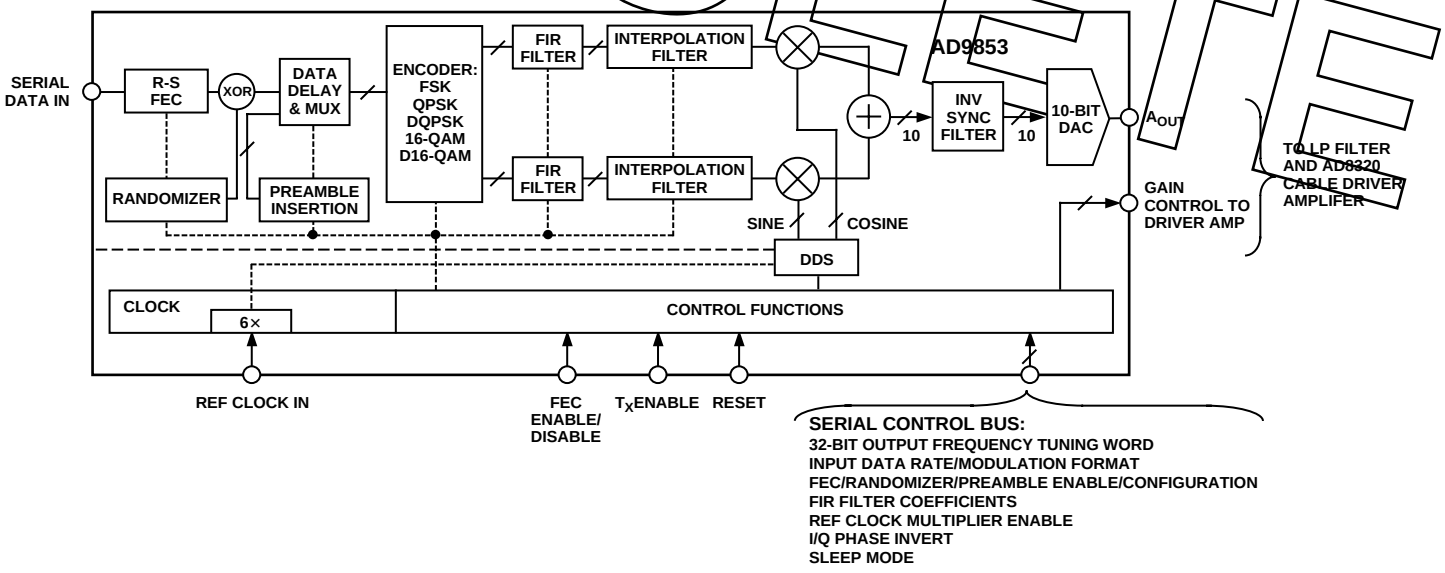
GENERAL DESCRIPTION

The AD9853 integrates a high speed direct-digital synthesizer (DDS), a high performance, high speed digital-to-analog converter (DAC), digital filters and other DSP functions onto a single chip, to form a complete and flexible digital modulator device. The AD9853 is intended to function as a modulator in network applications such as interactive HFC, WLAN and MMDS, where cost, size, power dissipation, functional integration and dynamic performance are critical attributes.

The AD9853 is fabricated on an advanced CMOS process and it sets a new standard for CMOS digital modulator performance. The device is loaded with programmable functionality and provides a direct interface port to the AD8320, digitally-programmable cable driver amplifier. The AD9853/AD8320 chipset forms a highly integrated, low power, small footprint and cost-effective solution for the HFC return-path requirement and other more general purpose modulator applications.

The AD9853 is available in a space saving surface mount package and is specified to operate over the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



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AD9853–SPECIFICATIONS (V_S = +3.3 V ± 5%, R_{SET} = 3.9 kΩ, Reference Clock Frequency = 20.48 MHz with 6× REFCLK Enabled, Symbol Rate = 2.56 MS/s, α = 0.25, unless otherwise noted)

Parameter	Temp	Test Level	Min	Typ	Max	Units
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
6× REFCLK Disabled (+3.3 V Supply)	Full	IV	42		126	MHz
6× REFCLK Enabled (+3.3 V Supply)	Full	IV	7		21	MHz
6× REFCLK Disabled (+5 V Supply)	Full	IV	108		168	MHz
6× REFCLK Enabled (+5 V Supply)	Full	IV	18		28	MHz
Duty Cycle	+25°C	IV	40		60	%
Input Capacitance	+25°C	V		3		pF
Input Impedance	+25°C	V		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				10		Bits
Full-Scale Output Current	+25°C	IV	5	10	20	mA
Gain Error	+25°C	I	–10		+10	% FS
Output Offset	+25°C	I			10	μA
Output Offset Temperature Coefficient	Full	V		50		nA/°C
Differential Nonlinearity	+25°C	I		0.5	0.75	LSB
Integral Nonlinearity	+25°C	I		0.5	1.5	LSB
Output Capacitance	+25°C	V		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
6× REFCLK Enabled	+25°C	V		–100		dBc
6× REFCLK Disabled	+25°C	V		–110		dBc
Voltage Compliance Range	+25°C	I	–0.5		+1.5	V
Wideband SFDR (Single Tone):						
1 MHz A_{OUT}	+25°C	IV	62	68		dBc
20 MHz A_{OUT}	+25°C	IV	52	54		dBc
42 MHz A_{OUT}	+25°C	IV	48	50		dBc
65 MHz A_{OUT}[1]	+25°C	IV	42	44		dBc
MODULATOR CHARACTERISTICS						
I/Q Offset	+25°C	IV	48			dB
Adjacent Channel Power	+25°C	IV	44			dBm
Error Vector Magnitude	+25°C	IV		1	2	%
In-Band Spurious Emission						
5 MHz–42 MHz A_{OUT}	+25°C	IV		42		dBc
5 MHz–65 MHz A_{OUT}[1]	+25°C	IV		40		dBc
Passband Amplitude Ripple	+25°C	V		±0.3		dB
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			25	MHz
Minimum Clock Pulsewidth Low (t_{PWL})	Full	IV	10			ns
Minimum Clock Pulsewidth High (t_{PWH})	Full	IV	10			ns
Maximum Clock Rise/Fall Time	Full	IV	100			ns
Minimum Data Setup Time (t_{DS})	Full	IV	10			ns
Minimum Data Hold Time (t_{DH})	Full	IV	10			ns
Minimum Clock Setup—Stop Condition (t_{CS})	Full	IV	10			ns
Minimum Clock Hold—Start Condition (t_{CH})	Full	IV	10			ns
RESET						
Minimum T_XENABLE Low to RESET Low (t_{TR})	Full	IV	10			ns
Minimum RESET High to Start Condition (t_{RH})	Full	IV	10			ns
FEC ENABLE						
Minimum FEC ENABLE/DISABLE to T_XENABLE High (t_{FH})	Full	IV	0			ns
Minimum FEC ENABLE/DISABLE to T_XENABLE Low (t_{FL})	Full	IV	0			ns

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Parameter	Temp	Test Level	Min	Typ	Max	Units
TIMING CHARACTERISTICS (Continued)						
Wake-Up Time–PLL Power-Down	+25°C	IV		1		ms
Wake-Up Time–DAC Power-Down	+25°C	IV		200		µs
Wake-Up Time–Digital Power-Down	+25°C	IV		5		µs
Data Latency (t_{DL})	+25°C	IV		6		Symbols
Minimum RESET Pulsewidth Low (t_{RL})	+25°C	IV		10		ns
CMOS LOGIC INPUTS						
Logic "1" Voltage, +5 V Supply	+25°C	I	+3.5			V
Logic "1" Voltage, +3.3 V Supply	+25°C	I	+3.0			V
Logic "0" Voltage	+25°C	I			+0.4	V
Logic "1" Current	+25°C	I			12	µA
Logic "0" Current	+25°C	I			12	µA
Input Capacitance	+25°C	V		3		pF
POWER SUPPLY[2]						
$+V_S$ Current (+3.3 V + 5%)						
Full Operating Conditions	+25°C	I		184	230	mA
With PLL Power-Down Enabled	+25°C	I		178	224	mA
With DAC Power-Down Enabled	+25°C	I		170	216	mA
With Digital Power-Down Enabled	+25°C	I		36	54	mA
With All Power-Down Enabled	+25°C	I		16	20	mA
$+V_S$ Current (+5 V + 5%)	+25°C	I		400	595	mA

NOTES
[1]Reference clock = 28 MHz with clock multiplier enabled; supply voltage = +5 V.
[2]Maximum values are obtained under worst case operating modes. Typical values are valid for most applications.

Specifications subject to change without notice.

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EXPLANATION OF TEST LEVELS

Test Level

I – 100% Production Tested.
III – Sample Tested Only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature . . . . . +150°C
V_S . . . . . +6 V
Digital Inputs . . . . . –0.7 V to $+V_S$
Digital Output Current . . . . . 5 mA
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –40°C to +85°C
Lead Temperature (10 sec Soldering) . . . . . +300°C
MQFP θ_{JA} Thermal Impedance . . . . . 36°C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9853AS	–40°C to +85°C	Metric Quad Flatpack (MQFP)	S-44A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9853 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

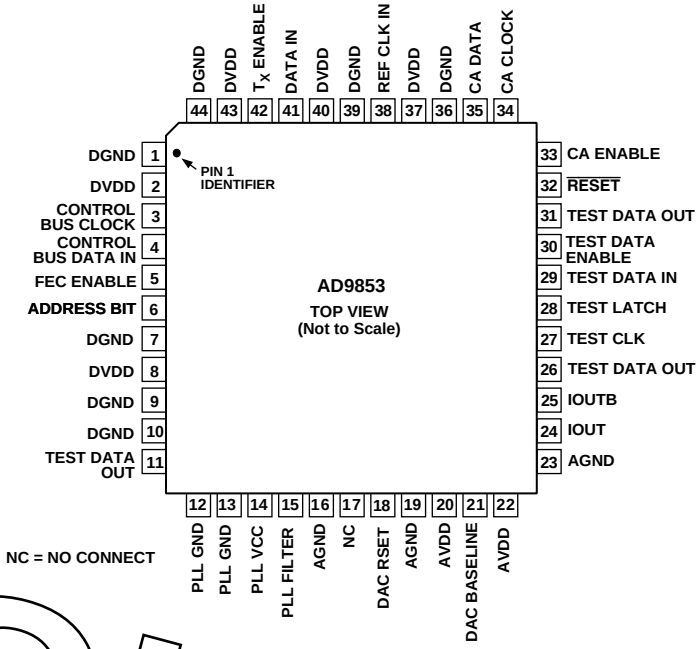


PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Pin Function
1, 7, 9, 10, 36, 39, 44	DGND	Digital Ground
2, 8, 37, 40, 43	DVDD	Digital Supply Voltage
3	Control Bus Clock	Bit Clock for Control Bus Data
4	Control Bus Data In	Control Bus Data In
5	FEC Enable	Enables/Disables FEC
6	Address Bit	Address Bit for Control Bus
11, 26, 31	Test Data Out	Factory Use—Serial Test Data Out
12, 13	PLL GND	PLL Ground
14	PLL VCC	Supply Voltage for PLL
15	PLL Filter	PLL Loop Filter Connection
16, 19, 23	AGND	Analog Ground
17	NC	No Connect
18	DAC Rset	Rset Resistor Connection
20, 22	AVDD	Analog Supply Voltage
21	DAC Baseline	DAC Baseline Voltage
24	IOUT	Analog Current Output of the DAC
25	IOUTB	Complementary Analog Current Output of the DAC
27	Test CLK	Factory Use—Scan Clock
28	Test Latch	Factory Use—Scan Latch
29	Test Data In	Factory Use—Serial Test Data In
30	Test Data Enable	Factory Use—Serial Test Data Enable, Grounded for Normal Operation
32	$\overline{\text{RESET}}$	Master Device Reset Function
33	CA Enable	Cable Amplifier Enable
34	CA Clock	Cable Amplifier Serial Control Clock
35	CA Data	Cable Amplifier Serial Control Data
38	REF CLK IN	Reference Clock Input
41	Data In	Input Serial Data Stream
42	T_XENABLE	Pulse that Frames the Valid Input Data Stream

PIN CONFIGURATION

44-Lead Metric Quad Flatpack (S-44A)



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Table I. Modulator Function Description

Modulation Encoding Format	FSK*, QPSK, DQPSK, 16-QAM, D16-QAM, Selectable via Control Bus
Output Carrier Frequency Range	DC – 63 MHz with +3.3 V Supply Voltage DC – 84 MHz with +5 V Supply Voltage
Serial Input Data Rate	Evenly Divisible Fraction of Reference Clock
Pulse-Shaping FIR Filter	41 Tap, Linear Phase, 10-Bit Coefficients Fully Programmable via Control Bus
Interpolation Range	*Interpolation Rate* = (4/*M*) × (*ICIC*1) × (*ICIC*2) where: *M* = 2 for QPSK, *M* = 4 for 16-QAM Minimum and Maximum Rates Minimum Interpolation Rate—QPSK = 2 × 3 × 2 = 12 16-QAM = 1 × 4 × 3 = 12 Maximum Interpolation Rate—QPSK = 2 × 31 × 63 = 3906 16-QAM = 1 × 31 × 63 = 1953 These are the minimum and maximum interpolation ratios from the input data rate to the system clock. The interpolation range is a function of the fixed interpolation factor of four in the FIR filters, the programmed CIC filter interpolation rates (ICIC1, ICIC2), as well as system timing constraints.
Maximum Reference Clock Frequency	+3.3 V Supply: 21 MHz with 6× REFCLK enabled, 126 MHz with 6× REFCLK disabled +5 V Supply: 28 MHz with 6× REFCLK enabled, 168 MHz with 6× REFCLK disabled
6× REFCLK	Fixed 6× reference clock multiplier, enable/disable control via control bus
R-S FEC	Enable/disable via control bus and dedicated control pin. Control pin enable/disable function: Logic "1" = Enable Logic "0" = Disable Primitive Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$ Code Generator Polynomial: $g(x) = (x + \alpha^0)(x + \alpha^1)(x + \alpha^2) \ldots (x + \alpha^{2t-1})$ Selectable via Control Bus t = 0–10 (Programmable) Codeword Length (N) = 255 max (Programmable) N = K + 2 t (K Range = 16 ≤ K ≤ 255 – 2 t) FEC/Randomizer can be transposed in signal chain via control bus.
I/Q Channel Spectrum	I × COS + Q × SIN (default) or I × COS – Q × SIN, selectable via control bus.
Preamble Insertion	0–96 Bits, Programmable Length and Content
Randomizer	Enable/Disable Control via Control Bus Generating Polynomial: $x^6 + x^5 + 1$, Programmable Seed (Davic/DVB-Compliant) or $x^{15} + x^{14} + 1$, Programmable Seed (DOCSIS-Compliant) Randomizer and FEC blocks can be transposed in signal chain, via control bus.

*In FSK mode, F0:F1 are direct DDS Cosine output. The two interpolator stages of the AD9853 are not used in the FSK mode and should be programmed for maximum interpolation rates to reduce unnecessary current consumption. This means that Interpolator #1 should be set to a decimal value of 31, and Interpolator #2 should be set to decimal value of 63. This is easily accomplished by programming Registers 12 and 13 (hex) with the values of FF (hex).

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Table II. Control Register Functional Assignment

Register Address (Note 1)	DATA D7	D6	D5	D4	D3	D2	D1	D0
00h	MSB	Value of *K* (Message Length in Bytes) for *Reed-Solomon* Encoder, where $16_{10} \le K \le 255_{10}$ (Note 2)						LSB
01h	MSB	The Number of Correctable Byte Errors (t) for the *Reed-Solomon Encoder*, where $0 \le t \le 10_{10}$. For $t = 0$, the RS encoder is effectively disabled.		LSB	Randomizer Insertion 0 = After RS 1 = Before RS	Randomizer Length 00_2 = 6 Bit 01_2 = 15 Bit 10_2 = Randomizer OFF 11_2 = Randomizer OFF		(Note 3)
02h	MSB	Lower Eight Bits of Seed Value for 15-Bit Randomizer (Not Used for 6-Bit Randomizer)						LSB
03h	MSB	Upper Seven Bits of Seed Value for 15-Bit Randomizer – OR – Seed Value for 6-Bit Randomizer (D1 not used in this case).					LSB	
04h	MSB	Preamble Length (L) where $0 \le L \le 96$ Bits (Note 4)					LSB	
05h	Modulation Mode 000_2 = QPSK , 001_2 = DQPSK, 010_2 = 16-QAM 011_2 = D16-QAM , 100_2 = FSK							
06h : 11h	The MSB of the preamble always resides in D7 of Address 11h and is the first preamble bit to be clocked out of the device during transmission of a packet. Up to 96 bits of preamble are available as specified in Register 04h. Unused bits are *don't care* for $L < 96$. MSB	Preamble Data. (Note 5)						
12h		MSB	Interpolator #1: RATE Rate Change Factor (*R*) where $3_{10} \le R \le 31_{10}$			LSB		
13h		MSB	Interpolator #2: RATE Rate Change Factor (*R*) where $2_{10} \le R \le 63_{10}$				LSB	
14h	MSB	Interpolator #1: SCALE			LSB	2× Multiplier 0 = OFF 1 = ON		
15h[6]	MSB	Interpolator #2: SCALE				LSB		
16h : 19h	MSB	Frequency Tuning Word #1 *FSK Mode*: Specifies the "space" frequency (F0). *All Other Modes*: Specifies the carrier frequency.						LSB
1Ah : 1Dh	MSB	Frequency Tuning Word #2 *FSK Mode*: Specifies the "mark" frequency (F1). (Addresses 1Ah–1Dh are only valid for FSK mode.)						LSB
1Eh[5]	MSB-2	MSB-3	10-Bit FIR End Tap Coefficient, a_0					LSB_0
1Fh	MSB_0	MSB-1	<— — — — — — — — — — — — — — — — — — Unused Bits — — — — — — — — — — — — — — — — — — >					
: : :	FIR Intermediate Tap Coefficients, $a_1 - a_{19}$							
46h	MSB-2	MSB-3	10-Bit FIR Center Tap Coefficient, a_{20}					LSB_{20}
47h	MSB_{20}	MSB-1	<— — — — — — — — — — — — — — — — — — Unused Bits — — — — — — — — — — — — — — — — — — >					
48h (Note 7)	Spectrum 0 = I × Cos + Q × Sin 1 = I × Cos – Q × Sin	Digital Power 0 = Normal 1 = Shutdown	6× RefClk 0 = Off 1 = On	PLL Mode 0 = Awake 1 = Sleep	DAC Mode 0 = Awake 1 = Sleep			
49h (Note 8)	MSB	AD8320 Cable Driver Gain Control Byte (GCB) The absolute gain, A_V, of the AD8320 is given by: $A_V = 0.316 + 0.077 \times GCB$ (where $0 \le GCB \le 255_{10}$)						LSB

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NOTES

[1]The 8-bit *Register Address* is preceded by an 8-bit *Device Address*, which is given by 000001XY, where the value of Bits X and Y are determined as follows:

X	Voltage Applied to Pin 6	Y	Desired Register Function
0	GND	0	WRITE
1	$+V_S$	1	READ

[2]This register must be loaded with a nonzero value even if the RS encoder has been disabled by setting $T = 0$ in register 01h.

[3]Unused regions are *don't care* bit locations.

[4]If a preamble is not used this register *must* be initialized to a value of 0 by the user.

[5]Addresses 06h–011h and 1Eh–47h are write only.

[6]Readback of register 15h results in a value that is 2× the actual programmed value. This is a design error in the readback function.

[7]Assertion of RESET (Pin 32) sets the contents of this register to 0.

[8]Registers 0h–48h may be written to using a single register address followed by a contiguous data sequence (see Figure 27). Register 49h, however, must be written to individually; i.e., a separately addressed 8-bit data sequence.

Modulated Output Spectrum with 3.3 V Supply, α = 0.25, 20.48 MHz REFCLK

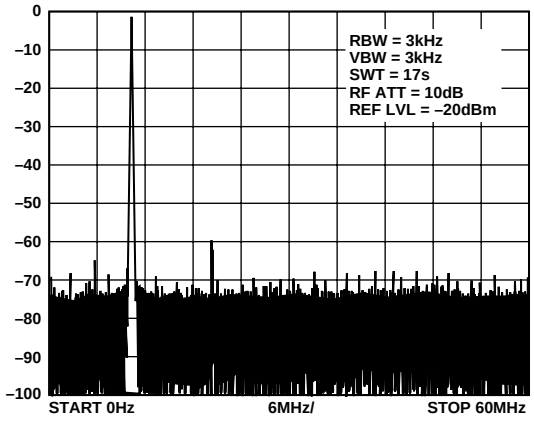


Figure 1. QPSK, 320 kb/s, A_{OUT} = 10 MHz

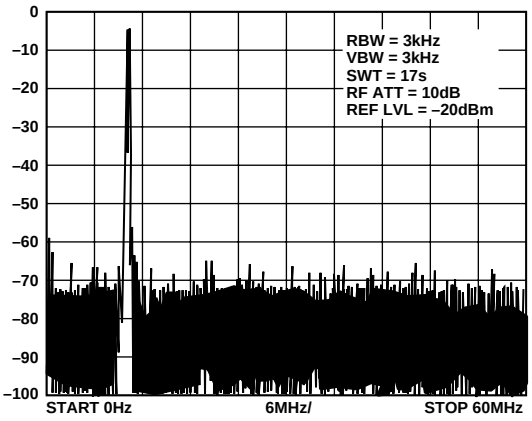


Figure 4. QPSK, 1.28 Mb/s, A_{OUT} = 10 MHz

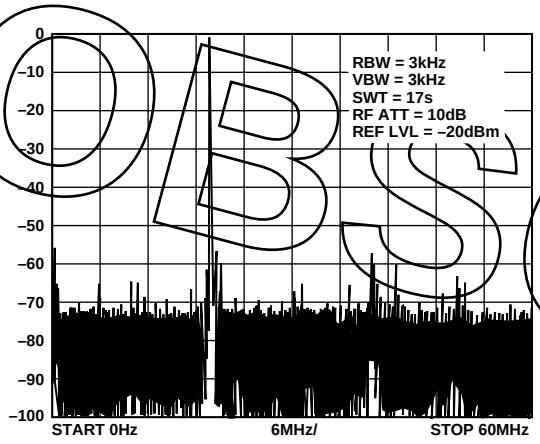


Figure 2. QPSK, 640 kb/s, A_{OUT} = 20 MHz

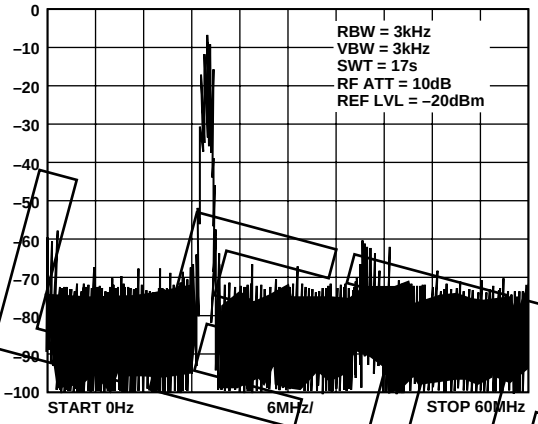


Figure 5. QPSK, 2.56 Mb/s, A_{OUT} = 20 MHz

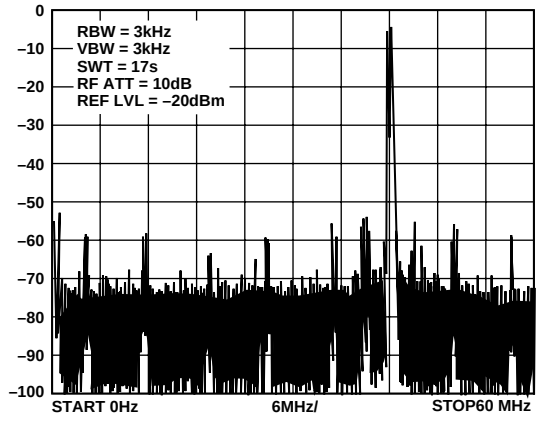


Figure 3. QPSK, 1.28 Mb/s, A_{OUT} = 42 MHz

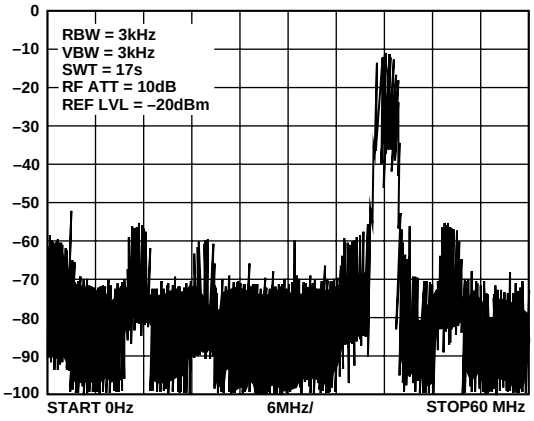


Figure 6. QPSK, 5.12 Mb/s, A_{OUT} = 42 MHz

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Modulated Output Spectrum with 5 V Supply, α = 0.25, 27.5 MHz REFCLK

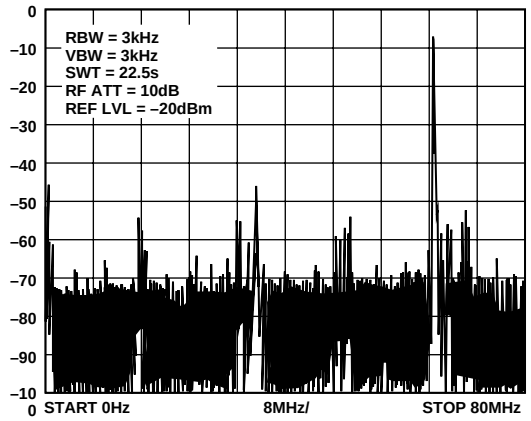


Figure 7. QPSK, 1.375 Mb/s, A_{OUT} = 65 MHz

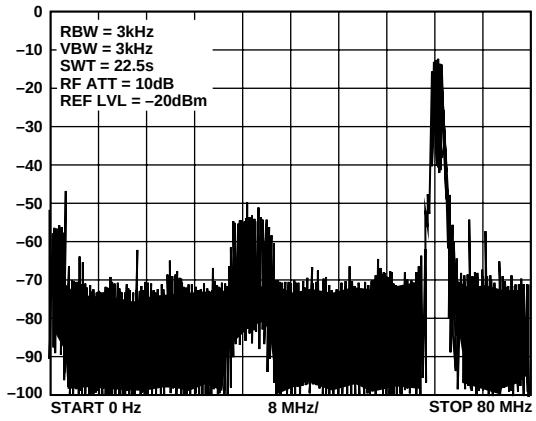


Figure 10. QPSK, 5.5 Mb/s, A_{OUT} = 65 MHz

Single Tone Output Spectrum with +3.3 V Supply, 20.48 MHz REFCLK

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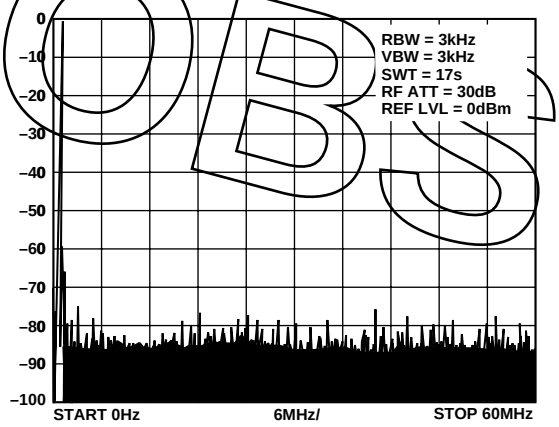


Figure 8. A_{OUT} = 1 MHz

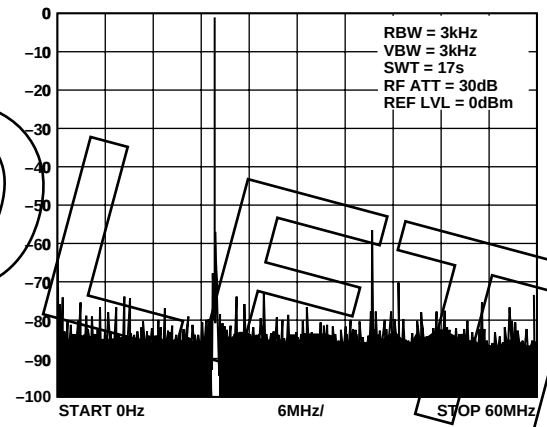


Figure 11. A_{OUT} = 20 MHz

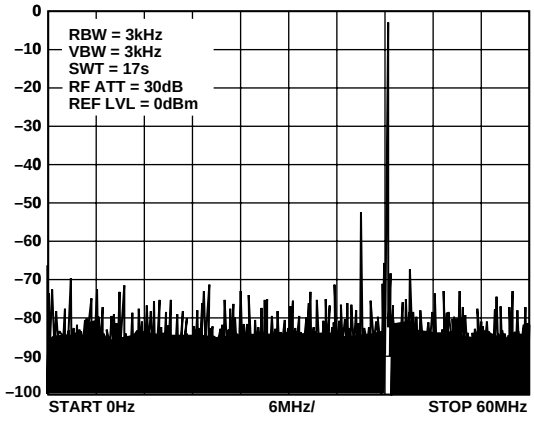


Figure 9. A_{OUT} = 42 MHz

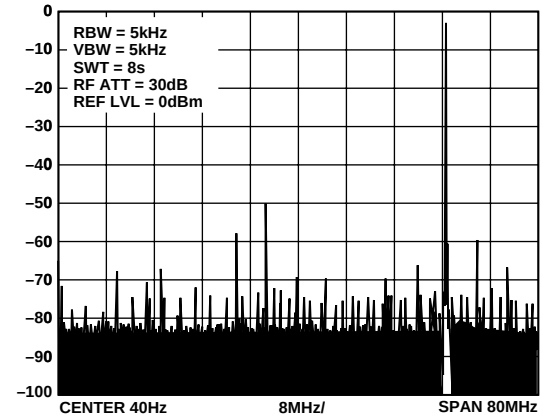


Figure 12. A_{OUT} = 65 MHz (+5 V Supply, 27.5 MHz REFCLK)

Output Phase Noise Plots, A_{OUT} = 40 MHz

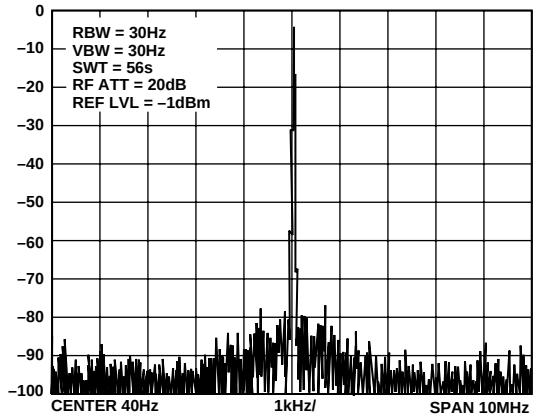


Figure 13. 6× REFCLK Enabled

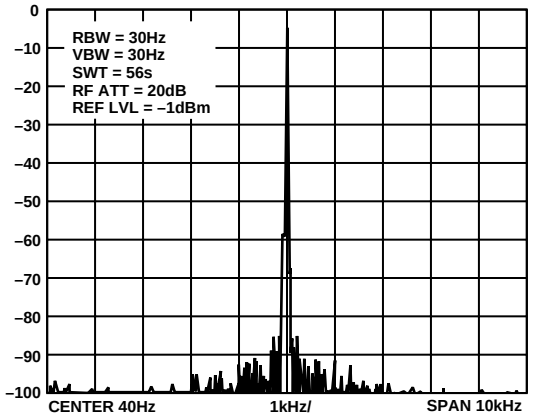


Figure 14. 6× REFCLK Disabled

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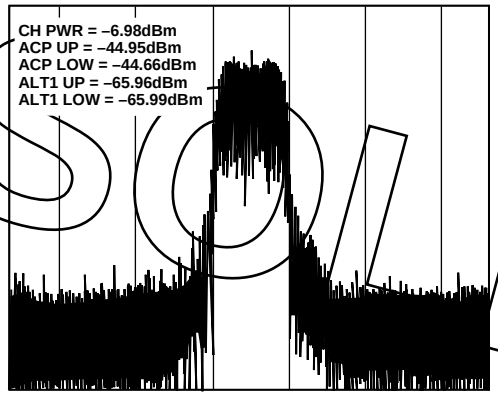


Figure 15. Adjacent Channel Power, A_{OUT} = 30 MHz, 2.56 MS/s, Channel BW = 3.2 MHz (α = 0.25)

Typical Plots of Eye Diagrams and Constellations

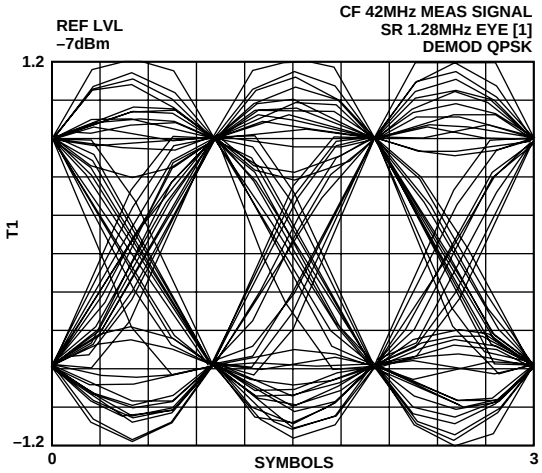


Figure 16. QPSK Modulation

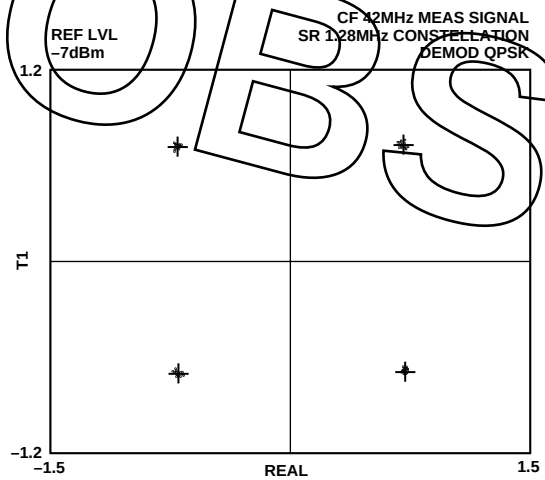


Figure 17. QPSK Modulation

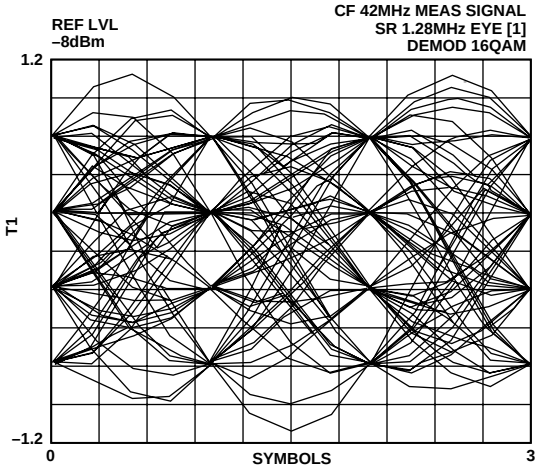


Figure 18. 16-QAM Modulation

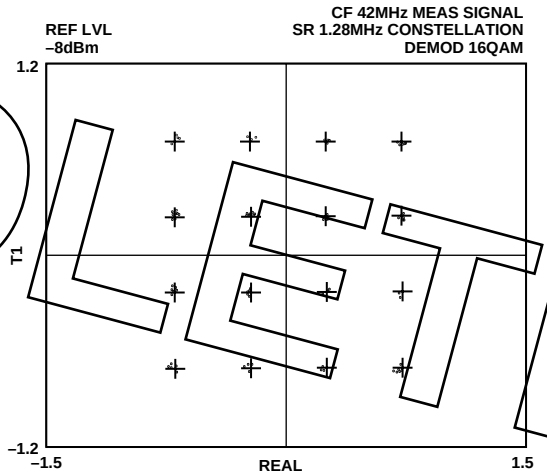


Figure 19. 16-QAM Modulation

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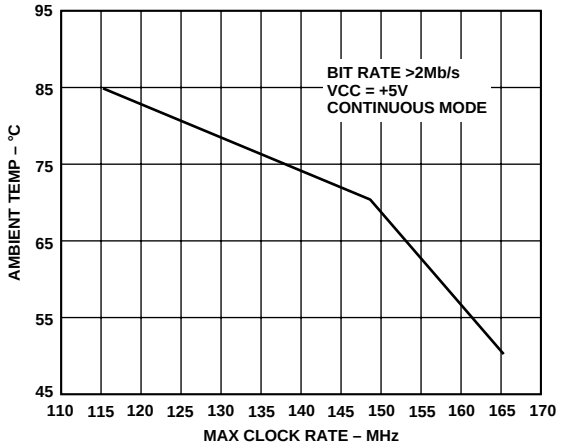


Figure 20. Max CLK Rate vs. Ambient Temperature (To Ensure Max Junction Temp is Not Exceeded)

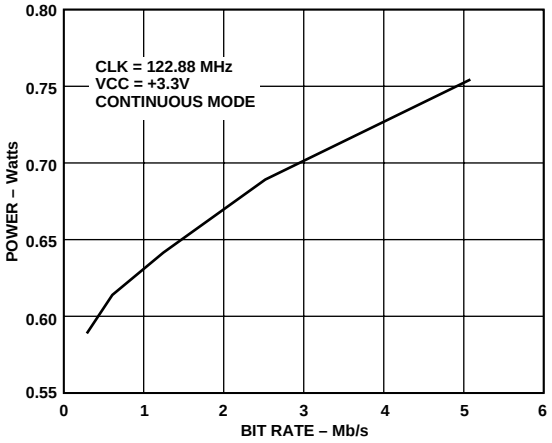


Figure 23. PWR Consumption vs. Bit Rate

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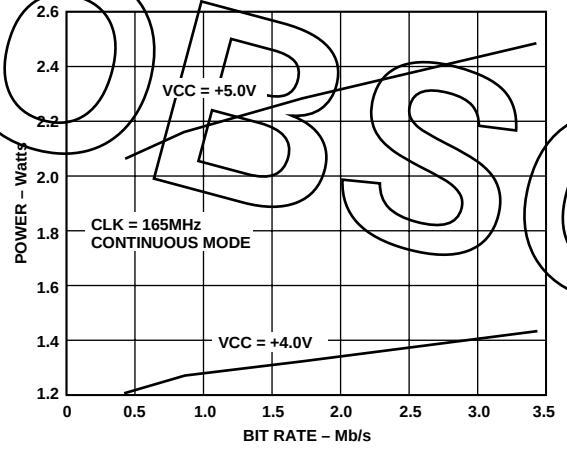


Figure 21. Power Consumption vs. Bit Rate

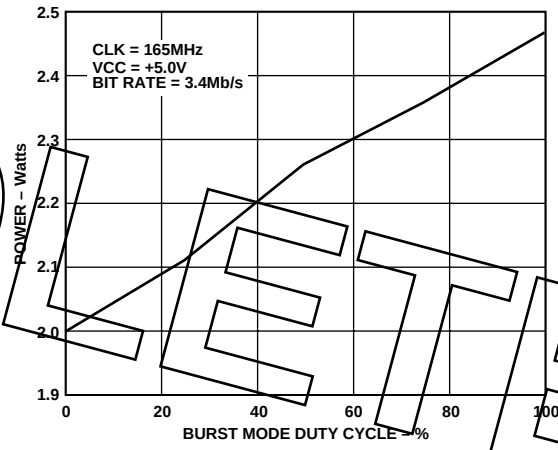


Figure 24. Power Consumption vs. Burst Duty Cycle

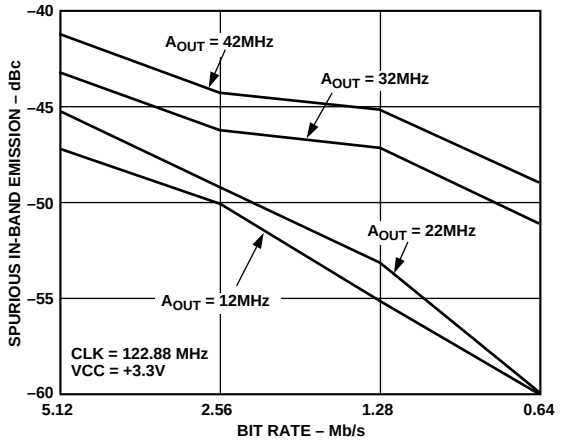


Figure 22. Spurious Emission vs. Bit Rate vs. A_{OUT}

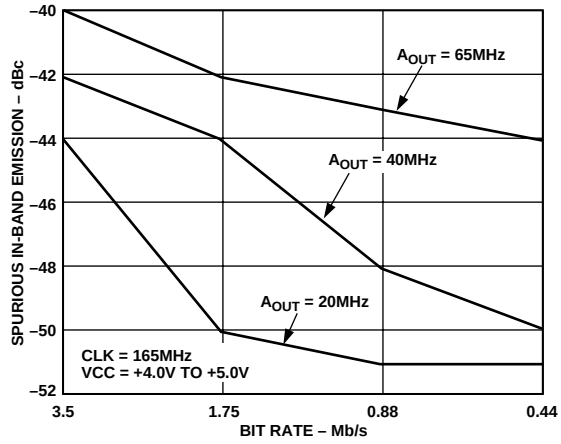
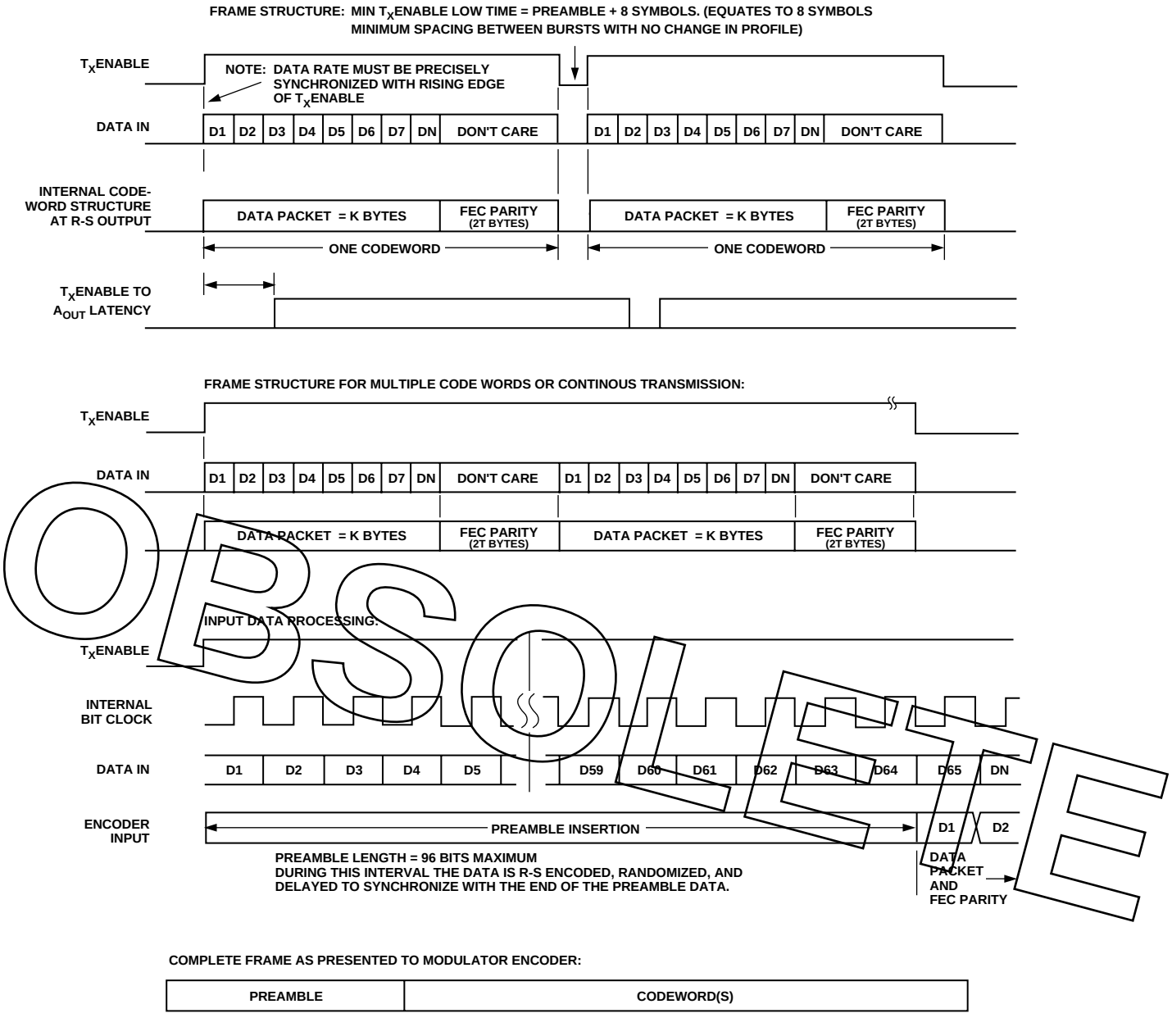


Figure 25. Spurious Emission vs. Bit Rate vs. A_{OUT}



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NOTES ON BURST TRANSMISSION OPERATION:

1. PACKET LENGTH = NUMBER OF INFORMATION BYTES, K
2. IN FEC MODE T_XENABLE MUST BE KEPT HIGH FOR N × (K+2T) BYTES WHERE N IS THE NUMBER OF CODEWORDS
3. IF NECESSARY, ZERO FILL THE LAST CODEWORD TO REACH ASSIGNED K DATA BYTES PER CODEWORD
4. THE INPUT DATA IS SAMPLED AT THE BIT RATE FREQUENCY (f_B) WITH THE FIRST SAMPLE TAKEN AT $\frac{1}{2 \times (f_B)}$ SECONDS AFTER THE RISING EDGE OF T_XENABLE
5. PREAMBLE DELAY = $\frac{\text{(\# OF PREAMBLE BITS)}}{\text{(BIT RATE FREQUENCY)}}$
6. DATA RATE MUST BE EXACT SUB-MULTIPLE OF REFERENCE CLOCK.

Figure 26. Data Framing and Processing

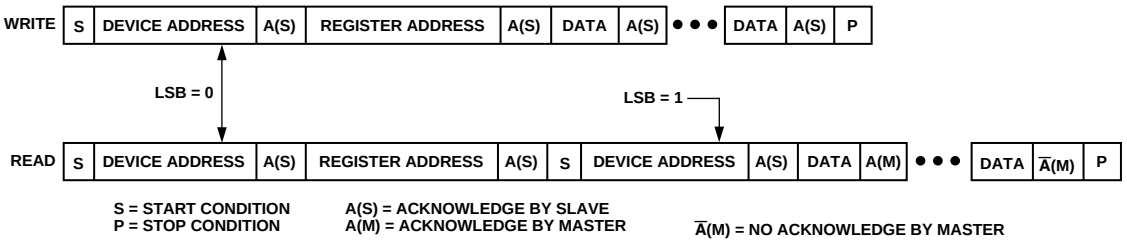


Figure 27. Serial Control Bus—Read and Write Sequences

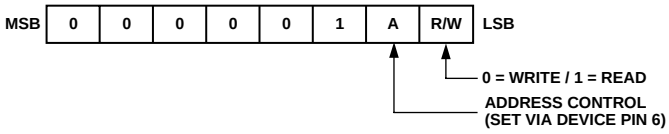


Figure 28. Serial Control Bus—8-Bit Device Address Detail

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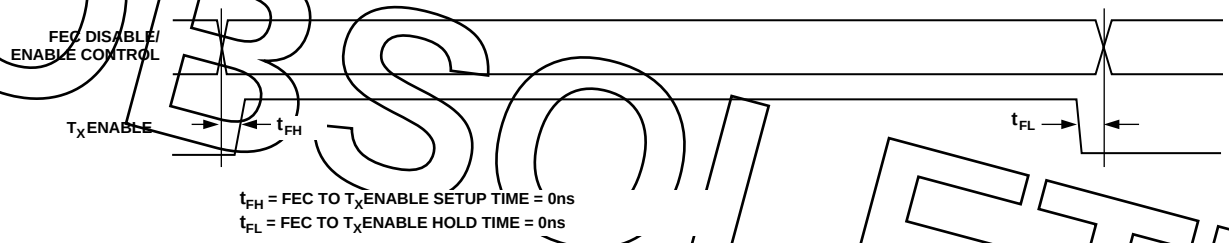


Figure 29. FEC Enable/Disable Timing Diagram

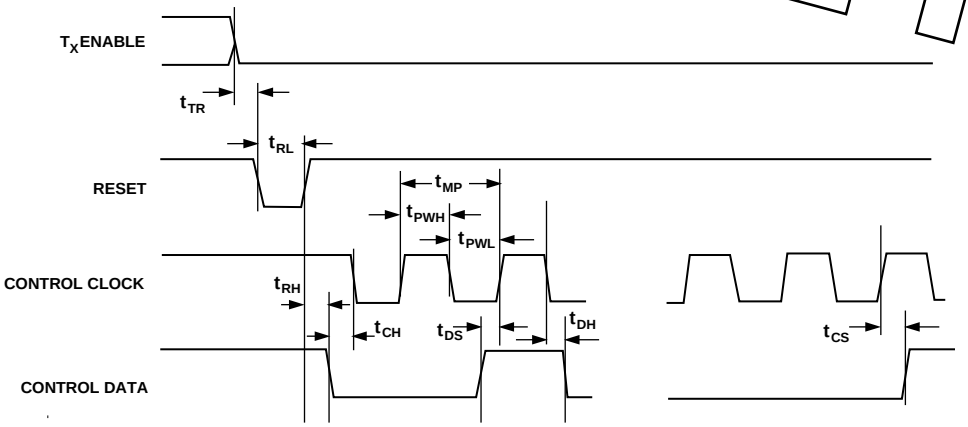
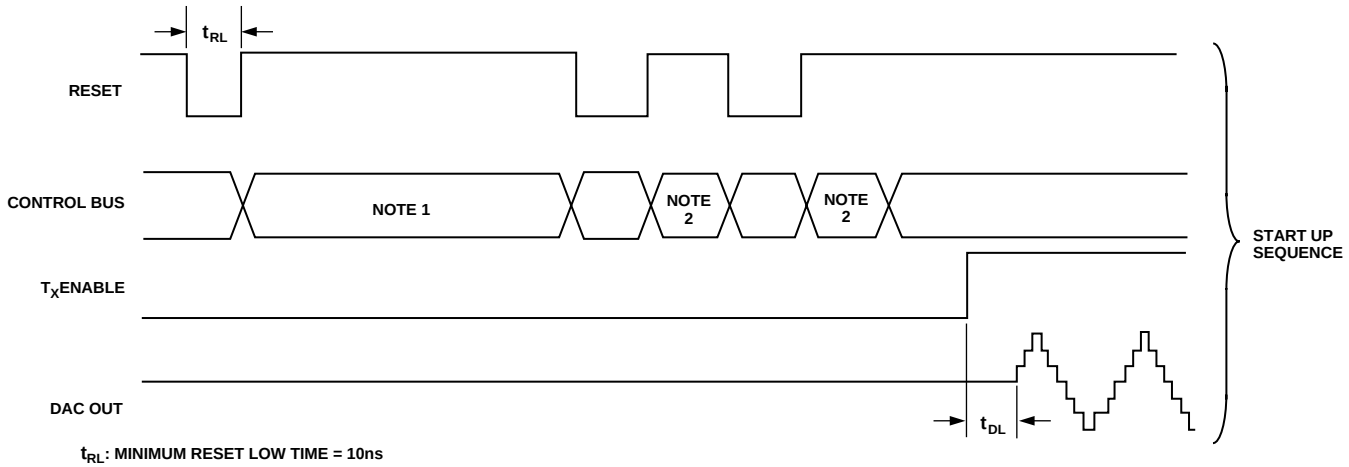


Figure 30. Serial Control Interface Timing Diagram



t_{RL}: MINIMUM RESET LOW TIME = 10ns
t_{DL}: DATA LATENCY = 6 SYMBOLS

NOTE 1. DURING THIS INTERVAL ALL CONTROL BUS REGISTERS MUST BE PROGRAMMED.
NOTE 2. DURING THIS INTERVAL THE CONTROL REGISTER (48h) MAY NEED TO BE REPROGRAMMED DUE TO BEING CLEARED BY THE PRECEDING RESET PULSE.
NOTE 3. THREE RESETS ARE REQUIRED TO ENSURE THAT THE DATA PATH IS ZERO'D.

Figure 31. Recommended Start-Up Sequence

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NOTES ON THE RESET FUNCTION:

1. RESET IS ACTIVE LOW
2. RESET ZEROS THE CONTROL REGISTER AT ADDRESS 48 HEX WHICH CAUSES THE FOLLOWING DEFAULT CONDITION TO EXIST:
   A. 6× REFCLK IS DISABLED
   B. OUTPUT SPECTRUM IS SET TO I×COS+Q×SIN
   C. DIGITAL PLL POWER-DOWN IS DISABLED
   D. PLL POWER-DOWN IS DISABLED
   E. DAC PLL POWER-DOWN IS DISABLED
3. SERIAL CONTROL BUS IS RESET AND INITIALIZED.
4. OUTPUTS OF MODULATION ENCODERS ARE SET TO ZERO. THIS ALLOWS THE FIR FILTERS AND SUBSEQUENT INTERPOLATION FILTERS TO BE FLUSHED WITH ZEROS AS LONG AS T_XENABLE IS HELD LOW.
5. THE PREAMBLE IS CLEARED UPON EXECUTION OF THE RESET FUNCTION.

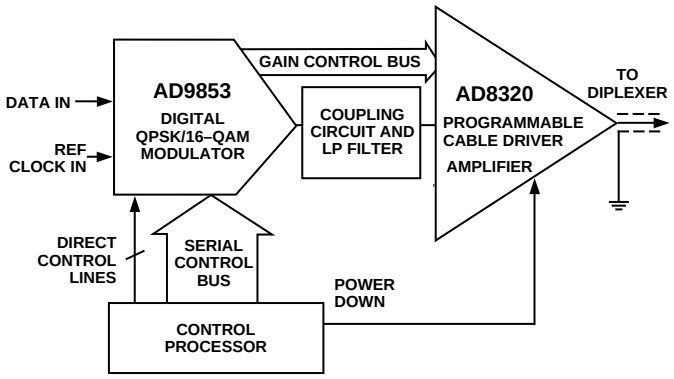


Figure 32. Basic Implementation of AD9853 Digital Modulator and AD8320 Programmable Cable Driver Amplifier in Return-Path Application

THEORY OF OPERATION

The AD9853 is a highly integrated modulator function that has been specifically designed to meet the requirements of the HFC upstream function for both interoperable and proprietary system implementations. The AD8320 is a companion cable driver amplifier with a digitally-programmable gain function, that interfaces to the AD9853 modulator and directly drives the cable plant with the modulated carrier. Together, the AD9853 and AD8320 provide an easily implementable transmitter solution for the HFC return-path requirement.

CONTROL AND DATA INTERFACE

As shown in the device's block diagram on the front page, the various transmit parameters, which include the input data rate, modulation format, FEC and randomizer configurations, as well as all the other modulator functions, are programmed into the AD9853 via a serial control bus. The AD8320 cable driver amp gain can be programmed directly from the AD9853 via a 3-wire bus by writing to the appropriate AD9853 register. The AD9853 also contains dedicated pins for FEC enable/disable and a RESET function.

Note: T_XENABLE pin must be held low for the duration of all serial control bus operations.

The AD9853's serial control bus consists of a bidirectional data line and a clock line. Communication is initiated upon a start condition, which is defined as a high-to-low transition of the data line while the clock is held high. Communication terminates upon a stop condition, which is defined as a low-to-high transition in the data line while the clock is held high. Ordinarily, the data line transitions only while the clock line is low to avoid a start or stop condition. Data is always written or read back in 8-bit bytes followed by a single acknowledge bit. The microcontroller or ASIC (i.e., the bus master) transfers eight data bits and the AD9853 (i.e., the slave) issues the acknowledge bit. The acknowledge bit is active low and is clocked out on every ninth clock pulse. The bus master must three-state the data line during the ninth clock pulse and allow the AD9853 to pull it low.

A valid write sequence consists of a minimum of three bytes. This means 27 clock pulses (three bytes with nine clock pulses each) must be provided by the bus master. The first byte is a chip address byte that is predefined except for Bit Positions 1 and 0. Bit Positions 7, 6, 5, 4 and 3 must be zero. Bit Position 2 must be a one. Bit 1 is set according to the external address pin on the AD9853 (1 if the pin is connected to $+V_S$; 0 if the pin is grounded). Bit 0 is set to 1 if a read operation is desired, 0 if a write operation is desired. The second byte is a register address with valid addresses between 00h and 49h. An address which is outside of this range will not be acknowledged. The third byte is data for the address register. Multiple data bytes are allowed and loaded sequentially. That is, the first data byte is written to the addressed register and any subsequent data bytes are written to subsequent register addresses. It is permissible to write all registers by issuing a valid chip address byte, then an address byte of 00h and then 72 (48h) data bytes. Address 49h must be written independently, that is, not in conjunction with any other address.

A valid read sequence consists of a minimum of four bytes (refer to Figure 27). This means the bus master must provide 36 clock pulses (four bytes with nine clock pulses each). Like the write sequence, the first two bytes are the Chip Address Byte, with the read/write bit set to 0, and the readback register address. After the slave provides an acknowledge at the end of the register address, the master must present a START condition on the bus, followed by the Chip Address Byte with the read/write bit set to a 1. The slave proceeds to provide an acknowledge. During the next eight clocks the slave will write to the bus from the register address. The master must provide an acknowledge on the ninth clock of this byte. Any subsequent clocks from the master will force the slave to read back from subsequent registers. At the end of the read-back cycle, the MASTER must force a "no-acknowledge" and then a STOP condition. This will take the SLAVE out of read-back mode. Not all of the serial control bus registers can be read back. Registers (06h–11h) and (1Eh–47h) are write only. Also, like the writing procedure, register 49h must be read from independently.

INPUT DATA SYNCHRONIZATION

The serial input data interface consists of two pins, the serial data input pin and a T_XENABLE pin. The input data arrives at the bit rate and is framed by the T_XENABLE signal as shown in Figure 26. A high frequency sampling clock continuously samples the T_XENABLE signal to detect the rising edge. Once the rising edge of T_XENABLE is detected, an internal sampler strobes the serial data at the correct point in time relative to the positive T_XENABLE transition and then continues to sample at the correct interval based on the programmed Input Data rate. For proper synchronization of the AD9853, 1) the input burst data must be accurately framed by T_XENABLE and 2) the input data rate must be an exact even submultiple of the system clock. Typically this will require that the input data rate clock be synchronized with reference clock.

REED-SOLOMON ENCODER

The AD9853 contains a programmable Reed-Solomon (R-S) encoder capable of generating an (N, K) code where N is the code word length and K is the message length.

Error correction becomes vital to reliable communications when the transmission channel conditions are less than ideal. The original message can be precisely reconstructed from a corrupted transmission as long as the number of message errors is within the encoder's limits. When forward error correction (FEC) is engaged, either through the serial control interface bus or hardware (logic high at Pin 5), it is implemented using the following MCNS-compatible field generator and primitive polynomials:

Primitive Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

Code Generator Polynomial: $g(x) = (x + a^0)(x + a^1)(x + a^2) \ldots (x + a^{2t-1})$

The code-word structure is defined as follows:

$$N = K + 2t \ (bytes)$$

where:

N = code-word length

K = message length (in bytes), programmable from 16–255

t = number of byte errors that can be corrected programmable from 0–10.

A *Code Word* is the sum of the *Message Length* (in bytes) and number of *Check Bytes* required to correct byte errors at the

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receive end. The values actually programmed on the serial control bus are "K" and "t," which will define *N* as shown in the above code-word structure equation. As can be seen from the code-word structure equation, two check bytes are required to correct each byte error. Setting $t = 0$ and $K > 0$ will bypass the Reed-Solomon encoding process.

Since Reed-Solomon works on bytes of information and not bits, a single byte error can be as small as one inverted bit out of a byte, or as large as eight inverted bits of one byte; in either instance the result is one byte error. For example, if the value "t" is specified as 5, the R-S FEC could be correcting as many as 40, or as few as 05, erroneous bits, but those errors must be contained in 5 message bytes. If the errors are spread among more than five bytes, the message will not be fully error corrected.

When using the R-S encoder, the message data needs to be partitioned or "gapped" with "don't care" data for the time duration of the check bytes as shown in the timing diagram of Figure 26. During the intervals between message data, the device ignores data at the input.

The position of the R-S encoder in the coding data path can be switched with the randomizer by exercising Register 1, Bit D3, via the serial control bus.

RANDOMIZER FUNCTION

The next stage in the modulation chain is the randomizing or "scrambling" stage. Randomizing is necessary due to the fact that impairments in digital transmission can be a function of the statistics of the digital source. Receiver symbol synchronization is more easily maintained if the input sequence appears random or equiprobable. Long strings of 0s or 1s can cause a bit or symbol synchronizer to lose synchronization. If there are repetitive patterns in the data, discrete spurs can be produced, causing interchannel interference. In modulation schemes relying on suppressed carrier transmission, nonrandom data can increase the carrier feedthrough. Using a randomizer effectively "whitens" the data.

The technique used in the AD9853 to randomize the data is to perform a modulo 2 logic addition of the data with a pseudorandom sequence. The pseudorandom sequence is generated by a shift register of length *m* with an exclusive OR combination of the nth bit and the last (mth) bit of the shift register that is fed back to the shift register input. By choosing the appropriate feedback point, a maximal length sequence is generated. The maximal length sequence will repeat after every 2^m clock cycles, but appears effectively "random" at the output. The criterion for maximal length is that the polynomial $1 + x^n + x^m$ be irreducible and prime over the Galois field. The AD9853 contains the following two polynomial configurations in hardware:

$x^{15} + x^{14} + 1$:MCNS (DOCSIS) compatible.

$x^6 + x^5 + 1$:DAVIC/DVB compatible.

The seed value is fully programmable for both configurations. The seed value is reset prior to each burst and is used to calculate the randomizer bit, which is combined in an exclusive XOR with the first bit of data from each burst. The first bit of data in a burst is the MSB of the first symbol following the last symbol of the internally generated preamble.

PREAMBLE INSERTION BLOCK

As shown in the block diagram of the AD9853, the circuit includes a programmable preamble insertion register. This register is 96 bits long and is transmitted upon receiving the T_XENABLE signal. It is transmitted without being Reed-Solomon encoded or scrambled. Ramp-up data, to allow for receiver synchronization, is included as the first bits in the preamble, followed by user burst profile or channel equalization information. The first bit of R-S encoded and scrambled information data is timed to immediately follow the last bit of preamble data.

For most modulation modes, a minimum preamble is required. This minimum is one symbol, two bits for DQPSK or four bits for either 16-QAM or D16-QAM. No preamble is required for either FSK or QPSK.

In conformance with DAVIC/DVB standards, the preamble is not differentially coded in DQPSK mode. However the preamble data can be differentially precoded when loaded into the preamble register. The last symbol of the preamble is used as the reference point for the first internal differentially coded symbol so the preamble and data will effectively be coded differentially. In the D16-QAM mode, the preamble is always differentially coded internally.

MODULATION ENCODER

The preamble, followed by the encoded and scrambled data is then modulation encoded according to the selected modulation format. The available modulation formats are FSK, QPSK, DQPSK, 16-QAM and D16-QAM. The corresponding symbol constellations support the interactive HFC cable specifications called out by MCNS (DOCSIS), 802.14 and DAVIC/DVB. The data arrives at the modulation encoder at the input bit rate and is demultiplexed as modulation encoded symbols into separate I and Q paths. For QPSK and DQPSK, the symbol rate is one-half of the bit rate and each symbol is comprised of two bits. For 16-QAM and D16-QAM, the symbol rate is one-fourth the bit rate and each symbol is comprised of four bits. In the FSK mode, although the 1 and 0 data is entered into the serial data input, it effectively bypasses the encoding, scrambling and modulation paths. The FSK data is directly routed to the direct digital synthesizer (DDS) where it is used to switch the DDS between two stored tuning words (F0:F1) to achieve FSK modulation in a phase-continuous manner. By holding the input at either 1 or 0, a single frequency continuous wave can be output for system test or CW transmission purposes.

Differential encoding of data is frequently used to overcome phase ambiguity error or a "false lock" condition that can be introduced in carrier-recovery circuits used to demodulate the signal. In straight QPSK and 16-QAM, the phase of the received signal is compared to that of a "recovered carrier" of known phase to demodulate the signal in a coherent manner. If the phase of the recovered carrier is in error, then demodulation will be in error. Differential encoding of data at the transmit end eliminates the need for absolute phase coherency of the recovered carrier at the receive end. If a coherent reference generated by a phase lock loop experiences a phase inversion while demodulating in a differentially coded format, the errors would be limited to the symbol during which the inversion occurred and the following symbol. Differential coding uses the phase of the "previously transmitted symbol" as a reference point to compare to the current symbol. The change in phase from one symbol to

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the next contains the message information and is used to demodulate the signal instead of the absolute phase of the signal. The transmitter and receiver must use the same symbol derivation scheme.

Differential encoding in the AD9853 occurs while data still exists as a serial data stream. When in straight QPSK or 16-QAM, the serial data stream passes to the symbol mapper/format encoder stage without modification. When differential encoding is engaged, the serial data stream is modified prior to the symbol mapper/format stage according to Table VI. Only I1 and Q1 are modified, even in the D16-QAM mode whose symbols are composed of Q1, I1, Q0, I0. In D16-QAM, only the two MSBs of the 4-bit symbol are modified; furthermore, the "previously transmitted symbol" referred to in Table VI are the two MSBs of the previous 4-bit symbol.

Symbol mapping for QPSK and DQPSK are identical. Symbol mapping for 16-QAM and D16-QAM are slightly different (see Figure 37) in accordance with MCNS (DOCSIS) specifications.

Special Note: For most modulation modes, a minimum preamble is required. For DQPSK the minimum preamble is one symbol (2 bits) and for either 16-QAM or D16-QAM the minimum preamble is one symbol (4 bits). For FSK or QPSK, no preamble is required.

User should be additionally aware that in the DQPSK mode, the preamble is not differentially encoded in accordance with MCNS (DOCSIS) specifications. If the preamble must be differentially encoded, it can "pre-encoded" using the derivation in Table VI. In D16-QAM, the preamble is always differentially encoded as is the "payload" data.

When initiating a new differentially encoded transmission, the "previously transmitted symbol" is always the last symbol of the preamble.

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PROGRAMMABLE PULSE-SHAPING FIR FILTERS

The I and Q data paths of the modulator each contain a pulse shaping filter. Each is a *41-tap, linear phase FIR*. They are used to provide bandwidth containment and pulse shaping of the data in order to minimize intersymbol interference. The filter coefficients are programmable, so any realizable linear phase response characteristic may be implemented. The linear phase restriction is due to the fact that the user may only define the center coefficient and the lower 20 coefficients. The hardware fills in the upper 20 coefficients as a mirror image of the lower 20. This forces a linear phase response. It should also be noted that the pulse shaping filter upsamples the symbol rate by a factor of four.

Normally, a *square-root raised cosine* (SRRC) response is desired. In fact, the AD9853 Evaluation Board software driver implements an SRRC response. When using the SRRC response, an excess bandwidth factor (α) is defined that affects the low pass roll-off characteristic of the filter (where $0 \le \alpha \le 1$). When $\alpha = 0$, the SRRC is an ideal low-pass filter with a "brick wall" at one-half of the symbol rate (the Nyquist bandwidth of the data). Although this provides maximum bandwidth containment, it has the adverse affect of causing the tails of the time domain response to be large, which increases intersymbol interference (ISI). On the other hand, when $\alpha = 1$, the SRRC yields a smooth roll-off characteristic that significantly reduces the time domain tails, which improves ISI. Unfortunately, the cost of this benefit is a doubling of the bandwidth of the data signal. Values of α between 0 and 1 yield a tradeoff between excess bandwidth in the frequency domain and tail suppression in the time domain.

The FIR filter coefficients for the SRRC response may be calculated using a variety of methods. One such method uses the *Inverse Fourier Transform Integral* to calculate the impulse response (time domain) from the SRRC frequency response (frequency domain). An example of this method is shown in Figure 33. Of course, this method requires that the SRRC frequency response be known beforehand.

The FIR filters in the AD9853 are implemented in hardware using a fixed point architecture of 10-bit, twos complement integers. Thus, each of the filter coefficients, a_i, is an integer such that:

$$-512 \le a_i \le 511 \qquad [i = 0, 1, \ldots, 40]$$

PROGRAMMABLE INTERPOLATION FILTERS

The AD9853 employs two stages of interpolation filters in each of the I and Q channels of the modulator. These filters are implemented as Cascaded Integrator-Comb (CIC) filters. CIC filters are unique in that they not only provide a low-pass frequency response characteristic, but also provide the ability to have one sampling rate at the input and another sampling rate at the output. In general, a CIC filter may either be used as an interpolator (low-to-high sample rate conversion) or as a decimator (high-to-low sample rate conversion). In the case of the AD9853, the CIC filters are configured as interpolators, only. Furthermore, the interpolation is done in two separate stages with each stage designed so that the rate change is programmable. The first interpolator stage offers rate change ratios of 3 to 31, while the second stage offers rate change ratios of 2 to 63.

As stated in the previous section, the data coming out of the FIR filters is oversampled by four. Spectral images appear at their output (a direct result of the sampling process). These images are replicas of the baseband spectrum which are repeated at intervals of four times the symbol rate (the rate at which the FIR filters sample the data). The images are an unwanted byproduct of the sampling process and effectively represent a source of noise.

Normally, the output of the FIR filters would be fed directly to the input of the I and Q modulator. This means that the spectral images produced by the FIRs would become part of the modulated signal—definitely not a desirable consequence. This is where the CIC filters play their role. Since they have a low-pass characteristic, they can be used to eliminate the spectral images produced by the FIRs.

Frequency Response of the CIC Filters

The frequency response of a CIC filter is predictable. It can be shown that the system function of a CIC filter is:

$$H(z) = \left(\sum_{k=0}^{R\,M-1} z^{-k} \right)^N$$

Where N is the number of cascaded integrator (or comb) sections, R is the rate change ratio, and M is the number of unit delays in each integrator/comb stage. For the AD9853, two of these variables are fixed as a result of the hardware implementation; specifically, $N = 4$ and $M = 1$. As mentioned earlier, R (the rate change ratio) is programmable.

SQUARE-ROOT RAISED COSINE (SRRC) FIR FILTER

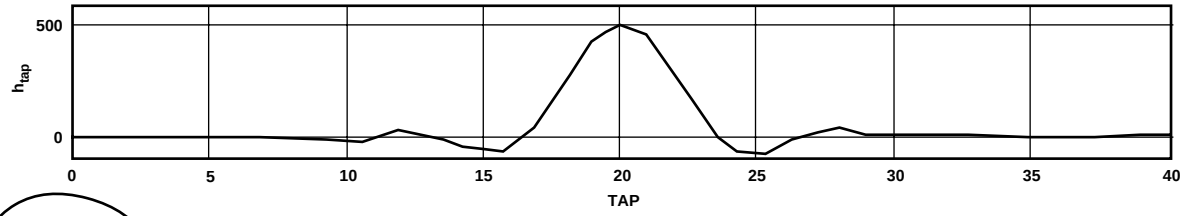
COMPUTE AND PLOT SRRC FILTER COEFFICIENTS:

$tap := 0..TAPS - 1 \quad t_{tap} := \frac{1}{FreqScale} \cdot \left(tap - \frac{TAPS - 1}{2}\right)$ ...MAP THE FILTER TAP INDEX TO TIME DOMAIN (CENTERED AT T=0)

$h(t) := \int_0^{BW} SRRC(f) \cdot \cos(2 \cdot \pi \cdot f \cdot t) df$ ...INVERSE FOURIER INTEGRAL COMPUTE SRRC IMPULSE RESPONSE (TIME DOMAIN) FROM THE SRRC FREQUENCY RESPONSE (FREQUENCY DOMAIN). THE COS() FUNCTION REPLACES THE NORMAL COMPLEX EXPONENTIAL BECAUSE WE ARE RESTRICTED TO REAL FILTER COEFFICIENTS.

$h_{tap} := h(t_{tap}) \quad h := INT\left(\frac{h \cdot SCALEPROC\ GAIN}{max(h)}\right)$ ...SRRC FILTER COEFFICIENTS INTEGERIZED AND SCALED

SRRC IMPULSE RESPONSE



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
$h^T =$	0	0	3	2	−2	−5	−2	5	7	1	−7	−7	7	19	7	−34	−71	−48	71	260	438	511

...FIR FILTER COEFFICIENTS

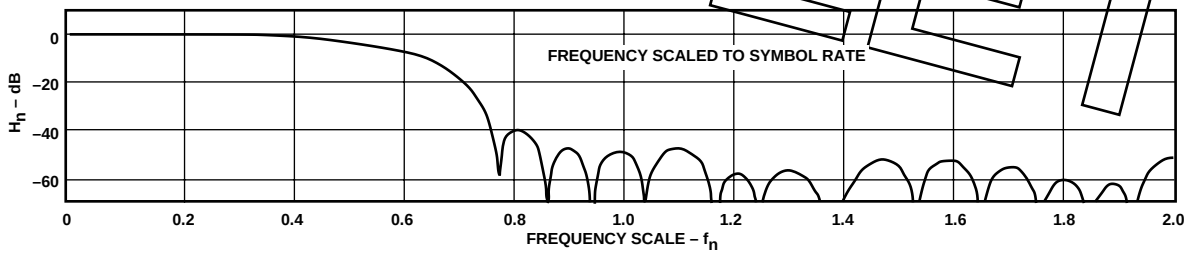
COMPUTE AND PLOT SRRC FREQUENCY RESPONSE:

$freq_pts := 250 \quad \Delta f := \frac{0.5}{freq_pts - 1}$ ...DEFINE NUMBER OF FREQUENCY POINTS AND FREQUENCY STEP SIZE (FOR PLOTTING PURPOSES)

$n := 0..freq_pts - 1 \quad f_n := \Delta f \cdot n$ ...CREATE VECTOR OF UNIFORMLY SPACED FREQUENCY POINTS {f_{max} = 0.5; A REQUIREMENT OF THE GAIN() FUNCTION},

$K := (|\ gain(h,0)\ |)^{-1} \quad H_n := K \cdot |\ gain\ (h, f_n)\ |$ ...NORMALIZED FREQUENCY RESPONSE

SRRC NORMALIZED FREQUENCY RESPONSE



OBSOLETE

GLOBAL DECLARATIONS

CONSTANTS:

$\alpha \equiv 0.5$ ...EXCESS BANDWIDTH FACTOR FOR SRRC FREQUENCY RESPONSE
$BW \equiv 0.5 \cdot (1 + \alpha)$ ...BANDWIDTH OF SRRC FILTER (RELATIVE TO SYMBOL RATE)
$PROC_GAIN \equiv 1$ ...PROCESSING GAIN OF CIC FILTERS (USED TO CORRELATE RESULTS WITH AD9853 EVAL. BD.)
$SCALE \equiv 511$ ...SETS MAX VALUE OF SRRC FILTER BASED ON FINITE WORD SIZE
$TAPS \equiv 41$ ...NUMBER OF FIR PULSE SHAPING FILTER TAPS
$FreqScale \equiv 4$ ...UPSAMPLING RATIO OF FIR PULSE SHAPING FILTER (RELATIVE TO THE SYMBOL RATE)

FUNCTIONS:

$InRange(x,a,b) \equiv (x \geq a) \cdot (x \leq b)$ ...RETURNS 1 IF a <= x <= b, 0 OTHERWISE
$INT(x) \equiv floor(x + 0.5)$ ...RETURNS NEAREST INTEGER TO x
$dB(x) \equiv if(|\ x\ | = 0, 200, 20 \cdot \log(|\ x\ |))$ ...RATIO TO DECIBEL CONVERSION FUNCTION

$SRRC(f) \equiv$ ...SRRC FREQUENCY RESPONSE FUNCTION (f IS RELATIVE TO THE SYMBOL RATE)

$passband \leftarrow 0.5 \cdot (1 - \alpha)$
$stopband \leftarrow 0.5 \cdot (1 + \alpha)$
if InRange (f, 0, stopband)
  1 if InRange (f, 0, passband)
  $\cos\left[\frac{\pi}{4 \cdot \alpha} \cdot (2 \cdot f + \alpha - 1)\right]$ if InRange (f, passband, stopband)
0 otherwise

Figure 33. Mathcad Simulation of a 41-Tap SRRC Filter

The frequency response, H(f), of a CIC filter is found by evaluating H(z) at $z = e^{j(2\pi f/R)}$:

$$H(f) = \left(\sum_{k=0}^{RM-1} e^{-j(2\pi f/R)k} \right)^N$$

where *f* is relative to the input sample rate of the CIC filter. With this formula, we can accurately predict the frequency response of the CIC filters.

Compensating for CIC Roll-Off

As discussed previously, the CIC filters offer a low-pass characteristic that can be used to eliminate the spectral images produced by the FIR filters. Unfortunately, the CIC response is not flat over the frequency range of the baseband signal. Thus, the inherent attenuation (or roll-off) of the CIC filters distorts the baseband data signal. So even though the CIC filters help to eliminate the images described earlier, they introduce another form of error to the baseband signal—frequency-dependent amplitude distortion. This ultimately manifests itself as a higher level of *Error Vector Magnitude* (EVM) at the output of the I and Q modulator. Also, the larger the bandwidth of the baseband signal, the more pronounced the CIC roll-off, the greater the amplitude distortion and the worse the EVM performance. This is a serious problem because if a value of $\alpha = 1$ is used for the SRRC response of the FIR filters, a doubling of the bandwidth of the baseband signal results and hence, a degradation in EVM performance.

Fortunately, there is a way to compensate for the effects of CIC roll-off. Since the frequency response of the CIC filters is predictable, it is possible to compensate for the CIC roll-off characteristic by adjusting the response of the FIR filters accordingly. The adjustment is accomplished by modifying the FIR filter response with a response that is the inverse of that of the CIC filters. This is done by precompensating the FIR filters.

To perform CIC compensation, we simply define a function (H_{COMP}) that has a response which is the inverse of the CIC response. Specifically,

$$H_{COMP}(f) = \left| \frac{1}{H(f)} \right|$$

By multiplying the original FIR filter frequency response by H_{COMP}, we obtain the necessary compensation.

Unfortunately, it's not quite this simple. Recall that the coefficients of the baseband filter were computed using an inverse Fourier transform integral which included the SRRC function. In order to compensate for the CIC filter response, the SRRC function must be multiplied by the H_{COMP} function. But the frequency scale of the SRRC response is computed based on frequencies relative to the symbol rate, while the H_{COMP} function is computed relative to the input sampling rate of the CIC filter. The input CIC sampling rate happens to be the same as the sample rate of the FIR filter (see Figure 36), or four times the symbol rate. Thus, we have a frequency scaling problem.

This problem is easily corrected by introducing a frequency scaling factor (FreqScale = 4) into the H_{COMP} function so that the frequency scales of the two functions match. Thus, the actual H_{COMP} function required is given by:

$$H_{COMP} = \left| \frac{1}{H\left(\frac{f}{FreqScale} \right)} \right|$$

It should be noted that in compensating for the CIC roll-off, only the first stage CIC filter need be considered. This is due to the fact that at the output of the first stage CIC filter the bandwidth of the signal is reduced to the point that the roll-off introduced by the second stage is negligible in the region of the baseband signal.

The CIC compensation method is demonstrated by example (using MathCad) in Figures 34 and 35. An interpolation rate (R) of 6 is used in the example. The improvement obtained by compensating for the CIC response is graphically demonstrated in Figure 35 which shows:

- the SRRC filter response (which is the desired overall response)
- the composite response of the SRRC in series with the CIC filter (distorted response)
- the composite response of the compensated SRRC in series with the CIC (corrected response)

Note that the ideal SRRC response and the compensated composite response are virtually identical in the region of the passband. Thus, the goal of correcting for the CIC filter response has been accomplished.

There is one subtlety to be noted in the example. The CIC compensation is only applied to the first 90% of the bandwidth of the baseband signal (note the variable β inside the integral). It was found that compensation over the full 100% of the bandwidth produced a reduction in the suppression of signals in the stopband region of the SRRC. This resulted in creating more distortion than by not correcting for the CIC roll-off in the first place. However, by slightly reducing the bandwidth over which correction is applied, the stopband suppression is once again restored and a significant improvement in EVM performance is obtained.

Determining the Necessary Interpolator Rate Change Ratio

The AD9853 contains three stages of digital interpolation:

1) Fixed 4× Pulse Shaping FIR Filter.
2) Programmable 3 to 31 First Interpolation Filter.
3) Programmable 2 to 63 Second Interpolation Filter.

After the serial input data stream has been encoded into QPSK or 16-QAM symbols, the symbol interpolation rate of the AD9853 is determined by the product of the three interpolating stages listed above. In QPSK mode, the minimum symbol interpolation rate that will work is $4 \times 3 \times 2 = 24$; for 16-QAM the minimum is $4 \times 4 \times 3 = 48$. The maximum symbol interpolation rate is $4 \times 31 \times 63 = 7812$. The symbol rate at the encoder output for QPSK is equal to 1/2 the bit rate of the data and for 16-QAM it is 1/4 the bit rate. Figure 36 is a partial block diagram of the AD9853 and follows the path of the data stream from the input of the I and Q encoder block to the output of the DAC.

OBSOLETE

MODIFICATION OF SQUARE-ROOT RAISED COSINE (SRRC) FIR FILTER RESPONSE TO COMPENSATE FOR CASCADED INTEGRATOR-COMB (CIC) FILTER RESPONSE

COMPUTE SRRC FILTER COEFFICIENTS:

$tap := 0..TAPS - 1 \quad t_{tap} := \frac{1}{FreqScale} \cdot \left(tap - \frac{TAPS - 1}{2} \right)$ ...MAP THE FILTER TAP INDEX TO TIME DOMAIN (CENTERED AT t = 0)

$h(t) := \int_0^{BW} SRRC(f) \cdot \cos(2 \cdot \pi \cdot f \cdot t) df$

...INVERSE FOURIER INTEGRAL COMPUTES SRRC IMPULSE RESPONSE (TIME DOMAIN) FROM THE SRRC FREQUENCY RESPONSE (FREQUENCY DOMAIN). THE COS() FUNCTION REPLACES THE NORMAL COMPLEX EXPONENTIAL BECAUSE WE ARE RESTICTED TO REAL FILTER COEFFICIENTS.

$h_{tap} := h(t_{tap}) \quad h := INT\left(\frac{\overrightarrow{h \cdot PROC_GAINSCALE}}{max(h)} \right)$ ...SRRC FILTER COEFFICIENTS INTEGERIZED AND SCALED

COMPUTE SRRC FILTER COEFFICIENTS MODIFIED FOR CORRECTION OF CIC RESPONSE:

$R := 6$ ...CIC INTERPOLATION RATIO (USER PROGRAMMABLE)

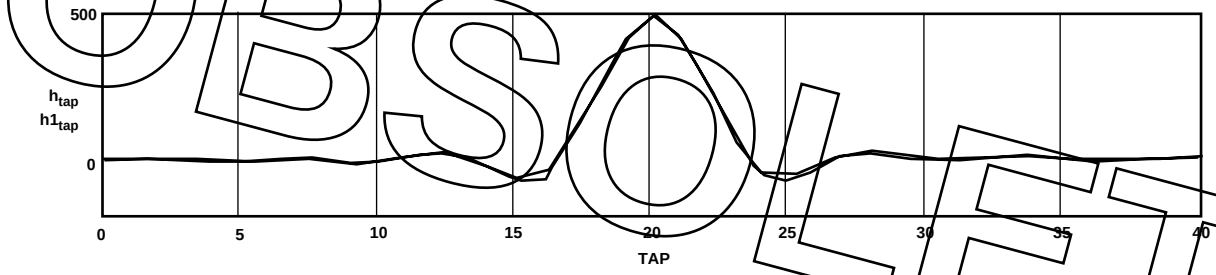
$h1(t) := \int_0^{BW} SRRC(f) \cdot if\left(f \le \beta \cdot BW, \left| \frac{H(0,R)}{H\left(\frac{f}{FreqScale}, R \right)} \right|, 1 \right) \cdot \cos(2 \cdot \pi \cdot f \cdot t) df$

...INVERSE FOURIER INTERGRAL MODIFIES THE SRRC RESPONSE BY THE RECIPROCAL OF THE NORMALIZED CIC FREQUENCY RESPONSE. THE MODIFICATION IS ONLY PERFORMED OVER THE FRACTION OF THE SRRC BANDWIDTH AS SPECIFIED BY β.

$h1_{tap} := h1(t_{tap}) \quad h1 := INT\left(\frac{\overrightarrow{h1 \cdot PROC_GAINSCALE}}{max(h1)} \right)$ ...MODIFIED SRRC FILTER COEFFICIENTS INTEGERIZED AND SCALED TO 10-BIT RANGE

OBSOLETE

SRRC AND MODIFIED SRRC IMPULSE RESPONSE



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
$h^T =$	0	0	3	2	–2	–5	–2	5	7	1	–7	–7	7	19	7	–34	–71	–48	71	260	438	511

...FIR FILTER COEFFICIENTS FOR SRRC RESPONSE

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
$h1^T =$	0	1	4	2	–3	–6	–1	7	9	1	–10	–9	8	24	12	–34	–78	–61	56	251	435	511

...FIR FILTER COEFFICIENTS FOR SRRC RESPONSE WITH CIC COMPENSATION

DISPLAY FREQUENCY RESPONSE PLOTS:

$f := 0, 0.001 .. 0.5$ ...NORMALIZED FREQUENCY RANGE [A REQUIREMENT OF MATHCAD'S GAIN() FUNCTION]

$SCALEsrrc := (|gain(h,0)|)^{-1} \quad SCALEsrrc := 5.559 \cdot 10^{-4}$

$SCALEcompsrrc := (|gain(h1,0)|)^{-1} \quad SCALEcompsrrc := 5.79 \cdot 10^{-4}$

$SCALEcic := (|H(0,R)|)^{-1} \quad SCALEcic := 7.716 \cdot 10^{-4}$

...SCALE FACTORS TO ADJUST SRRC, COMPENSATED SRRC, AND CIC FREQUENCY RESPONSES TO UNITY AT f = 0

$FIR(f) := dB(SCALEsrrc \cdot |gain(h,f)|)$ ...FUNCTION TO COMPUTE NORMALIZED, UNCOMPENSATED FIR RESPONSE (SRRC) IN dB

$CIC(f) := dB(SCALEcic \cdot |H(f,R)|)$ ...FUNCTION TO COMPUTE NORMALIZED CIC RESPONSE IN dB

$COMP(f) := dB(SCALEcompsrrc \cdot |gain(h1,f)|)$ ...FUNCTION TO COMPUTE NORMALIZED, COMPENSATED FIR RESPONSE (SRRC + CIC^{-1}) IN dB

$SYSuncomp(f) := FIR(f) + CIC(f)$ ...FUNCTION TO COMPUTE OVERALL SYSTEM RESPONSE OF SRRC AND CIC TOGETHER IN dB

$SYScomp(f) := COMP(f) + CIC(f)$ ...FUNCTION TO COMPUTE OVERALL SYSTEM RESPONSE OF COMPENSATED SRRC AND CIC TOGETHER

SRRC, CIC, AND CORRECTED SRRC RESPONSE

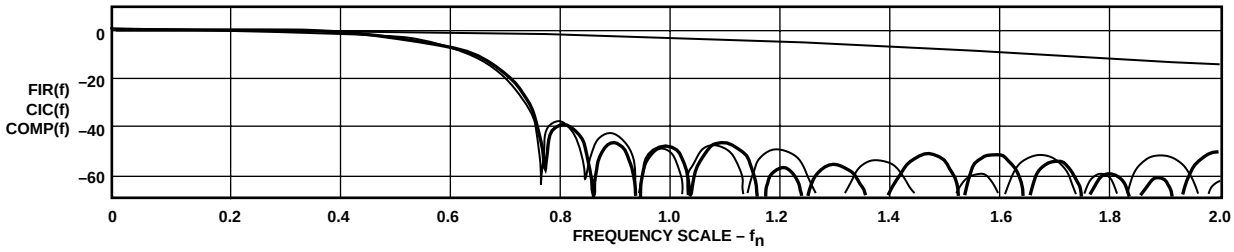
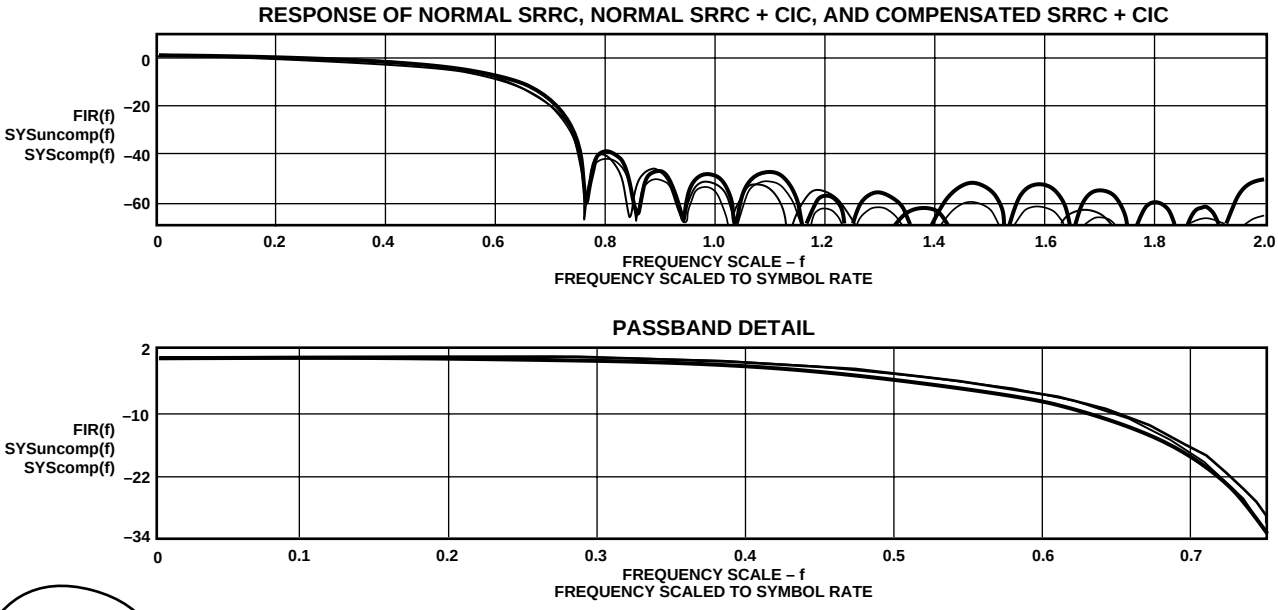


Figure 34. Mathcad Simulation of 41-Tap SRRC Filter with CIC Compensation



OBSOLETE

GLOBAL DECLARATIONS

CONSTANTS:

$\alpha \equiv 0.5$ ...EXCESS BANDWIDTH FACTOR FOR SRRC FREQUENCY RESPONSE

$\beta \equiv 0.9$ ...PORTION OF SRRC BANDWIDTH OVER WHICH APPLY CIC CORRECTION ($0<\beta <= 1$)

$BW \equiv 0.5 \cdot (1+ \alpha)$ ...BANDWIDTH OF SRRC FILTER (RELATIVE TO SYMBOL RATE)

$TAPS \equiv 41$ ...NUMBER OF FIR PULSE SHAPING FILTER TAPS

$SCALE \equiv 511$ ...SETS MAX VALUE OF FIR PULSE SHAPING FILTER BASED ON FINITE WORD SIZE

$FreqScale \equiv 4$ ...UPSAMPLING RATIO OF FIR PULSE SHAPING FILTER (RELATIVE TO THE SYMBOL RATE)

$PROC_GAIN \equiv 1$ ...PROCESSING GAIN OF CIC FILTERS (USED TO CORRELATE RESULTS WITH AD9853 EVAL. BD.)

$N \equiv 4$ ...NUMBER OF COMB/INTEGRATOR STAGES IN CIC FILTER

$M \equiv 1$ ...UNIT DELAYS PER STAGE OF CIC FILTER

FUNCTIONS:

$InRange(x,a,b) \equiv (x \geq a) \cdot (x \leq b)$ ...RETURNS 1 IF a<= x <= b, 0 OTHERWISE

$INT(x) \equiv floor(x + 0.5)$ ...RETURNS NEAREST INTEGER TO x

$dB(x) \equiv if(|x| = 0, -200, 20 \cdot \log(|x|))$ ...RATIO TO DECIBEL CONVERSION FUNCTION

$z(f) \equiv e^{2j \cdot \pi \cdot f}$ ...Z TRANSFORM

$$SRRC(f) \equiv \begin{cases} passband \leftarrow 0.5 \cdot (1 - \alpha) \\ stopband \leftarrow 0.5 \cdot (1 + \alpha) \\ 1 \text{ if } InRange(f, 0, stopband) \\ \quad \begin{cases} \text{if } InRange(f, 0, passband) \\ \quad \cos\left[\frac{\pi}{4 \cdot \alpha} \cdot (2 \cdot f + \alpha - 1)\right] \text{ if } InRange(f, passband, stopband) \end{cases} \\ 0 \text{ otherwise} \end{cases}$$

...SRRC FREQUENCY RESPONSE FUNCTION
(f IS RELATIVE TO THE SYMBOL RATE)

$$H(f,R) \equiv \left(\sum_{k=0}^{R \cdot M - 1} z\left(\frac{f}{R}\right)^{-k} \right)^{N}$$

...CIC FILTER TIME INDEX FREQUENCY RESPONSE FUNCTION

Figure 35. MathCad Simulation (Continued)

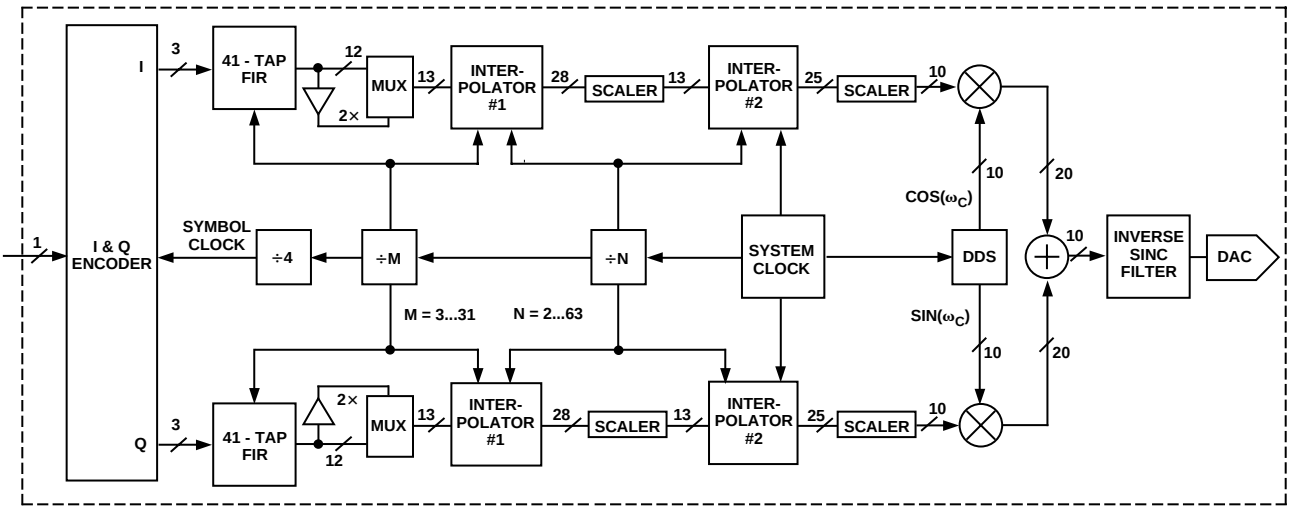


Figure 36. Block Diagram of AD9853 Data Path and Clock Stages

The goal of interpolation is to up-sample the baseband information to the system clock rate and to suppress aliases in the passband. The system clock rate is the sample rate of the sine and cosine signal carriers generated by the DDS in the quadrature modulator stage. Alias suppression is accomplished by the CIC filters as described previously. For timing synchronization, the overall interpolation rate must be set such that the bit rate of the baseband signal be an even integer factor of the system clock rate. The importance of the relationship between the data and system clock rates can not be overstressed. It is restated here for clarity:

The SYSTEM CLOCK RATE must be an EVEN INTEGER MULTIPLE of the DATA BIT RATE.

Following is a design example that demonstrates the principles outlined above.

System Requirements:
- Baseband Bit Rate 1.024 Mb/s
- Carrier Frequency 49 MHz
- Modulation Scheme 16-QAM
- System Power 3.3 V

It should be noted that with a 3.3 V power supply, the maximum system clock rate of the AD9853 is 126 MHz. This sets an upper bound on the system clock.

The first consideration is to make sure that the required carrier frequency is within the AD9853's output frequency range. The carrier frequency should be ≤ 40% of the system clock rate. The given carrier frequency requirement of 49 MHz means that a minimum system clock rate of 122.5 MHz is required; a value within the range of the AD9853's 126 MHz capability.

We must next ensure that the system clock rate is an even integer multiple of the input bit rate. Dividing the system clock rate (122.5 MHz) by the data rate (1.024 Mbps) yields 119.63. Obviously this is not an integer, so we must select the nearest even integer value (in this case, 120) as the data rate multiplier. Thus, a system clock rate of 122.88 MHz is required (120 × 1.024 Mbps). With 6× REFCLK engaged, the reference clock input will be 1/6th of the system clock rate, or 20.48 MHz.

Finally, the two interpolator rates must be determined. Since the FIR filter and interpolator stages will be operating on 16-QAM symbols, the data rate must be converted from bits/second to symbols/second (baud). Each 16-QAM symbol is composed of four serial data bits. Therefore, the baud rate at the input to the FIR filter is 1.024 Mbps/4 = 256k baud. The FIR pulse shaping filters up-sample by a factor of 4. This fixes the FIR sample clock at 256k baud × 4, or 1.024 MSPS. With the FIR sampling at a 1.024 MSPS rate, and a previously determined system clock rate of 122.88 MHz, the interpolators must up-sample by a factor of 120 (122.88/1.024 = 120).

Rule of Thumb: divide the interpolating burden as equally as possible among the two interpolators.

Since the required rate change ratio is 120, select a value of 10 for interpolator #1 and 12 for interpolator #2 (10 × 12 = 120). This satisfies the requirements for the two programmable interpolator stages.

Thus far we have established the rate change ratios for the interpolators. However, there is an additional consideration. By default, the interpolators have an intrinsic gain (or loss) that is dependent on the selected interpolation rate. Since there is the potential to have overall CIC gains of greater than unity, care must be taken to avoid the occurrence of overflow in the interpolators.

Interpolator Scaling

Proper signal processing in the AD9853 depends on data propagating through the pulse-shaping filter and interpolator stages with as flat a baseband response as possible. In addition to the frequency response issue, it is also necessary to ensure that the numerical data propagating through the interpolators does not result in an overflow condition.

As mentioned earlier, the interpolators are implemented using a CIC filter. In the AD9853, the CIC filter is designed using fixed-point processing and two cascaded CIC filter sections (Interpolator #1 and Interpolator #2). It is important to understand that in a CIC filter, the integration portion of the circuit will require the accumulation of values based on the rate change factor, *R*. This means that the size of the data word grows in a manner dependent on the choice of R. In the case of Interpolator #1, the circuit is designed around a maximum R of 32 and this results in an output register width of 28 bits. The design of Interpolator #2 requires an output register width of 25 bits.

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These register widths have been chosen to accommodate the highest values of R for each interpolator. When values of R are chosen that are less than the maximum value, then data will accumulate only in the lesser significant bits of the output register. This is an important point to consider since only 13 bits of 28 are passed on from Interpolator #1 to Interpolator #2, and only 10 bits of 25 are passed on from Interpolator #2 to the I and Q modulator (see Figure 36). If only the most significant bits were to be passed on, then low R values would result in most (possibly all) of the bits being 0s because data would have accumulated only in the less significant bits of the output register. Obviously, it is necessary to have a mechanism that allows one to select which group of bits to pass on to the next stage in order to prevent the loss of data by truncation.

In the AD9853 this mechanism is handled by means of the Interpolator #1 and #2 Scaling Registers (control bus addresses 14h and 15h). The scaling word written into each register selects a group of bits at the output of the appropriate interpolator. In the case of Interpolator #1 this is a 13-bit group, while in the case of Interpolator #2 it is a 10-bit group. Inspection of the scaling registers indicates that Interpolator #1 uses a 5-bit scaling word while Interpolator #2 uses a 6-bit scaling word.

At first inspection it would seem as though there are 32 and 64 scaling steps for Interpolator #1 and #2, respectively. This is not the case, however. The scaling word is actually decoded in a nonlinear manner and there is considerable overlap; i.e., several different register values may actually select the same group of bits at the interpolator output. Table III lists the relationship between the scaling word value and the highest bit of the interpolator output register which becomes the most significant bit (MSB) of the group selected.

Table III. Interpolator Scale Bit Selection

Interpolator #1		Interpolator #2	
Scaling Register Value (Decimal)	**Highest Bit Selected from Output Register**	**Scaling Register Value (Decimal)**	**Highest Bit Selected from Output Register**
0	12	0	12
1	15	1	14
2	16	2	15
3–4	18	3–4	16
5	19	5–6	17
6	20	7–10	18
7–9	21	11–14	19
10–11	22	15–21	20
12–14	23	22–30	21
15–19	24	31–44	22
20–24	25	45–62	23
25–30	26	63	24
31	27		

Selection of the proper scaling value is dependent on the selection of R for the interpolator. It is desirable to choose a scale value that ensures that the MSB of the selected group of bits coincides with the highest useful bit in the output register. To accomplish this condition, use the following rule:

Scaling Rule: For a particular interpolator, choose a nominal Scaling Register value that is ONE LESS than the interpolation rate (R) for the same interpolator.

For example, if Interpolator #1 is set for an interpolation rate of 6, then choose a Scaling Register value of 5 for Interpolator #1.

It has already been mentioned that the required number of bits at the output of the CIC filter is a function of R. It turns out that for values of R that are a power of 2, the number of bits required to handle the growth of the output register is an integer. This results in a processing gain of unity for the CIC filter. For values of R that are not a power of 2, the required number of output bits is not an integer. This results in a processing gain that is not unity. Tables IV and V detail the relationship between the Scaling Register values and the processing gain for Interpolator #1 and Interpolator #2. Note that certain Scale Register values for a particular R yield a processing gain greater than unity. Thus, it is possible that the nominal Scaling Register values will result in a total CIC processing gain of > 1.

WARNING: It is of utmost importance the user make certain that the total processing gain of the data path be ≤ 1.

That is, the product of the FIR gain, Interpolator #1 gain, and Interpolator #2 gain must be ≤ 1. This is because total processing gains of > 1 may result in an overflow condition within the CIC filters, which puts the hardware in a nonrecoverable state (short of resetting the device). The contents of Tables IV and V offer the user some flexibility in the choice of processing gains for a particular interpolation rate. For example, let us assume that an overall interpolation rate of 25 is required. A value of R = 5 for both interpolators satisfies this requirement, which leads to a Scale Register value of 4 for each interpolator. Note, however, that under these conditions the processing gain for the CIC filters alone is 3.053 (1.953 × 1.563).

There are two ways in which we can handle this situation. The first is to scale the coefficients of the FIR filter by 0.3275 (1/3.053), which reduces the total processing gain to 1. The disadvantage here is that the FIR coefficients are 10-bit signed integers and scaling by 0.3275 may result in an unacceptable level of truncation caused by the finite resolution. The second method makes use of Tables IV and V. We can choose the Alternate Scale Value of 5 (instead of 4) for Interpolator #2. This results in a processing gain of 1.525 (1.953 × 0.781). We can now scale the FIR coefficients by a more modest value of 0.6557 (1/1.525) and net an overall gain of unity through the three stages. Of course, we could just as easily have chosen the Alternate Scale Value for Interpolator #1 and modified the FIR coefficients accordingly. Typically, the choice of interpolator scale values that results in an overall gain closest to (but not less than) one is selected. Then the FIR coefficients are scaled downward to yield unity gain.

OBSOLETE

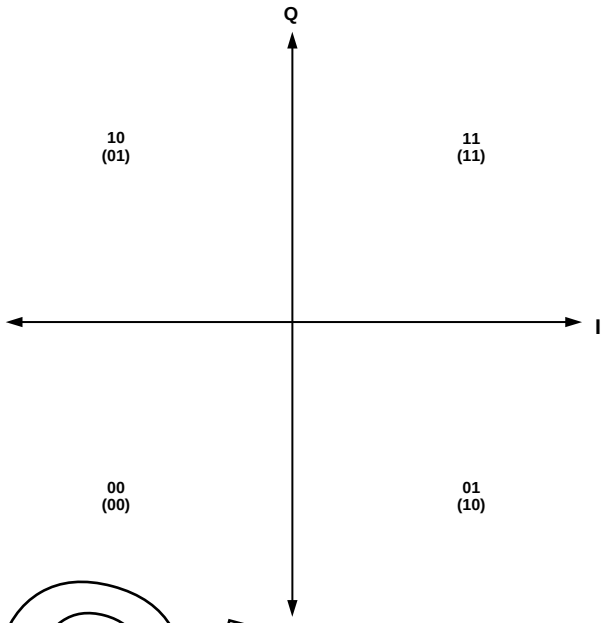
Table IV. Interpolator #1

Rate Change Factor (R)	Nominal Scale Value (R-1)	Nominal Gain	Alternate Scale Value	Resulting Gain
03	02	1.688	03	0.844
04	03	1.000	05	0.500
05	04	1.953	05	0.977
06	05	1.688	06	0.844
07	06	1.340	07	0.670
08	07	1.000	10	0.500
09	08	1.424	10	0.712
10	09	1.953	10	0.977
11	10	1.300	12	0.650
12	11	1.688	12	0.844
13	12	1.073	15	0.536
14	13	1.340	15	0.670
15	14	1.648	15	0.824
16	15	1.000	20	0.500
17	16	1.199	20	0.600
18	17	1.424	20	0.712
19	18	1.675	20	0.837
20	19	1.953	20	0.977
21	20	1.130	25	0.565
22	21	1.300	25	0.650
23	22	1.485	25	0.743
24	23	1.688	25	0.844
25	24	1.907	25	0.954
26	25	1.073	31	0.536
27	26	1.201	31	0.601
28	27	1.340	31	0.670
29	28	1.489	31	0.744
30	29	1.648	31	0.824
31	30	1.818	31	0.909

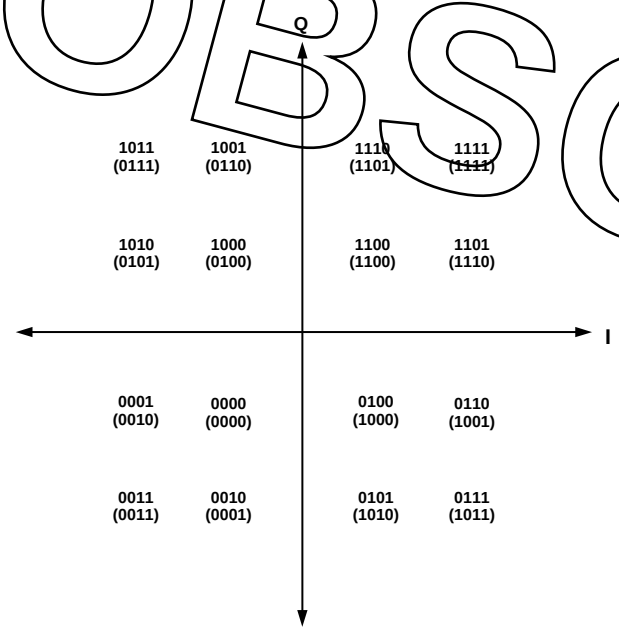
Table V. Interpolator #2

Rate Change Factor (R)	Nominal Scale Value (R-1)	Nominal Gain	Alternate Scale Value	Resulting Gain
02	01	1.000	02	0.500
03	02	1.125	03	0.563
04	03	1.000	05	0.500
05	04	1.563	05	0.781
06	05	1.125	07	0.563
07	06	1.531	07	0.766
08	07	1.000	11	0.500
09	08	1.266	11	0.633
10	09	1.563	11	0.781
11	10	1.891	11	0.945
12	11	1.125	15	0.563
13	12	1.320	15	0.660
14	13	1.531	15	0.766
15	14	1.758	15	0.879
16	15	1.000	22	0.500
17	16	1.129	22	0.564
18	17	1.266	22	0.633
19	18	1.410	22	0.705
20	19	1.563	22	0.781
21	20	1.723	22	0.861
22	21	1.891	22	0.945
23	22	1.033	31	0.517
24	23	1.125	31	0.563
25	24	1.221	31	0.610
26	25	1.320	31	0.660
27	26	1.424	31	0.712
28	27	1.531	31	0.766
29	28	1.645	31	0.821
30	29	1.758	31	0.879
31	30	1.877	31	0.938
32	31	1.000	45	0.500
33	32	1.063	45	0.532
34	33	1.129	45	0.564
35	34	1.196	45	0.598
36	35	1.266	45	0.633
37	36	1.337	45	0.668
38	37	1.410	45	0.705
39	38	1.485	45	0.743
40	39	1.563	45	0.781
41	40	1.642	45	0.821
42	41	1.723	45	0.861
43	42	1.806	45	0.903
44	43	1.891	45	0.945
45	44	1.978	45	0.989
46	45	1.033	63	0.517
47	46	1.079	63	0.539
48	47	1.125	63	0.563
49	48	1.172	63	0.586
50	49	1.221	63	0.610
51	50	1.270	63	0.635
52	51	1.320	63	0.660
53	52	1.372	63	0.686
54	53	1.424	63	0.712
55	54	1.477	63	0.739
56	55	1.531	63	0.766
57	56	1.586	63	0.793
58	57	1.643	63	0.821
59	58	1.700	63	0.850
60	59	1.758	63	0.879
61	60	1.817	63	0.908
62	61	1.877	63	0.938
63	62	1.938	63	0.969

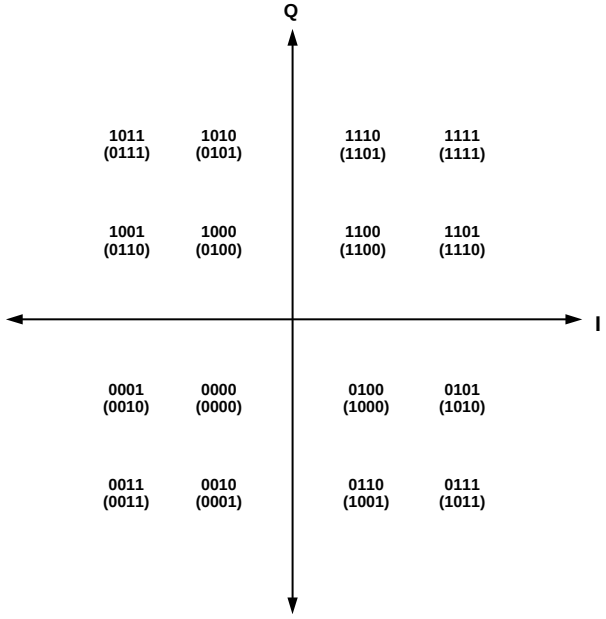
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a. QPSK Symbol Mapping



b. D16-QAM Symbol Mapping



c. 16-QAM Gray-Coded Symbol Mapping

Figure 37. Symbol Mapping for QPSK, 16-QAM, and DQAM, Spectrum = I × COS + Q × SIN (Spectrum = I × COS – Q × SIN)

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MIXERS, ADDER, INVERSE SINC FUNCTIONS

At the output of the Interpolation filters, the pulse-shaped, upsampled I and Q baseband data is multiplied with digitized quadrature versions of the carrier, $\cos(\omega_C t)$ and $\sin(\omega_C t)$ respectively, which are provided by a direct digital synthesizer (DDS) block. The DDS block has a 32-bit tuning word that results in an extremely fine frequency tuning resolution of $f_{CLOCK}/2^{32}$, as well as extremely fast output frequency switching. The multiplier outputs are then summed to form the QPSK/QAM-modulated signal. This signal is then filtered by an inverse sinc filter to compensate for the SINx/x roll-off function inherent in the digital-to-analog conversion process. The inverse sinc filter flattens the gain response across the Nyquist bandwidth. This is most critical for higher data rate signals that are placed on carriers at the high end of the spectrum where the uncompensated SINx/x roll-off would be getting progressively steeper. Gain attenuation across a channel will result in modulation quality impairments, such as degraded error vector magnitude (EVM).

The spectral inversion bit, when enabled, inverts the Q data at the input to the adder circuit in the quadrature amplitude modulator section. This has the effect of reversing the direction of the phase rotation around the constellation map. Positive phase rotation on the I/Q constellation plane corresponds to counterclockwise movement. For example, the symbols in parentheses on the QPSK constellation in Figure 37 corresponds to a spectral mapping of I × COS – Q × SIN. The phase rotation from symbol value 11 to 01 is a positive 90 degree rotation. Traversing around the constellation in a positive direction, there are also positive 90 degree rotations from 01 to 00, 00 to 10, and 10 back to 11. If the spectral invert bit is disabled, providing the spectral map I × COS + Q × SIN as shown in Figure 37, a phase rotation from symbol value 11 to 01 now corresponds to a negative 90 degrees of phase rotation. Similarly, there are now negative 90 degree phase rotations from 01 to 00, 00 to 10 and 10 back to 11. In other words, the direction of phase rotation

around the constellation has simply been reversed. This effect also holds true for the 16-QAM and D16-QAM constellations shown in the respective I × COS – Q × SIN and I × COS + Q × SIN mappings shown in Figure 37.

DIRECT DIGITAL SYNTHESIZER FUNCTION

The direct digital synthesizer (DDS) block delivers the sine/cosine carriers that are digitally modulated by the I/Q data paths. The DDS function is frequency tuned via the control bus with a 32-bit tuning word. This allows the AD9853's output carrier frequency to be very precisely tuned while still providing output frequency agility.

The equation relating output frequency of the AD9853 digital modulator to the frequency tuning word (FTWORD) and the reference clock (REFCLK) is given as:

$$f_{OUT} = (FTWORD \times REFCLK)/2^{32}$$

where: f_{OUT} and *REFCLK* frequencies are in Hz and *FTWORD* is a decimal number from 0 to $(2^{32})/2$

Example: Find the FTWORD for f_{OUT} = 41 MHz and REFCLK = 122.88 MHz.

If f_{OUT} = 41 MHz and REFCLK = 122.88 MHz, then:

$$FTWORD = 556AAAAA\ hex$$

Loading 556AAAAAh into control bus registers 16h–19h programs the AD9853 for f_{OUT} = 41 MHz, given a REFCLK frequency of 122.88 MHz.

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D/A CONVERTER

Up to this point all the processing has been in the digital domain. In order to pass the modulated signal onto the cable driver for amplification to the levels required to drive the 75 ohm cable, a digital-to-analog converter (DAC) is implemented. The DAC needs to have good enough transient characteristics so as not to add significant spurious in the spectrum. Typically the worst spurs from the DAC are due to harmonics of the fundamental signal and their aliases (please see the AD9850 complete-DDS data sheet for a detailed explanation of aliased images). These harmonics are worst case for the higher carrier frequencies. The AD9853 contains a wideband 10-bit DAC which maintains spurious-free dynamic range (SFDR) performance of –50 dBc up to 42 MHz A_{OUT} and –44 dBc up to 65 MHz A_{OUT}.

The conversion process will produce aliased components at the DAC output at $n \times f_{CLOCK} \pm f_{CARRIER}$ (n = 1, 2, 3, ...). These are typically filtered with an external RLC filter between the DAC and the line driver amplifier. Again, it is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid the aforementioned modulation impairments. A relatively inexpensive seventh order elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

The AD9853 provides true and complement outputs, Pins 24 and 25, which are current outputs. The full-scale output current is set by the R_{SET} resistor at Pin 18. The value of R_{SET} for a particular I_{OUT} is determined using the following equation:

$$R_{SET} = 32\ (1.248\ V/I_{OUT})$$

For example, if a full-scale output current of 20 mA is desired, then R_{SET} = 32(1.248/0.02), or approximately 2 kΩ. Every doubling of the R_{SET} value will halve the output current. Maximum output current is specified as 20 mA.

The full-scale output current range of the AD9853 is 5 mA–20 mA, with 10 mA being the optimal value for best spurious-free dynamic range (SFDR). Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching, that is, for best SFDR, the two outputs should be equally terminated.

The output load should be located as close as possible to the AD9853 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads (such as an LC filter). Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance, that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9853 will see for signals within the filter passband. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9853. The resistor at the filter input will mask the reactive components of the LC filter and provide a termination for signals outside the filter pass band.

The output compliance voltage of the AD9853 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V, otherwise, signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The use of a transformer with a grounded center-tap for common-mode rejection results in signals at the AD9853 DAC output pins that are symmetrical about ground.

As previously mentioned, by differentially combining the two signals the user can provide some degree of common-mode signal rejection. The amount of rejection is dependent upon how closely the common-mode signals of each output are matched in amplitude and phase. If the signals are exactly alike, then ideally, there would be 100 percent rejection in a perfect differential amplifier or combiner. A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or "clock feed through" that is present on both input signals. The AD9853 true and complement outputs can be differentially combined and, in fact, are configured as such on the AD9853-XXPCB evaluation board. This evaluation board utilizes a broadband 1:1 transformer with a grounded, center-tapped primary to perform differential combining of the two DAC outputs.

REFERENCE CLOCK MULTIPLIER

Due to the fact that the AD9853 is a DDS-based modulator, a relatively high frequency system clock is required. For DDS applications the carrier is typically limited to about 40% of f_{CLOCK}. For a 65 MHz carrier, the system clock required is above 150 MHz. To avoid the cost associated with these high frequency references, and the aggravating noise coupling issues associated with operating a high frequency clock on a PC board, the AD9853 provides an on-chip 6× clock multiplier. With the 6× on-chip multiplier, the input reference clock required for the AD9853 can be kept in the 20 MHz to 30 MHz range, which results in cost and system implementation savings. The 6× REFCLK multiplier maintains clock integrity as evidenced by the AD9853's system phase noise characteristics of –100 dBc/Hz and virtually no clock related spurious in the output spectrum. External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 µF) provide the compensation zero for the 6× REFCLK PLL loop. The overall loop performance has been optimized for these component values.

Table VI. Derivation of Currently Transmitted Symbol Quadrant

Current Input Bits I Q	Quadrant Phase Change	MSBs of Previously Transmitted Symbol	MSBs for Currently Transmitted Symbol
00	0°	11	11
00	0°	01	01
00	0°	00	00
00	0°	10	10
01	90°	11	01
01	90°	01	00
01	90°	00	10
01	90°	10	11
11	180°	11	00
11	180°	01	10
11	180°	00	11
11	180°	10	01
10	270°	11	10
10	270°	01	11
10	270°	00	01
10	270°	10	00

Note: This table applies to both DQPSK and D16-QAM formats. In DQPSK a symbol is comprised of two bits that are denoted as " I(1) Q(1)." In this case, I(1) and Q(1) are the MSBs and the table can be interpreted directly. In D16-QAM a symbol is defined as comprised of four bits denoted as "I(1) Q(1) I(0) Q(0)." I(1), Q(1) are the MSBs and I(0), Q(0) are the LSBs. As indicated in the table, only the MSBs I(1) and Q(1) are altered as a function of the differential coding; I(0) and Q(0) are not altered.

DEVICE THERMAL CONSIDERATIONS

The AD9853 is specified to operate at an ambient temperature of up to +85°C. The maximum junction temperature (T_J) is specified at +150°C, which provides a worst case junction-to-air differential of +65°C. Thus, with the specified θ_{JA} of +36°C/W, a maximum device dissipation of 1.8 W is achievable under the worst case conditions. It is important to understand that a significant portion of the heat generated by the device is transferred to the environment via the package leads. The specified θ_{JA} value assumes that the device is soldered to a multilayer printed circuit board (PCB) with the device power and ground pins connected directly to power and ground planes of the PCB.

The amount of power internally generated by the device is primarily dependent on four factors:

- Power Supply Voltage
- System Clock Rate
- Input Data Rate
- T_XENABLE Duty Cycle (assuming the device is operated in the burst data mode)

The power generated by the device increases with an increase in any one of the four factors. It turns out that the contribution of generated power due to the system clock rate, input data rate and T_XENABLE duty cycle may be ignored at power supply voltages of less than 4 V (as the total power generated by the device will not exceed 1.8 W). However, for supply voltages greater than 4 V, operation at +85°C ambient temperature will require a tradeoff among the other three factors; i.e., a reduced system clock rate, a reduced data rate, a reduced T_XENABLE duty cycle, or some combination of the three. It should be mentioned, that operation at a power supply voltage of 4 V yields the same level of performance as specified at 5 V operation. For example, the user may still take advantage of the 165 MHz maximum system clock rate specified for 5 V operation.

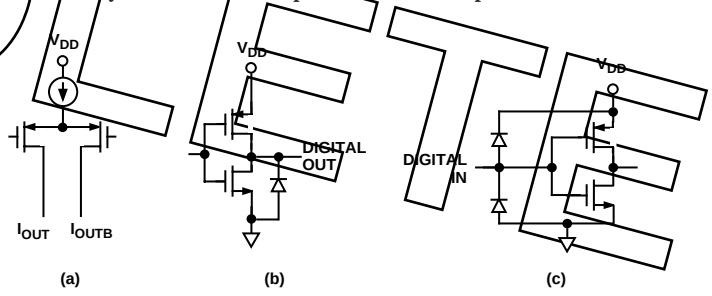


Figure 38. Equivalent I/O Circuits

AD9853-xxPCB EVALUATION BOARD

Two versions of evaluation boards are available for the AD9853 digital QPSK/16-QAM modulator: the AD9853-45PCB and the AD9853-65PCB. The –45 contains a 45 MHz low-pass filter to support a 5 MHz–42 MHz output bandwidth and the –65 has a 65 MHz low-pass filter to support a 5 MHz–65 MHz output bandwidth.

Both versions of the evaluation board contain the AD9853 device, a REFCLOCK oscillator, a seventh order elliptic low-pass filter of the designated frequency, an AD8320 programmable cable driver amplifier, operating software for Windows® 3.1 or Windows 95, and a booklet of complete operating instructions and performance graphs. The evaluation board provides an optimal environment for menu-driven programming of the devices and analysis of output spectral performance.

Part Number	On-Board Low-Pass Filter
AD9853-45PCB	45 MHz
AD9853-65PCB	65 MHz

Windows is a registered trademark of Microsoft, Corporation.

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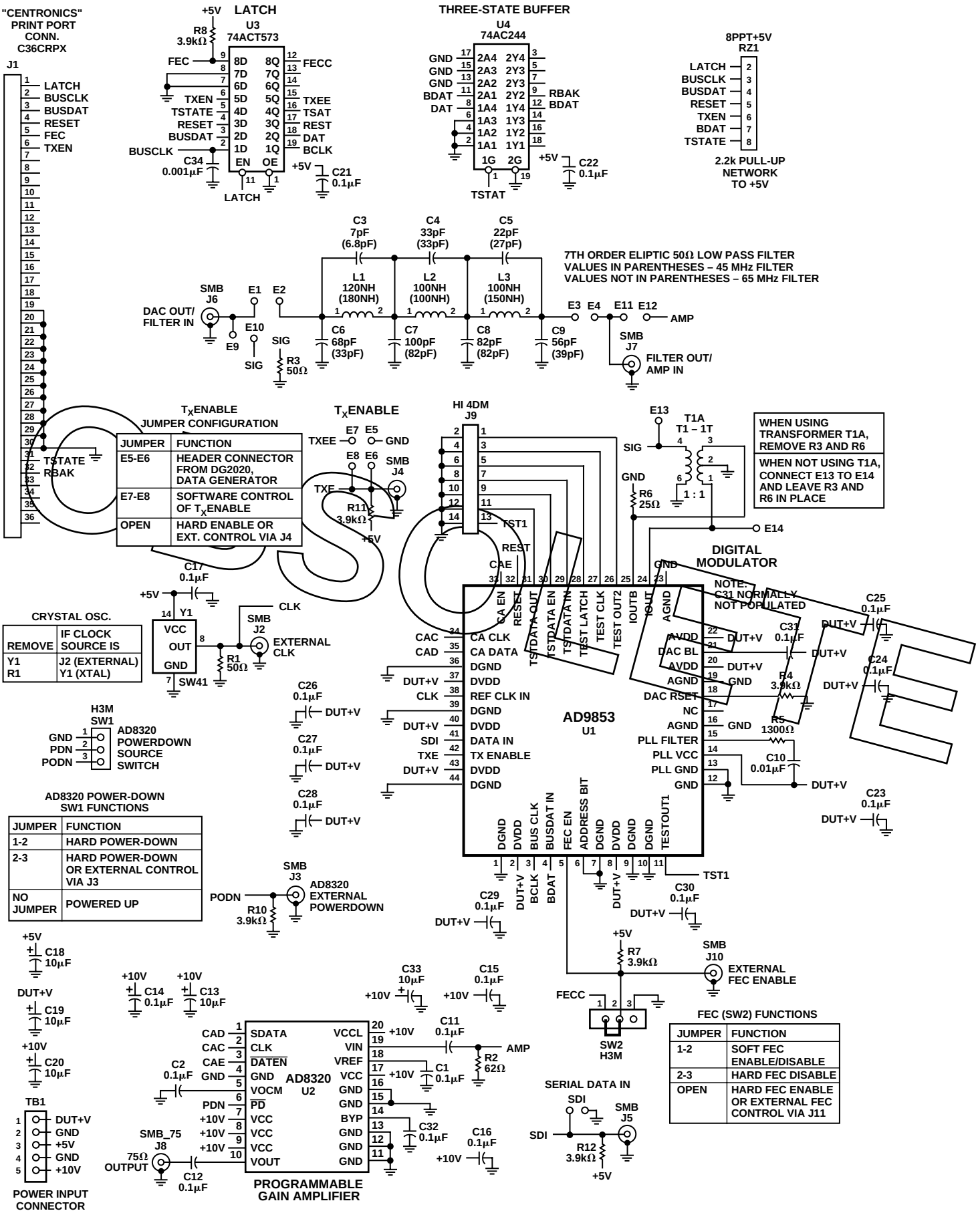
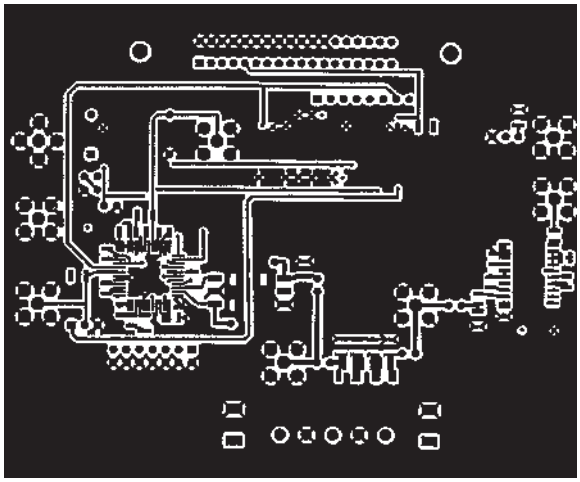
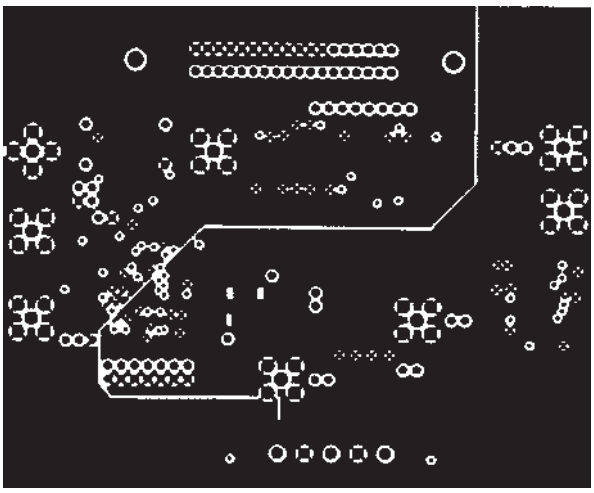


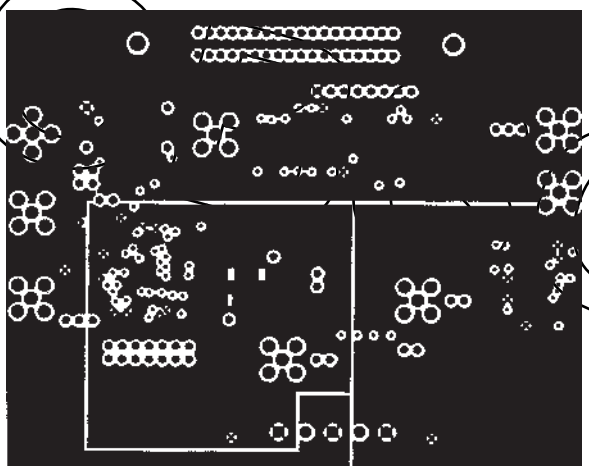
Figure 39. Electrical Schematic of AD9853-xxPCB Evaluation Board



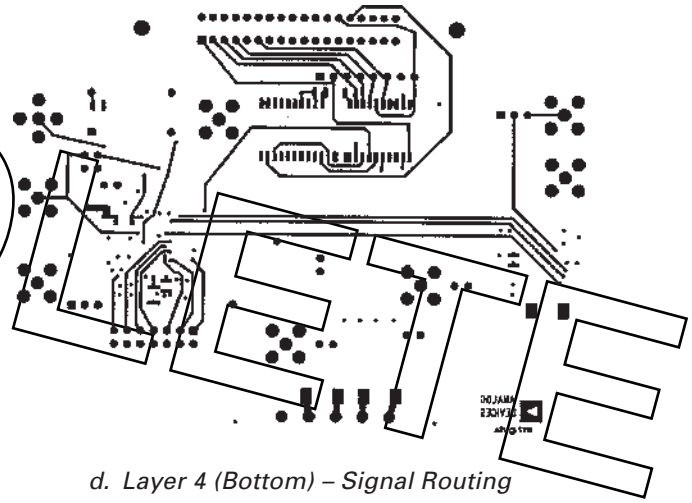
a. Layer 1 (Top) – Signal Routing and Ground Plane



c. Layer 3 – DUT +V, +5 V, and +12 V Power Plane



b. Layer 2 – Ground Plane



d. Layer 4 (Bottom) – Signal Routing

Figure 40. PCB Layout Patterns for the Four-Layer AD9853-xxPCB Evaluation Board

Plots of typical output spectrum from the AD9853-45PCB evaluation board (conditions: DUT supply voltage = +3.3 V, QPSK modulation, 2.048 Mb/s, 20.48 MHz ext. REFCLK, 6× REFCLK enabled, SRRC filter function, A_{OUT} = 40 MHz, α = 0.25, 50 MHz low-pass filter).

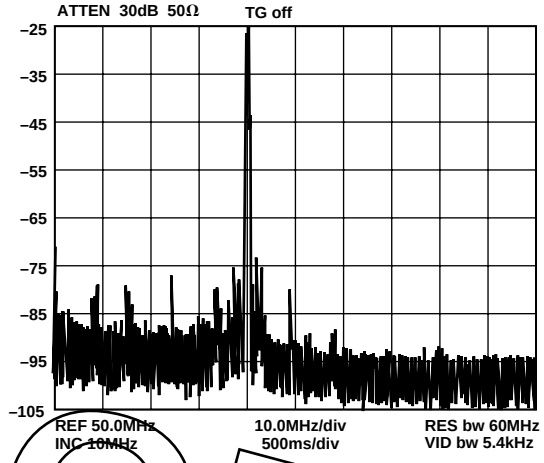


Figure 41. Direct DAC Output

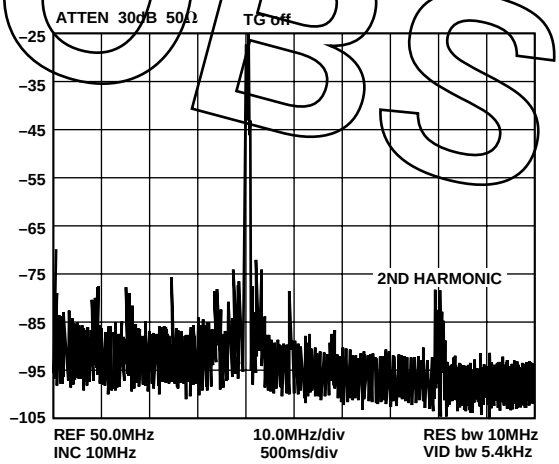


Figure 42. Output of AD8320 Programmable Line Driver Amplifier Driven by AD9853 Modulator

Plots of typical output spectrum from the AD9853-65PCB evaluation board (conditions: DUT supply voltage = +4.0 V, QPSK modulation, 2.7792 Mb/s, 27.792 MHz ext. REFCLK, 6× REFCLK enabled, SRRC filter function, A_{OUT} = 60 MHz, α = 0.25, 70 MHz low-pass filter).

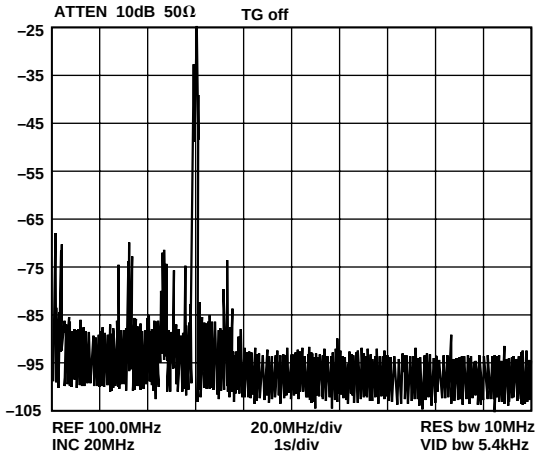


Figure 43. Direct DAC Output

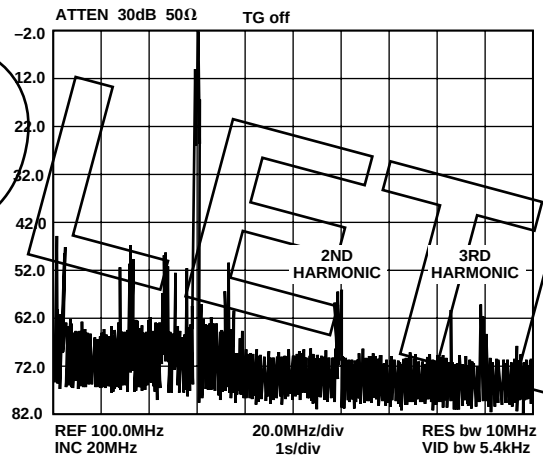


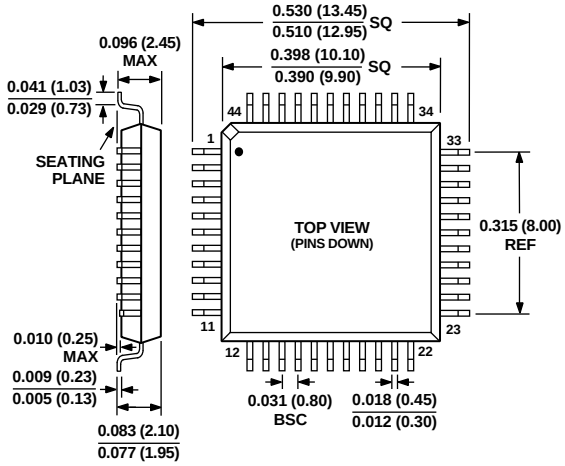
Figure 44. Output of AD8320 Programmable Line Driver Amplifier Driven by AD9853 Modulator

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Metric Quad Flatpack (MQFP)
(S-44A)



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