CMOS 300 MSPS Quadrature Complete DDS

Data Sheet

AD9854

FEATURES

- 300 MHz internal clock rate
- FSK, BPSK, PSK, chirp, AM operation
- Dual integrated 12-bit digital-to-analog converters (DACs)
- Ultrahigh speed comparator, 3 ps rms jitter
- Excellent dynamic performance
  - 80 dB SFDR at 100 MHz (±1 MHz) A_{OUT}
- 4× to 20× programmable reference clock multiplier
- Dual 48-bit programmable frequency registers
- Dual 14-bit programmable phase offset registers
- 12-bit programmable amplitude modulation and on/off output shaped keying function
- Single-pin FSK and BPSK data interfaces
- PSK capability via input/output interface
- Linear or nonlinear FM chirp functions with single-pin frequency hold function
- Frequency-ramped FSK
- <25 ps rms total jitter in clock generator mode
- Automatic bidirectional frequency sweeping
- Sin(x)/x correction
- Simplified control interfaces
  - 10 MHz serial 2- or 3-wire SPI compatible
  - 100 MHz parallel 8-bit programming
- 3.3 V single supply
- Multiple power-down functions
- Single-ended or differential input reference clock
- Small, 80-lead LQFP or TQFP with exposed pad

APPLICATIONS

- Agile, quadrature LO frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Commercial and amateur RF exciters

FUNCTIONAL BLOCK DIAGRAM

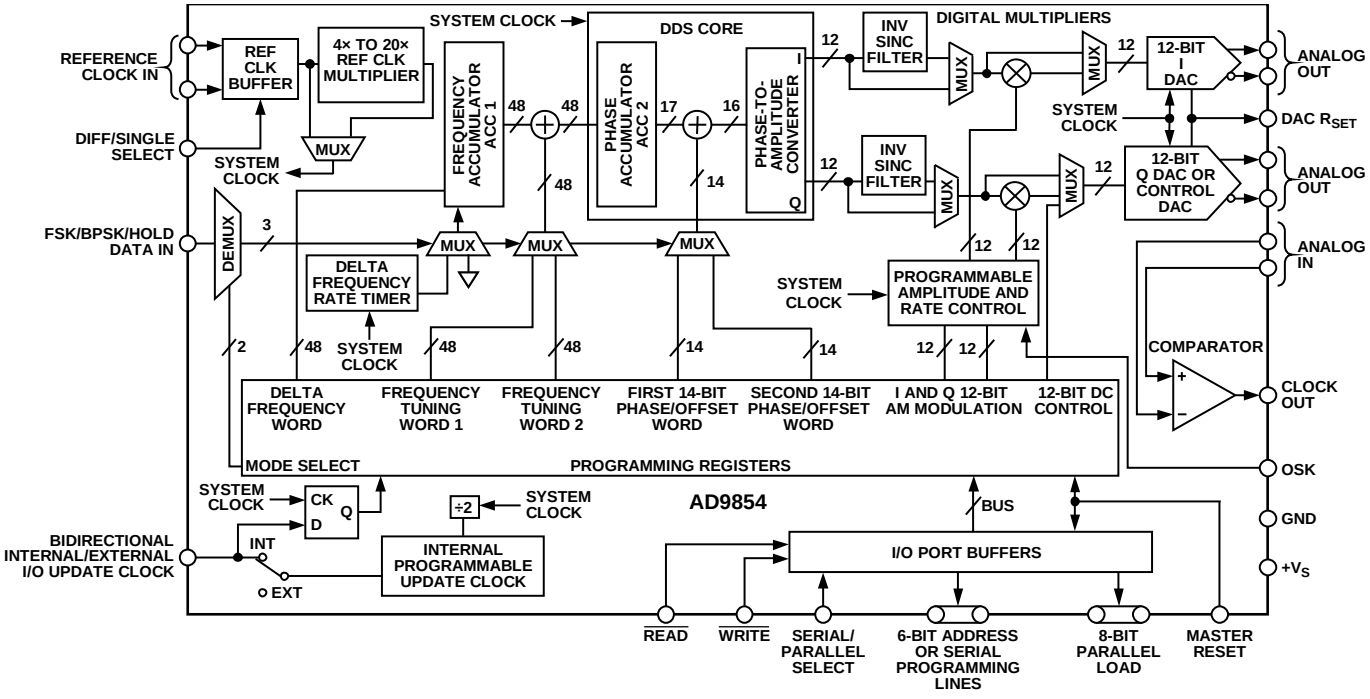


Figure 1.

Rev. F

Document Feedback

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8/2019—Rev. E to Rev. F

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7/2007—Rev. D to Rev. E

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Changed AD9854AST to AD9854ASTZ ... Universal
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3/2002—Rev. A to Rev. B

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Renumbered Figures and Tables ..... Universal
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10/1999—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high speed, high performance quadrature DACs to form a digitally programmable I and Q synthesizer function. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase, amplitude-programmable sine and cosine outputs that can be used as an agile LO in communications, radar, and many other applications. The innovative high speed DDS core of the AD9854 provides 48-bit frequency resolution (1 μHz tuning resolution with 300 MHz SYSCLK). Retaining 16 bits for phase-to-amplitude conversion ensures excellent spurious-free dynamic range (SFDR).

The circuit architecture of the AD9854 allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The sine wave output (externally filtered) can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides two 14-bit phase registers and a single pin for BPSK operation.

For higher-order PSK operation, the I/O interface can be used for phase changes. The 12-bit I and Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrow-band output SFDR. The Q DAC can also be configured as a user-programmable control DAC if the quadrature function is not desired. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in high speed clock generator applications.

Two 12-bit digital multipliers permit programmable amplitude modulation, on/off output shaped keying, and precise amplitude control of the quadrature output. Chirp functionality is also included to facilitate wide bandwidth frequency sweeping applications. The programmable 4× to 20× REFCLK multiplier circuit of the AD9854 internally generates the 300 MHz system clock from an external lower frequency reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source.

Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of ramped FSK are supported. The AD9854 uses advanced 0.35 μm CMOS technology to provide a high level of functionality on a single 3.3 V supply.

The AD9854 is pin-for-pin compatible with the AD9852 single-tone synthesizer. It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

V_S = 3.3 V ± 5%, R_{SET} = 3.9 kΩ, external reference clock frequency = 30 MHz with REFCLK multiplier enabled at 10× for AD9854ASVZ, external reference clock frequency = 20 MHz with REFCLK multiplier enabled at 10× for AD9854ASTZ, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9854ASVZ Min	AD9854ASVZ Typ	AD9854ASVZ Max	AD9854ASTZ Min	AD9854ASTZ Typ	AD9854ASTZ Max	Unit
REFERENCE CLOCK INPUT CHARACTERISTICS[1]									
Internal System Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	20		300	20		200	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
External Reference Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	5		75	5		50	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
Duty Cycle	25°C	IV	45	50	55	45	50	55	%
Input Capacitance	25°C	IV		3			3		pF
Input Impedance	25°C	IV		100			100		kΩ
Differential Mode Common-Mode Voltage Range									
Minimum Signal Amplitude[2]	25°C	IV	400			400			mV p-p
Common-Mode Range	25°C	IV	1.6	1.75	1.9	1.6	1.75	1.9	V
V_{IH} (Single-Ended Mode)	25°C	IV	2.3			2.3			V
V_{IL} (Single-Ended Mode)	25°C	IV			1			1	V
DAC STATIC OUTPUT CHARACTERISTICS									
Output Update Speed	Full	I			300			200	MSPS
Resolution	25°C	IV		12			12		Bits
I and Q Full-Scale Output Current	25°C	IV	5	10	20	5	10	20	mA
I and Q DAC DC Gain Imbalance[3]	25°C	I	−0.5	+0.15	+0.5	−0.5	+0.15	+0.5	dB
Gain Error	25°C	I	−6		+2.25	−6		+2.25	% FS
Output Offset	25°C	I			2			2	µA
Differential Nonlinearity	25°C	I		0.3	1.25		0.3	1.25	LSB
Integral Nonlinearity	25°C	I		0.6	1.66		0.6	1.66	LSB
Output Impedance	25°C	IV		100			100		kΩ
Voltage Compliance Range	25°C	I	−0.5		+1.0	−0.5		+1.0	V
DAC DYNAMIC OUTPUT CHARACTERISTICS									
I and Q DAC Quadrature Phase Error	25°C	IV		0.2	1		0.2	1	Degrees
DAC Wideband SFDR									
1 MHz to 20 MHz A_{OUT}	25°C	V		58			58		dBc
20 MHz to 40 MHz A_{OUT}	25°C	V		56			56		dBc
40 MHz to 60 MHz A_{OUT}	25°C	V		52			52		dBc
60 MHz to 80 MHz A_{OUT}	25°C	V		48			48		dBc
80 MHz to 100 MHz A_{OUT}	25°C	V		48			48		dBc
100 MHz to 120 MHz A_{OUT}	25°C	V		48			48		dBc
DAC Narrow-Band SFDR									
10 MHz A_{OUT} (±1 MHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±250 kHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±50 kHz)	25°C	V		91			91		dBc
41 MHz A_{OUT} (±1 MHz)	25°C	V		82			82		dBc
41 MHz A_{OUT} (±250 kHz)	25°C	V		84			84		dBc
41 MHz A_{OUT} (±50 kHz)	25°C	V		89			89		dBc
119 MHz A_{OUT} (±1 MHz)	25°C	V		71			71		dBc
119 MHz A_{OUT} (±250 kHz)	25°C	V		77			77		dBc
119 MHz A_{OUT} (±50 kHz)	25°C	V		83			83		dBc

Parameter	Temp	Test Level	AD9854ASVZ Min	AD9854ASVZ Typ	AD9854ASVZ Max	AD9854ASTZ Min	AD9854ASTZ Typ	AD9854ASTZ Max	Unit
Residual Phase Noise									
(A_{OUT} = 5 MHz, External Clock = 30 MHz									
REFCLK Multiplier Engaged at 10×)									
1 kHz Offset	25°C	V		140			140		dBc/Hz
10 kHz Offset	25°C	V		138			138		dBc/Hz
100 kHz Offset	25°C	V		142			142		dBc/Hz
(A_{OUT} = 5 MHz, External Clock = 300 MHz,									
REFCLK Multiplier Bypassed)									
1 kHz Offset	25°C	V		142			142		dBc/Hz
10 kHz Offset	25°C	V		148			148		dBc/Hz
100 kHz Offset	25°C	V		152			152		dBc/Hz
PIPELINE DELAYS[4, 5, 6]									
DDS Core (Phase Accumulator and Phase-to-Amp Converter)	25°C	IV		33			33		SYSCLK cycles
Frequency Accumulator	25°C	IV		26			26		SYSCLK cycles
Inverse Sinc Filter	25°C	IV		16			16		SYSCLK cycles
Digital Multiplier	25°C	IV		9			9		SYSCLK cycles
DAC	25°C	IV		1			1		SYSCLK cycles
I/O Update Clock (Internal Mode)	25°C	IV		2			2		SYSCLK cycles
I/O Update Clock (External Mode)	25°C	IV		3			3		SYSCLK cycles
MASTER RESET DURATION	25°C	IV	10			10			SYSCLK cycles
COMPARATOR INPUT CHARACTERISTICS									
Input Capacitance	25°C	V		3			3		pF
Input Resistance	25°C	IV		500			500		kΩ
Input Current	25°C	I		±1	±5		±1	±5	µA
Hysteresis	25°C	IV		10	20		10	20	mV p-p
COMPARATOR OUTPUT CHARACTERISTICS									
Logic 1 Voltage, High-Z Load	Full	VI	3.1			3.1			V
Logic 0 Voltage, High-Z Load	Full	VI			0.16			0.16	V
Output Power, 50 Ω Load, 120 MHz Toggle Rate	25°C	I	9	11		9	11		dBm
Propagation Delay	25°C	IV		3			3		ns
Output Duty Cycle Error[7]	25°C	I	−10	±1	+10	−10	±1	+10	%
Rise/Fall Times, 5 pF Load	25°C	V		2			2		ns
Toggle Rate, High-Z Load	25°C	IV	300	350		300	350		MHz
Toggle Rate, 50 Ω Load	25°C	IV	375	400		375	400		MHz
Output Cycle-to-Cycle Jitter[8]		IV			4.0			4.0	ps rms
COMPARATOR NARROW-BAND SFDR[9]									
10 MHz (±1 MHz)	25°C	V		84			84		dBc
10 MHz (±250 MHz)	25°C	V		84			84		dBc
10 MHz (±50 MHz)	25°C	V		92			92		dBc
41 MHz (±1 MHz)	25°C	V		76			76		dBc
41 MHz (±250 MHz)	25°C	V		82			82		dBc
41 MHz (±50 MHz)	25°C	V		89			89		dBc
119 MHz (±1 MHz)	25°C	V		73					dBc
119 MHz (±250 MHz)	25°C	V		73					dBc
119 MHz (±50 MHz)	25°C	V		83					dBc
CLOCK GENERATOR OUTPUT JITTER[9]									
5 MHz A_{OUT}	25°C	V		23			23		ps rms
40 MHz A_{OUT}	25°C	V		12			12		ps rms
100 MHz A_{OUT}	25°C	V		7			7		ps rms

Parameter	Temp	Test Level	AD9854ASVZ Min	AD9854ASVZ Typ	AD9854ASVZ Max	AD9854ASTZ Min	AD9854ASTZ Typ	AD9854ASTZ Max	Unit
PARALLEL I/O TIMING CHARACTERISTICS									
t_{ASU} (Address Setup Time to $\overline{WR}$ Signal Active)	Full	IV	8.0	7.5		8.0	7.5		ns
t_{ADHW} (Address Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV	0			0			ns
t_{DSU} (Data Setup Time to $\overline{WR}$ Signal Inactive)	Full	IV	3.0	1.6		3.0	1.6		ns
t_{DHD} (Data Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV		0		0			ns
t_{WRLOW} ($\overline{WR}$ Signal Minimum Low Time)	Full	IV	2.5	1.8		2.5	1.8		ns
t_{WRHIGH} ($\overline{WR}$ Signal Minimum High Time)	Full	IV	7			7			ns
t_{WR} (Minimum $\overline{WR}$ Time)	Full	IV	10.5			10.5			ns
t_{ADV} (Address to Data Valid Time)	Full	V	15		15	15		15	ns
t_{ADHR} (Address Hold Time to $\overline{RD}$ Signal Inactive)	Full	IV	5			5			ns
t_{RDLOV} ($\overline{RD}$ Low to Output Valid)	Full	IV			15			15	ns
t_{RDHOZ} ($\overline{RD}$ High to Data Three-State)	Full	IV			10			10	ns
SERIAL I/O TIMING CHARACTERISTICS									
t_{PRE} ($\overline{CS}$ Setup Time)	Full	IV	30			30			ns
t_{SCLK} (Period of Serial Data Clock)	Full	IV	100			100			ns
t_{DSU} (Serial Data Setup Time)	Full	IV	30			30			ns
$t_{SCLKPWH}$ (Serial Data Clock Pulse Width High)	Full	IV	40			40			ns
$t_{SCLKPWL}$ (Serial Data Clock Pulse Width Low)	Full	IV	40			40			ns
t_{DHLD} (Serial Data Hold Time)	Full	IV	0			0			ns
t_{DV} (Data Valid Time)	Full	V		30			30		ns
CMOS LOGIC INPUTS[10]									
Logic 1 Voltage	25°C	I	2.2			2.2			V
Logic 0 Voltage	25°C	I			0.8			0.8	V
Logic 1 Current	25°C	IV			±5			±12	µA
Logic 0 Current	25°C	IV			±5			±12	µA
Input Capacitance	25°C	V		3			3		pF
POWER SUPPLY[11, 15]									
V_S Current[11, 12, 15]	25°C	I		1050	1210		755	865	mA
V_S Current[11, 13, 15]	25°C	I		710	816		515	585	mA
V_S Current[14]	25°C	I		600	685		435	495	mA
P_{DISS}[11, 12, 15]	25°C	I		3.475	4.190		2.490	3.000	W
P_{DISS}[11, 13, 15]	25°C	I		2.345	2.825		1.700	2.025	W
P_{DISS}[14]	25°C	I		1.975	2.375		1.435	1.715	W
P_{DISS} Power-Down Mode	25°C	I		1	50		1	50	mW

[1] The reference clock inputs are configured to accept a 1 V p-p (typical) dc offset square or sine wave centered at one-half the applied V_{DD} or a 3 V TTL-level pulse input.
[2] An internal 400 mV p-p differential voltage swing equates to 200 mV p-p applied to both REFCLK input pins.
[3] The I and Q gain imbalance is digitally adjustable to less than 0.01 dB.
[4] Pipeline delays of each individual block are fixed; however, if the first eight MSBs of a tuning word are 0s, the delay appears longer. This is due to insufficient phase accumulation per system clock period to produce enough LSB amplitude to the DAC.
[5] If a feature such as the inverse sinc, which has 16 pipeline delays, can be bypassed, the total delay is reduced by that amount.
[6] The I/O UD CLK transfers data from the I/O port buffers to the programming registers. This transfer is measured in system clocks.
[7] Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.
[8] Represents the comparator's inherent cycle-to-cycle jitter contribution. The input signal is a 1 V, 40 MHz square wave, and the measurement device is a Wavecrest DTS-2075.
[9] Comparator input originates from the analog output section via the external 7-pole elliptic low-pass filter. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.
[10] Avoid overdriving digital inputs. (Refer to the equivalent circuits in Figure 3.)
[11] If all device functions are enabled, it is not recommended to simultaneously operate the device at the maximum ambient temperature of 85°C and at the maximum internal clock frequency. This configuration may result in violating the maximum die junction temperature of 150°C. Refer to the Power Dissipation and Thermal Considerations section for derating and thermal management information.
[12] All functions engaged.
[13] All functions except inverse sinc engaged.
[14] All functions except inverse sinc and digital multipliers engaged.
[15] In most cases, disabling the inverse sinc filter reduces power consumption by approximately 30%.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
V_S	4 V
Digital Inputs	−0.7 V to +V_S
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Maximum Clock Frequency (ASVZ)	300 MHz
Maximum Clock Frequency (ASTZ)	200 MHz

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The heat sink of the AD9854ASVZ 80-lead TQFP package must be soldered to the PCB.

Table 3.

Thermal Characteristic	TQFP	LQFP
θ_{JA} (0 m/sec airflow)[1, 2, 3]	16.2°C/W	38°C/W
θ_{JMA} (1.0 m/sec airflow)[2, 3, 4, 5]	13.7°C/W	
θ_{JMA} (2.5 m/sec airflow)[2, 3, 4, 5]	12.8°C/W	
Ψ_{JT}[1, 2]	0.3°C/W	
θ_{JC}[6, 7]	2.0°C/W	

[1] Per JEDEC JESD51-2 (heat sink soldered to PCB).
[2] 2S2P JEDEC test board.
[3] Values of θ_{JA} are provided for package comparison and PCB design considerations.
[4] Per JEDEC JESD51-6 (heat sink soldered to PCB).
[5] Airflow increases heat dissipation, effectively reducing θ_{JA}. Furthermore, the more metal that is directly in contact with the package leads from metal traces through holes, ground, and power planes, the more θ_{JA} is reduced.
[6] Per MIL-Std 883, Method 1012.1.
[7] Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

To determine the junction temperature on the application PCB use the following equation:

$$T_J = T_{case} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature expressed in degrees Celsius.
T_{case} is the case temperature expressed in degrees Celsius, as measured by the user at the top center of the package.
Ψ_{JT} = 0.3°C/W.
PD is the power dissipation (PD); see the Power Dissipation and Thermal Considerations section for the method to calculate PD.

EXPLANATION OF TEST LEVELS

Table 3.

Test Level	Description
I	100% production tested.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

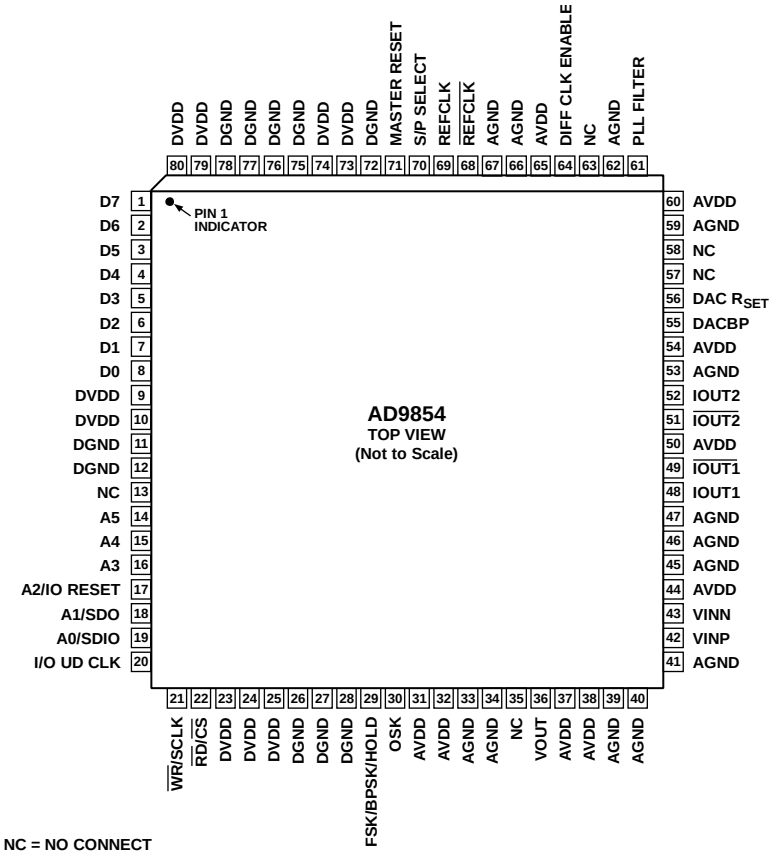


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 8	D7 to D0	8-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode.
9, 10, 23, 24, 25, 73, 74, 79, 80	DVDD	Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
11, 12, 26, 27, 28, 72, 75 to 78	DGND	Connections for the Digital Circuitry Ground Return. Same potential as AGND.
13, 35, 57, 58, 63	NC	No Internal Connection.
14 to 16	A5 to A3	Parallel Address Inputs for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0). Used only in parallel programming mode.
17	A2/IO RESET	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/IO Reset. A2 is used only in parallel programming mode. IO RESET is used when the serial programming mode is selected, allowing an IO RESET of the serial communication bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming, nor does it invoke the default programming values listed in Table 8. Active high.
18	A1/SDO	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/Unidirectional Serial Data Output. A1 is used only in parallel programming mode. SDO is used in 3-wire serial communication mode when the serial programming mode is selected.
19	A0/SDIO	Parallel Address Input for Program Registers (Part of 6-Bit Parallel Address Inputs for Program Register, A5:A0)/Bidirectional Serial Data I/O. A0 is used only in parallel programming mode. SDIO is used in 2-wire serial communication mode.

Pin No.	Mnemonic	Description
20	I/O UD CLK	Bidirectional I/O Update Clock. Direction is selected in control register. If this pin is selected as an input, a rising edge transfers the contents of the I/O port buffers to the programming registers. If I/O UD CLK is selected as an output (default), an output pulse (low to high) with a duration of eight system clock cycles indicates that an internal frequency update has occurred.
21	$\overline{WR}$/SCLK	Write Parallel Data to I/O Port Buffers. Shared function with SCLK. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with $\overline{WR}$ when the parallel mode is selected. The mode is dependent on Pin 70 (S/P SELECT).
22	$\overline{RD}$/$\overline{CS}$	Read Parallel Data from Programming Registers. Shared function with $\overline{CS}$. Chip-select signal associated with the serial programming bus. Active low. This pin is shared with $\overline{RD}$ when the parallel mode is selected.
29	FSK/BPSK/HOLD	Multifunction pin according to the mode of operation selected in the programming control register. In FSK mode, logic low selects F1 and logic high selects F2. In BPSK mode, logic low selects Phase 1 and logic high selects Phase 2. In chirp mode, logic high engages the hold function, causing the frequency accumulator to halt at its current location. To resume or commence chirp mode, logic low is asserted.
30	OSK	Output Shaped Keying. Must first be selected in the programming control register to function. A logic high causes the I and Q DAC outputs to ramp up from zero-scale to full-scale amplitude at a preprogrammed rate. Logic low causes the full-scale output to ramp down to zero scale at the preprogrammed rate.
31, 32, 37, 38, 44, 50, 54, 60, 65	AVDD	Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67	AGND	Connections for Analog Circuitry Ground Return. Same potential as DGND.
36	VOUT	Noninverted Output of the Internal High Speed Comparator. Designed to drive 10 dBm to 50 Ω load as well as standard CMOS logic levels.
42	VINP	Voltage Input Positive. The noninverting input of the internal high speed comparator.
43	VINN	Voltage Input Negative. The inverting input of the internal high speed comparator.
48	IOUT1	Unipolar Current Output of I, or the Cosine DAC. (Refer to Figure 3.)
49	$\overline{IOUT1}$	Complementary Unipolar Current Output of I, or the Cosine DAC.
51	$\overline{IOUT2}$	Complementary Unipolar Current Output of Q, or the Sine DAC.
52	IOUT2	Unipolar Current Output of Q, or the Sine DAC. This DAC can be programmed to accept external 12-bit data in lieu of internal sine data, allowing the AD9854 to emulate the AD9852 control DAC function.
55	DACBP	Common Bypass Capacitor Connection for Both I and Q DACs. A 0.01 µF chip capacitor from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible, but results in a slight degradation in SFDR.
56	DAC R_{SET}	Common Connection for Both I and Q DACs. Used to set the full-scale output current. $R_{SET} = 39.9/I_{OUT}$. Normal R_{SET} range is from 8 kΩ (5 mA) to 2 kΩ (20 mA).
61	PLL FILTER	Connection for the External Zero-Compensation Network of the REFCLK Multiplier's PLL Loop Filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected to AVDD as close as possible to Pin 60. For optimum phase noise performance, the REFCLK multiplier can be bypassed by setting the bypass PLL bit in Control Register 1E hex.
64	DIFF CLK ENABLE	Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK and $\overline{REFCLK}$ (Pin 69 and Pin 68, respectively).
68	$\overline{REFCLK}$	Complementary (180° Out of Phase) Differential Clock Signal. User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REFCLK.
69	REFCLK	Single-Ended Reference Clock Input (CMOS Logic Levels Required) or One of Two Differential Clock Signals. In differential reference clock mode, both inputs can be CMOS logic levels or have greater than 400 mV p-p square or sine waves centered about 1.6 V dc.
70	S/P SELECT	Selects serial programming mode (logic low) or parallel programming mode (logic high).
71	MASTER RESET	Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a do-nothing state defined by the default values listed in Table 8. Active on logic high. Asserting this pin is essential for proper operation upon power-up.

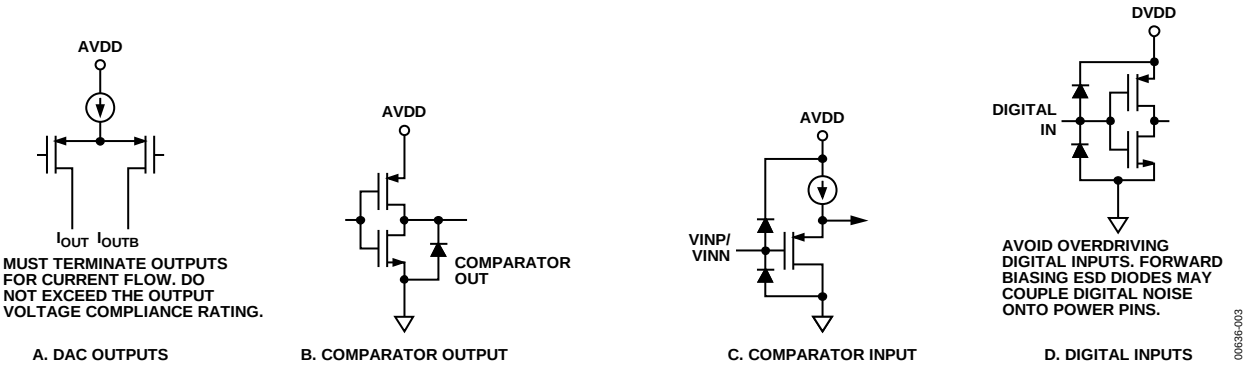


Figure 3. Equivalent Input and Output Circuits

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4 to Figure 9 indicate the wideband harmonic distortion performance of the AD9854 from 19.1 MHz to 119.1 MHz fundamental output, reference clock = 30 MHz, REFCLK multiplier = 10×. Each graph is plotted from 0 MHz to 150 MHz (Nyquist).

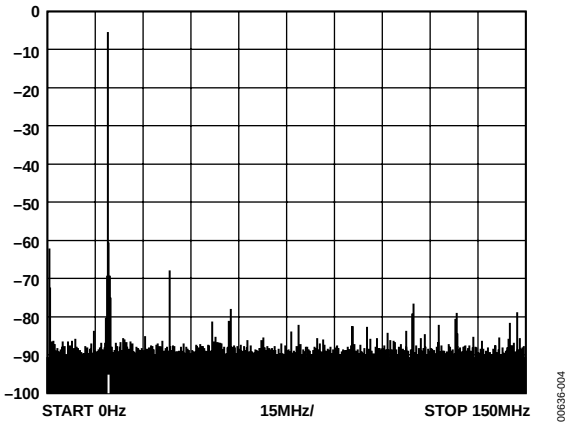


Figure 4. Wideband SFDR, 19.1 MHz

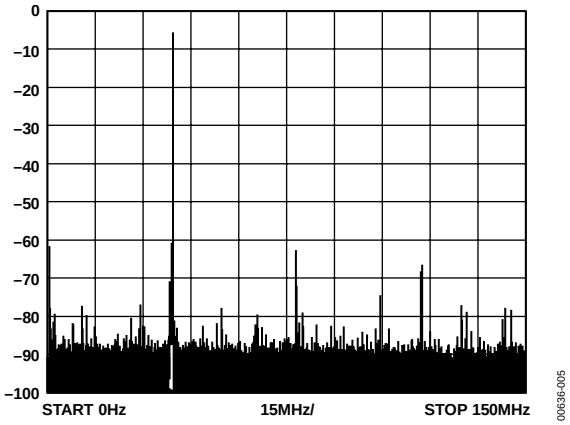


Figure 5. Wideband SFDR, 39.1 MHz

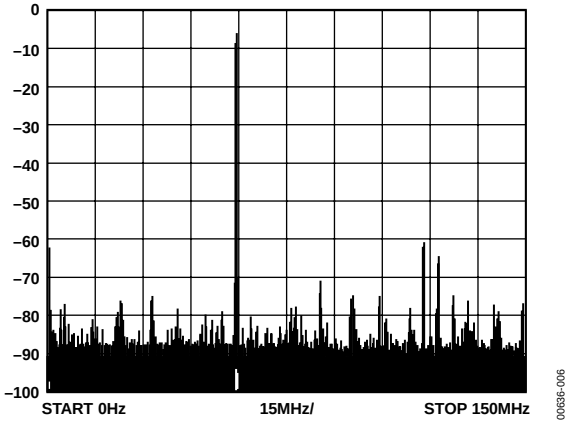


Figure 6. Wideband SFDR, 59.1 MHz

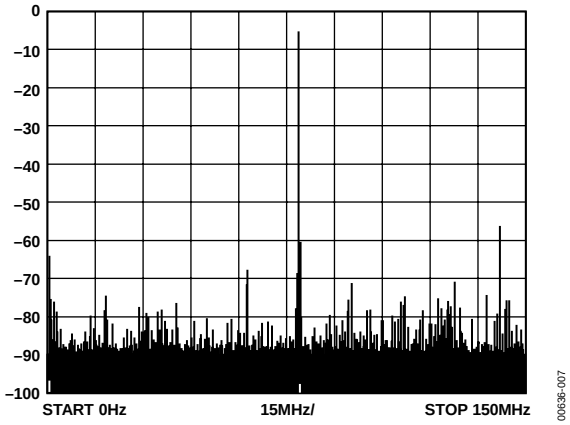


Figure 7. Wideband SFDR, 79.1 MHz

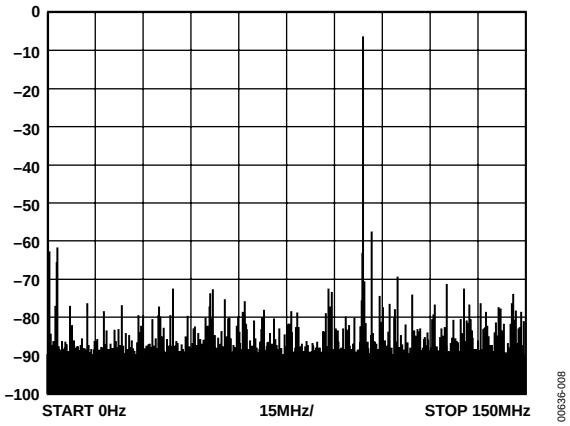


Figure 8. Wideband SFDR, 99.1 MHz

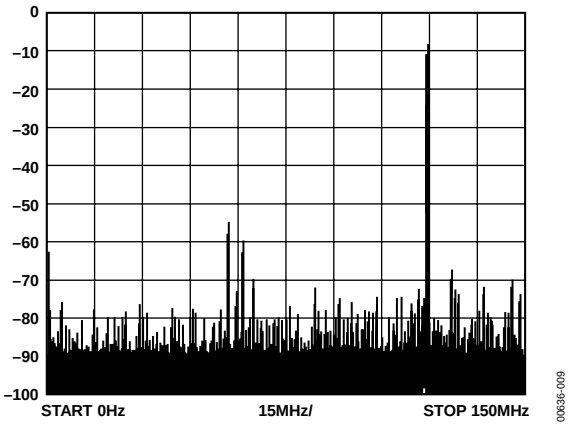


Figure 9. Wideband SFDR, 119.1 MHz

Figure 10 to Figure 15 show the trade-off in elevated noise floor, increased phase noise (PN), and discrete spurious energy when the internal REFCLK multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown. Compare the noise floor of Figure 11 and Figure 12 with that of Figure 14 and Figure 15. The improvement seen in Figure 11 and Figure 12 is a direct result of sampling the fundamental at a higher rate. Sampling at a higher rate spreads the quantization noise of the DAC over a wider bandwidth, which effectively lowers the noise floor.

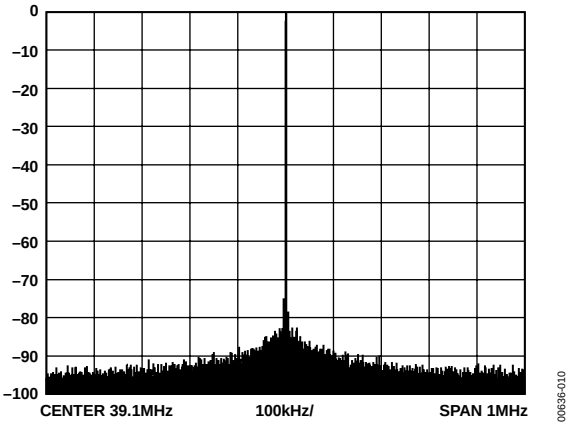


Figure 10. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed

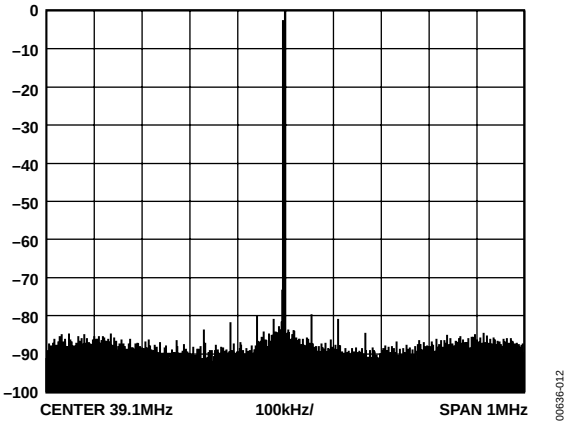


Figure 13. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×

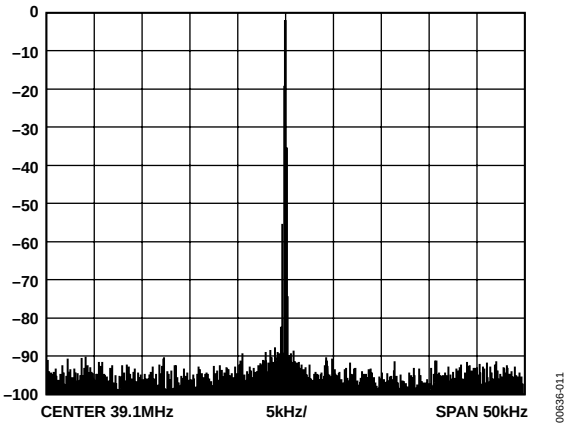


Figure 11. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 300 MHz REFCLK with REFCLK Multiplier Bypassed

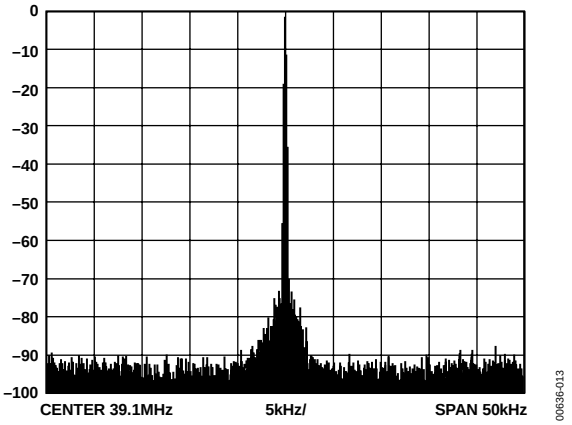


Figure 14. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 30 MHz REFCLK with REFCLK Multiplier = 10×

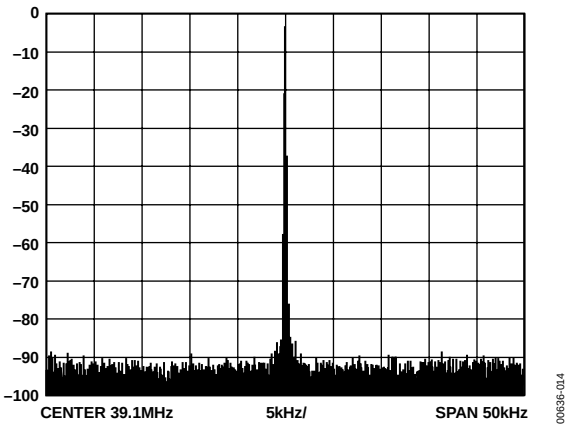


Figure 12. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 100 MHz REFCLK with REFCLK Multiplier Bypassed

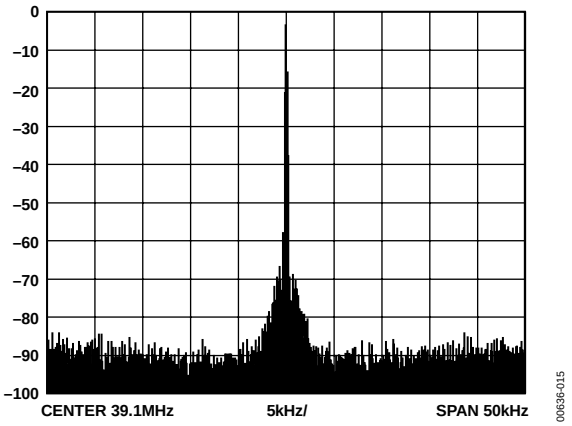


Figure 15. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 10 MHz REFCLK with REFCLK Multiplier = 10×

Figure 16 and Figure 17 show the narrow-band performance of the AD9854 when operating with a 200 MHz reference clock with the REFCLK multiplier bypassed vs. a 20 MHz reference clock and the REFCLK multiplier enabled at 10×.

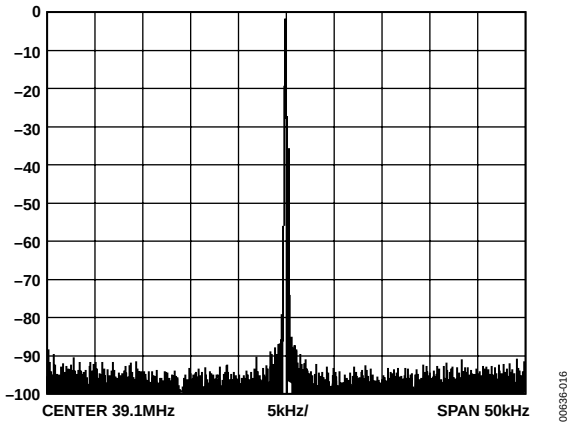


Figure 16. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 200 MHz REFCLK with REFCLK Multiplier Bypassed

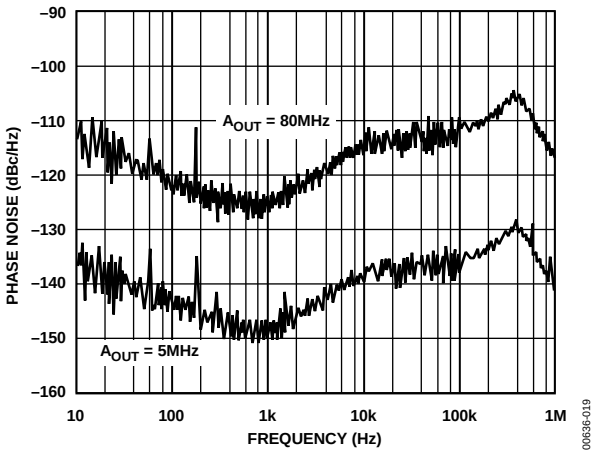


Figure 19. Residual Phase Noise, 30 MHz REFCLK with REFCLK Multiplier = 10×

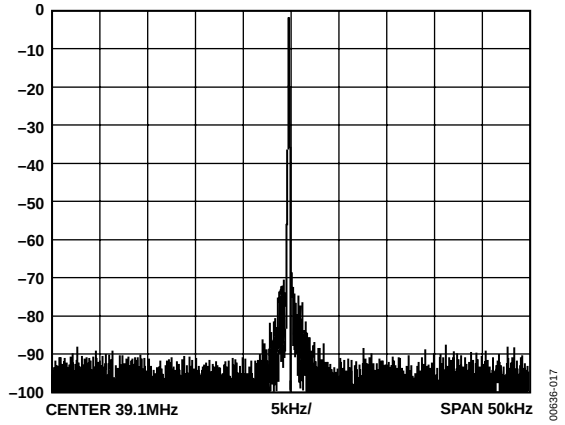


Figure 17. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 20 MHz REFCLK with REFCLK Multiplier = 10×

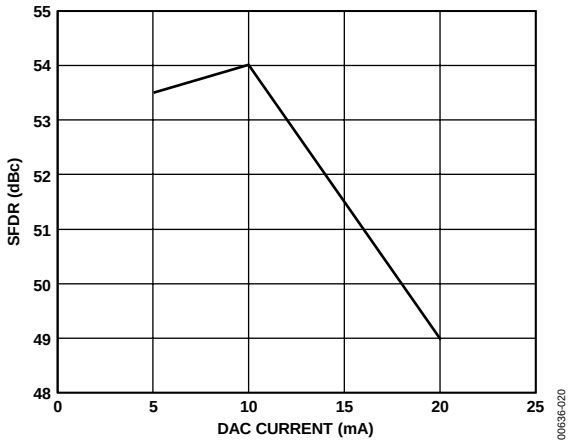


Figure 20. SFDR vs. DAC Current, 59.1 A_{OUT}, 300 MHz REFCLK with REFCLK Multiplier Bypassed

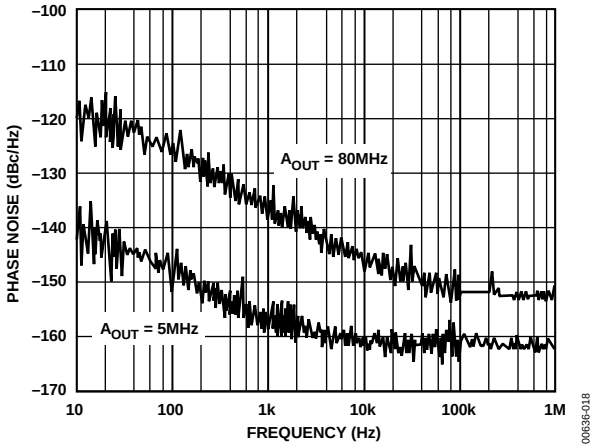


Figure 18. Residual Phase Noise, 300 MHz REFCLK with REFCLK Multiplier Bypassed

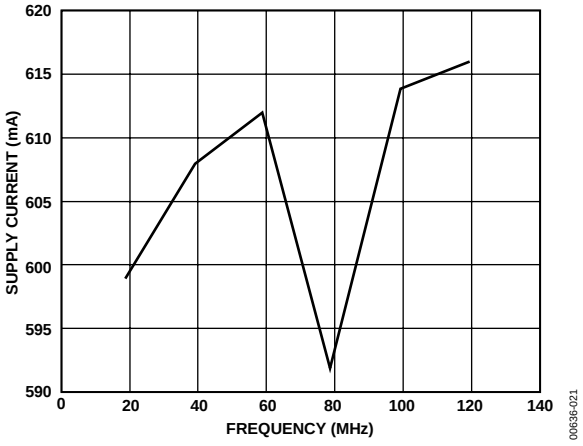


Figure 21. Supply Current vs. Output Frequency (Variation Is Minimal, Expressed as a Percentage, and Heavily Dependent on Tuning Word)

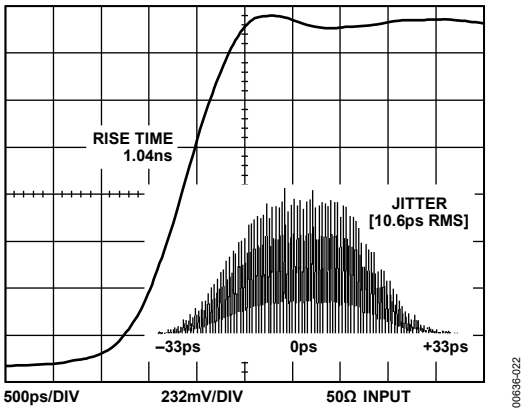


Figure 22. Typical Comparator Output Jitter, 40 MHz A_{OUT}, 300 MHz RFCLK with REFCLK Multiplier Bypassed

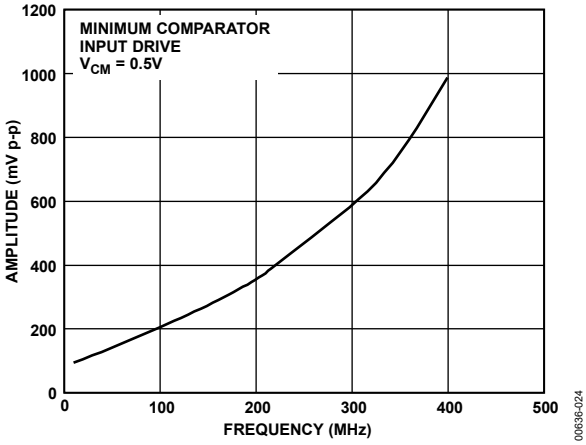


Figure 24. Comparator Toggle Voltage Requirement

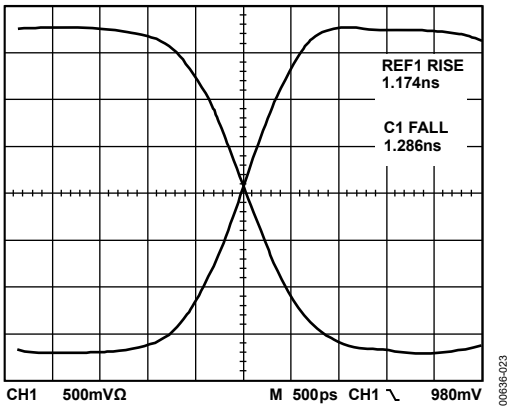


Figure 23. Comparator Rise/Fall Times

TYPICAL APPLICATIONS

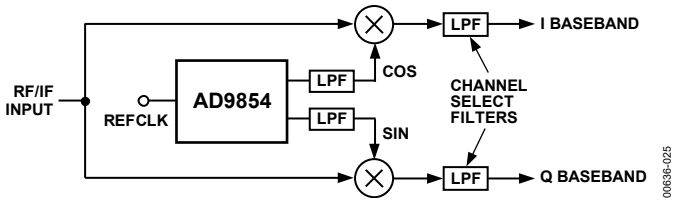


Figure 25. Quadrature Downconversion

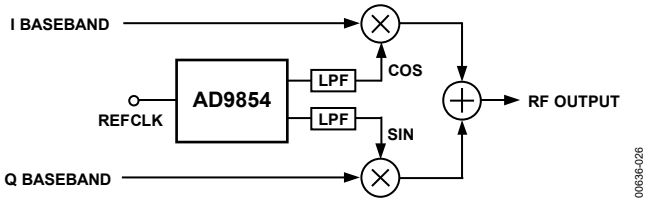


Figure 26. Direct Conversion Quadrature Upconverter

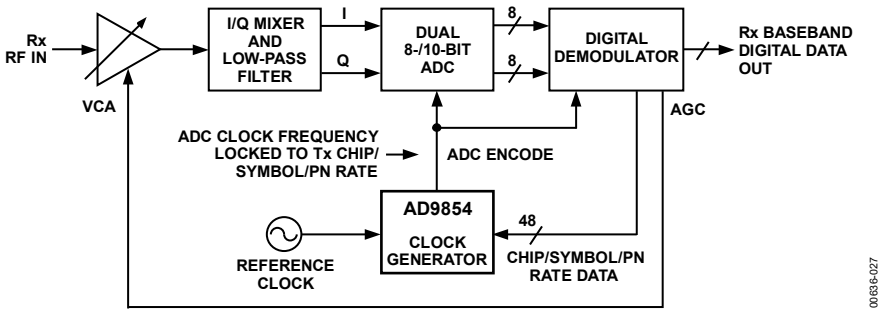


Figure 27. Chip Rate Generator in Spread Spectrum Application

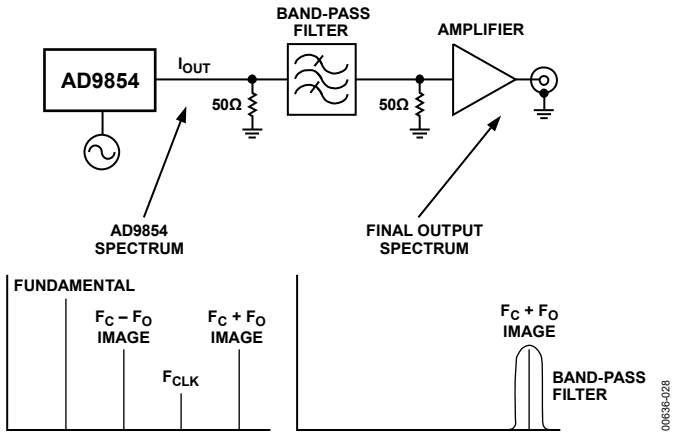


Figure 28. Using an Aliased Image to Generate a High Frequency

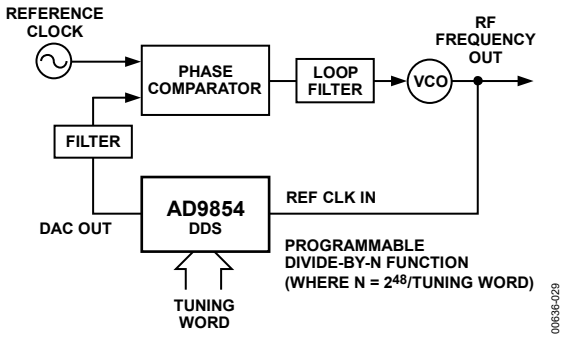


Figure 29. Programmable Fractional Divide-by-N Synthesizer

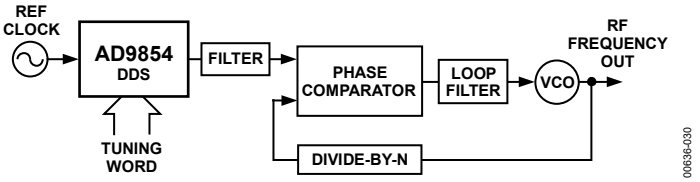


Figure 30. Agile High Frequency Synthesizer

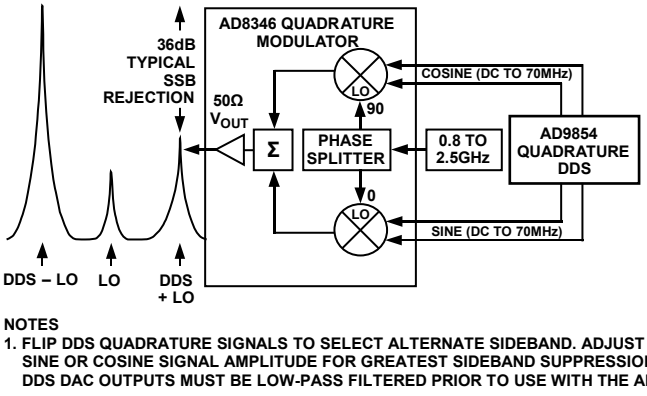


Figure 31. Single Sideband Upconversion

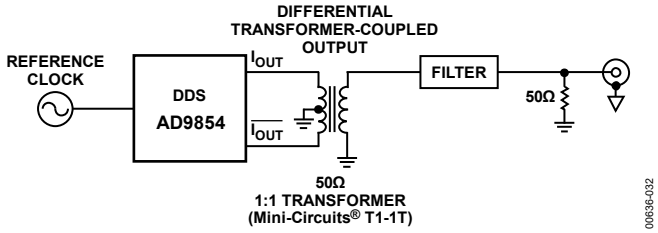


Figure 32. Differential Output Connection for Reduction of Common-Mode Signals

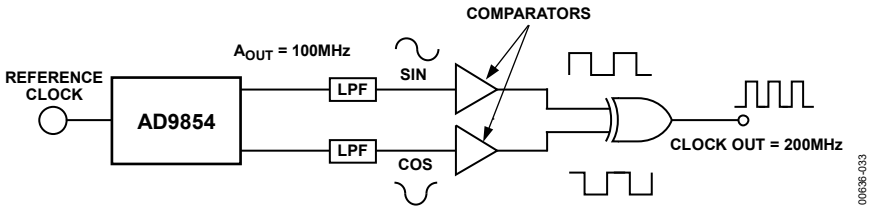


Figure 33. Clock Frequency Doubler

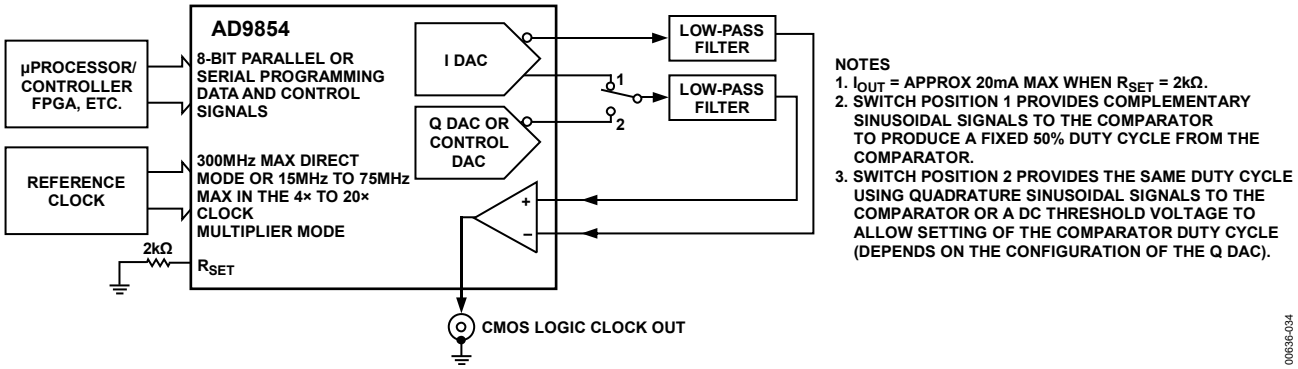


Figure 34. Frequency Agile Clock Generator Applications for the AD9854

THEORY OF OPERATION

The AD9854 quadrature output digital synthesizer is a highly flexible device that addresses a wide range of applications. The device consists of an NCO with a 48-bit phase accumulator, a programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, a high speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, an agile clock generator, or an FSK/BPSK modulator.

Analog Devices, Inc., provides a technical tutorial about the operational theory of the functional blocks of the device. The tutorial includes a technical description of the signal flow through a DDS device and provides basic applications information for a variety of digital synthesis implementations. The document, *A Technical Tutorial on Digital Signal Synthesis,* is available from the DDS Technical Library, on the Analog Devices DDS website at www.analog.com/dds.

MODES OF OPERATION

The AD9854 has five programmable operational modes. To select a mode, three bits in the control register (parallel Address 1F hex) must be programmed, as described in Table 5.

Table 5. Mode Selection Table

Mode 2	Mode 1	Mode 0	Result
0	0	0	Single tone
0	0	1	FSK
0	1	0	Ramped FSK
0	1	1	Chirp
1	0	0	BPSK

In each mode, some functions may be prohibited. Table 6 lists the functions and their availability for each mode.

Single Tone (Mode 000)

This is the default mode when the MASTER RESET pin is asserted. It can also be accessed if the user programs this mode into the control register. The phase accumulator, responsible for generating an output frequency, is presented with a 48-bit value from the Frequency Tuning Word 1 registers that have default values of 0. Default values from the remaining applicable registers further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hz and zero phase. At power-up and reset, the output from the I and Q DACs is a dc value equal to the midscale output current. This is the default mode amplitude setting of 0. See the On/Off Output Shaped Keying (OSK) section for more details about the output amplitude control. All or some of the 28 program registers must be programmed to produce a user-defined output signal.

Figure 35 shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

Table 6. Functions Available for Modes

	Mode				
Function	**Single Tone**	**FSK**	**Ramped FSK**	**Chirp**	**BPSK**
Phase Adjust 1	•	•	•	•	•
Phase Adjust 2					•
Single-Pin FSK/BPSK or HOLD		•	•	•	•
Single-Pin Shaped Keying	•	•	•	•	•
Phase Offset or Modulation	•	•	•	•	
Amplitude Control or Modulation	•	•	•	•	•
Inverse Sinc Filter	•	•	•	•	•
Frequency Tuning Word 1	•	•	•	•	•
Frequency Tuning Word 2		•	•		
Automatic Frequency Sweep			•	•	

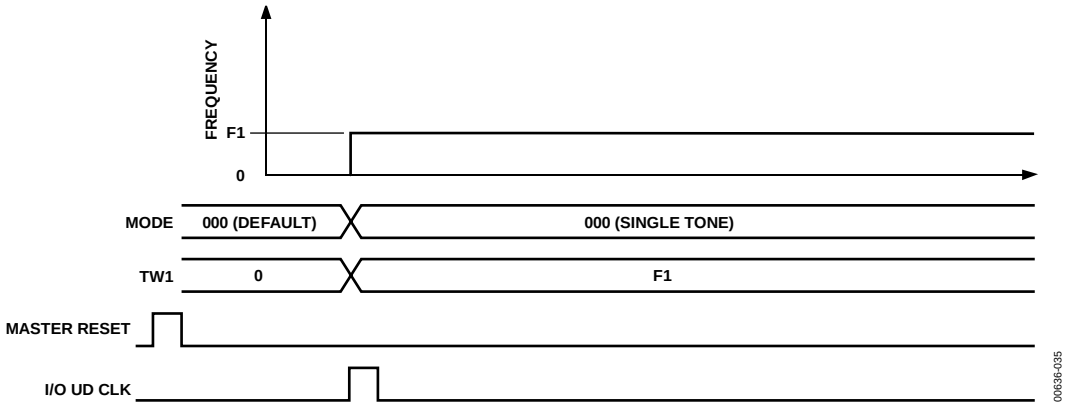


Figure 35. Default State to User-Defined Output Transition

As with all Analog Devices DDS devices, the value of the frequency tuning word is determined by

$$FTW = (Desired\ Output\ Frequency \times 2^N)/SYSCLK$$

where:
N is the phase accumulator resolution (48 bits in this instance).
Desired Output Frequency is expressed in hertz.
FTW (frequency tuning word) is a decimal number.

After a decimal number has been calculated, it must be rounded to an integer and then converted to binary format, that is, a series of 48 binary-weighted 1s and 0s. The fundamental sine wave DAC output frequency range is from dc to one-half SYSCLK.

Changes in frequency are phase continuous, meaning that the first sampled phase value of the new frequency is referenced from the time of the last sampled phase value of the previous frequency.

The I and Q DACs of the AD9854 are always 90° out of phase. The 14-bit phase registers do not independently adjust the phase of each DAC output. Instead, both DACs are affected equally by a change in phase offset.

The single-tone mode allows the user to control the following signal qualities:

- Output frequency to 48-bit accuracy
- Output amplitude to 12-bit accuracy
  - Fixed, user-defined amplitude control
  - Variable, programmable amplitude control
  - Automatic, programmable, single-pin-controlled on/off output shaped keying
- Output phase to 14-bit accuracy

These qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel byte rate or at a 10 MHz serial rate. Incorporating this attribute permits FM, AM, PM, FSK, PSK, and ASK operation in single-tone mode.

Unramped FSK (Mode 001)

When the unramped FSK mode is selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word Register 1 and Frequency Tuning Word Register 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (Frequency Tuning Word 1, Parallel Address 4 hex to Parallel Address 9 hex), and a logic high chooses F2 (Frequency Tuning Word 2, Parallel Register Address A hex to Parallel Register Address F hex). Changes in frequency are phase continuous and are internally coincident with the FSK data pin (Pin 29); however, there is deterministic pipeline delay between the FSK data signal and the DAC output. (Refer to the pipeline delays in Table 1.)

The unramped FSK mode, shown in Figure 36, represents traditional FSK, radio teletype (RTTY), or teletype (TTY) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF spectrum. Ramped FSK, shown in Figure 37, is a method of conserving bandwidth.

Ramped FSK (Mode 010)

This mode is a method of FSK whereby changes from F1 to F2 are not instantaneous, but are accomplished in a frequency sweep or ramped fashion (the ramped notation implies that the sweep is linear). Although linear sweeping, or frequency ramping, is easily and automatically accomplished, it is only one of many schemes. Other frequency transition schemes can be implemented by changing the ramp rate and ramp step size on the fly in a piecewise fashion.

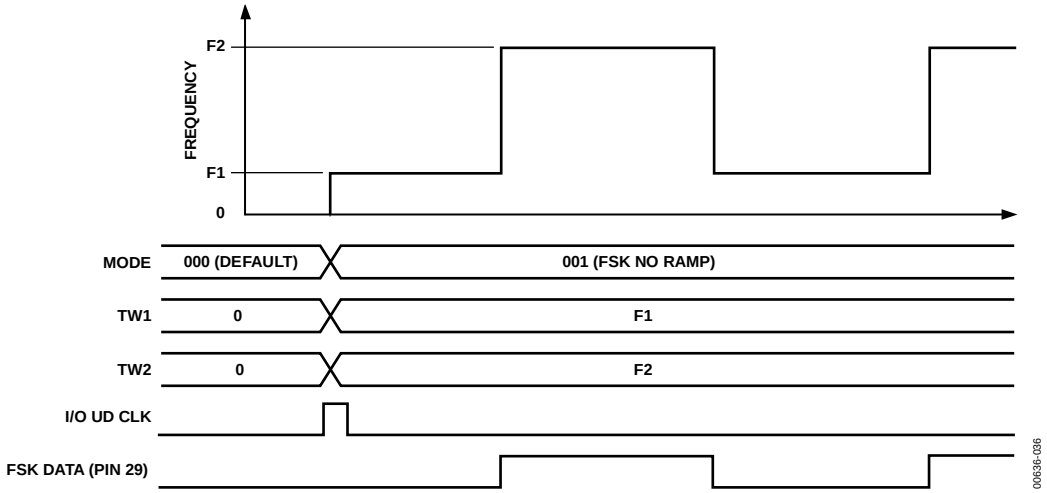


Figure 36. Unramped (Traditional) FSK Mode

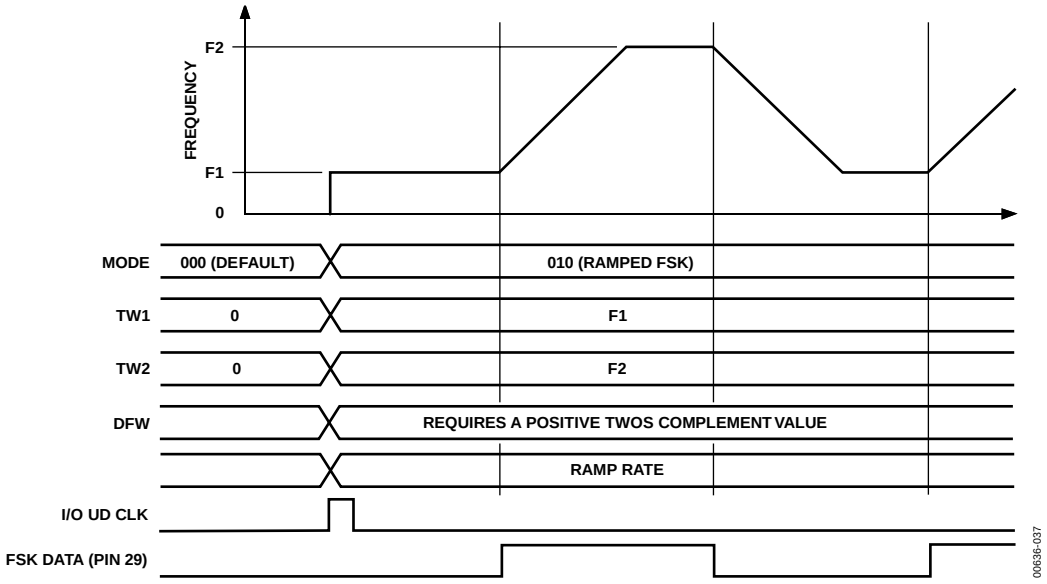


Figure 37. Ramped FSK Mode (Start at F1)

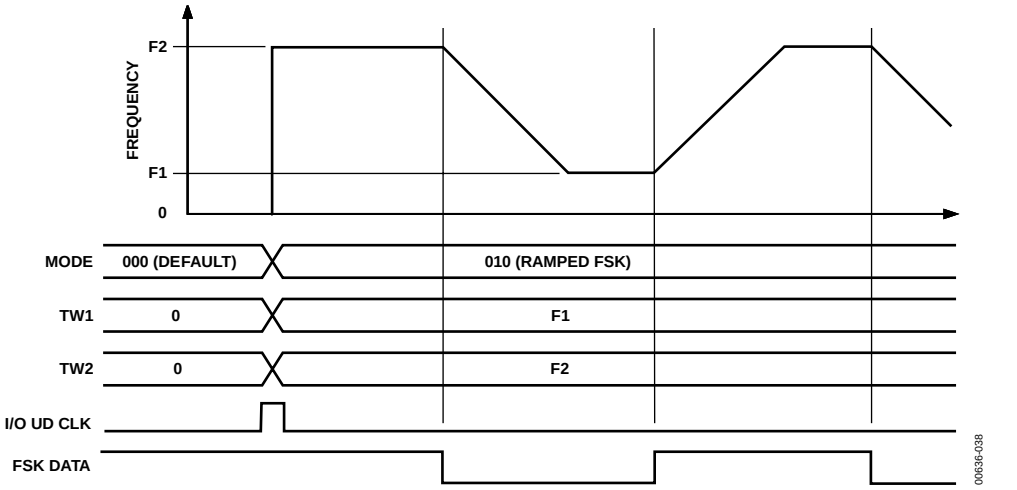


Figure 38. Ramped FSK Mode (Start at F2)

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 are output in addition to the primary F1 and F2 frequencies. Figure 37 and Figure 38 depict the frequency vs. time characteristics of a linear ramped FSK signal.

Note that in ramped FSK mode, the delta frequency word (DFW) is required to be programmed as a positive twos complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies, and the time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency to be loaded into F2 registers.

Several registers must be programmed to instruct the DDS on the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to ensure that the frequency accumulator is starting from an all 0s output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in progress to affect the desired response.

Parallel Register Address 1A hex to Parallel Register Address 1C hex comprise the 20-bit ramp rate clock registers. This is a countdown counter that outputs a single pulse whenever the count reaches 0. The counter is activated when a logic level change occurs on the FSK input, Pin 29. This counter is run at the system clock rate, 300 MHz maximum. The time period between each output pulse is given as

$$(N + 1) \times \textit{System Clock Period}$$

where N is the 20-bit ramp rate clock value programmed by the user.

The allowable range of N is from 1 to $(2^{20} - 1)$. The output of this counter clocks the 48-bit frequency accumulator shown in Figure 39. The ramp rate clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The dwell time spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

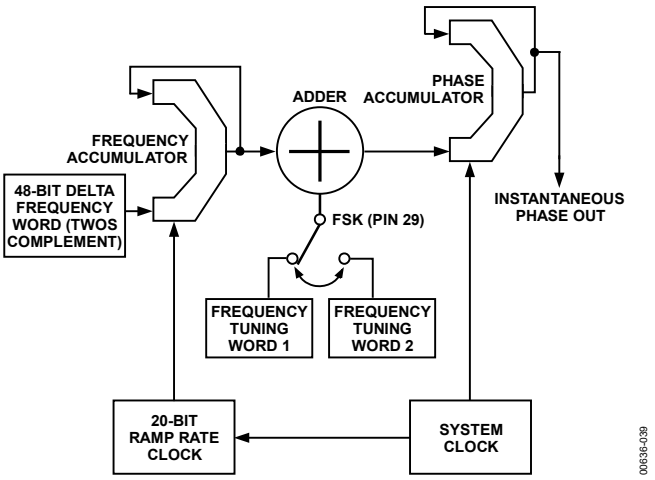


Figure 39. Block Diagram of Ramped FSK Function

Parallel Register Address 10 hex to Parallel Register Address 15 hex comprise the 48-bit, twos complement, delta frequency word registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is added to or subtracted from the F1 or F2 frequency word, which is then fed into the input of the 48-bit phase accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency according to the logic state of Pin 29. This ramping rate is a function of the 20-bit ramp rate clock. When the destination frequency is achieved, the ramp rate clock is stopped, halting the frequency accumulation process.

Generally speaking, the delta frequency word is a much smaller value compared with the value of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the delta frequency word might be only 25 Hz.

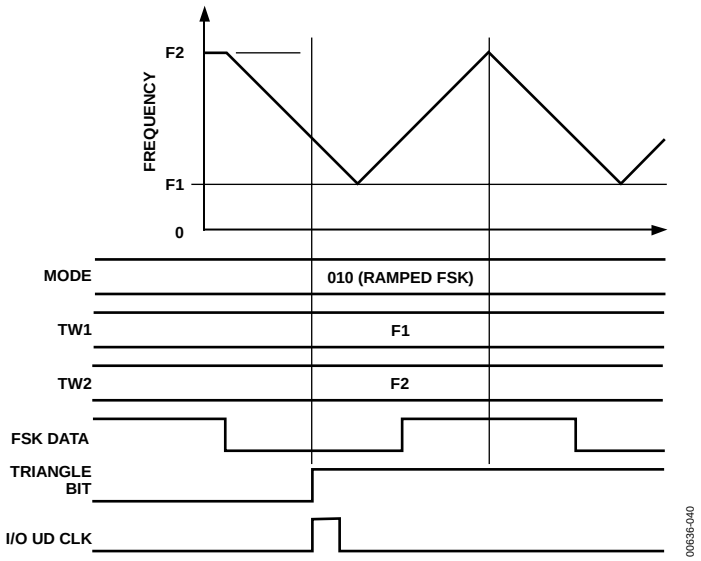


Figure 40. Effect of Triangle Bit in Ramped FSK Mode

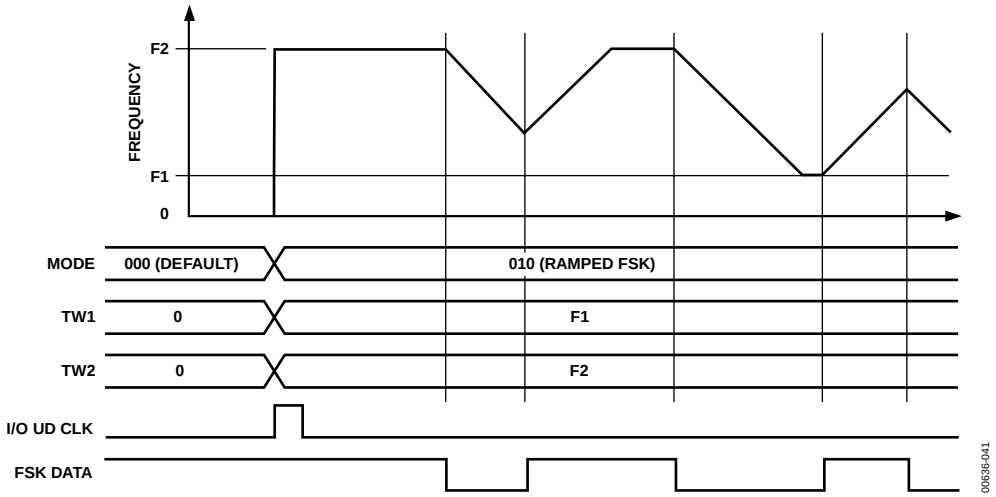


Figure 41. Effect of Premature Ramped FSK Data

Figure 41 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution until the original frequency is reached.

The control register contains a triangle bit at Parallel Register Address 1F hex. Setting this bit high in Mode 010 causes an automatic ramp-up and ramp-down between F1 and F2 to occur without toggling Pin 29, as shown in Figure 40. The logic state of Pin 29 has no effect once the triangle bit is set high. This function uses the ramp rate clock time period and the step size of the delta frequency word to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Use this function to automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode with the triangle bit set high, an automatic frequency sweep begins at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs (Figure 42). If the FSK data bit is high instead of low, F2, rather than F1, is chosen as the start frequency.

Additional flexibility in the ramped FSK mode is provided by the AD9854's ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp rate counter at any time during the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps with different slopes in a piecewise fashion. This is done by programming and executing a linear ramp at a rate or slope and then altering the slope (by changing the ramp rate clock or delta frequency word, or both). Changes in slope can be made as often as needed before the destination frequency has been reached to form the desired nonlinear frequency sweep response. These piecewise changes can be precisely timed using

the 32-bit internal update clock (see the Internal and External Update Clock section).

Nonlinear ramped FSK has the appearance of the chirp function shown in Figure 43. The difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2, whereas chirp operation has no F2 limit frequency.

Two additional control bits (CLR ACC1 and CLR ACC2) are available in the ramped FSK mode that allow more options. If CLR ACC1 (Register Address 1F hex) is set high, it clears the 48-bit frequency accumulator (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1 bit is left high, a one-shot pulse is delivered on the rising edge of every update clock. The effect is to interrupt the current ramp, reset the frequency to the start point (F1 or F2), and then continue to ramp up (or down) at the previous rate. This occurs even when a static F1 or F2 destination frequency has been achieved.

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

Chirp (Mode 011)

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern, but the AD9854 can also support nonlinear patterns. In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the result that a single-frequency radar system would produce. Figure 43 shows a very low resolution nonlinear chirp, demonstrating the different slopes that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

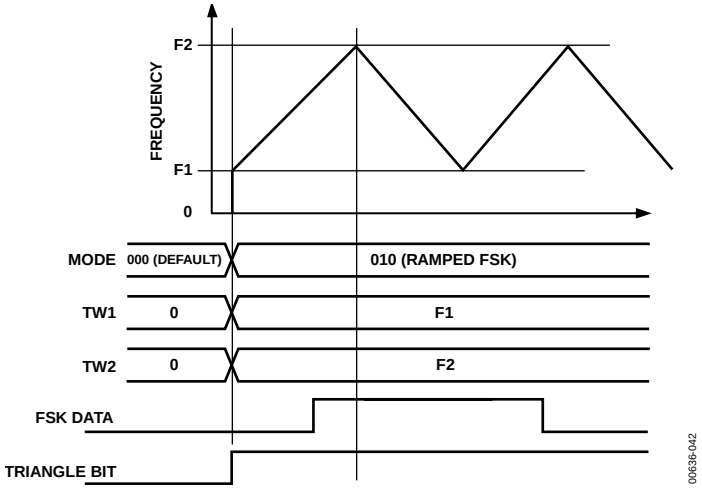


Figure 42. Automatic Linear Ramping Using the Triangle Bit

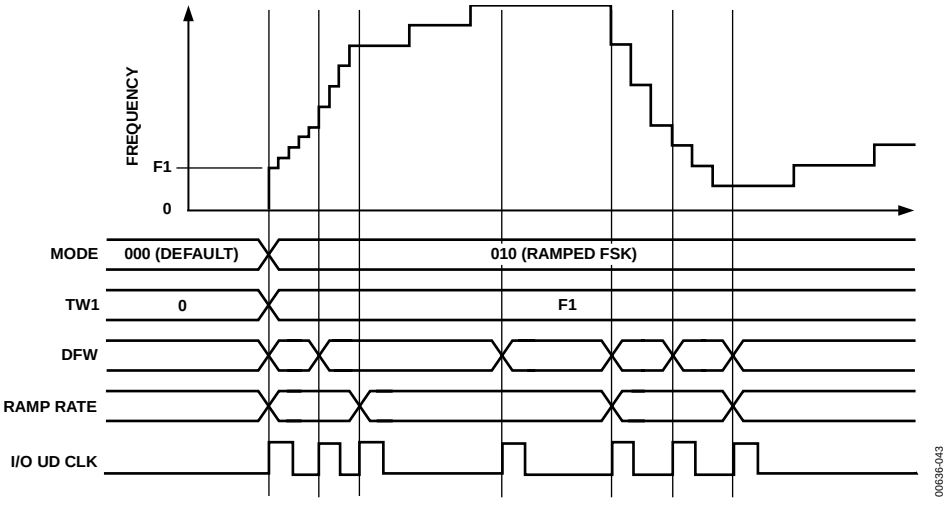


Figure 43. Example of a Nonlinear Chirp

The AD9854 permits precise, internally generated linear, or externally programmed nonlinear, pulsed or continuous FM over the complete frequency range, duration, frequency resolution, and sweep direction(s). All of these are user programmable. Figure 44 shows a block diagram of the FM chirp components.

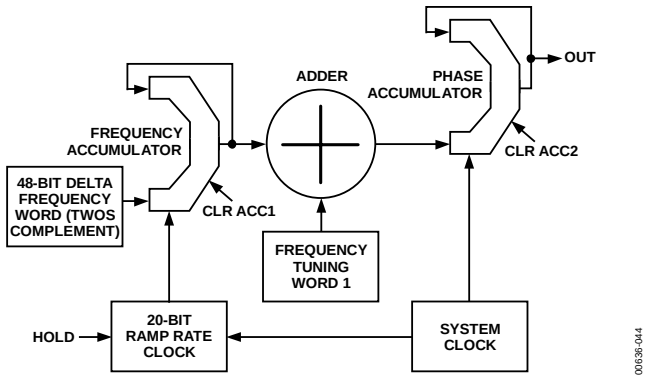


Figure 44. FM Chirp Components

Basic FM Chirp Programming Steps

1. Program a start frequency into Frequency Tuning Word 1 (FTW1) at Parallel Register Address 4 hex to Parallel Register Address 9 hex.
2. Program the frequency step resolution into the 48-bit, twos complement delta frequency word (Parallel Register Address 10 hex to Parallel Register Address 15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit ramp rate clock (Parallel Register Address 1A hex to Parallel Register Address 1C hex).

When programming is complete, an I/O update pulse at Pin 20 engages the program commands.

The necessity for a twos complement delta frequency word is to define the direction in which the FM chirp moves. If the 48-bit delta frequency word is negative (MSB is high), the incremental frequency changes are in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), the incremental frequency changes are in a positive direction from FTW1.

It is important to note that FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp begins, it is free to move (under program control) within the Nyquist bandwidth (dc to one-half the system clock). However, instant return to FTW1 can be easily achieved.

Two control bits (CLR ACC1 and CLR ACC2) are available in the FM chirp mode that allow the return to the beginning frequency, FTW1, or to 0 Hz. When the CLR ACC1 bit (Register Address 1F hex) is set high, the 48-bit frequency accumulator (ACC1) output is cleared with a retriggerable one-shot pulse of one system clock duration. The 48-bit delta frequency word input to the accumulator is unaffected by the CLR ACC1 bit. If the CLR ACC1 bit is held high, a one-shot pulse is delivered to the frequency accumulator (ACC1) on every rising edge of the I/O update clock. The effect is to interrupt the current chirp, reset the frequency to that programmed into FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the output of the frequency accumulator in the chirp mode is illustrated in Figure 45. Shown in the diagram is the I/O update clock, which is either user supplied or internally generated.

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to the previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

Figure 46 illustrates the effect of the CLR ACC2 bit on the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function that is available only in chirp mode is the HOLD pin (Pin 29). This function stops the clock signal to the ramp rate counter, halting any further clocking pulses to the frequency accumulator, ACC1. The effect is to halt the chirp at the frequency existing just before the HOLD pin is pulled high. When Pin 29 is returned low, the clock and chirp resumes. During a hold condition, the user can change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of 0 is obtained before a new ramp rate count can be loaded. Figure 47 shows the effect of the hold function on the DDS output frequency.

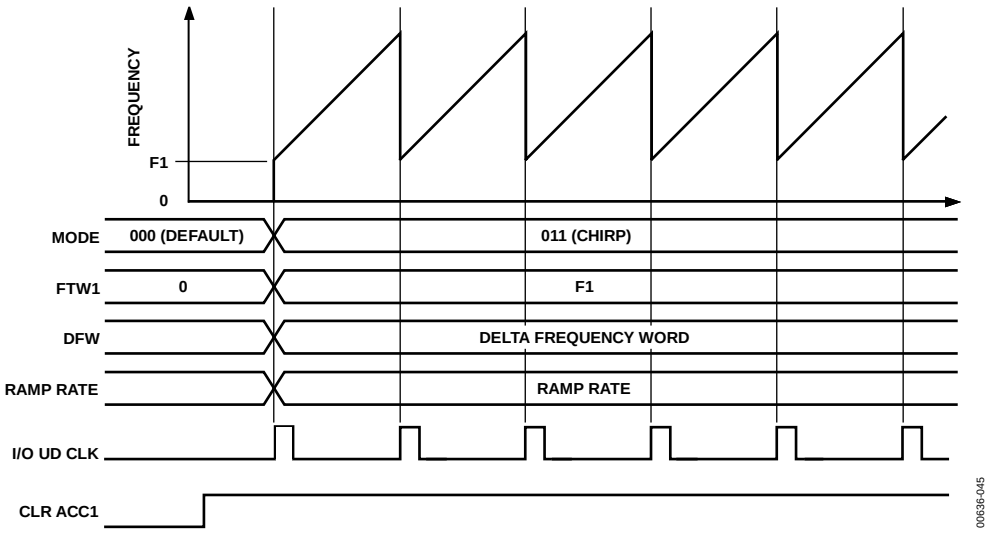


Figure 45. Effect of CLR ACC1 in FM Chirp Mode

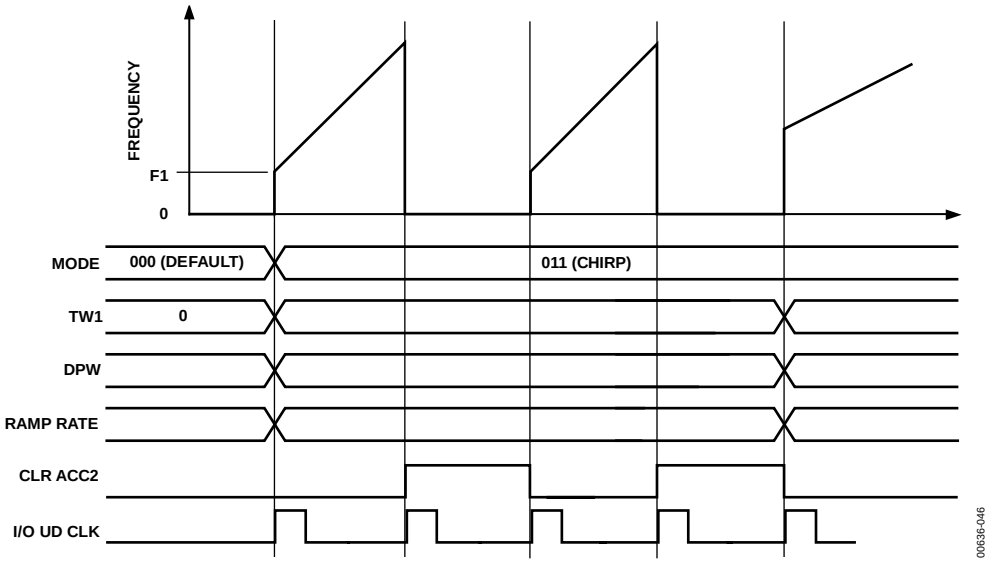


Figure 46. Effect of CLR ACC2 in Chirp Mode

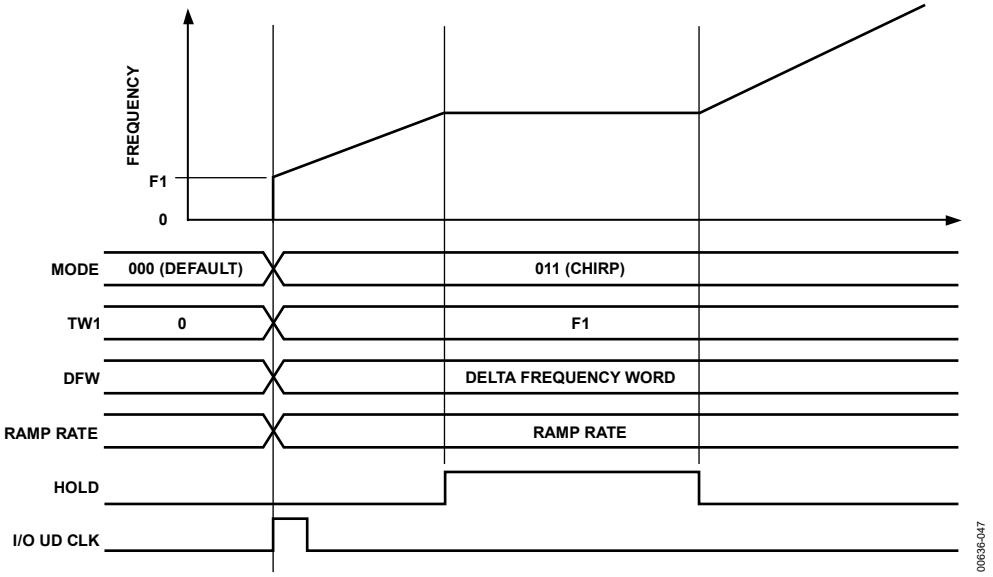


Figure 47. Example of Hold Function

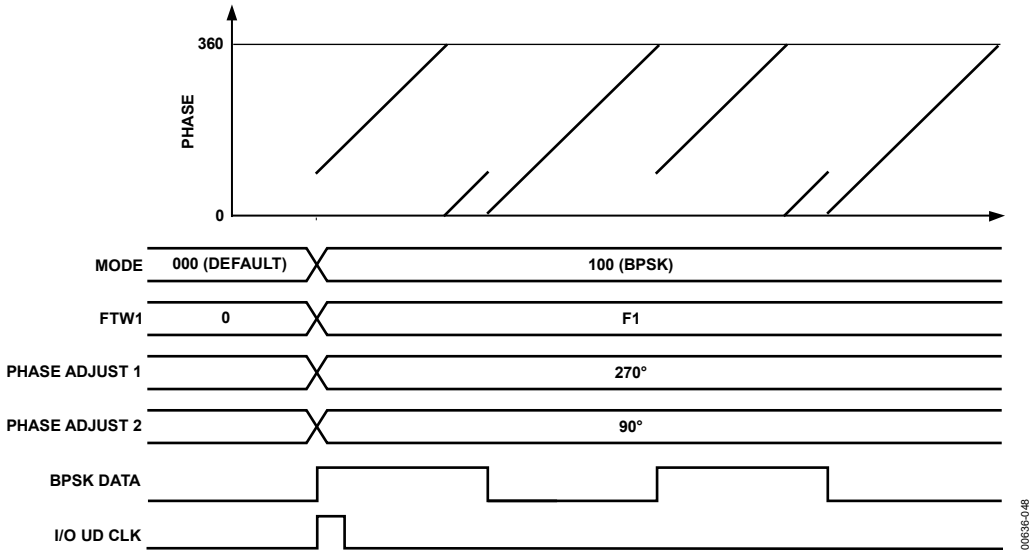


Figure 48. BPSK Mode

The 32-bit automatic I/O update counter can be used to construct complex chirp or ramped FSK sequences. Because this internal counter is synchronized with the AD9854 system clock, precisely timed program changes are possible. For such changes, the user need only reprogram the desired registers before the automatic I/O update clock is generated.

In chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS automatically confines itself to the frequency range between dc and Nyquist. Unless terminated by the user, the chirp continues until power is removed.

When the chirp destination frequency is reached, the user can choose any of the following actions:

- Stop at the destination frequency by using the HOLD pin or by loading all 0s into the delta frequency word registers of the frequency accumulator (ACC1).
- Use the HOLD pin function to stop the chirp, and then ramp down the output amplitude by using the digital multiplier stages and the output shaped keying pin (Pin 30), or by using the program register control (Address 21 to Address 24 hex).
- Abruptly end the transmission with the CLR ACC2 bit.
- Continue chirp by reversing direction and returning to the previous or another destination frequency in a linear or user-directed manner. If this involves reducing the frequency, a negative 48-bit delta frequency word (the MSB is set to 1) must be loaded into Register 10 hex to Register 15 hex. Any decreasing frequency step of the delta frequency word requires the MSB to be set to logic high.

- Continue chirp by immediately returning to the beginning frequency (F1) in a sawtooth fashion, and then repeating the previous chirp process using the CLR ACC1 control bit. An automatic, repeating chirp can be set up by using the 32-bit update clock to issue the CLR ACC1 command at precise time intervals. Adjusting the timing intervals or changing the delta frequency word changes the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

BPSK (Mode 100)

Binary, biphase, or bipolar phase shift keying is a means to rapidly select between two preprogrammed 14-bit output phase offsets that equally affect both the I and Q outputs of the AD9854. The logic state of Pin 29, the BPSK pin, controls the selection of Phase Adjust Register 1 or Phase Adjust Register 2. When low, Pin 29 selects Phase Adjust Register 1; when high, it selects Phase Adjust Register 2. Figure 48 illustrates phase changes made to four cycles of an output carrier.

Basic BPSK Programming Steps

1. Program a carrier frequency into Frequency Tuning Word 1.
2. Program the appropriate 14-bit phase words into Phase Adjust Register 1 and Phase Adjust Register 2.
3. Attach the BPSK data source to Pin 29.
4. Activate the I/O update clock when ready.

Note that for higher-order PSK modulation, the user can select the single-tone mode and program Phase Adjust Register 1 using the serial or high speed parallel programming bus.

USING THE AD9854

INTERNAL AND EXTERNAL UPDATE CLOCK

This update clock function is comprised of a bidirectional I/O pin (Pin 20) and a programmable 32-bit down-counter. To program changes that are to be transferred from the I/O buffer registers to the active core of the DDS, a clock signal (low-to-high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit update clock.

When the user provides an external update clock, it is internally synchronized with the system clock to prevent a partial transfer of program register information due to a violation of data setup or hold time. This mode allows the user to completely control when updated program information becomes effective. The default mode for the update clock is internal (the internal update clock control register bit is logic high). To switch to external update clock mode, the internal update clock control register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses at intervals set by the user.

An internally generated update clock can be established by programming the 32-bit update clock registers (Address 16 hex to Address 19 hex) and setting the internal update clock control register bit (Address 1F hex) to logic high. The update clock down-counter function operates at half the rate of the system clock (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O update of the DDS output or functions is generated. The update clock is internally and externally routed to Pin 20 to allow users to synchronize the programming of update information with the update clock rate. The time between update pulses is given as

$$(N + 1)(System\ Clock\ Period \times 2)$$

where N is the 32-bit value programmed by the user, and the allowable range of N is from 1 to $(2^{32} - 1)$.

The internally generated update pulse that is output from Pin 20 has a fixed high time of eight system clock cycles.

Programming the update clock register to a value less than five causes the I/O UD CLK pin to remain high. Although the update clock can function in this state, it cannot be used to indicate when data is transferring. This is an effect of the minimum high pulse time when I/O UD CLK functions as an output.

ON/OFF OUTPUT SHAPED KEYING (OSK)

The on/off OSK feature allows the user to control the amplitude vs. time slope of the I and Q DAC output signals. This function is used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the OSK EN bit (Control Register Address 20 hex) to logic high in the control register. Otherwise, if the OSK EN bit is set low, the digital multipliers responsible for amplitude control are bypassed and the I and Q DAC outputs are set to full-scale amplitude.

In addition to setting the OSK EN bit, a second control bit, OSK INT (also at Address 20 hex), must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multipliers to user-programmable 12-bit registers, allowing users to dynamically shape the amplitude transition in practically any fashion. These 12-bit registers, labeled Output Shape Key I and Output Shape Key Q, are located at Address 21 hex through Address 24 hex, as listed in Table 8. The maximum output amplitude is a function of the R_{SET} resistor and is not programmable when OSK INT is enabled.

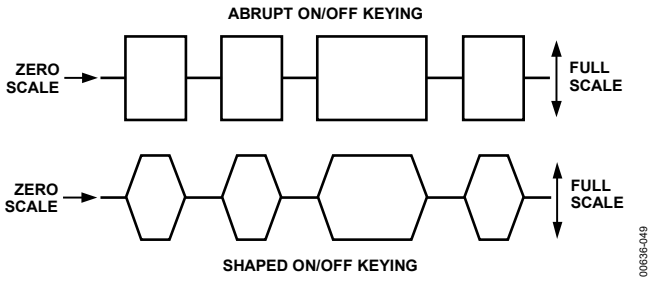


Figure 49. On/Off Output Shaped Keying

The transition time from zero scale to full scale must also be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the programmable 8-bit ramp rate counter. This is a down-counter that is clocked at the system clock rate (300 MHz maximum) and that generates one pulse whenever the counter reaches 0. This pulse is routed to a 12-bit counter that increments with each pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all 0s at its inputs, the input signal is multiplied by 0, producing zero scale. When the multiplier has a value of all 1s, the input signal is multiplied by a value of 4095 or 4096, producing nearly full scale. There are 4094 remaining fractional multiplier values that produce output amplitudes scaled according to their binary values.

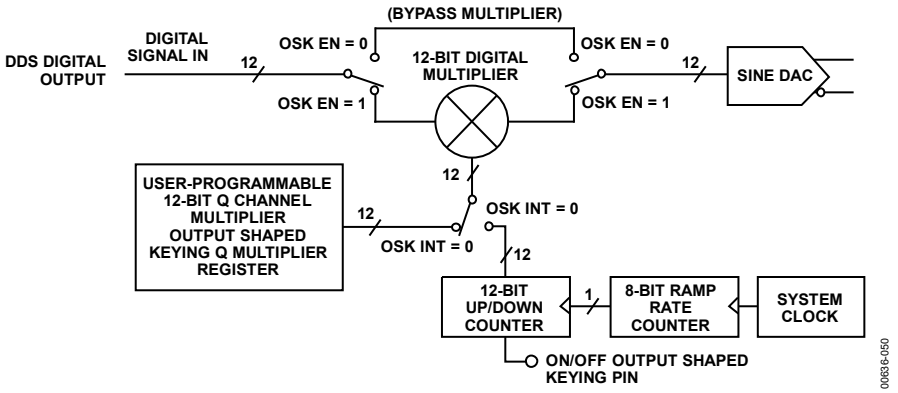


Figure 50. Block Diagram of Q DAC Pathway of the Digital Multiplier Section Responsible for the Output Shaped Keying Function

The two fixed elements of the transition time are the period of the system clock (which drives the ramp rate counter) and the number of amplitude steps (4096). For example, if the system clock of the AD9854 is 100 MHz (10 ns period) and the ramp rate counter is programmed for a minimum count of 3, the transition takes two system clock periods (one rising edge loads the countdown value, and the next edge decrements the counter from 3 to 2). If the countdown value is less than 3, the ramp rate counter stalls and therefore produces a constant scaling value to the digital multipliers. This stall condition may have an application for the user.

The relationship of the 8-bit countdown value to the time between output pulses is given as

$$(N + 1) \times System\ Clock\ Period$$

where N is the 8-bit countdown value.

It takes 4096 of these pulses to advance the 12-bit up-counter from zero scale to full scale. Therefore, the minimum output shaped keying ramp time for a 100 MHz system clock is

$$4096 \times 4 \times 10\ ns \approx 164\ \mu s$$

The maximum ramp time is

$$4096 \times 256 \times 10\ ns \approx 10.5\ ms$$

Finally, changing the logic state of Pin 30, output shaped keying automatically performs the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp up to full-scale amplitude and to hold until the logic level is changed to low, causing the outputs to ramp down to zero scale.

I AND Q DACS

The sine and cosine outputs of the DDS drive the Q and I DACs, respectively (300 MSPS maximum). The maximum amplitudes of these output are set by the DAC R_{SET} resistor at Pin 56. These are current-output DACs with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides the best SFDR performance. The value of R_{SET} is 39.93/I_{OUT}, where I_{OUT} is expressed in amps. DAC output compliance specifications limit the maximum voltage developed at the outputs to −0.5 V to +1 V. Voltages developed beyond this limitation cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to the compliance limits. Both DAC outputs should be terminated equally for best SFDR, especially at higher output frequencies, where harmonic distortion errors are more prominent.

Both DACs are preceded by inverse sin(x)/x filters (also called inverse sinc filters) that precompensate for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. Both DACs can be powered down when not needed by setting the DAC PD bit high (Address 1D hex of the control register). I DAC outputs are designated as IOUT1 and $\overline{\text{IOUT1}}$, Pin 48 and Pin 49, respectively. Q DAC outputs are designated as IOUT2 and $\overline{\text{IOUT2}}$, Pin 52 and Pin 51, respectively.

CONTROL DAC

The 12-bit Q DAC can be reconfigured to perform as a control or auxiliary DAC. The control DAC output can provide dc control levels to external circuitry, generate ac signals, or enable duty cycle control of the on-board comparator. When the SRC Q DAC bit in the control register (Parallel Address 1F hex) is set high, the Q DAC inputs are switched from internal 12-bit Q data source (default setting) to external 12-bit, twos complement data supplied by the user. Data is channeled through the serial or parallel interface to the 12-bit Q DAC register (Address 26 hex and Address 27 hex) at a maximum data rate of 100 MHz. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the I DAC. The single R_{SET} resistor on the AD9854 sets the full-scale output current for both DACs. When not needed, the control DAC can be separately powered down to conserve power by setting the Q DAC power-down bit high (Address 1D hex). Control DAC outputs are designated as IOUT2 and $\overline{\text{IOUT2}}$, Pin 52 and Pin 51, respectively.

INVERSE SINC FUNCTION

The inverse sinc function precompensates input data to both DACs for the sin(x)/x roll-off characteristic inherent in the DAC's output spectrum. This allows wide bandwidth signals (such as QPSK) to be output from the DACs without appreciable amplitude variations as a function of frequency. The inverse sinc function can be bypassed to reduce power consumption significantly, especially at higher clock speeds. When the Q DAC is configured as a control DAC, the inverse sinc function does not apply to the Q path.

Inverse sinc is engaged by default and is bypassed by bringing the bypass inverse sinc bit high in Control Register 20 hex, as noted in Table 8.

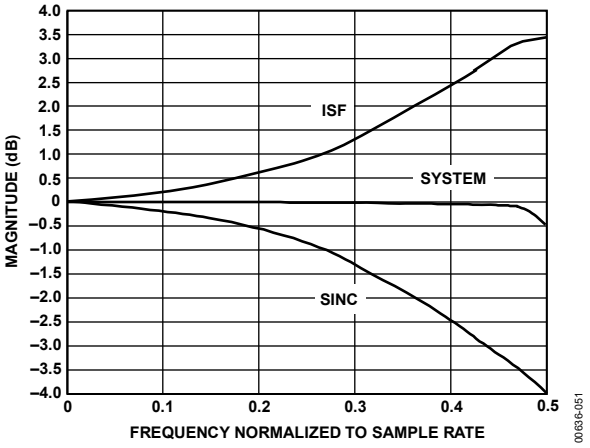


Figure 51. Inverse Sinc Filter Response

REFCLK MULTIPLIER

The REFCLK multiplier is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20×. With this function, users can input as little as 15 MHz at the REFCLK input to produce a 300 MHz internal system clock. Five bits in Control Register 1E hex set the multiplier value, as detailed in Table 7.

The REFCLK multiplier function can be bypassed to allow direct clocking of the AD9854 from an external clock source. The system clock for the AD9854 is either the output of the REFCLK multiplier (if it is engaged) or the REFCLK inputs. REFCLK can be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE, low or high, respectively.

PLL Range Bit

The PLL range bit selects the frequency range of the REFCLK multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate), the PLL range bit should be set to Logic 1. For operation below 200 MHz, the PLL range bit should be set to Logic 0. The PLL range bit adjusts the PLL loop parameters for best phase noise performance within each range.

PLL Filter

The PLL FILTER pin (Pin 61) provides the connection for the external zero-compensation network of the PLL loop filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected as close as possible to Pin 60, AVDD. For optimum phase noise performance, the clock multiplier can be bypassed by setting the bypass PLL bit in Control Register Address 1E hex.

Differential REFCLK Enable

A high level on the DIFF CLK ENABLE pin enables the differential clock inputs, REFCLK and $\overline{\text{REFCLK}}$ (Pin 69 and Pin 68, respectively). The minimum differential signal amplitude required is 400 mV p-p at the REFCLK input pins. The center point or common-mode range of the differential signal can range from 1.6 V to 1.9 V.

When Pin 64 (DIFF CLK ENABLE) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as single-ended mode. In this mode, Pin 68 ($\overline{\text{REFCLK}}$) should be tied low or high.

High Speed Comparator

The comparator is optimized for high speed and has a toggle rate greater than 300 MHz, low jitter, sensitive input, and built-in hysteresis. It also has an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be powered down separately to conserve power. This comparator is used in clock-generator applications to square up the filtered sine wave generated by the DDS.

Power-Down

The programming registers allow several individual stages to be powered down to reduce power consumption while maintaining the functionality of the desired stages. These stages are identified in Table 8, Address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, the inverse sinc filters and the digital multiplier stages can be bypassed to achieve significant power reduction by programming the control registers in Address 20 hex. Again, logic high causes the stage to be bypassed. Of particular importance is the inverse sinc filter; this stage consumes a significant amount of power.

A full power-down occurs when all four PD bits in Control Register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

PROGRAMMING THE AD9854

The AD9854 register layout table (Table 8) contains information for programming the chip for the desired functionality. Although many applications require very little programming to configure the AD9854, some use all 12 accessible register banks. The AD9854 supports an 8-bit parallel I/O operation or an SPI®-compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

S/P SELECT (Pin 70) is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to V_{DD}. Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of the mode, the I/O port data is written to a buffer memory and only affects operation of the part after the contents of the buffer memory are transferred to the register banks. This transfer of information occurs synchronously to the system clock in one of two ways:

- Internally, at a rate programmable by the user.
- Externally, by the user. I/O operations can occur in the absence of REFCLK, but the data cannot be moved from the buffer memory to the register bank without REFCLK. (See the Internal and External Update Clock section for more details.)

MASTER RESET

The MASTER RESET pin must be held at logic high active for a minimum of 10 system clock cycles. This initializes the communications bus and loads the default values listed in the Table 8 section.

Table 7. REFCLK Multiplier Control Register Values

	Reference Multiplier				
Multiplier Value	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0

Table 8. Register Layout[1]

Parallel Address (Hex)	Serial Address (Hex)	AD9854 Register Layout								Default Value (Hex)
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00	0	Phase Adjust Register 1 <13:8> (Bits 15, 14, don't care)					Phase 1			00
01		Phase Adjust Register 1 <7:0>								00
02	1	Phase Adjust Register 2 <13:8> (Bits 15, 14, don't care)					Phase 2			00
03		Phase Adjust Register 2 <7:0>								00
04	2	Frequency Tuning Word 1 <47:40>					Freq 1			00
05		Frequency Tuning Word 1 <39:32>								00
06		Frequency Tuning Word 1 <31:24>								00
07		Frequency Tuning Word 1 <23:16>								00
08		Frequency Tuning Word 1 <15:8>								00
09		Frequency Tuning Word 1 <7:0>								00
0A	3	Frequency Tuning Word 2 <47:40>								
0B		Frequency Tuning Word 2 <39:32>								00
0C		Frequency Tuning Word 2 <31:24>								00
0D		Frequency Tuning Word 2 <23:16>								00
0E		Frequency Tuning Word 2 <15:8>								00
0F		Frequency Tuning Word 2 <7:0>								00
10	4	Delta frequency word <47:40>								00
11		Delta frequency word <39:32>								00
12		Delta frequency word <31:24>								00
13		Delta frequency word <23:16>								00
14		Delta frequency word <15:8>								00
15		Delta frequency word <7:0>								00
16	5	Update clock <31:24>								00
17		Update clock <23:16>								00
18		Update clock <15:8>								00
19		Update clock <7:0>								40
1A	6	Ramp rate clock <19:16> (Bits 23, 22, 21, 20, don't care)								00
1B		Ramp rate clock <15:8>								00
1C		Ramp rate clock <7:0>								00
1D	7	Don't care CR [31]	Don't care	Don't care	Comp PD	Reserved, always low	QDAC PD	DAC PD	DIG PD	10
1E		Don't care	PLL range	Bypass PLL	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0	64
1F		CLR ACC 1	CLR ACC 2	Triangle	SRC QDAC	Mode 2	Mode 1	Mode 0	Internal/external update clock	01
20		Don't care	Bypass inv sinc	OSK EN	OSK INT	Don't care	Don't care	LSB first	SDO active CR [0]	20
21	8	Output shaped keying I multiplier <11:8> (Bits 15, 14, 13, 12 don't care)								00
22		Output shaped keying I multiplier <7:0>								00
23	9	Output shaped keying Q multiplier <11:8> (Bits 15, 14, 13, 12 don't care)								00
24		Output shaped keying Q multiplier <7:0>								00
25	A	Output shaped keying ramp rate <7:0>								80
26	B	QDAC <11:8> (Bits 15, 14, 13, 12 don't care)								00
27		QDAC <7:0> (data is required to be in twos complement format)								

[1] The shaded sections comprise the control register.

PARALLEL I/O OPERATION

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry-standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits, and separate write/read control inputs comprise the I/O port pins.

Parallel I/O operation allows write access to each byte of any register in a single I/O operation of up to one per 10.5 ns. Readback capability for each register is included to ease designing with the AD9854. (Reads are not guaranteed at 100 MHz because they are intended for software debugging only.)

Parallel I/O operation timing diagrams are shown in Figure 52 and Figure 53.

SERIAL PORT I/O OPERATION

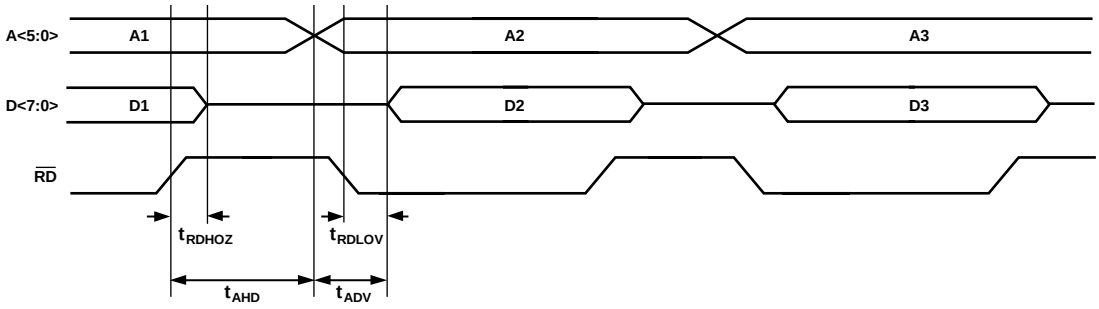
With the S/P SELECT pin tied low, the serial I/O mode is active. The serial port is a flexible, synchronous, serial communication port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and Intel® 8051 SSR protocols. The interface allows read/write access to all 12 registers that configure the AD9854 and can be configured as a single-pin I/O (SDIO) or two unidirectional pins for input and output (SDIO/SDO). Data transfers are supported in MSB-or the LSB-first format for up to 10 MHz.

When configured for serial I/O operation, most AD9854 parallel port pins are inactive; only some pins are used for the serial I/O operation. Table 9 describes pin requirements for serial I/O operation.

Note that when operating the device in serial I/O mode, it is best to use the external I/O update clock mode to avoid an update occurring during a serial communication cycle. Such an occurrence may cause incorrect programming due to a partial data transfer. To exit the default internal update mode, program the device for external update operation at power-up before starting the REFCLK signal but after a master reset. Starting the REFCLK causes this information to transfer to the register bank, forcing the device to switch to external update mode.

Table 9. Serial I/O Pin Requirements

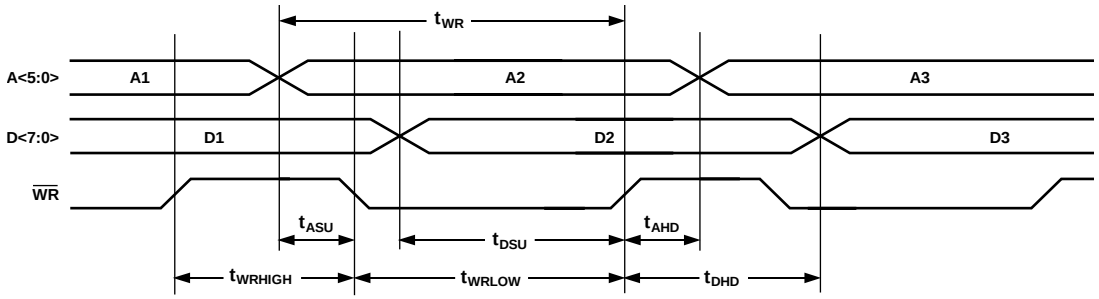
Pin Number	Mnemonic	Serial I/O Description
1 to 8	D [7:0]	The parallel data pins are not active; tie to VDD or GND.
14 to 16	A [5:3]	The A5, A4, and A3 parallel address pins are not active; tie these pins to VDD or GND.
17	A2/IO RESET	IO RESET.
18	A1/SDO	SDO.
19	A0/SDIO	SDIO.
20	I/O UD CLK	Update Clock. Same functionality for serial mode as parallel mode.
21	$\overline{WR}$/SCLK	SCLK.
22	$\overline{RD}$/$\overline{CS}$	$\overline{CS}$—Chip Select.



SPECIFICATION	VALUE	DESCRIPTION
t_{ADV}	15ns	ADDRESS TO DATA VALID TIME (MAXIMUM)
t_{AHD}	5ns	ADDRESS HOLD TIME TO RD SIGNAL INACTIVE (MINIMUM)
t_{RDLOV}	15ns	$\overline{RD}$ LOW TO OUTPUT VALID (MAXIMUM)
t_{RDHOZ}	10ns	$\overline{RD}$ HIGH TO DATA THREE-STATE (MAXIMUM)

00636-052

Figure 52. Parallel Port Read Timing Diagram



SPECIFICATION	VALUE	DESCRIPTION
t_{ASU}	8.0ns	ADDRESS SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
t_{DSU}	3.0ns	DATA SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
t_{ADH}	0ns	ADDRESS HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
t_{DHD}	0ns	DATA HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
t_{WRLOW}	2.5ns	$\overline{WR}$ SIGNAL MINIMUM LOW TIME
t_{WRHIGH}	7ns	$\overline{WR}$ SIGNAL MINIMUM HIGH TIME
t_{WR}	10.5ns	MINIMUM WRITE TIME

00636-053

Figure 53. Parallel Port Write Timing Diagram

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases of a serial communication cycle with the AD9854. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9854 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9854 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write and the register address to be acted upon.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9854. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9854 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. (Table 10 describes how many bytes must be transferred.) The AD9854 internal serial I/O controller expects every byte of the register being accessed to be transferred. Therefore, the user should write between I/O update clocks.

At the completion of a communication cycle, the AD9854 serial port controller expects the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IO RESET pin immediately terminates the current communication cycle. After IO RESET returns low, the AD9854 serial port controller requires the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9854 is registered on the rising edge of SCLK, and all data is driven out of the AD9854 on the falling edge of SCLK.

Figure 54 and Figure 55 show the general operation of the AD9854 serial port.

Table 10. Register Address vs. Data Bytes Transferred

Serial Register Address	Register Name	Number of Bytes Transferred
0	Phase Offset Tuning Word Register 1	2
1	Phase Offset Tuning Word Register 2	2
2	Frequency Tuning Word 1	6
3	Frequency Tuning Word 2	6
4	Delta frequency register	6
5	Update clock rate register	4
6	Ramp rate clock register	3
7	Control register	4
8	I path digital multiplier register	2
9	Q path digital multiplier register	2
A	Shaped on/off keying ramp rate register	1
B	Q DAC register	2

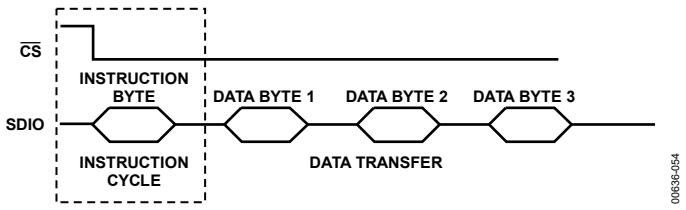


Figure 54. Using SDIO as a Read/Write Transfer

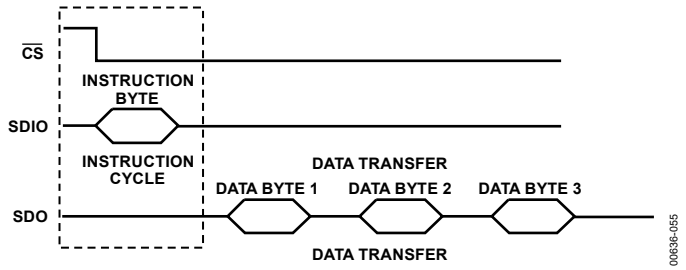


Figure 55. Using SDIO as an Input and SDO as an Output

INSTRUCTION BYTE

The instruction byte contains the following information:

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	X	X	X	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 determines whether a read or write data transfer occurs following the instruction byte. Logic high indicates read operation. Logic 0 indicates a write operation.

Bit 6, Bit 5, and Bit 4 are dummy bits (don't care).

A3, A2, A1, A0—Bit 3, Bit 2, Bit 1, and Bit 0 determine which register is accessed during the data transfer portion of the communication cycle (see Table 8 for register address details).

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9854 and to run the internal state machines. The SCLK maximum frequency is 10 MHz.

$\overline{CS}$

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communication line. The SDO and SDIO pins go to a high impedance state when this input is high. If this pin is driven high during a communication cycle, the cycle is suspended until $\overline{CS}$ is reactivated low. The chip select pin can be tied low in systems that maintain control of SCLK.

SDIO

Serial Data I/O (Pin 19). Data is always written to the AD9854 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of Register Address 20 hex. The default is Logic 0, which configures the SDIO pin as bidirectional.

SDO

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9854 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

IO RESET

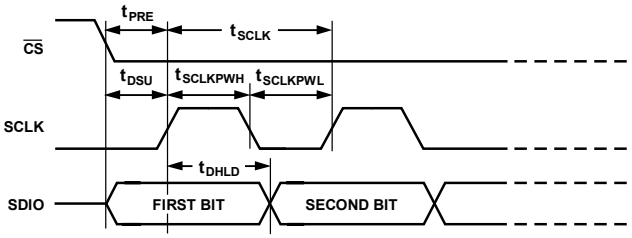
Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the contents of the addressable registers. An active high input on the IO RESET pin causes the current communication cycle to terminate. After the IO RESET pin returns low (Logic 0), another communication cycle can begin, starting with the instruction byte.

NOTES ON SERIAL PORT OPERATION

The AD9854 serial port configuration bits reside in Bit 1 and Bit 0 of Register Address 20 hex. It is important to note that the configuration changes immediately upon a valid I/O update. For multibyte transfers, writing to this register can occur during the middle of a communication cycle. The user must compensate for this new configuration for the remainder of the current communication cycle.

The system must maintain synchronization with the AD9854; otherwise, the internal control logic is not able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register and then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle properly write the first two data bytes into the AD9854, but the subsequent eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9854, the IO RESET pin provides a means to re-establish synchronization without reinitializing the entire chip. Asserting the IO RESET pin (active high) resets the AD9854 serial port state machine, terminating the current I/O operation and forcing the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The IO RESET pin must be deasserted (low) before the next instruction byte write can begin. Any information written to the AD9854 registers during a valid communication cycle prior to loss of synchronization remains intact.



SYMBOL	MIN	DEFINITION
t_{PRE}	30ns	$\overline{CS}$ SETUP TIME
t_{SCLK}	100ns	PERIOD OF SERIAL DATA CLOCK
t_{DSU}	30ns	SERIAL DATA SETUP TIME
$t_{SCLKPWH}$	40ns	SERIAL DATA CLOCK PULSE WIDTH HIGH
$t_{SCLKPWL}$	40ns	SERIAL DATA CLOCK PULSE WIDTH LOW
t_{DHLD}	0ns	SERIAL DATA HOLD TIME

Figure 56. Timing Diagram for Data Write to AD9854

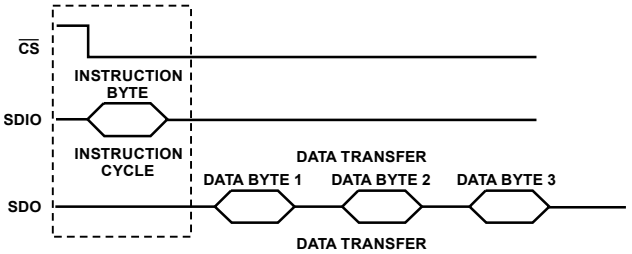


Figure 57. Timing Diagram for Read from AD9854

MSB/LSB TRANSFERS

The AD9854 serial port can support MSB- and LSB-first data formats. This functionality is controlled by Bit 1 of Serial Register Bank 20 hex. When this bit is set active high, the AD9854 serial port is in LSB-first format. This bit defaults low, to the MSB-first format. The instruction byte must be written in the format indicated by Bit 1 of Serial Register Bank 20 hex. Therefore, if the AD9854 is in LSB-first mode, the instruction byte must be written from least significant bit to most significant bit.

CONTROL REGISTER DESCRIPTION

The control register is located in the shaded portion of Table 8 at Address 1D to Address 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position, and Bit 0 is located in the lower right position of the shaded portion. In the text that follows, the register descriptions have been subdivided to make it easier to locate the text associated with specific control categories.

CR [31:29] are open.

CR [28] is the comparator power-down bit. When this bit is set (Logic 1), its signal indicates to the comparator that a power-down mode is active. This bit is an output of the digital section and is an input to the analog section.

CR [27] must always be written to Logic 0. Writing this bit to Logic 1 causes the AD9854 to stop functioning until a master reset is applied.

CR [26] is the Q DAC power-down bit. When this bit is set (Logic 1), it indicates to the Q DAC that a power-down mode is active.

CR [25] is the full DAC power-down bit. When this bit is set (Logic 1), it indicates to both the I and Q DACs, as well as the reference, that a power-down mode is active.

CR [24] is the digital power-down bit. When this bit is set (Logic 1), its signal indicates to the digital section that a power-down mode is active. Within the digital section, the clocks are forced to dc, effectively powering down the digital section. In this state, the PLL still accepts the REFCLK signal and continues to output the higher frequency.

CR [23] is reserved. Write to 0.

CR [22] is the PLL range bit, which controls the VCO gain. The power-up state of the PLL range bit is Logic 1; a higher gain is required for frequencies greater than 200 MHz.

CR [21] is the bypass PLL bit, active high. When this bit is active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1 with PLL bypassed.

CR [20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

CR [15] is the Clear Accumulator 1 bit. This bit has a one-shot type of function. When this bit is written active (Logic 1), a Clear Accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to 0. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a sawtooth frequency sweep pattern with minimal intervention. This bit is intended for chirp mode only, but its function is still retained in other modes.

CR [14] is the clear accumulator bit. When this bit is active high, it holds both the Accumulator 1 and Accumulator 2 values at 0 for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR [13] is the triangle bit. When this bit is set, the AD9854 automatically performs a continuous frequency sweep from F1 to F2 frequencies and back. This results in a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR [12] is the source Q DAC bit. When this bit is set high, the Q path DAC accepts data from the Q DAC register.

CR [11:9] are the three bits that describe the five operating modes of the AD9854:

0x0 = single-tone mode

0x1 = FSK mode

0x2 = ramped FSK mode

0x3 = chirp mode

0x4 = BPSK mode

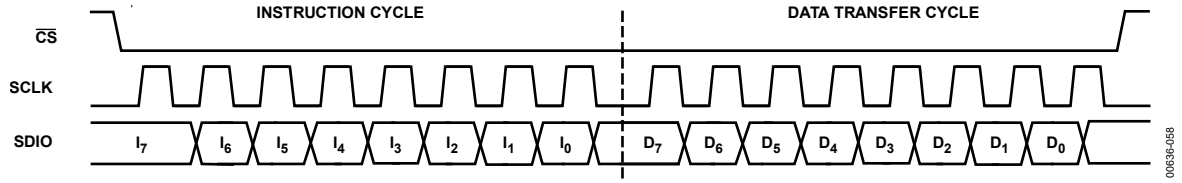


Figure 58. Serial Port Write Timing Clock Stall Low

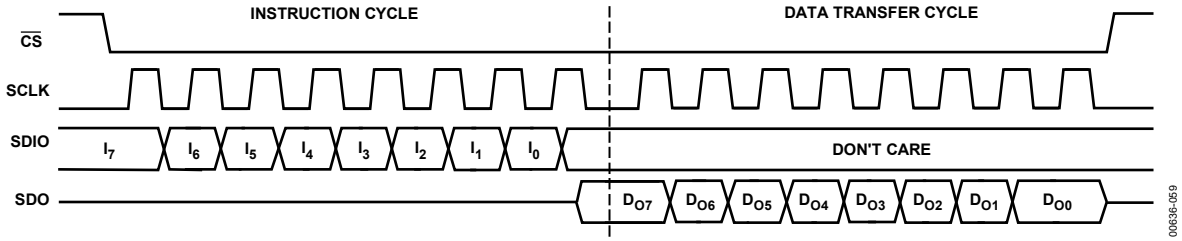


Figure 59. 3-Wire Serial Port Read Timing Clock Stall Low

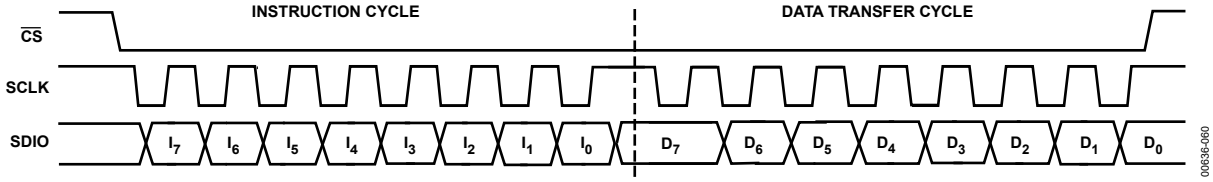


Figure 60. Serial Port Write Timing Clock Stall High

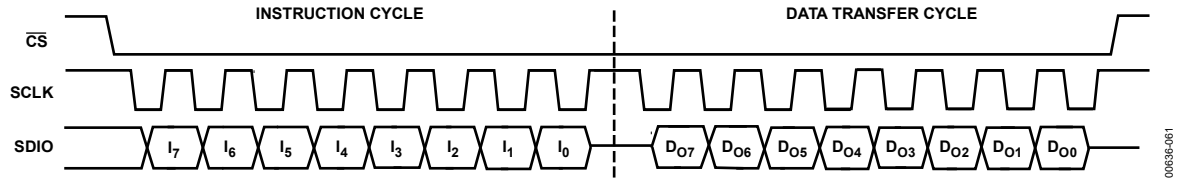


Figure 61. 2-Wire Serial Port Read Timing Clock Stall High

CR [8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD CLK pin is an output and the AD9854 generates the I/O UD CLK signal. When this bit is set to Logic 0, external I/O UD CLK functionality is performed and the I/O UD CLK pin is configured as an input.

CR [7] is reserved. Write to 0.

CR [6] is the inverse sinc filter bypass bit. When this bit is set, the data from the DDS block goes directly to the output shaped keying logic, and the clock to the inverse sinc filter is stopped. Default is clear with the filter enabled.

CR [5] is the shaped keying enable bit. When this bit is set, the output ramping function is enabled and is performed in accordance with the CR [4] bit requirements.

CR [4] is the internal/external output shaped keying control bit. When this bit is set to Logic 1, the output shaped keying factor is internally generated and applied to both the I and Q paths. When this bit is cleared (default), the output shaped keying function is externally controlled by the user, and the ouput shaped keying factor is the value of the I and Q output shaped keying factor register. The two registers that are the output shaped keying factors also default low such that the output is off at power-up until the device is programmed by the user.

CR [3:2] are reserved. Write to 0.

CR [1] is the serial port MSB-/LSB-first bit. Default is low, MSB first.

CR [0] is the serial port SDO active bit. Default is low, inactive.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9854 is a multifunctional, high speed device that targets a wide variety of synthesizer and agile clock applications. The numerous innovative features contained in the device each consume incremental power. If enabled in combination, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9854. However, in most cases, disabling the inverse sinc filter prevents exceeding the maximum die temperature, because the inverse sinc filter consumes approximately 30% of the total power.

The AD9854 is specified to operate within the industrial temperature range of −40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

Many variables contribute to the operating junction temperature within the device, including

- Package style
- Selected mode of operation
- Internal system clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9854 for a given set of operating conditions.

The AD9854 is available in two package styles: a thermally enhanced surface-mount package with an exposed heat sink and a standard (nonthermally enhanced) surface-mount package. The thermal impedance of these packages is 16.2°C/W and 38°C/W, respectively, measured under still air conditions.

THERMAL IMPEDANCE

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance is determined by the package material and the physical dimensions of the package. The dissipation of the heat from the package is directly dependent on the ambient air conditions and the physical connection made between the IC package and the PCB.

Adequate dissipation of heat from the AD9854 relies on all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9854ASVZ has an exposed paddle on the bottom of the package that must be soldered to a large copper plane, which, for convenience, can be the ground plane. Sockets for either package style of the device are not recommended.

JUNCTION TEMPERATURE CONSIDERATIONS

The power dissipation (P_{DISS}) of the AD9854 in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with P_{DISS}, such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device and its effect on the junction temperature must be considered when using the device. The junction temperature of the device is given by

$$(\textit{Thermal Impedance} \times \textit{Power Consumption}) + \textit{Ambient Temperature}$$

The maximum ambient temperature combined with the maximum junction temperature establishes the following power consumption limits for each package: 4.06 W for ASVZ models and 1.71 W for ASTZ models.

Supply Voltage

The supply voltage affects power dissipation and junction temperature because $P_{DISS} = V \times I$. Users should design for 3.3 V nominal; however, the device is guaranteed to meet specifications over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

Clock Speed

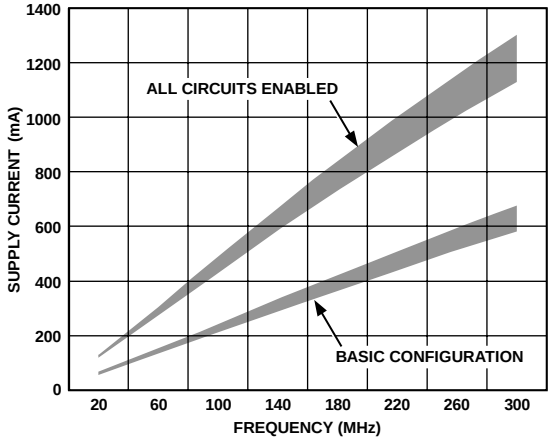
Clock speed directly and linearly influences the total power dissipation of the device and therefore the junction temperature. As a rule, to minimize power dissipation, the user should select the lowest possible internal clock speed to support a given application. Typically, the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to ensure that the requirements of the output low-pass filter are reasonable. For a typical DDS application, the system clock frequency should be 2.5 times the highest desired output frequency.

Mode of Operation

The selected mode of operation of the AD9854 significantly influences the total power consumption. Although the AD9854 offers many features targeting a wide variety of applications, the device is designed to operate with only a few features enabled at once for a given application. If multiple features are enabled at higher clock speeds, the maximum junction temperature of the die may be exceeded, severely limiting the long-term reliability of the device. Figure 62 and Figure 63 show the power requirements associated with each feature of the AD9854. These graphs should be used as a guide in determining power consumption for specific feature sets.

Figure 62 shows the supply current consumed by the AD9854 over a range of frequencies for two possible configurations. All circuits enabled means that the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are enabled. Basic configuration means that the output scaling

multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are disabled.

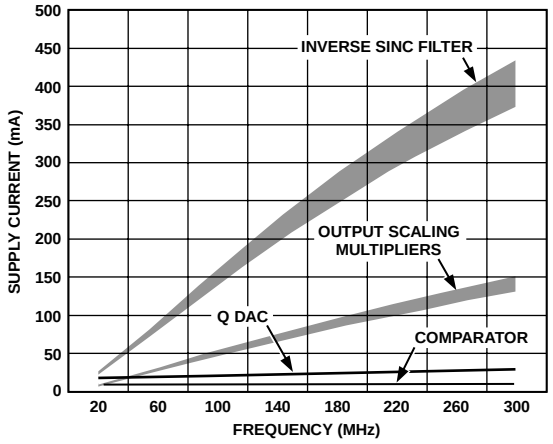


NOTES
THIS GRAPH ASSUMES THAT THE AD9854 DEVICE IS SOLDERED TO A MULTILAYER PCB PER THE RECOMMENDED BEST MANUFACTURING PRACTICES AND PROCEDURES FOR THE GIVEN PACKAGE TYPE.

00636-062

Figure 62. Current Consumption vs. Clock Frequency

Figure 63 shows the approximate current consumed by each of four functions.



NOTES
THIS GRAPH ASSUMES THAT THE AD9854 DEVICE IS SOLDERED TO A MULTILAYER PCB PER THE RECOMMENDED BEST MANUFACTURING PRACTICES AND PROCEDURES FOR THE GIVEN PACKAGE TYPE.

00636-063

Figure 63. Current Consumption by Function vs. Clock Frequency

EVALUATION OF OPERATING CONDITIONS

The first step in applying the AD9854 is to select the internal clock frequency. Clock frequency selections greater than 200 MHz require the use of the thermally enhanced package (AD9854ASVZ); other clock frequencies may allow the use of the standard plastic surface-mount package, but more information is needed to make that determination.

The second evaluation step is to determine the maximum required operating temperature for the AD9854 in a given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9854. For the extended industrial temperature range, the maximum operating temperature is 85°C, which results in a difference of 65°C. This is the maximum temperature gradient that the device can experience due to power dissipation.

The third evaluation step is to divide the maximum temperature gradient by the thermal impedance to determine the maximum power dissipation allowed for the application. For example, 65°C divided by the thermal impedance of the package being used yields the total power dissipation limit (4.06 W for the ASVZ models and 1.71 W for the ASTZ models). Therefore, for a 3.3 V nominal power supply voltage, the current consumed by the device with full operating conditions must not exceed 515 mA for the standard plastic package and 1242 mA for the thermally enhanced package. The total set of enabled functions and operating conditions of the AD9854 application must support these current consumption limits.

To determine the suitability of a given AD9854 application in terms of the power dissipation requirements use Figure 62 and Figure 63. These graphs assume that the AD9854 device is soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications are achieved.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

Refer to the AN-772 Application Note for details on mounting devices with an exposed paddle.

OUTLINE DIMENSIONS

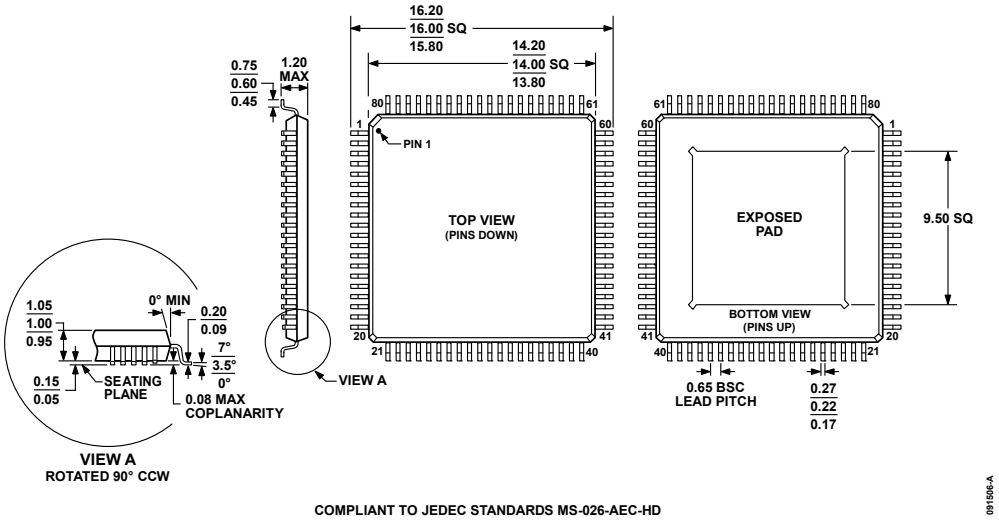


Figure 64. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-80-4)
Dimensions shown in millimeters

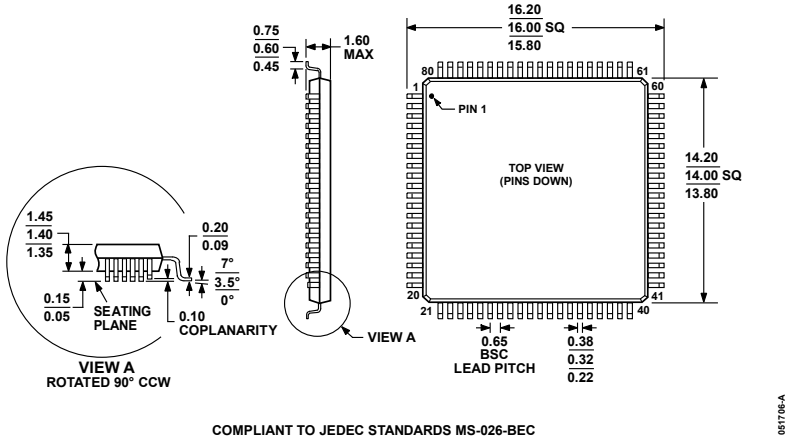


Figure 65. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9854ASVZ	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-4
AD9854ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2

[1] Z = RoHS Compliant Part.

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