400 MSPS, 14-Bit, 1.8 V CMOS, Direct Digital Synthesizer

Data Sheet **AD9954**

FEATURES

400 MSPS internal clock speed
Integrated 14-bit DAC
Programmable phase/amplitude dithering
32-bit frequency tuning accuracy
14-bit phase tuning accuracy
Phase noise better than −120 dBc/Hz
Excellent dynamic performance
>80 dB narrowband SFDR
Serial input/output (I/O) control
Ultrahigh speed analog comparator
Automatic linear and nonlinear frequency sweeping
4 frequency/phase offset profiles
1.8 V power supply
Software and hardware controlled power-down
48-lead TQFP
Integrated 1024 word × 32-bit RAM
PLL-based REFCLK multiplier
Internal oscillator, can be driven by a single crystal
Phase modulation capability
Multichip synchronization

APPLICATIONS

Agile LO frequency synthesis
Programmable clock generators
FM chirp source for radar and scanning systems
Automotive radars
Test and measurement equipment
Acousto-optic device drivers

GENERAL DESCRIPTION

The AD9954 is a direct digital synthesizer (DDS) that uses advanced technology, coupled with an internal high speed, high performance DAC to form a complete, digitally programmable, high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 160 MHz. The AD9954 enables fast frequency hopping coupled with fine tuning of both frequency (0.01 Hz or better) and phase (0.022° granularity).

The AD9954 is programmed via a high speed serial I/O port. The device includes static RAM to support flexible frequency sweep capability in several modes, plus a user-defined linear sweep mode of operation. Also included is an on-chip high speed comparator for applications requiring a square wave output. An on-chip oscillator and PLL circuitry provide users with multiple approaches to generate the device's system clock.

The AD9954 is specified to operate over the extended industrial temperature range (see Table 2).

BASIC BLOCK DIAGRAM

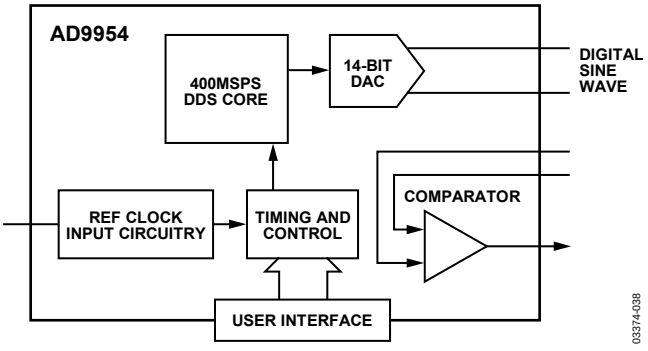


Figure 1.

Rev. C **Document Feedback**
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REVISION HISTORY

2/2017—Rev. B to Rev. C

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5/2009—Rev. A to Rev. B

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10/2003—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

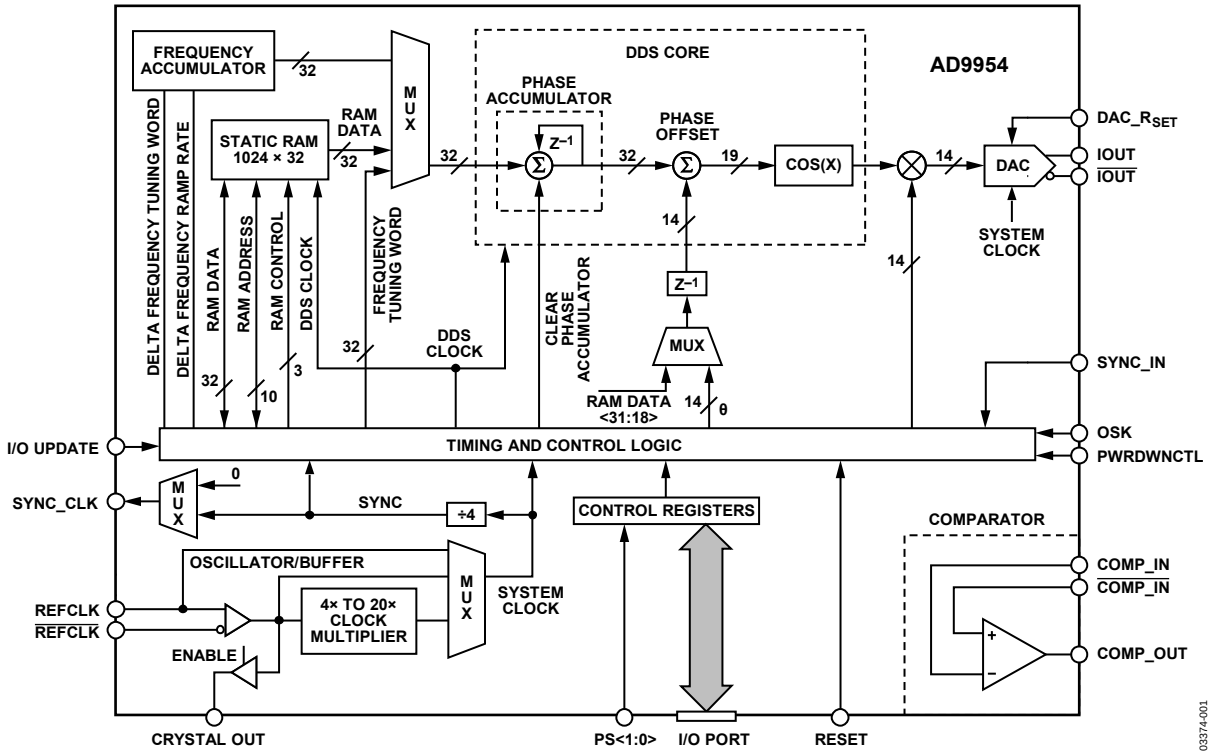


Figure 2.

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, AVDD, DVDD = 1.8 V ± 5%, DVDD_I/O = 3.3 V ± 5%, R_{SET} = 3.92 kΩ, external reference clock frequency = 400 MHz. DAC output must be referenced to AVDD, not AGND.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	1		400	MHz
REFCLK Multiplier Enabled at 4×	Full	VI	20		100	MHz
REFCLK Multiplier Enabled at 20×	Full	VI	4		20	MHz
Crystal Oscillator Operating Frequency	Full	IV	20		30	MHz
Input Capacitance	25°C	V		3		pF
Input Impedance	25°C	V		1.5		kΩ
Duty Cycle	25°C	V		50		%
Duty Cycle with REFCLK Multiplier Enabled	25°C	V	35		65	%
REFCLK Input Voltage Swing	Full	IV	100		1000	mV p-p
DAC OUTPUT CHARACTERISTICS						
Full-Scale Output Current	25°C		5	10	15	mA
Gain Error	25°C	I	−10		+10	%FS
Output Offset	25°C	I			0.6	µA
Differential Nonlinearity	25°C	V		1		LSB
Integral Nonlinearity	25°C	V		2		LSB
Output Capacitance	25°C	V		5		pF
Residual Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
REFCLK Multiplier Enabled @ 20×	25°C	V		−105		dBc/Hz
REFCLK Multiplier Enabled @ 4×	25°C	V		−115		dBc/Hz
REFCLK Multiplier Disabled	25°C	V		−132		dBc/Hz
Voltage Compliance Range	25°C	I	AVDD − 0.5		AVDD + 0.5	V
Wideband SFDR						
1 MHz to 10 MHz Analog Out	25°C	V		73		dBc
10 MHz to 40 MHz Analog Out	25°C	V		67		dBc
40 MHz to 80 MHz Analog Out	25°C	V		62		dBc
80 MHz to 120 MHz Analog Out	25°C	V		58		dBc
120 MHz to 160 MHz Analog Out	25°C	V		52		dBc
Narrow-Band SFDR						
40 MHz Analog Out (±1 MHz)	25°C	V		87		dBc
40 MHz Analog Out (±250 kHz)	25°C	V		89		dBc
40 MHz Analog Out (±50 kHz)	25°C	V		91		dBc
40 MHz Analog Out (±10 kHz)	25°C	V		93		dBc
80 MHz Analog Out (±1 MHz)	25°C	V		85		dBc
80 MHz Analog Out (±250 kHz)	25°C	V		87		dBc
80 MHz Analog Out (±50 kHz)	25°C	V		89		dBc
80 MHz Analog Out (±10 kHz)	25°C	V		91		dBc
120 MHz Analog Out (±1 MHz)	25°C	V		83		dBc
120 MHz Analog Out (±250 kHz)	25°C	V		85		dBc
120 MHz Analog Out (±50 kHz)	25°C	V		87		dBc
120 MHz Analog Out (±10 kHz)	25°C	V		89		dBc
160 MHz Analog Out (±1 MHz)	25°C	V		81		dBc
160 MHz Analog Out (±250 kHz)	25°C	V		83		dBc
160 MHz Analog Out (±50 kHz)	25°C	V		85		dBc
160 MHz Analog Out (±10 kHz)	25°C	V		87		dBc

Parameter	Temp	Test Level	Min	Typ	Max	Unit
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	25°C	V		3		pF
Input Resistance	25°C	IV		500		kΩ
Input Current	25°C	I		±12		μA
Hysteresis	25°C	IV	30		45	mV
COMPARATOR OUTPUT CHARACTERISTICS						
Logic 1 Voltage, High-Z Load	Full	VI	1.6			V
Logic 0 Voltage, High-Z Load	Full	VI			0.4	V
Propagation Delay	25°C	IV		3		ns
Output Duty-Cycle Error	25°C	IV		±5		%
Rise/Fall Time, 5 pF Load	25°C	IV			1	ns
Toggle Rate, High-Z Load	25°C	IV	200			MHz
Output Jitter[1]	25°C	IV			1	ps rms
COMPARATOR NARROW-BAND SFDR						
10 MHz to 160 MHz F_{OUT}						
Measured over a 1 MHz BW	25°C	V		80		dBc
Measured over a 250 kHz BW	25°C	V		85		dBc
Measured over a 50 kHz BW	25°C	V		90		dBc
Measured over a 10 Hz BW	25°C	V		95		dBc
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV		25		Mbps
Minimum Clock Pulse Width Low	Full	IV	7			ns
Minimum Clock Pulse Width High	Full	IV	7			ns
Maximum Clock Rise/Fall Time	Full	IV		2		ns
Minimum Data Setup Time DVDD_I/O = 3.3 V	Full	IV	3			ns
Minimum Data Setup Time DVDD_I/O = 1.8 V	Full	IV	5			ns
Minimum Data Hold Time	Full	IV	0			ns
Maximum Data Valid Time	Full	IV		25		ns
Wake-Up Time[2]	Full	IV		1		ms
Minimum Reset Pulse Width High	Full	IV	5			SYSCLK cycles[3]
I/O UPDATE, PS0, PS1 to SYNC_CLK Setup Time, DVDD_I/O = 3.3 V	Full	I	4			ns
I/O UPDATE, PS0, PS1 to SYNC_CLK Setup Time, DVDD_I/O = 1.8 V	Full	I	6			ns
I/O UPDATE, PS0, PS1 to SYNC_CLK Hold Time	Full	I	0			ns
Latency						
I/O UPDATE to Frequency Change Prop Delay	25°C	IV	24			SYSCLK cycles
I/O UPDATE to Phase Offset Change Prop Delay	25°C	IV	24			SYSCLK cycles
I/O UPDATE to Amplitude Change Prop Delay	25°C	IV	16			SYSCLK cycles
PS0, PS1 to RAM Driven Frequency Change Prop Delay	25°C	IV	28			SYSCLK cycles
PS0, PS1 to RAM Driven Phase Change Prop Delay	25°C	IV	28			SYSCLK cycles
PS0 to Linear Frequency Sweep Prop Delay	25°C	IV	28			SYSCLK cycles

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CMOS LOGIC INPUTS						
Logic 1 Voltage @ DVDD_I/O (Pin 43) = 1.8 V	25°C	I	1.25			V
Logic 0 Voltage @ DVDD_I/O (Pin 43) = 1.8 V	25°C	I			0.6	V
Logic 1 Voltage @ DVDD_I/O (Pin 43) = 3.3 V	25°C	I	2.2			V
Logic 0 Voltage @ DVDD_I/O (Pin 43) = 3.3 V	25°C	I			0.8	V
Logic 1 Current	25°C	V		3	12	µA
Logic 0 Current	25°C	V			12	µA
Input Capacitance	25°C	V		2		pF
CMOS LOGIC OUTPUTS (1 mA Load) DVDD_I/O = 1.8 V						
Logic 1 Voltage	25°C	I	1.35			V
Logic 0 Voltage	25°C	I			0.4	V
CMOS LOGIC OUTPUTS (1 mA Load) DVDD_I/O = 3.3 V						
Logic 1 Voltage	25°C	I	2.8			V
Logic 0 Voltage	25°C	I			0.4	V
POWER CONSUMPTION (AVDD = DVDD = 1.8 V)						
Single-Tone Mode (Comparator Off)	25°C	I		162	171	mW
With RAM or Linear Sweep Enabled	25°C	I		175	190	mW
With Comparator Enabled	25°C	I		180	190	mW
With RAM and Comparator Enabled	25°C	I		198	220	mW
Rapid Power-Down Mode	25°C	I		150	160	mW
Full-Sleep Mode	25°C	I		20	27	mW
SYNCHRONIZATION FUNCTION[4]						
Maximum Sync Clock Rate (DVDD_I/O = 1.8 V)	25°C	VI	62.5			MHz
Maximum Sync Clock Rate (DVDD_I/O = 3.3 V)	25°C	VI	100			MHz
SYNC_CLK Alignment Resolution[5]	25°C	V		±1		SYSCLK cycles

[1] Represents the cycle-to-cycle residual jitter from the comparator alone.
[2] Wake-up time refers to the recovery from analog power-down modes (see section on Power-Down Modes of Operation). The primary limiting factor is the settling time of the PLL multiplier in the reference circuitry. The wake-up time assumes there is no capacitor on DAC BP and that the recommended PLL loop filter values are used.
[3] SYSCLK cycle refers to the clock frequency used on-chip to drive the DDS core. This is equal to the frequency of the reference source times the value of the PLL-based reference clock multiplier.
[4] SYNC_CLK = ¼ SYSCLK rate. Be sure the high speed sync enable bit, CFR2<11>, is programmed appropriately.
[5] This parameter indicates that the digital synchronization feature cannot compensate for phase delays (timing skew) between system clock rising edges. If the system clock edges are aligned, the synchronization function should not increase the skew between the two edges.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 43)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	−0.7 V to +5.25 V
Digital Input Voltage (DVDD_I/O = 1.8 V)	−0.7 V to +2.2 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	38°C/W
θ_{JC}	15°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

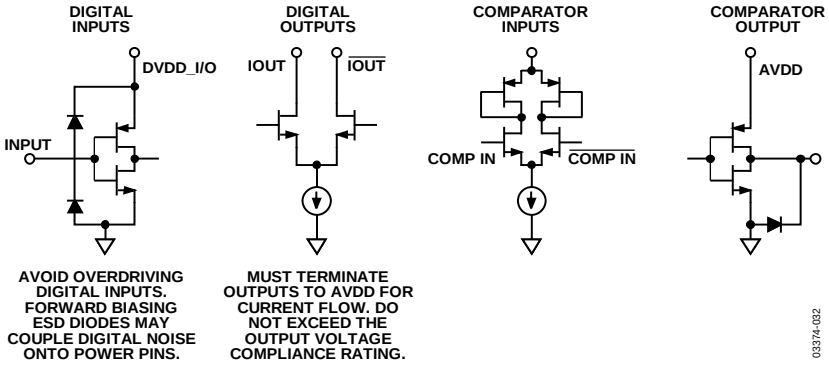


Figure 3. Equivalent Input and Output Circuits

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

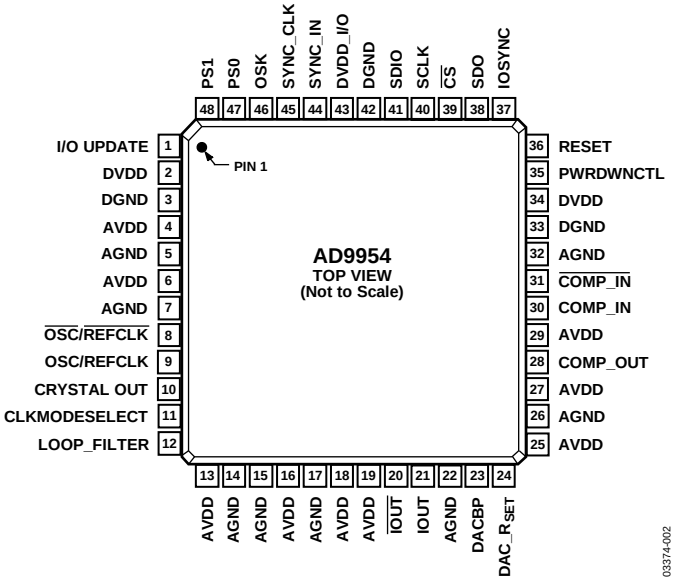


Figure 4. Pin Configuration

Note that the exposed paddle on the bottom of the package forms an electrical connection for the DAC and must be attached to analog ground. Note that Pin 43, DVDD_I/O, can be powered to 1.8 V or 3.3 V. The DVDD pins (Pin 2 and Pin 34) must be powered to 1.8 V.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	I/O UPDATE	I	The rising edge transfers the contents of the internal buffer memory to the I/O registers. See Synchronization—Register Updates (I/O UPDATE) section for details.
2, 34	DVDD	I	Digital Power Supply Pins (1.8 V).
3, 33, 42	DGND	I	Digital Power Ground Pins.
4, 6, 13, 16, 18, 19, 25, 27, 29	AVDD	I	Analog Power Supply Pins (1.8 V).
5, 7, 14, 15, 17, 22, 26, 32	AGND	I	Analog Power Ground Pins.
8	$\overline{\text{OSC}}$/REFCLK	I	Oscillator Input/Complementary Reference Clock. When the REFCLK port is operated in single-ended mode, $\overline{\text{REFCLK}}$ should be decoupled to AVDD with a 0.1 µF capacitor.
9	OSC/REFCLK	I	Oscillator Input/Reference Clock. See Table 5 for details on the OSC/REFCLK operation.
10	CRYSTAL OUT	O	Output of the Oscillator Section.
11	CLKMODESELECT	I	Control Pin for the Oscillator Section (1.8 V logic only). See REFCLK Input section for detailed instructions.
12	LOOP_FILTER	I	This pin provides the connection for the external zero compensation network of the REFCLK multiplier's PLL loop filter. The network varies based on the multiplication value in the PLL loop. See Table 4 for details.
20	$\overline{\text{IOUT}}$	O	Complementary DAC Output. Should be biased through a resistor to AVDD, not AGND.
21	IOUT	O	DAC Output. Should be biased through a resistor to AVDD, not AGND.
23	DACBP	I	DAC Band Gap Decoupling Pin. A 0.1 µF capacitor to AGND is recommended.
24	DAC_R_{SET}	I	A resistor (3.92 kΩ nominal) connected from AGND to DAC_R_{SET} establishes the reference current for the DAC. See equation in DAC Output section.
28	COMP_OUT	O	Comparator Output.
30	COMP_IN	I	Comparator Input.

Pin No.	Mnemonic	I/O	Description
31	$\overline{\text{COMP_IN}}$	I	Comparator Complementary Input.
35	PWRDWNCTL	I	Input Pin Used as an External Power-Down Control (see Table 9 for details).
36	RESET	I	Active High Hardware Reset Pin. Assertion of the RESET pin forces the AD9954 to the default state, as described in the right-hand column of Table 12, which is the I/O port register map.
37	IOSYNC	I	Asynchronous Active High Reset of the Serial Port Controller. When high, the current I/O operation is immediately terminated, enabling a new I/O operation to commence once IOSYNC is returned low. If unused, ground this pin; do not allow this pin to float.
38	SDO	O	See Serial Interface Port Pin Description section for details.
39	$\overline{\text{CS}}$	I	See Serial Interface Port Pin Description section for details.
40	SCLK	I	See Serial Interface Port Pin Description section for details.
41	SDIO	I/O	See Serial Interface Port Pin Description section for details.
43	DVDD_I/O	I	Digital Power Supply. This pin is for I/O cells only, 3.3 V.
44	SYNC_IN	I	Input Signal Used to Synchronize Multiple AD9954s. This input is connected to the SYNC_CLK output of a master AD9954.
45	SYNC_CLK	O	Clock Output Pin that Serves as a Synchronizer for External Hardware.
46	OSK	I	Input Pin Used to Control the Direction of the Shaped On-Off Keying Function When Programmed for Operation. OSK is synchronous to the SYNC_CLK pin. When OSK is disabled, this pin should be tied to DGND.
47, 48	PS0, PS1	I	Input Pins Used to Select One of the Internal Phase/Frequency Profiles. PS1 and PS0 are synchronous to the SYNC_CLK pin. Change on these pins triggers a transfer of the contents of the chosen internal buffer memory to the I/O registers (sends an internal I/O UPDATE).
<49>	AGND	I	The Exposed Paddle on the Bottom of the Package. It is a ground connection for the DAC and must be attached to AGND in any board layout.

TYPICAL PERFORMANCE CHARACTERISTICS

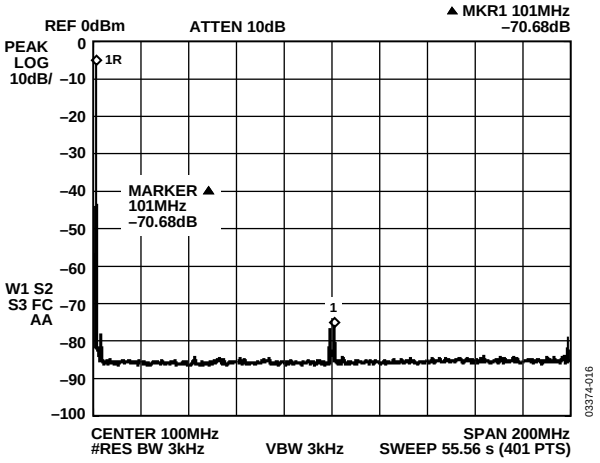


Figure 5. f_{OUT} = 1 MHz, f_{CLK} = 400 MSPS, WBSFDR

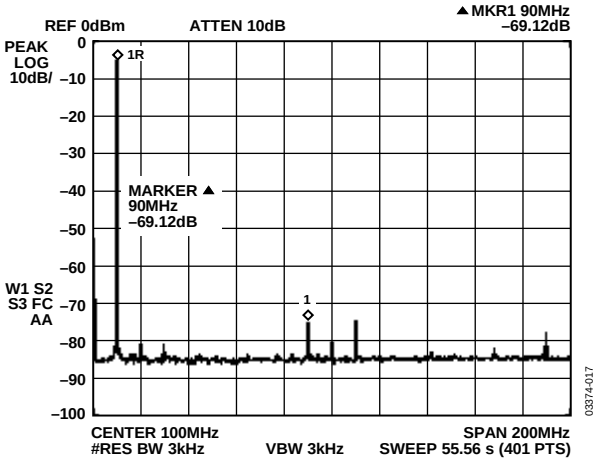


Figure 6. f_{OUT} = 10 MHz, f_{CLK} = 400 MSPS, WBSFDR

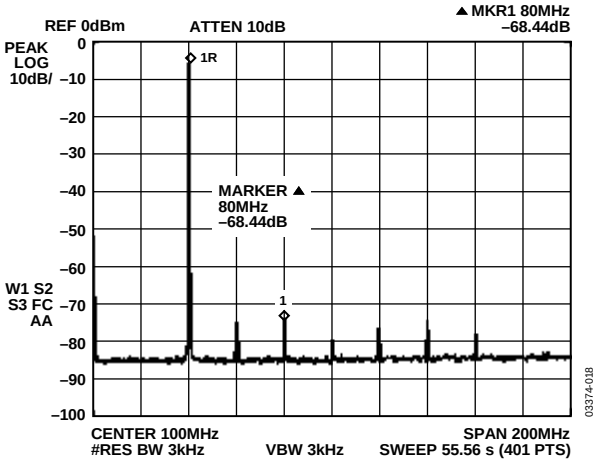


Figure 7. f_{OUT} = 40 MHz, f_{CLK} = 400 MSPS, WBSFDR

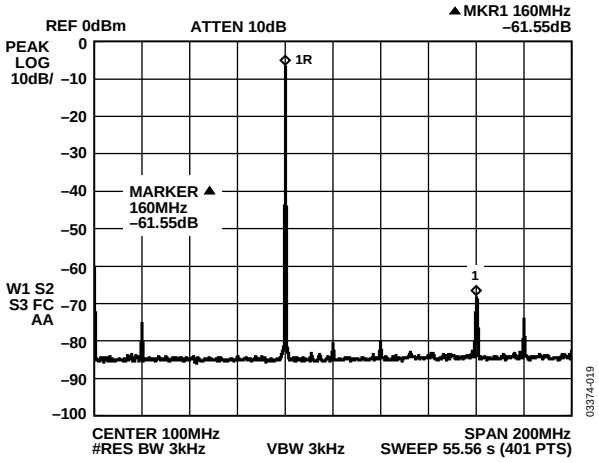


Figure 8. f_{OUT} = 80 MHz, f_{CLK} = 400 MSPS, WBSFDR

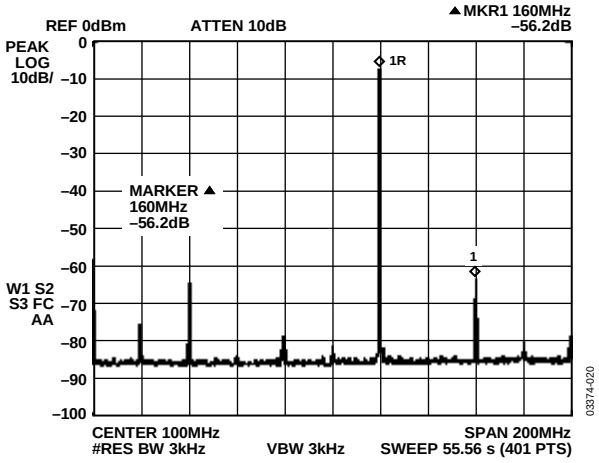


Figure 9 f_{OUT} = 120 MHz, f_{CLK} = 400 MSPS, WBSFDR

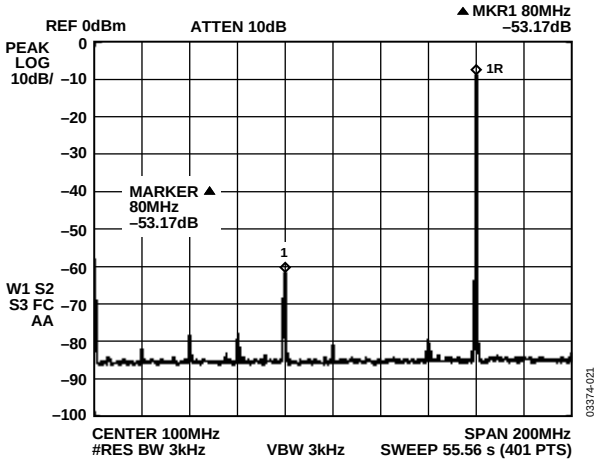


Figure 10. f_{OUT} = 160 MHz, f_{CLK} = 400 MSPS, WBSFDR

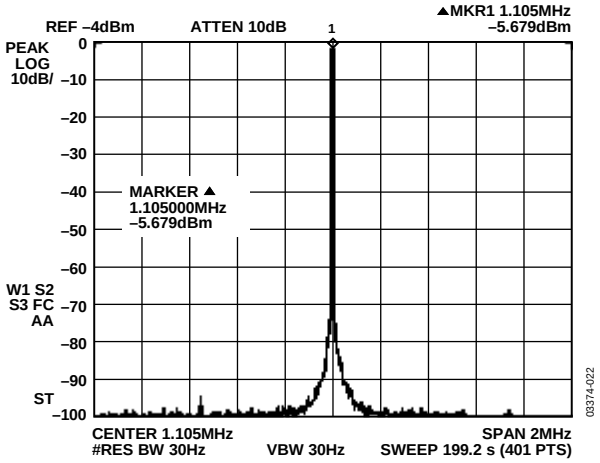


Figure 11. f_{OUT} = 1.1 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

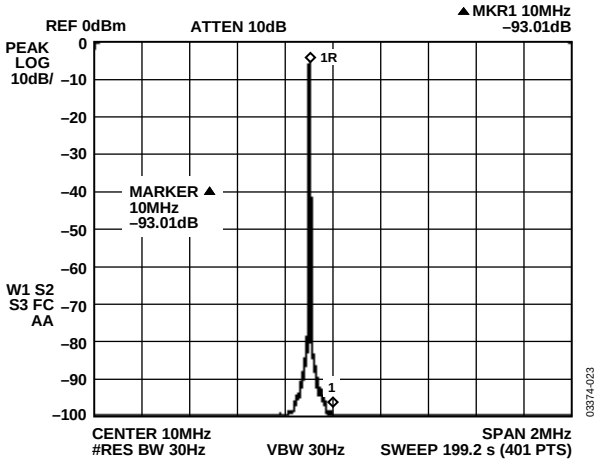


Figure 12. f_{OUT} = 9.5 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

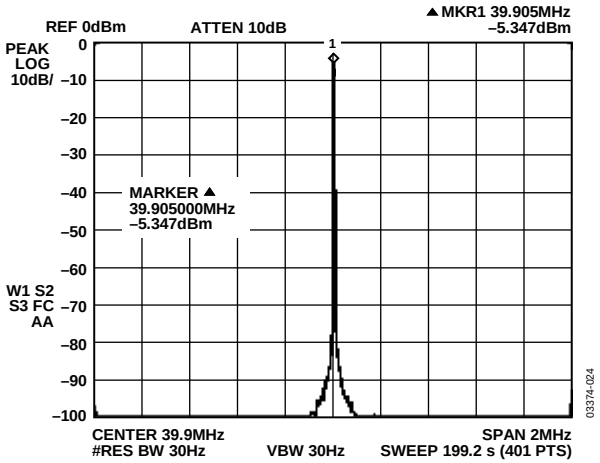


Figure 13. f_{OUT} = 39.9 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

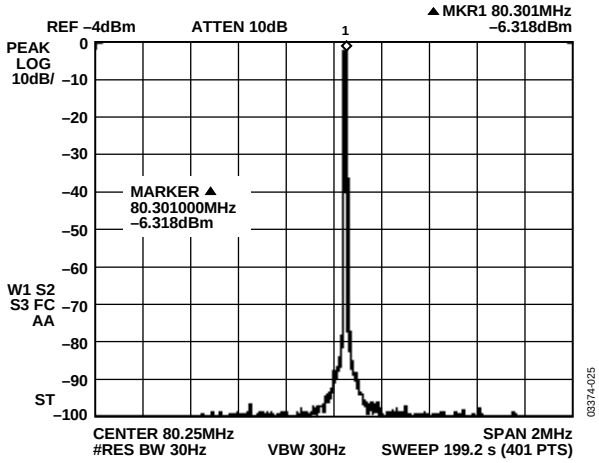


Figure 14. f_{OUT} = 80.3 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

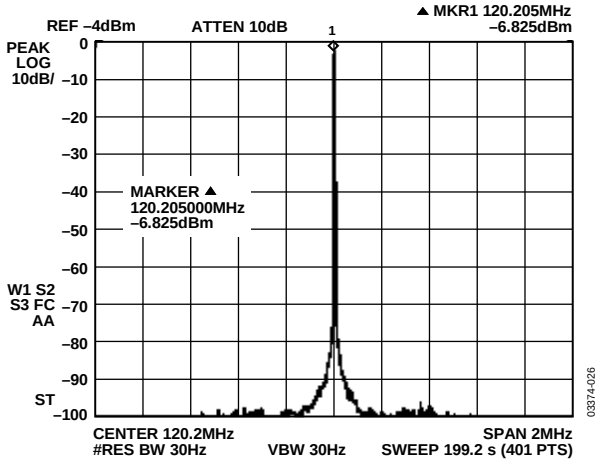


Figure 15. f_{OUT} = 120.2 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

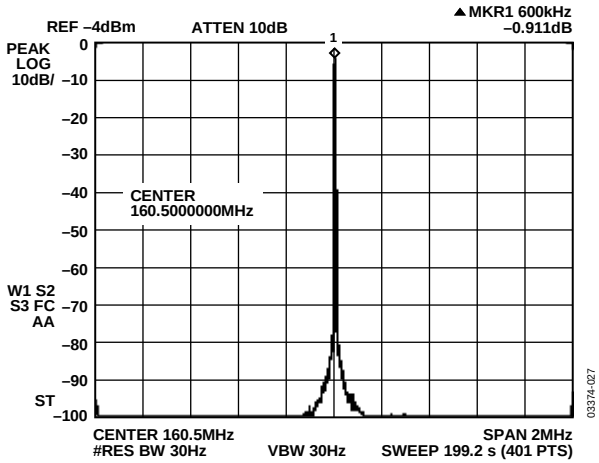


Figure 16. f_{OUT} = 160 MHz, f_{CLK} = 400 MSPS, NBSFDR, ±1 MHz

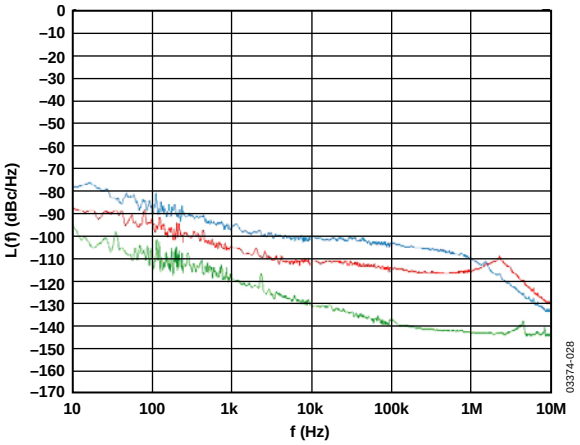


Figure 17. Residual Phase Noise with f_{OUT} = 159.5 MHz, f_{CLK} = 400 MSPS; PLL Bypassed (Green), PLL Set to 4× (Red), and PLL Set to 20× (Blue)

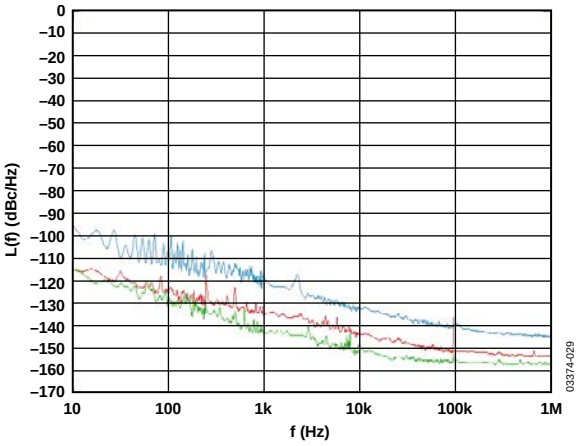


Figure 18. Residual Phase Noise with f_{OUT} = 9.5 MHz, f_{CLK} = 400 MSPS; PLL Bypassed (Green), PLL Set to 4× (Red), and PLL Set to 20× (Blue)

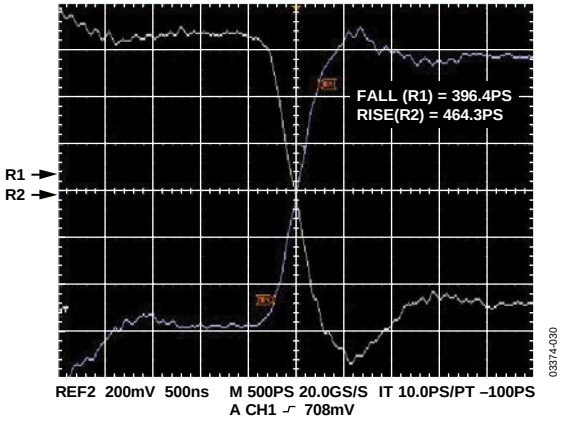


Figure 19. Comparator Rise and Fall Time at 160 MHz

THEORY OF OPERATION

COMPONENT BLOCKS

REFCLK Input

The AD9954 supports several methods for generating the internal system clock. An on-chip oscillator circuit is available for initiating the low frequency reference signal by connecting a crystal to the clock input pins. The system clock can be generated using an internal, PLL-based reference clock multiplier, allowing the part to operate with a low frequency clock source while still providing a high sample rate for the DDS and DAC. For best phase noise performance, a clean, stable clock with a high slew rate should be used to drive the REFCLK pin and bypass the multiplier.

The available modes are configured using the CLKMODESELECT pin, CFR1<4> and CFR2<7:3>. Note that the CLKMODESELECT pin is a 1.8 V logic only and does not apply to 3.3 V logic. Pulling CLKMODESELECT high enables the on-chip crystal oscillator circuit. With the on-chip oscillator enabled, users of the AD9954 connect an external crystal to the REFCLK and $\overline{\text{REFCLK}}$ inputs to produce a low frequency reference clock (see Table 1 for the crystal frequency range supported). The signal generated by the oscillator is buffered, and then delivered to the rest of the chip. This buffered signal is provided on the CRYSTAL OUT pin.

When the internal oscillator is disabled, an external oscillator must provide the REFCLK and/or $\overline{\text{REFCLK}}$ signals. For differential operation, these pins are driven with complementary signals. For single-ended operation, a 0.1 µF capacitor should be connected between the unused pin and the analog power supply. With the capacitor in place, the clock input pin bias voltage is 1.35 V. Table 5 summarizes the clock modes of operation. Note the PLL multiplier is controlled via the CFR2<7:3> bits, independent of the CFR1<4> bit.

Clock Multiplier

An on-board PLL allows multiplication of the REFCLK frequency. The multiplication factor is set using CFR2<7:3>. When programmed for values ranging from 0x04 to 0x14 (decimal 4 to 20), the PLL multiplies the REFCLK input frequency by the programmed value. The user must consider the specified maximum frequency for the PLL when programming. If the multiplication factor is changed, the user must allocate time to allow the PLL to lock (approximately 1 ms).

The PLL is bypassed by programming a value outside the range of 4 to 20 (decimal). When bypassed, the PLL is shut down to conserve power.

The VCO in the PLL has a selectable frequency range. Use the VCO

range bit (CFR2<2>) to set the appropriate range.

The PLL in the clock multiplier has a loop filter comprised of on-chip components as well as external components. Recommended values for the external resistor/capacitor are provided in Table 4.

Table 4. External Loop Filter Components for Clock Multiplier

Multiply Value	Resistor Value	Capacitor Value (µF)
4×	0 Ω	0.1
10×	1 kΩ	0.1
20×	243 Ω	0.01

DAC Output

Unlike many DACs, the DAC output on the AD9954 is referenced to AVDD, not AGND.

Two complementary outputs provide a combined full-scale output current (I_{OUT}). Differential outputs reduce the amount of common-mode noise that may be present at the DAC output, resulting in a better signal-to-noise ratio. The full-scale current is controlled by means of an external resistor (R_{SET}) connected between the DAC_R_{SET} pin and the DAC ground pin (Pin 49, the exposed paddle). The full-scale current is proportional to the resistor value by the equation

$$R_{SET} = \left(39.19/I_{OUT}\right)\Omega$$

The maximum full-scale output current of the combined DAC outputs is 15 mA. Limiting the output to 10 mA maximum provides the best spurious-free dynamic range (SFDR) performance. The DAC output compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range result in excessive DAC distortion and could potentially damage the DAC output circuitry. Proper attention should be paid to the load termination to keep the output voltage within this compliance range.

Table 5. Clock Input Modes of Operation

CFR1<4>	CLKMODESELECT	CFR2<7:3>	Oscillator Enabled?	System Clock	Frequency Range (MHz)
Low	High	4 ≤ M ≤ 20	Yes	$f_{CLK} = f_{OSC} \times M$	$80 < f_{CLK} < 400$
Low	High	M < 4 or M > 20	Yes	$f_{CLK} = f_{OSC}$	$20 < f_{CLK} < 30$
Low	Low	4 ≤ M ≤ 20	No	$f_{CLK} = f_{OSC} \times M$	$80 < f_{CLK} < 400$
Low	Low	M < 4 or M > 20	No	$f_{CLK} = f_{OSC}$	$10 < f_{CLK} < 400$
High	X	X	No	$f_{CLK} = 0$	N/A

Comparator

Some applications (for example, clocking) prefer a square-wave signal rather than a sine wave. In support of such applications, the AD9954 includes an on-chip comparator. The comparator has a bandwidth greater than 200 MHz and a common-mode input range of 1.3 V to 1.8 V. The comparator can be turned off to reduce power consumption using the comparator power-down bit, CFR1<6>.

Frequency Accumulator

This block is used for linear sweep mode; transitioning from the start frequency (F0) to the terminal frequency (F1) is not instantaneous but instead is implemented in a swept or ramped fashion. This frequency ramping is accomplished by stepping through intermediate frequencies between F0 and F1.

The linear sweep block uses the falling and rising delta frequency tuning words, the falling and rising delta frequency ramp rates, and the frequency accumulator. The Linear Sweep Enable Bit CFR1<21> enables the linear sweep block. The linear sweep no dwell bit establishes the action to be performed upon reaching the terminal frequency in a sweep. See the Modes of Operation section for more details.

DDS Core

The output frequency (f_O) of the DDS is a function of the frequency of system clock (SYSCLK), the value of the frequency tuning word (FTW), and the capacity of the phase accumulator (2^{32}, in this case). The exact relationship is given below with f_S defined as the frequency of SYSCLK.

$$f_O = (FTW)(f_S)/2^{32} \text{ with } 0 \le FTW \le 2^{31}$$

$$f_O = f_S \times (1 - (FTW/2^{32})) \text{ with } 2^{31} < FTW < 2^{32} - 1$$

Each system clock cycle, the FTW is added to the value previously held in the phase accumulator. The value at the output of the phase accumulator is then summed with a user-defined, 14-bit phase offset value (POW). The most significant 19 bits of that summation are then translated to an amplitude value via the cos(x) functional block. Truncation of the LSBs is implemented to reduce the power consumption of the DDS core. This truncation does not reduce frequency resolution.

In certain applications, it is desirable to have the ability to force the output signal to zero phase. Simply setting the FTW to 0 does not accomplish this; it only stalls the core at its current phase value. A control bit is provided to force the phase accumulator output to zero.

At power-up, the clear phase accumulator bit is set to Logic 1, but the buffer memory for this bit is cleared (Logic 0). Therefore, upon power-up, the phase accumulator remains clear until the first I/O UPDATE is issued. I/O UPDATE transfers data from the input buffers to the active control registers. See the Functionality of the SYNC_CLK and I/O UPDATE section for more details.

Frequency Tuning Word Mux

As shown in Figure 2, there are three sources for the FTW that are fed to the DDS core as the seed value for the phase accumulator: a frequency accumulator, the static RAM, and the registers of the control logic.

For applications where a static output frequency or more than four predefined output frequencies need to be switched between, in some variable or undefined order, the primary method of setting the FTW is by programming the desired value into the FTW0 register.

For applications where up to four specific sets of FTWs, or pre-defined series of FTWs are needed, the on-board RAM can be programmed with the desired FTWs, and the profile pins can be used to toggle between those sets/series.

For applications where a steady sweeping of frequency is desired, a second frequency accumulator is provided. The seed value and minimum/maximum numbers for the frequency accumulator are user programmable, although certain rules must be followed to avoid overflowing that accumulator.

Phase Offset Word Mux

As shown in Figure 2, there are two sources for the POW that are fed to the DDS core as an adder to the output of the phase accumulator: the static RAM and the registers of the control logic. Using this feature enables synchronization of the DDS output to other system signals as well as phase modulation.

For applications where a static output phase or more than four predefined output phases need to be switched between, in some variable or undefined order, the primary method of setting the POW is by programming the desired value into the POW0 register.

For applications where up to four specific sets of POWs, or predefined series of POWs are needed, the on-board RAM can be programmed with the desired POWs, and the profile pins can be used to toggle between those sets/series.

The phase offset formula is

$$\Phi = \left(\frac{\text{POW}}{2^{14}}\right) \times 360°$$

A digital delay block exists in the phase offset programming path to ensure matched latency with changes to the frequency tuning word. This enables users to easily program the device to change from one combined phase/frequency combination to another smoothly and seamlessly.

Continuous and Clear-and-Release Frequency and Phase Accumulator Clear Functions

The AD9954 allows for a continuous zeroing of the frequency sweep logic and the phase accumulator as well as a clear and release or automatic zeroing function. The auto clear bits are CFR1<14:13>. The continuous clear bits are CFR1<11:10>.

Clear-and-Release Function

When set for auto clearing, the corresponding accumulator is cleared and then begins to accumulate again upon receipt of an I/O update or change on one of the profile pins. This is repeated for every subsequent I/O update or change on one of the profile pins until the appropriate autoclear control bit is cleared. It is perfectly valid to have one accumulator set to autoclearing and the other set to continuous clear.

Amplitude Control Options

Shaped On-Off Keying

The shaped on-off keying function is enabled/disabled using the OSK enable bit (CFR1<25>). This function allows the user to control the ramp-up and ramp-down time when turning the DAC on or off. This function is primarily used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data.

Both auto and manual shaped on-off keying modes are supported. CFR1<24> is used to select between auto and manual on-off keying modes. Figure 20 shows the block diagram of the OSK circuitry.

Autoshaped On-Off Keying Mode Operation

When autoshaped on-off keying mode is enabled, a single-scale factor is internally generated and applied to the multiplier input for scaling the output of the DDS core block (see Figure 20). The scale factor is the output of a 14-bit counter that increments/decrements at a rate determined by the contents of the 8-bit output ramp rate register. The scale factor increments if the OSK pin is high and decrements if the OSK pin is low. The scale factor is an unsigned value; all 0s multiply the DDS core output by 0 (decimal), and 0x3FFF multiplies the DDS core output by 16,383 (decimal).

Table 6 details the increment/decrement step size of the internally generated scale factor per the ASF<15:14> bits.

Note that the maximum amplitude allowed is limited by the contents of the amplitude scale factor register, allowing the user to ramp to a value less than full scale.

Table 6. Autoscale Factor Internal Step Size

ASF<15:14> (Binary)	Increment/Decrement Size
00	1
01	2
10	4
11	8

OSK Ramp Rate Timer

The OSK ramp rate timer is a loadable down counter, which generates the clock signal to the 14-bit counter that generates the internal scale factor. The ramp rate timer is loaded with the value of the autoscale factor register (ASFR) every time the counter reaches 1 (decimal). This load and countdown operation continues for as long as the timer is enabled, unless the timer is forced to load before reaching a count of 1.

If the load ARR control bit (CFR1<26>) is set, the ramp rate timer is loaded upon an I/O update, upon a change in profile input, or upon reaching a value of 1. The ramp timer can be loaded before reaching a count of 1 by three methods.

The first method is by toggling the OSK pin or sending a rising edge to the I/O UPDATE pin (or changing the state of a profile pin). For this method, the ASFR value is loaded into the ramp rate timer, which then proceeds to count down as normal.

The second method is if the load ARR control bit (CFR1<26>) is set and an I/O update (or change in profile) is issued.

The last method is by setting the sweep enable bit. This switches from inactive autoshaped on-off keying mode to the active autoshaped on-off keying mode.

Manual Shaped On-Off Keying Mode Operation

When configured for manual shaped on-off keying, the content of the ASFR sets the scale factor for the data path

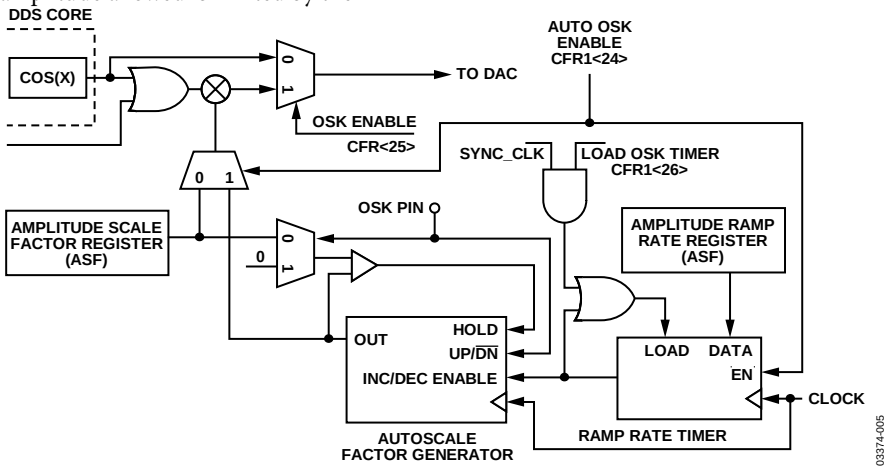


Figure 20. On-Off Shaped Keying, Block Diagram

MODES OF OPERATION

Single-Tone Mode

In single-tone mode, the DDS core uses a static tuning word. Whatever value is stored in FTW0 is supplied to the phase accumulator. This value can only be changed manually by writing a new value to FTW0 and then by issuing an I/O update. Phase adjustments are made using the phase offset register.

RAM-Controlled Modes of Operation

Three important points apply to the RAM-controlled modes:

- The user must ensure that the beginning address is lower than the final address.
- Changing profiles or issuing an I/O update automatically terminates the current sweep and starts the next sweep, unless otherwise stated.
- Setting the RAM destination bit true such that the RAM output drives the phase offset adder is valid. While the sections that follow describe frequency sweeps, phase sweep operation is also available. The RAM destination bit (CFR1<30>) controls whether the RAM output drives the phase accumulator (frequency) or the phase offset adder (phase).

The AD9954 offers five modes of RAM-controlled operation (see Table 7).

Table 7. RAM Modes of Operation

RSCW<7:5> (Binary)	Mode	Notes
000	Direct Switch	No sweeping, profiles valid, no dwell ignored
001	Ramp Up	Sweeping, profiles valid, no-dwell valid
010	Bidirectional Ramp	Sweeping, PS0 is a direction control pin, no-dwell ignored
011	Continuous Bidirectional Ramp	Sweeping, profiles valid, no-dwell ignored
100	Continuous Recirculation	Sweeping, profiles valid, no-dwell ignored
101, 110, 111	Invalid mode	Default to direct switch

Direct Switch Mode

Direct switch mode enables frequency shift keying (FSK) or phase shift keying (PSK) modulation. The AD9954 is programmed for direct switch using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 000(b). This mode simply reads the RAM contents at the RAM segment beginning address for the current profile. No address ramping occurs in this mode.

To perform 4-tone shift keying, the user programs each RAM segment control word for direct switch mode and a unique beginning address value. Program the RAM enable and RAM destination bits (CFR1<31:30>) to enable the RAM and direct the RAM output to be the FTW (FSK) or the POW (PSK). The PS1 and PS0 inputs are the 4-tone FSK/PSK data inputs. When the profile is changed, the data stored at the new profile is loaded into either the phase accumulator (FSK) or the phase offset adder (PSK). When set for PSK, Bits<17:0> of the RAM output are unused when the RAM destination bit is set. Two-tone shift keying only uses one profile pin.

Ramp-Up Mode

Ramp-up mode, in conjunction with the segmented RAM capability, allows up to four different sweep profiles to be programmed into the AD9954. The AD9954 is programmed for ramp-up mode by enabling the RAM using the RAM enable bit (CFR1<31>) and programming the RAM mode control bits of each profile to be used to 001(b).

When a sweep is initiated (via an I/O update or change in profile bits), the RAM address generator loads the RAM segment beginning address bits of the current RSCW, driving the RAM output from this address, and the ramp rate timer loads the RAM segment address ramp rate bits. When the ramp rate timer finishes a cycle, the RAM address generator increments to the next address, the timer reloads the ramp rate bits and begins a new countdown cycle. This sequence continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. At this point, the next state is dependent upon whether no-dwell mode is active. See the no-dwell bit (CFR1<2>) in the register maps (see Table 12 and Table 13).

In this mode, asymmetrical FSK modulation can be implemented by configuring the RAM for two segments, and using the PS0 pin as the data input.

Bidirectional Ramp Mode

Bidirectional ramp mode allows the AD9954 to offer a symmetrical sweep between two frequencies using the PS0 signal as the control input. The AD9954 is programmed for bidirectional ramp mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 010(b). PS1 input is ignored; the PS0 input is the ramp direction indicator. The memory is not segmented, using only one beginning and one final address. The address registers for controlling RAM are located in the RAM segment control word (RSCW) associated with Profile 0.

Upon entering this mode (via an I/O update or changing the PS0 pin), the RAM address generator loads the RAM segment beginning address bits of RSCW0 and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins counting down to 1. When the timer reaches zero, the RAM address is incremented if PS0 is high and decrements if PS0 is low. Toggling the PS0 pin does not cause the device to generate an internal I/O update; transfers of data from the I/O buffers to the internal registers are only initiated by a rising edge on the I/O UPDATE pin.

RAM address control is now a function of the PS0 input. When polarity of the PS0 bit is changed, the RAM address generator increments/decrements to the next address and the ramp rate timer is reloaded. As in the ramp-up mode, this sequence continues until the RAM address generator has incremented/decremented to an address equal to the final/beginning address as long as the PS0 input remains high/low. Once the final/beginning address is reached, the sweep stalls until the polarity on PS0 is changed.

All data in the RAM segment control words associated with Profile 1, Profile 2, and Profile 3 are ignored. Only the information in the RAM segment control word for Profile 0 is used to control the RAM.

Continuous Bidirectional Ramp Mode

Continuous bidirectional ramp mode allows the AD9954 to offer an automatic, symmetrical sweep between two frequencies. The AD9954 is programmed for continuous bidirectional ramp mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 011(b). In general, this mode is identical in control to the bidirectional ramp mode, except the ramp up and down is automatic (no external control via the PS0 input), and switching profiles are valid. This mode enables generation of an automatic saw tooth sweep characteristic.

Upon entering this mode (via an I/O update or changing the PS1 or PS0 pins), the RAM address generator loads the RAM segment beginning address bits of the current RSCW and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins counting down to 1. When the ramp rate timer completes the countdown, the RAM address generator increments to the next address, and the timer reloads the ramp rate bits and continues counting down. This continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. Upon reaching this final address, the RAM address generator begins decrementing each time the ramp rate timer completes a countdown cycle until it reaches the RAM segment beginning address. Upon reaching the beginning address, the entire sequence repeats until a new mode is selected.

Continuous Recirculation Mode

Continuous recirculation mode allows the AD9954 to offer an automatic, continuous unidirectional sweep between two frequencies. The AD9954 is programmed for continuous recirculation mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 100(b).

Upon entering this mode (via an I/O update or changing Pin PS1 or Pin PS0), the RAM address generator loads the RAM segment beginning address bits of the current RSCW and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins to count down to 1. When the ramp rate timer completes a cycle, the RAM address generator increments to the next address, and the timer reloads the ramp rate bits and continues counting down. This sequence continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. Upon reaching this terminal address, the RAM address generator reloads the RAM segment beginning address bits and the sequence repeats until a new mode is selected.

Internal Profile Control

The AD9954 offers a mode in which a composite frequency sweep can be built with software-programmable timing control. Internal profile control capability disengages the PS1 pin and the PS0 pin and enables the AD9954 to take control of switching between profiles. Modes are defined that allow continuous or single-burst profile switches for three combinations of profile selection bits (see Table 8). Internal profile control mode is engaged using Bits CFR1<29:27> per Table 8 Internal profile control is only valid when the device is operating in RAM mode. There is no internal profile control for linear sweeping operations.

When the internal profile control mode is engaged, the RAM segment mode control bits are ignored; the device operates all profiles in ramp-up mode. Switching between profiles occurs when the RAM address generator has exhausted the memory contents for the current profile.

Table 8. Internal Profile Control

CFR1<29:27> (Binary)	Mode Description
000	Internal control inactive
001	Internal control active, single-burst, activate Profile 0, then Profile 1, then stop
010	Internal control active, single-burst, activate Profile 0, then Profile 1, then Profile 2, then stop
011	Internal control active, single-burst, activate Profile 0, then Profile 1, then Profile 2, then Profile 3, then stop
100	Internal control active, continuous, activate Profile 0, then Profile 1, then Loop Starting 0
101	Internal control active, continuous, activate Profile 0, then Profile 1, then Profile 2, then Loop Starting 0
110	Internal control active, continuous, activate Profile 0, then Profile 1, then Profile 2, then Profile 3, and then Loop Starting 0
111	Invalid

A single-burst mode is one in which the composite sweep is executed once. For example, assume the device is programmed for ramp-up mode and the CFR1<29:27> bits are written to Logic 010(b). Upon receiving an I/O update, the internal control logic signals the device to begin executing the ramp-up mode sequence for Profile 0. Upon reaching the RAM segment final address value for Profile 0, the device jumps to the beginning address of Profile 1 and begins executing that ramp-up sequence. Upon reaching the RAM segment final address value for Profile 1, the device jumps to the beginning address of Profile 2 and begins executing that ramp-up sequence. When the RAM segment final address value for Profile 2 is reached, the sequence is over and the composite sweep has completed. Issuing another I/O update restarts the burst process.

A continuous internal profile control mode is one in which the composite sweep is continuously executed for as long as the device is programmed into that mode. Using the previous example, except programming the CFR1<29:27> bits to Logic 101(b), the operation would be identical until the RAM segment final address value for Profile 2 is reached. At this point, instead of stopping the sequence, the device jumps back to the beginning address of Profile 0 and continues sweeping.

Linear Sweep Mode

The AD9954 is placed in linear sweep mode using the Linear Sweep Enable Bit CR1<21>. PS1 must be tied low. When in linear sweep mode, the AD9954 output frequency ramps up from a starting frequency, programmed by FTW0 to a finishing frequency FTW1, or down from FTW1 to FTW0. The delta frequency tuning words and the ramp rate word determine the rate of this ramping. The Linear Sweep No-Dwell Bit CFR1<2> controls the behavior of the device upon reaching the final frequency.

When PS0 is high, the 32-bit rising delta frequency tuning word (RDFTW) is the seed value for the frequency accumulator, it ramps from FTW0 to FTW1 and the RSRR register is loaded into the sweep rate timer. When the timer counts down to one, the frequency accumulator cycles once, increasing by the seed value. This accumulation of the RDFTW at the rate given by the ramp rate (RSRR) continues until the output of the frequency adder is equal to the FTW1 register value, or PS0 is pulled low.

When PS0 is low, the 32-bit falling delta frequency tuning word (FDFTW) is the seed value for the frequency accumulator, it ramps down from FTW1 to FTW0 and the FSRR register is loaded into the sweep rate timer. When the timer counts down to one, the frequency accumulator cycles once, decreasing by the seed value. This accumulation of the FDFTW at the rate given by the ramp rate (FSRR) continues until the output of the frequency adder is equal to the FTW0 register value, or PS0 is pulled high.

Pin PS0 controls the direction of the sweep, rising to FTW1 or falling to FTW0. Upon reaching the destination frequency, the AD9954 linear sweep function either holds at the destination frequency until the state on PS0 is changed or immediately returns to the initial frequency, FTW0, depending on the state of the Linear Sweep No-Dwell Bit CFR1<02>. While operating in linear sweep mode, toggling PS0 does not cause the device to generate an internal I/O update. When PS0 is acting as the sweep direction indicator, any transfer of data from the I/O buffers to the internal registers can only be initiated by a rising edge on the I/O UPDATE pin.

The linear sweep function of the AD9954 requires the lowest frequency to be loaded into the FTW0 register and the highest frequency into the FTW1 register. For piece-wise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in process.

After a reset, the device is initially in single-tone mode. The programming steps to operate in linear sweep mode are:

1. PS1:0 = 00.
2. Set the linear sweep enable bit (CFR1<21>) and set or clear the linear sweep no-dwell bit (CFR1<2>) as desired.
3. Program the rising and falling delta frequency tuning words and ramp rate values.
4. Program the lower and higher output frequencies into the FTW0 and FTW1 registers, respectively.
5. Apply an I/O update to move this data into the registers (the instantaneous output frequency is FTW0).
6. Change the PS0 input as desired to sweep between the lower to higher frequency and back.

Figure 21 depicts a typical frequency ramping operation. The device initially powers up in single-tone mode. The profile inputs are low, setting FTW0 as the seed value for the phase accumulator. The user then writes to the linear sweep enable bit, the rising and falling delta frequency tuning words, and ramp rates via the serial port (Point A in Figure 21. In this example, the linear sweep no-dwell bit is cleared (CFR1<2>).

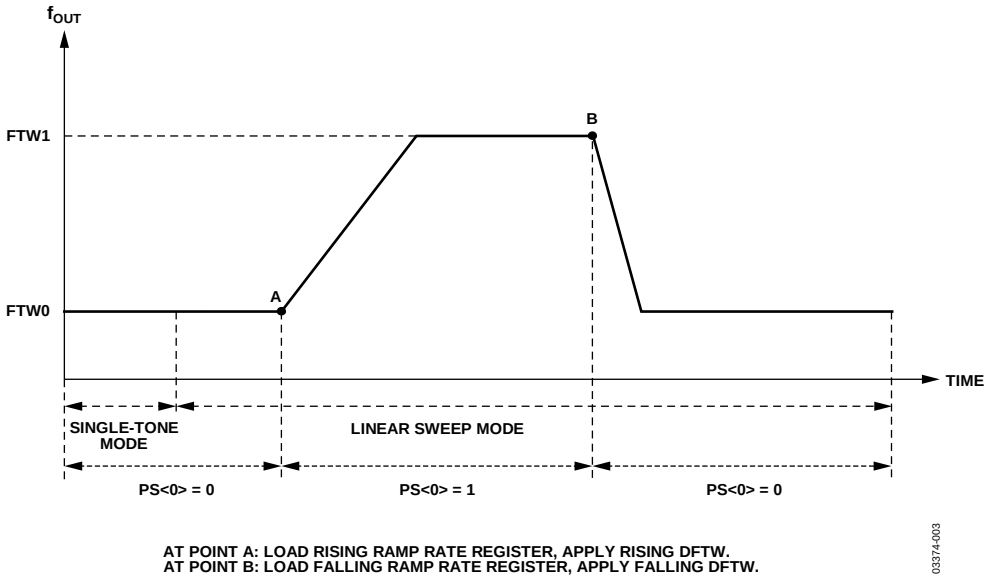


Figure 21. Linear Sweep Frequency Plan

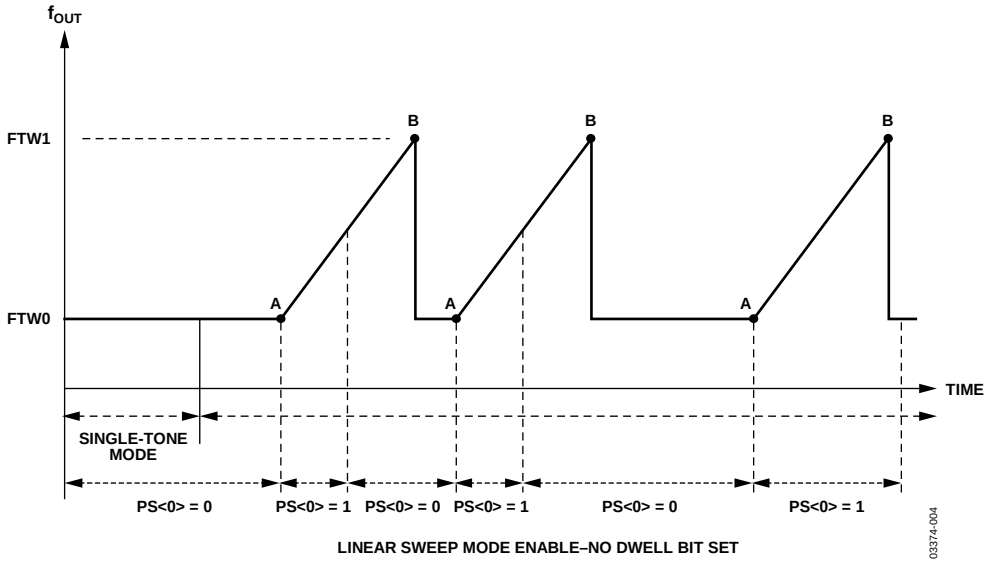


Figure 22. Linear Sweep Using No-Dwell Frequency Plan

Linear Sweep No-Dwell Feature

See CFR1<2> in the register maps (see Table 12 and Table 13) for general details of the no-dwell mode. Figure 22 depicts the linear sweep mode operation when the linear sweep no-dwell bit is set. The Label A points indicate where a rising edge on PS0 is detected; the Label B points indicate where the AD9954 has determined f_{OUT} has reached the terminal frequency and automatically returns to the starting frequency. Note that in this mode, only sweeps from FTW0 to FTW1 using the positive linear sweep control word are supported. Toggling PS0 from 1 to 0 neither initiates a falling sweep when the no-dwell bit is set, nor interrupts a positive sweep already underway.

Resetting the Ramp Rate Timer

The ramp timer can be reset before reaching a count of 1 by three methods.

Method one is by changing the PS0 input pin. When the PS0 input pin toggles from 0 to 1, the RSRRW value is loaded into the ramp rate timer, which then proceeds to countdown as normal. When the PS0 input pin toggles from 0 to 1, the falling sweep ramp rate word (FSRRW) value is loaded into the ramp rate timer, which then proceeds to countdown as normal.

The second method uses the LOAD SRR @ I/O UD bit (CFR1<15>), see Table 12 for details.

The last method in which the sweep ramp rate timer can be reset is changing from inactive linear sweep mode to active linear sweep mode using the linear sweep enable bit (CFR1<21>).

For methods two and three, the ramp rate timer loads a value determined by the state of PS0 (0 = FSRRW, 1 = RSRRW).

Power-Down Functions of the AD9954

The AD9954 supports an externally controlled (or hardware) power-down feature as well as software-programmable power-down bits capable of individually powering down specific unused circuit blocks.

Software-controlled power-down enables individual powering down of the DAC, comparator, PLL, input clock circuitry, and the digital logic (CFR1<7:4>). With the exception of CFR1<6>, these bits are superseded when the externally controlled power-down pin (PWRDWNCTL) is high. External power-down control is supported on the AD9954 via the PWRDWNCTL input pin. When the PWRDWNCTL input pin is high, the AD9954 enters a power-down mode based on the CFR1<3> bit. When the PWRDWNCTL input pin is low, it operates normally. See CFR1<3> in Table 12 for details.

Table 9 details the logic level for each power-down bit that drives out of the AD9954 core logic to the analog section and the digital clock generation section of the chip for the external power-down operation.

Table 9. Power-Down Control Functions

Control	Mode Active	Description
PWRDWNCTL = 0, CFR1<3> don't care	Software control	Digital power-down = CFR1<7> Comparator power-down = CFR1<6> DAC power-down = CFR1<5> Clock input power-down = CFR1<4>
PWRDWNCTL = 1, CFR1<3> = 0	External control, fast recovery power-down mode	Digital power-down = 1'b1 Comparator power-down = 1'b0 or CFR1<6> DAC power-down = 1'b0 Clock input power-down = 1'b0
PWRDWNCTL = 1, CFR1<3> = 1	External control, full power-down mode	Digital power-down = 1'b1 Comparator power-down = 1'b1 DAC power-down = 1'b1 Clock input power-down = 1'b1

SYNCHRONIZATION—REGISTER UPDATES (I/O UPDATE)

Functionality of the SYNC_CLK and I/O UPDATE

Data into the AD9954 is synchronous to the SYNC_CLK signal (supplied externally to the user on the SYNC_CLK pin). The I/O UPDATE pin is sampled on the rising edge of the SYNC_CLK.

Internally, SYSCLK is fed to a divide-by-four frequency divider to produce the SYNC_CLK signal. The SYNC_CLK signal is made available to the system on the SYNC_CLK pin. This enables synchronization of external hardware with the device's internal clocks. This is accomplished by providing the SYNC_CLK signal as an output that external hardware can then use to synchronize against.

The I/O update signal coupled with SYNC_CLK is used to transfer internal buffer contents into the control registers. The combination of the SYNC_CLK pin and the I/O UPDATE pin provides the user with constant latency relative to SYSCLK and ensures phase continuity of the analog output signal when a new tuning word or phase offset value is asserted.

Figure 23 and Figure 24 demonstrate an I/O update timing cycle and synchronization.

Synchronization logic notes include the following:

- The I/O update signal is edge detected to generate a single-cycle clock signal that drives the register bank flops. The I/O update signal has no constraints on duty cycle. The minimum low time on I/O update is one SYNC_CLK clock cycle.
- The I/O UPDATE pin is set up and held around the rising edge of SYNC_CLK. Setup and hold time specifications can be found in Table 2.

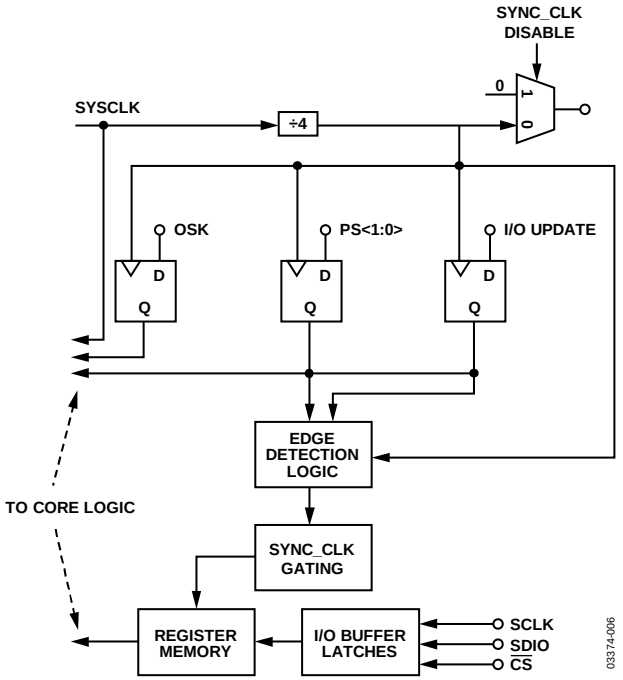


Figure 23. I/O Synchronization Block Diagram

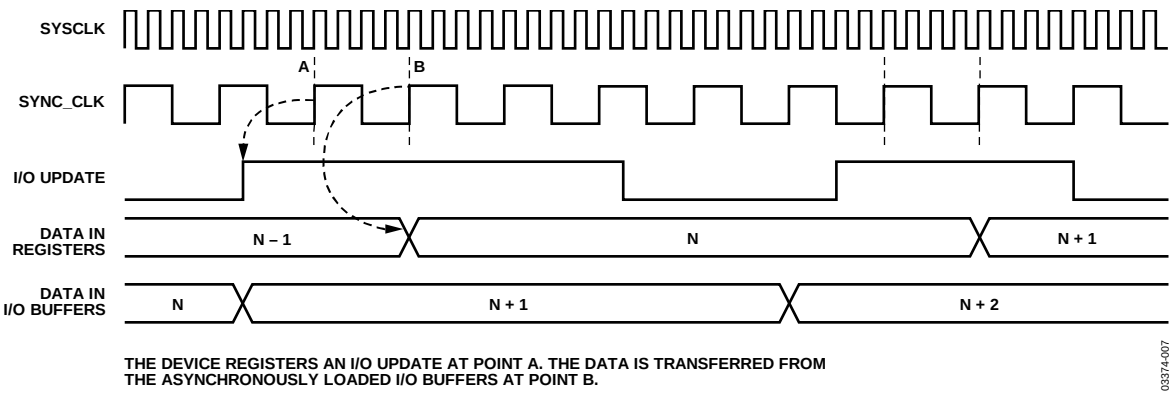


Figure 24. I/O Synchronization Timing Diagram

Synchronizing Multiple AD9954s

There are three modes of synchronization available to the user: an automatic synchronization mode, a software-controlled manual synchronization mode, and a hardware-controlled manual synchronization mode. The following requirements apply to all modes. First, all units must share a common clock source. Trace lengths and path impedance of the clock tree must be designed to keep the phase delay of the different clock branches as closely matched as possible. Second, the I/O update signal's rising edge must be provided synchronously to all devices being synchronized. Finally, the DVDD_I/O supply should be set to 3.3 V for all devices that are to be synchronized. AVDD and DVDD should be left at 1.8 V.

In automatic synchronization mode, one device is chosen as a master, the other device(s) is slaved to this master. All slaves automatically synchronize their internal clocks to the SYNC_CLK output signal of the master device. Use the automatic synchronization bit (CFR1<23>) to configure each slave. Connect the SYNC_IN input(s) to the master SYNC_CLK output. Slave devices continuously update the phase relationship of their SYNC_CLK until it is in phase with the SYNC_IN input. The high speed sync enhancement enable bit (CFR2<11>) must be programmed correctly.

In software manual synchronization mode, the user can force the device to advance the SYNC_CLK rising edge one SYSCLK cycle (¼ SYNC_CLK period). Manual synchronization mode is established using the slave device's software manual synchronization bit (CFR1<22>). See the bit description in Table 12 for more details.

In hardware manual synchronization mode, the SYNC_IN input pin is configured such that it now advances the rising edge of the SYNC_CLK signal each time the device detects a rising edge on the SYNC_IN pin. Hardware manual synchronization mode is established using the hardware manual synchronization bit (CFR2<10>). See the bit description in Table 12 for more details.

Using a Single Crystal to Drive Multiple AD9954 Clock Inputs

The AD9954 crystal oscillator output signal is available on the CRYSTAL OUT pin, enabling one crystal to drive multiple AD9954s. To drive multiple AD9954s with one crystal, the CRYSTAL OUT pin of the AD9954 using the external crystal should be connected to the REFCLK input of the other AD9954.

The CRYSTAL OUT pin must be enabled using the CRYSTAL OUT Pin Active Bit CFR2<9>. The drive strength of the CRYSTAL OUT pin is fairly low; therefore, the signal should be buffered if multiple loads are being driven.

RAM

The AD9954 incorporates a block of SRAM. The RAM is a bidirectional single port. Read and write operations cannot occur simultaneously. Write operations to the serial I/O port take precedence; therefore, if an attempt to write to RAM is made during a read operation, the read operation is halted. The RAM is configurable using the RAM Segment Control Word<7:5> and data in the control function register.

Using the RAM enable bit (CFR1<31>), the RAM output can be enabled to drive the input to either the phase accumulator or the phase offset adder; the RAM destination bit (CFR1<30>) sets the routing. When the RAM output drives the phase accumulator, the phase offset word (POW, Address 0x05) drives the phase-offset adder. Conversely, when the RAM output drives the phase-offset adder, the frequency tuning word (FTW, Address 0x04) drives the phase accumulator. When CFR1<31> disables the RAM, it is inactive unless being written to via the serial port. The RAM is mapped into one of four profiles determined by the PS1 and PS0 input pins. Note that these profiles may overlap. For example, Profile 0 may use RAM Address Location 0 to Address Location 12, and Profile 1 may use RAM Address Location 5 to Address Location 20, and so forth.

All RAM write or read operations to/from the RAM are controlled by the PS1 and PS0 input pins and the respective RAM segment control word. To write to the RAM, a RAM segment must be defined in a RAM segment control word. The RAM segment that was defined must then be selected by use of the profile select pins, PS0 and PS1. With the correct RAM segment selected, the special instruction byte of 0xB0 should be sent. When the instruction byte to write to the RAM is sent to the part, the serial port controller immediately polls the corresponding RAM segment control word. From this register, the serial port controller makes note of the start address and the stop address. It then calculates how many entries there are in the segment, and how many bytes of data to expect. After sending the special instruction byte of 0xB0, the user must send all RAM entries for the currently selected profile to the part.

For example, consider a case where RAM Segment 2 begins at Address 21 and ends at Address 120. First, write to RAM Segment Control Word 2 with a starting address of 21, with a stop address of 120, and specify a ramp rate and a mode of operation. Next, set PS1 to 1 and PS0 to 0 to select RAM Segment 2 and then send the instruction byte of 0xB0. The part is now ready to put the first 32-bit word into the RAM at Address 21, to expect 100 32-bit words, and to store the last one at Address 120. It automatically controls sending the data from the serial port to the correct RAM address. Therefore, precede sending 100 32-bit words of data to the part. After the 3200th SCLK cycle, the write operation is complete, and all 100 words are stored in the RAM, from Address 21 to Address 120.

Serial I/O Port

The AD9954 serial port is a flexible, synchronous, serial communications port that easily interfaces to many industry-standard microcontrollers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI® and Intel® 8051 SSR protocols.

The interface accesses all registers that configure the AD9954. MSB first and LSB first transfer formats are supported. In addition, the AD9954's serial interface port can be configured as a single pin I/O (SDIO), which allows a 2-wire interface, or two unidirectional pins for in/out (SDIO/SDO), which enables a 3-wire interface. Two optional pins, IOSYNC and $\overline{CS}$, provide further flexibility for system design with the AD9954.

SERIAL PORT OPERATION

With the AD9954, the instruction byte specifies read/write operation and register address. Serial operations on the AD9954 only occur at the register level, they do not occur on the byte level. For the AD9954, the serial port controller recognizes the instruction byte register address and automatically generates the proper register byte address. In addition, the controller expects to access all bytes of that register. It is a requirement that all bytes of a register be accessed during serial I/O operations, with one exception; the IOSYNC function can be used to abort an I/O operation, thereby allowing less than all bytes to be accessed.

There are two phases to a communication cycle with the AD9954. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9954, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9954 serial port controller with information regarding Phase 2, the data transfer cycle. The instruction byte defines whether the upcoming data transfer is a read or a write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9954. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9954 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed. For example, when accessing the Control Function Register 2, which is three bytes wide, Phase 2 requires that three bytes be transferred. If accessing the frequency tuning word, which is four bytes wide, four bytes must be transferred. After transferring all data bytes per the instruction byte, the communication cycle is complete.

At the completion of any communication cycle, the AD9954 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. All data input to the AD9954 is registered on the rising edge of SCLK. All data is driven out of the AD9954 on the falling edge of SCLK. Figure 25 through Figure 28 are provided to aid in understanding the general operation of the AD9954 serial port.

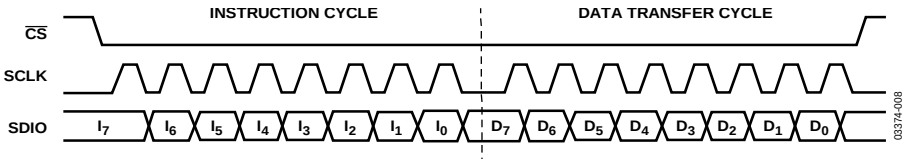


Figure 25. Serial Port Write Timing–Clock Stall Low

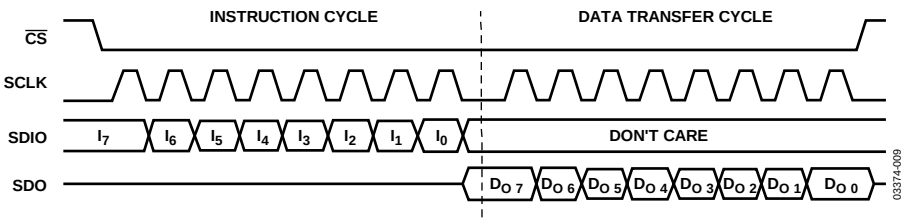


Figure 26. 3-Wire Serial Port Read Timing–Clock Stall Low

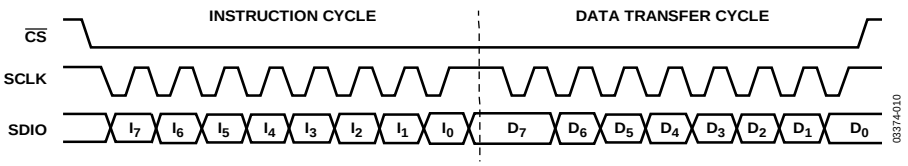


Figure 27. Serial Port Write Timing–Clock Stall High

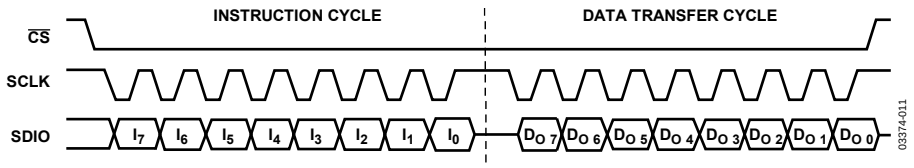


Figure 28. 2-Wire Serial Port Read Timing—Clock Stall High

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9954 and to run internal state machines. SCLK maximum frequency is 25 MHz.

$\overline{CS}$—Chip Select. $\overline{CS}$ is an active low input that enables devices sharing a serial communications line to be individually programmed. The SDO and SDIO pins go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip select can be tied low if it is not needed.

SDIO —Serial Data I/O. Data written to the AD9954 must be sent to this pin. However, this pin can be used as a bidirectional data line. CFR1<9> controls the configuration of this pin.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. When in 2-wire serial programming mode, this pin is set to a high impedance state.

IOSYNC—synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the IOSYNC pin aborts the current communication cycle. After IOSYNC returns low (Logic 0), another communication cycle may begin, starting with the instruction byte write.

MSB/LSB TRANSFERS

The AD9954 serial port can support either MSB first or LSB first data formats. This functionality is controlled by the LSB First Bit CFR1<8>.

For MSB first operation, the serial port controller generates the most significant byte (of the specified register) address first followed by the next lesser significant byte addresses until the I/O operation is complete. All data written to (read from) the AD9954 must be in MSB first order.

If the LSB mode is active, the serial port controller generates the least significant byte address first followed by the next greater significant byte addresses until the I/O operation is complete. All data written to (read from) the AD9954 must be in LSB first order.

Example Operation

As an example, consider the case of writing the amplitude scale factor (ASF) register to a value of 0.5 full scale. First, calculate the binary equivalent of 0.5. As the ASF is 16 bits wide, the hexadecimal equivalent is 0x80. Next, for MSB first format, transmit an instruction byte of 0x02 (serial address of ASF is 00010(b)). From this instruction, the internal controller polls the register at this memory location and notes that the ASF is 2 bytes wide. The serial port controller's state machines sets to 16 and awaits 16 rising edges on the SCLK and 16 bits of data on the SDIO line. Send 16 rising edges on SCLK, and the binary data 10000000 00000000 on the SDIO line.

To write the amplitude scale factor register in LSB first format, the process is the same as in MSB first; however, the data is bit wise inverted on a word-by-word basis. The instruction byte is 0x40. The binary data for the ASF is 00000000 00000001.

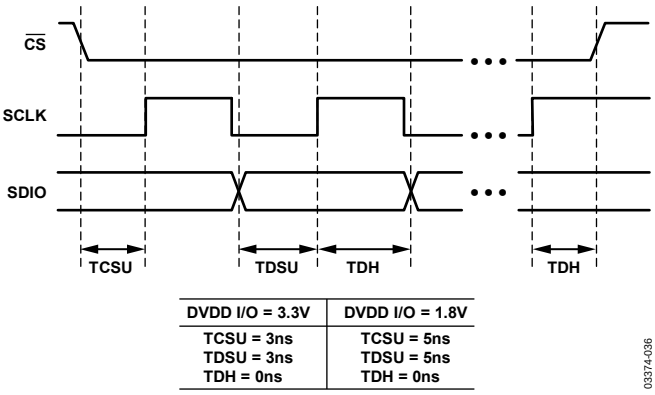


Figure 29. Timing Diagram for Data Write to AD9954

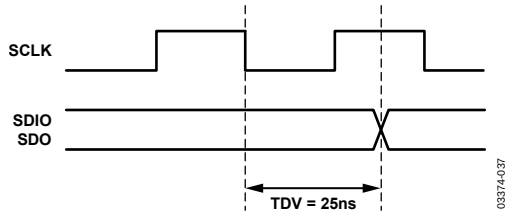


Figure 30. Timing Diagram for Data Read to AD9954

RAM I/O VIA SERIAL PORT

Accessing the RAM via the serial port is identical to any other serial I/O operation except that the number of bytes transferred is determined by the address space between the beginning address and the final address as specified in the current RAM segment control word (RSCW). The final address describes the most significant word address for all I/O transfers and the beginning address specifies the least significant address.

RAM I/O supports MSB/LSB first operation as set using the LSB First Bit CFR1<8>. When in MSB first mode, the first data byte is for the most significant byte of the memory address described by the final address with the remaining three bytes making up the lesser significant bytes of that address. The remaining bytes come in most significant to least significant, destined for RAM addresses generated in descending order

until the final four bytes are written into the address specified as the beginning address. When in LSB first mode, the first data byte is for the least significant byte of the memory (specified by the beginning address) with the remaining three bytes making up the greater significant bytes of that address. The remaining bytes come in least significant to most significant, destined for RAM addresses generated in ascending order until the final four bytes are written into the memory address described by the final address.

The RAM uses Serial Address 01011(b); therefore, the instruction byte to write the RAM is 0x0B, in MSB first notation. As previously mentioned, the RAM addresses generated are specified by the beginning and final address of the RSCW currently selected by Pin PS1 and Pin PS0.

Notes on serial port operation

- The configuration changes made using CFR1<9:8> are implemented immediately upon writing to this register. For multibyte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.
- The system must maintain synchronization with the AD9954 or the internal control logic cannot recognize further instructions. For example, if the system sends an instruction byte that describes writing a 2-byte register, and then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle properly write the first two data bytes into the AD9954, but the next eight rising SCLK edges are interpreted as the next instruction byte. In the case where synchronization is lost between the system and the AD9954, the IOSYNC pin enables the user to reset the AD9954 serial port controller state machine. Any information that is written to the AD9954 registers during a valid communication cycle prior to loss of synchronization and assertion of the IOSYNC pin remain intact.
- Reading a RAM profile requires that the profile select pins, Pin PS1 and Pin PS0, be configured to select the desired profile. When reading a register that resides in one of the profiles, the register address acts as an offset to select one of the registers among the group of registers defined by the profile, while the profile select pins select the appropriate register group.

INSTRUCTION BYTE

The instruction byte contains the following information.

Table 10.

MSB	D6	D5	D4	D3	D2	D1	LSB
R/$\overline{W}$	X	X	A4	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 of the instruction byte defines whether a read or write data transfer occurs after the instruction byte write. Logic High indicates read operation. Logic 0 indicates a write operation.

X, X—Bit 6 and Bit 5 of the instruction byte are don't care.

A4, A3, A2, A1, A0—Bit 4, Bit 3, Bit 2, Bit 1, Bit 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. Addresses for registers can be found in the first column of the register maps (see Table 12 and Table 13).

REGISTER MAPS AND DESCRIPTIONS

The register maps are listed in Table 12 and Table 13. The active register map depends on the state of the linear sweep enable bit; certain registers are remapped depending on which mode the part is operating in. Specifically, Register 0x07, Register 0x08, Register 0x09, and Register 0x0A are affected. Because the linear sweep operation takes precedence over RAM operations, Analog Devices, Inc. recommends that the RAM be disabled using Bit CFR1<31> when linear sweep is enabled by Bit CFR1<21> to conserve power. The serial address numbers associated with each of the registers are in hexadecimal format. Angle brackets <> are used to reference specific bits or ranges of bits. For example, <3> designates Bit 3 and <7:3> designates the range of bits from Bit 7 to Bit 3, inclusive.

Table 11. Register Mapping Based on Linear Sweep Enable Bit

Linear Sweep Enable Bit (CFR1<21>)	Register Map
Cleared (= 0)	RAM Segment Control Words Active
Set (= 1)	Linear Sweep Control Words Active

Table 12. Register Map—When Linear Sweep Enable Bit Is False (CFR1<21> = 0)

Note that the RAM Enable Bit CFR1<31> only activates the RAM itself, not the RAM segment control words.

Register Name (Serial Address)	Bit Range	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value Or Profile
Control Function Register No.1 (CFR1) (0x00)	<7:0>	Digital Power-Down	Comp Power-Down	DAC Power-Down	Clock Input Power-Down	External Power-Down Mode	Linear Sweep No-Dwell	SYNC_CLK Disable	Not Used	0x00
	<15:8>	SRR Load Enable	AutoClr Freq Accum	AutoClr Phase Accum	Sine/ Cosine Select	Clear Freq Accum	Clear Phase Accum	SDIO Input Only	LSB First	0x00
	<23:16>	Automatic Sync Enable	Software Manual Sync	Linear Sweep Enable	Not Used	Not Used	Not Used	Not Used	Not Used	0x00
	<31:24>	RAM Enable	RAM Destination	Internal Profile Control<2:0>			Load ARR Control	OSK Enable	Auto OSK Enable	0x00
Control Function Register No. 2 (CFR2) (0x01)	<7:0>	REFCLK Multiplier					VCO Range	Charge Pump Current<1:0>		0x00
	<15:8>	Not Used				High Speed Sync Enable	Hardware Manual Sync Enable	XTAL OUT Enable	Not Used	0x00
	<23:16>	Not Used								0x18
Amplitude Scale Factor (ASF) (0x02)	<7:0>	Amplitude Scale Factor Register<7:0>								0x00
	<15:8>	Auto Ramp Rate Speed Control<1:0>		Amplitude Scale Factor Register<13:8>						0x00
Amplitude Ramp Rate (ARR) (0x03)	<7:0>	Amplitude Ramp Rate Register<7:0>								0x00
Frequency Tuning Word (FTW0) (0x04)	<7:0>	Frequency Tuning Word No. 0<7:0>								0x00
	<15:8>	Frequency Tuning Word No. 0<15:8>								0x00
	<23:16>	Frequency Tuning Word No. 0<23:16>								0x00
	<31:24>	Frequency Tuning Word No. 0<31:24>								0x00
Phase Offset Word (POW0) (0x05)	<7:0>	Phase Offset Word No. 0<7:0>								0x00
	<15:8>	Not Used<1:0>		Phase Offset Word No. 0<13:8>						0x00
Frequency Tuning Word (FTW1) (0x06)	<7:0>	Frequency Tuning Word No. 1<7:0>								0x00
	<15:8>	Frequency Tuning Word No. 1<15:8>								0x00
	<23:16>	Frequency Tuning Word No. 1<23:16>								0x00
	<31:24>	Frequency Tuning Word No. 1<31:24>								0x00
Profile 0 RAM Segment Control Word No. 0 (RSCW0) (0x07)	<7:0>	RAM Segment 0 Mode Control<2:0>			No-Dwell Active	RAM Segment 0 Beginning Address<9:6>				PS0 = 0 PS1 = 0
	<15:8>	RAM Segment 0 Beginning Address<5:0>						RAM Segment 0 Final Address<9:8>		PS0 = 0 PS1 = 0
	<23:16>	RAM Segment 0 Final Address<7:0>								PS0 = 0 PS1 = 0
	<31:24>	RAM Segment 0 Address Ramp Rate<15:8>								PS0 = 0 PS1 = 0
	<39:32>	RAM Segment 0 Address Ramp Rate<7:0>								PS0 = 0 PS1 = 0

Register Name (Serial Address)	Bit Range	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value Or Profile
Profile 1 RAM Segment Control Word No. 1 (RSCW1) (0x08)	<7:0>	RAM Segment 1 Mode Control<2:0>			No-Dwell Active	RAM Segment 1 Beginning Address<9:6>				PS0 = 1 PS1 = 0
	<15:8>	RAM Segment 1 Beginning Address<5:0>						RAM Segment 1 Final Address<9:8>		PS0 = 1 PS1 = 0
	<23:16>	RAM Segment 1 Final Address<7:0>								PS0 = 1 PS1 = 0
	<31:24>	RAM Segment 1 Address Ramp Rate<15:8>								PS0 = 1 PS1 = 0
	<39:32>	RAM Segment 1 Address Ramp Rate<7:0>								PS0 = 1 PS1 = 0
Profile 2 RAM Segment Control Word No. 2 (RSCW2) (0x09)	<7:0>	RAM Segment 2 Mode Control<2:0>			No-Dwell Active	RAM Segment 2 Beginning Address<9:6>				PS0 = 0 PS1 = 1
	<15:8>	RAM Segment 2 Beginning Address <5:0>						RAM Segment 2 Final Address<9:8>		PS0 = 0 PS1 = 1
	<23:16>	RAM Segment 2 Final Address<7:0>								PS0 = 0 PS1 = 1
	<31:24>	RAM Segment 2 Address Ramp Rate<15:8>								PS0 = 0 PS1 = 1
	<39:32>	RAM Segment 2 Address Ramp Rate<7:0>								PS0 = 0 PS1 = 1
Profile 3 RAM Segment Control Word No. 3 (RSCW3) (0x0A)	<7:0>	RAM Segment 3 Mode Control<2:0>			No-Dwell Active	RAM Segment 3 Beginning Address<9:6>				PS0 = 1 PS1 = 1
	<15:8>	RAM Segment 3 Beginning Address<5:0>						RAM Segment 3 Final Address <9:8>		PS0 = 1 PS1 = 1
	<23:16>	RAM Segment 3 Final Address<7:0>								PS0 = 1 PS1 = 1
	<31:24>	RAM Segment 3 Address Ramp Rate<15:8>								PS0 = 1 PS1 = 1
	<39:32>	RAM Segment 3 Address Ramp Rate<7:0>								PS0 = 1 PS1 = 1
RAM (0x0B)		RAM [1023:0]<31:0> (Read Instructions Write Out RAM Signature Register Data)								

Table 13. Register Map—When Linear Sweep Enable Bit Is True (CFR1<21> = 1)

Note that the RAM Enable Bit CFR1<31> only activates the RAM itself, not the RAM segment control words.

Register Name (Serial Address)	Bit Range	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value Or Profile
Control Function Register No. 1 (CFR1) (0x00)	<7:0>	Digital Power-Down	Comp Power-Down	DAC Power-Down	Clock Input Power Down	External Power-Down Mode	Linear Sweep No Dwell	SYNC_CLK Disable	Not Used	0x00
	<15:8>	SRR Load Enable	AutoClr Freq Accum	AutoClr Phase Accum	Sine/ Cosine Select	Clear Freq Accum	Clear Phase Accum	SDIO Input Only	LSB First	0x00
	<23:16>	Automatic Sync Enable	Software Manual Sync	Linear Sweep Enable	Not Used	Not Used	Not Used	Not Used	Not Used	0x00
	<31:24>	RAM Enable	RAM Destination	Internal Profile Control<2:0>			Load ARR Control	OSK Enable	Auto OSK Enable	0x00
Control Function Register No. 2 (CFR2) (0x01)	<7:0>	REFCLK Multiplier					VCO Range	Charge Pump Current<1:0>		0x00
	<15:8>	Not Used				High Speed Sync Enable	Hardware Manual Sync Enable	XTAL OUT Enable	Not Used	0x00
	<23:16>	Not Used								0x18
Amplitude Scale Factor (ASF) (0x02)	<7:0> (0x07)	Amplitude Scale Factor Register<7:0>								
	<15:8>	Auto Ramp Rate Speed Control<1:0>	Amplitude Scale Factor Register<13:8>							
Amplitude Ramp Rate (ARR) (0x03)	<7:0>	Amplitude Ramp Rate Register<7:0>								
Frequency Tuning Word (FTW0) (0x04)	<7:0>	Frequency Tuning Word No. 0<7:0>								0x00
	<15:8>	Frequency Tuning Word No. 0<15:8>								0x00
	<23:16>	Frequency Tuning Word No. 0<23:16>								0x00
	<31:24>	Frequency Tuning Word No. 0<31:24>								0x00
Phase Offset Word (POW0) (0x05)	<7:0>	Phase Offset Word No. 0<7:0>								0x00
	<15:8>	Open<1:0>	Phase Offset Word No. 0<13:8>							0x00
Frequency Tuning Word (FTW1) (0x06)	<7:0>	Frequency Tuning Word No. 1<7:0>								
	<15:8>	Frequency Tuning Word No. 1<15:8>								
	<23:16>	Frequency Tuning Word No. 1<23:16>								
	<31:24>	Frequency Tuning Word No. 1<31:24>								
Negative Linear Sweep Control Word (NLSCW) (0x07)	<7:0>	Falling Delta Frequency Tuning Word<7:0>								PS0 = 0
	<15:8>	Falling Delta Frequency Tuning Word<15:8>								PS0 = 0
	<23:16>	Falling Delta Frequency Tuning Word<23:16>								PS0 = 0
	<31:24>	Falling Delta Frequency Tuning Word<31:24>								PS0 = 0
	<39:32>	Falling Sweep Ramp Rate Word<7:0>								PS0 = 0
Positive Linear Sweep Control Word (PLSCW) (0x08)	<7:0>	Rising Delta Frequency Tuning Word<7:0>								PS0 = 1
	<15:8>	Rising Delta Frequency Tuning Word<15:8>								PS0 = 1
	<23:16>	Rising Delta Frequency Tuning Word<23:16>								PS0 = 1
	<31:24>	Rising Delta Frequency Tuning Word <31:24>								PS0 = 1
	<39:32>	Rising Sweep Ramp Rate Word<7:0>								PS0 = 1

CONTROL REGISTER BIT DESCRIPTIONS

Control Function Register No. 1 (CFR1)

The CFR1 is used to control the various functions, features, and modes of the AD9954. The functionality of each bit follows.

CFR1<31>: RAM Enable Bit

CFR1<31> = 0 (default). The RAM is disabled for operation. Either single-tone mode of operation or linear sweep mode of operation is enabled.

CFR1<31> = 1. The RAM is enabled for operation. Access control for normal operation is controlled via the mode control bits of the RSCW for the current profile.

CFR1<30>: RAM Destination Bit

If CFR1<31> is cleared, CFR1<30> is ignored.

CFR1<30> = 0 (default). If CFR1<31> is set, the RAM output drives the phase accumulator (provides the FTW).

CFR1<30> = 1. If CFR1<31> is set, the RAM output drives the phase-offset adder (POW).

CFR1<29:27>: Internal Profile Control Bits

These bits cause the profile bits to be ignored when the RAM is being used and puts the AD9954 into an automatic profile loop sequence that allows the user to implement a frequency/phase composite sweep that runs without external inputs. See the Internal Profile Control section for more details.

CFR1<26>: Load Amplitude Ramp Rate Control Bit

CFR1<26> = 0 (default). The amplitude ramp rate timer is loaded only upon timeout (timer == 1); it is not loaded due to an I/O update input signal.

CFR1<26> = 1. The amplitude ramp rate timer is loaded upon either timeout (timer == 1) or at the time of an I/O update input signal.

CFR1<25>: Shaped On-Off Keying Enable Bit

CFR1<25> = 0 (default). Shaped on-off keying is bypassed.

CFR1<25> = 1. Shaped on-off keying is enabled. See also CFR1<24>.

CFR1<24>: Autoshaped On-Off Keying Enable Bit

If CFR1<25> is cleared, CFR1<24> is ignored.

CFR1<24> = 0 (default). Manual shaped on-off keying operation. See the Shaped On-Off Keying section for details.

CFR1<24> = 1. Autoshaped on-off keying operation. See the Shaped On-Off Keying section for details.

CFR1<23>: Automatic Synchronization Enable Bit

CFR1<23> = 0 (default). The automatic synchronization feature of multiple AD9954s is inactive.

CFR1<23> = 1. The automatic synchronization feature of multiple AD9954s is active. See the Synchronizing Multiple AD9954s section for details.

CFR1<22>: Software Manual Synchronization of Multiple AD9954s

CFR1<22> = 0 (default). The manual synchronization feature is inactive.

CFR1<22> = 1. The software-controlled manual synchronization feature is executed. The SYNC_CLK rising edge is advanced by one SYNC_CLK cycle, and this bit is autocleared. To advance the rising edge multiple times, this bit needs to be set once for each advance.

CFR1<21>: Linear Frequency Sweep Enable

CFR1<21> = 0 (default). The linear frequency sweep capability of the AD9954 is inactive.

CFR1<21> = 1. The linear frequency sweep capability of the AD9954 is enabled. See the Linear Sweep Mode section for details.

CFR1<20:16>: Not Used, Leave Clear

CFR1<15>: Linear Sweep Ramp Rate Load Control Bit

CFR1<15> = 0 (default). The linear sweep ramp rate timer is loaded only upon timeout (timer == 1); it is not loaded due to an I/O update input signal.

CFR1<15> = 1. The linear sweep ramp rate timer is loaded either upon timeout (timer == 1) or at the time of an I/O update input signal.

CFR1<14>: Autoclear Frequency Accumulator Bit

CFR1<14> = 0 (default). The current state of the frequency accumulator is not impacted by receipt of an I/O update signal.

CFR1<14> = 1. The frequency accumulator is automatically and synchronously cleared for one cycle upon receipt of an I/O UPDATE signal.

CFR1<13>: Autoclear Phase Accumulator Bit

CFR1<13> = 0 (default). The current state of the phase accumulator is not impacted by receipt of an I/O update signal.

CFR1<13> = 1. The phase accumulator is automatically and synchronously cleared for one cycle upon receipt of an I/O update signal.

CFR1<12>: Sine/Cosine Select Bit

CFR1<12> = 0 (default). The angle-to-amplitude conversion logic employs a cosine function.

CFR1<12> = 1. The angle-to-amplitude conversion logic employs a sine function.

CFR1<11>: Clear Frequency Accumulator

CFR1<11> = 0 (default). The frequency accumulator functions as normal.

CFR1<11> = 1. The frequency accumulator memory elements are cleared and held clear until this bit is cleared.

CFR1<10>: Clear Phase Accumulator

CFR1<10> = 0 (default). The phase accumulator functions as normal.

CFR1<10> = 1. The phase accumulator memory elements are cleared and held clear until this bit is cleared.

CFR1<9>: SDIO Input Only

CFR1<9> = 0 (default). The SDIO pin is bidirectional (2-wire serial programming mode).

CFR1<9> = 1. The SDIO is configured as an input-only pin (3-wire serial programming mode).

CFR1<8>: LSB First

CFR1<8> = 0 (default). MSB first format is active.

CFR1<8> = 1. LSB first format is active.

CFR1<7>: Digital Power-Down Bit

CFR1<7> = 0 (default). All digital functions and clocks are active.

CFR1<7> = 1. All non-I/O digital functionality is suspended, lowering the power significantly.

CFR1<6>: Comparator Power-Down Bit

CFR1<6> = 0 (default). The comparator is enabled for operation.

CFR1<6> = 1. The comparator is disabled and is in its lowest power dissipation state.

CFR1<5>: DAC Power-Down Bit

CFR1<5> = 0 (default). The DAC is enabled for operation.

CFR1<5> = 1. The DAC is disabled and is in its lowest power dissipation state.

CFR1<4>: Clock Input Power-Down Bit

CFR1<4> = 0 (default). The clock input circuitry is enabled for operation.

CFR1<4> = 1. The clock input circuitry is disabled and the device is in its lowest power dissipation state.

CFR1<3>: External Power-Down Mode

CFR1<3> = 0 (default). The external power-down mode selected is the rapid recovery power-down mode. In this mode, when the PWRDWNCTL input pin is high, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, PLL, oscillator, and clock input circuitry are not powered down. CFR1<6> determines whether the comparator is powered down. CFR1<7>, and CFR1<5:4> are ignored.

CFR1<3> = 1. The external power-down mode selected is the full power-down mode. In this mode, when the PWRDWNCTL input pin is high, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up. CFR1<7:4> are all ignored.

CFR1<2>: Linear Sweep No-Dwell Bit

If CFR1<21> is clear, this bit is a don't care (ignored).

CFR1<2> = 0 (default). The linear sweep no-dwell function is inactive. If the no-dwell mode is inactive when the sweep completes, sweeping does not restart until an I/O update or change in profile initiates another sweep as previously described. The output frequency holds at the final value in the sweep.

CFR1<2> = 1. The linear sweep no-dwell function is active. If the no-dwell mode is active when the sweep completes, the phase accumulator is cleared. The phase accumulator remains cleared until another sweep is initiated via an I/O update input or change in profile.

CFR1<1>: SYNC_CLK Disable Bit

CFR1<1> = 0 (default). The SYNC_CLK pin is active.

CFR1<1> = 1. The SYNC_CLK pin assumes a static Logic 0 state to minimize noise generated by the digital circuitry. The synchronization circuitry remains active internally to maintain normal device timing.

CFR1<0>: Not Used, Leave Clear

Control Function Register No. 2 (CFR2)

The CFR2 is used to control the various functions, features, and modes of the AD9954, primarily related to the analog sections of the chip.

CFR2<23:12>: Not Used, Leave Clear

CFR2<11>: High Speed Sync Enable Bit

CFR2<11> = 0 (default). The high speed sync enhancement is off.

CFR2<11> = 1. The high speed sync enhancement is on. This bit should be set when using the autosynchronization feature for SYNC_CLK > 50 MHz (SYSCLK > 200 MSPS).

CFR2<10>: Hardware Manual Sync Enable Bit

CFR2<10> = 0 (default). The hardware manual sync function is off.

CFR2<10> = 1. The hardware manual sync function is enabled. While this bit is set, a rising edge on the SYNC_IN pin causes the device to advance the SYNC_CLK rising edge by one REFCLK cycle. This bit does not self-clear.

CFR2<9>: CRYSTAL OUT Enable Bit

CFR2<9> = 0 (default). The CRYSTAL OUT pin is inactive.

CFR2<9> = 1. The CRYSTAL OUT pin is active. The crystal oscillator circuitry output drives the CRYSTAL OUT pin, which can be used as a reference frequency for additional devices.

CFR2<8>: Not Used, Leave Clear

CFR2<7:3>: Reference Clock Multiplier Control Bits

This 5-bit word controls the multiplier value out of the clock-multiplier (PLL) block. See the Clock Multiplier section for more details.

CFR2<2>: VCO Range Control Bit

CFR2<2> = 0 (default), VCO operates between 100 MHz and 250 MHz.

CFR2<2> = 1, VCO operates between 250 MHz and 400 MHz.

CFR2<1:0>: Charge Pump Current Control Bits

These bits are used to control the current setting on the charge pump. The default setting, CFR2<1:0>, sets the charge pump current to the default value of 75 μA. For each bit added, 25 μA of current is added to the charge pump current:
01 = 100 μA, 10 = 125 μA, and 11 = 150 μA.

OTHER REGISTER DESCRIPTIONS

Amplitude Scale Factor (ASF)

The ASF register stores the 2-bit auto ramp rate speed value and the 14-bit amplitude scale factor used in the output shaped keying (OSK) operation. In auto-OSK operation, ASF<15:14> tells the OSK block how many amplitude steps to take for each increment or decrement. ASF<13:0> sets the maximum value achievable by the OSK internal multiplier. In manual OSK mode, ASF<15:14> has no effect. ASF<13:0> provide the output scale factor directly. If the OSK is disabled using CFR1<25>, this register has no effect on device operation.

Amplitude Ramp Rate (ARR)

The ARR register stores the 8-bit amplitude ramp rate used in the auto-OSK mode. See the Amplitude Control Options section for details.

Frequency Tuning Word 0 (FTW0)

The frequency tuning word is a 32-bit register that controls the rate of accumulation in the phase accumulator of the DDS core. Its specific role is dependent on the device mode of operation.

Phase Offset Word (POW)

The phase offset word is a 14-bit register that stores a phase offset value. See the Phase Offset Word Mux section for additional details.

Frequency Tuning Word 1 (FTW1)

The frequency tuning word is a 32-bit register that sets the upper frequency in a linear sweep operation.

Register 0x07 and Register 0x08 are multifunctional registers.

Negative and Positive Linear Sweep Control Word (NLSCW and PLSCW)

When linear sweep bit is enabled, Register 0x07 provides the negative linear sweep control word (NLSCW) and Register 0x08 provides the positive linear sweep control word (PLSCW). Each of the linear sweep control words contains a 32-bit delta frequency tuning word (FDFTW and RDFTW) and an 8-bit sweep ramp rate word (FSRRW and RSRRW). See the Modes of Operation section for more details.

RAM Segment Control Words (RSCW0, RSCW1, RSCW2, and RSCW3)

When linear sweep is disabled, Register 0x07, Register 0x08, Register 0x09, and Register 0x0A act as the RAM segment control words for each of the RAM segments. Each of the RAM segment control words is comprised of a RAM segment address ramp rate, a final address value, a beginning address value, a RAM segment mode control, and a no-dwell bit. Note the discontinuities of the address registers, since they may make programming a little more challenging.

RAM Segment Address Ramp Rate, RSCW<39:24>

For RAM modes that step through address values, such as ramping, this 16-bit word defines the number of SYNC_CLK cycles the RAM controller dwells at each address. A value of 0 is invalid. Any other value from 1 to 65,535 can be used.

RAM Segment Final Address RSCW<9:8>, RSCW<23:16>

This discontinuous 10-bit sequence defines the final address value for the given RAM segment. The order in which the bits are previously listed is MSB first: RSCW<9> is the MSB and RSCW<16> is the LSB of the final address value.

RAM Segment Beginning Address RSCW<3:0>, RSCW <15:10>

This discontinuous 10-bit sequence defines the final address value for the given RAM segment. The order in which the bits are previously listed is MSB first: RSCW<3> is the MSB and RSCW<10> is the LSB of the final address value.

RAM Segment No-Dwell Bit RSCW<4>

This bit sets the no-dwell feature of sweeping profiles. In profiles that sweep from a defined beginning to a defined end, the RAM controller can either dwell at the final address until the next profile is selected or, when this bit is set, the RAM controller returns to the beginning address and dwells there until the next profile is selected.

RAM Segment Mode Control RSCW<7:5>

This 3-bit sequence determines the RAM segment's mode of operation. There are only five possible RAM modes, so only values of 0 to 4 are valid (see Table 7).

LAYOUT CONSIDERATIONS

For the best performance, the following layout guidelines should be observed. Always separate the analog power supply (AVDD) and the digital power supply (DVDD), even if just from two different voltage regulators driven by a common supply. Likewise, the ground connections (AGND and DGND) should be kept separate as far back to the source as possible (for example, separate the ground planes on a localized board, even if the grounds connect to a common point in the system). Bypass capacitors should be placed as close to device pins as possible. Usually a multitiered bypassing scheme consisting of a small high frequency capacitor (100 pF) placed close to the supply pin and progressively larger capacitors (0.1 μF and 10 μF) further back to the actual supply source works best.

DETAILED PROGRAMMING EXAMPLES

SINGLE-TONE MODE

1. Write to Control Register 1 instructing the part to autoclear the phase accumulator whenever the phase offset word changes and issues an I/O update. Set Bit 13 in the CFR1 register. The address for CFR1 is 0; therefore, an instruction byte of 0x00 is sent and 0x00 00 00 20 for data. Note that users must write to all four bytes of the register.
2. Write to Control Register 2 setting the clock multiplier value to 20, and the VCO range bit to its upper value. In CFR2, Bit 7 to Bit 3 control the multiply value. To get a multiplied value of 20 from 5 bits, the binary value is 10100. As previously mentioned, also send Bit 2 to put the VCO into its upper range (to get 400 MHz). Therefore, the instruction byte is 0x01 and 0x00 00 A4 for data.
3. Calculate the tuning word to generate a 122 MHz output from a 400 MSPS clock, load it into FTW0, and latch the data written to the I/O buffers into their respective registers. The frequency tuning word equation becomes (122 MHz/ 400 MHz) × 2^{32}, which yields 0x4E 14 7A E1. Send the Instruction Byte 0x04 and four data bytes of 0x4E 14 7A E1. Issue an I/O update, which transfers the data into the part.
   Whenever a phase change is desired, calculate and write the phase offset word to the part and issue an I/O update. For example, if the first value is 45°, the phase offset word is (45/360) × 2^{14}, or in decimal, 2048. Therefore, write an instruction byte of 0x05 and Data Byte 0x0800. When an I/O update is issued, the phase accumulator clears, which starts it from a known phase of 0°. It again accumulates at a 122 MHz rate, except now phase shifting each and every sample by 45°.

In this example, the part is programmed to output a 122 MHz single-tone carrier, the device is clocked with a 20 MHz crystal oscillator, and the clock multiplier is used to push the internal system clock up to 400 MHz. Phase offsets are then added to the carrier.

The programming steps include the following:

LINEAR SWEEP MODE

In this example, the part is programmed to generate a chirp from 61.53 MHz to 62.73 MHz. The chirp up is in 1.20 µs, the chirp down is in 1.8 µs, and the chirp is made as finely linearized as possible. Therefore, users must calculate and program:

- FTW0 for 61.53 MHz (the start frequency)
- FTW1 for 62.73 MHz (the stop frequency)
- CFR1 to put the part into linear sweep mode
- The positive linear sweep control word (PLSCW), to make as linearized a chirp in 1.20 µs
- The negative linear sweep control word (NLSCW), to make as linearized a chirp in 1.80 µs

The last example programmed the clock multiplier; therefore, start with a 400 MSPS clock. FTW0 is (61.53/400) × 2^{32} or 0x27611340, and FTW1 is (62.73/400) × 2^{32} or 0x2825AEE6. To turn the linear sweep on, set CFR1<21>.

The PLSCW and NLSCW are five bytes wide: one byte for the ramp rate and four bytes for the incremental frequency value. To begin, calculate the ramp rate, and cover 1.2 MHz on both sweeps. The ramp rate tells the part how many SYNC_CLK cycles (for SYSCLK cycles) to send at each incremental value. When the shortest time possible is spent at each incremental frequency, the most linearized sweep is achieved; therefore, the part should only spend one SYNC_CLK period at each incremental frequency, which ensures that the smallest frequency steps possible are taken. For a 400 MSPS SYSCLK, the result is a 100 MHz SYNC_CLK rate or a 10 ns SYNC_CLK period. This means on the finest resolution, 120 incremental steps squeeze into the rising sweep (1.2 µs/10 ns) and 180 on the falling sweep (1.8 µs/10 ns).

For the rising delta frequency, a 1.2 MHz/120 steps is calculated, which means each step is approximately 10 kHz for the rising delta frequency and approximately 666.6666 Hz for the falling delta frequency. The logic in the linear sweep block ensures that FTW1 on a rising sweep or FTW0 on a falling sweep is not exceeded. If the exact incremental tuning word is not achieved using the 32-bit resolution, round up, not down, to ensure the entire range during the sweep is covered. To calculate the rising delta frequency word, simply calculate (10 K/400 M) × 2^{32} = 0x0001A36F. Combining the rising ramp rate, first byte, and the rising delta frequency, the second byte to fifth byte yields the PLSCW: 0x010001A36F. Likewise, the NLSCW works out to 0x0100001BF4. Table 14 is a summary table of instruction and data bytes to write to.

Table 14. Linear Sweep Example Write Instructions

Register	Instruction Byte	Data Byte
CFR1	0x00	0x00200000
FTW0	0x04	0x27611340
FTW1	0x06	0x2825AEE6
NLSCW	0x07	0x0100001BF4
RLSCW	0x08	0x010001A36F

RAM MODE

This example programs the RAM. Use the RAM on the AD9954 to simulate the nonlinear filter shape of a Gaussian filter response on the FSK data. Begin by plotting the filter response from F0 to F1 and from F1 to F0. The transition time specification (see Table 1) tells how long it takes to transition from F0 to F1 and from F1 to F0, either as an actual time value or as a fraction of the symbol rate. Both ways show how long it can take to change symbols, and for this application, it is 100 ns. To program the RAM, decide how many RAM segments to use, program the RAM segment control word for each of those segments, and load the RAM data for each of those segments.

Because there is a ramp-up, but no ramp-down, RAM mode, two RAM segments are generated; one for the transition from F0 to F1, and one for the transition from F1 to F0. Step through the intermediary frequencies as quickly as possible, because the faster the steps, the less the output frequency deviates from the ideal frequency response of the filter. The fastest the AD9954 can step through the values in the RAM is at the SYNC_CLK rate, or ¼ of the SYSCLK rate, which works out to 10 ns, assuming the maximum SYSCLK rate of 400 MSPS. Dividing the total transition time of 100 ns by the time for each transition, 100 steps can be taken. The intermediary frequencies are solved by looking at the instantaneous frequency on the curve every 10 ns and by recording that value. This gives 200 frequency values, 100 representing the change from F0 to F1 and 100 representing the change from F1 to F0. This is the information needed to program the RAM.

Begin by programming CFR1 to set the RAM enable bit. Calculate and program RSCW0 and RSCW1. Each of the RAM segment control words has an address ramp rate (16 bits), a final address (10 bits), a beginning address (10 bits), a mode control value (3 bits), and a no-dwell flag. Stepping through the intermediary frequencies as quickly as possible was previously discussed; therefore, the ramp rate for each word is 0x0000. Define RAM Segment 0 to occupy the RAM space from Address 0 to Address 99, which gives 100 values. Define RAM Segment 1 to occupy Address 100 to Address 199 (also 100 values). Look at the modes of operation choice and recognize that the ramp-up mode is used to step through each of the addresses and then holds the final value in the profile. Therefore, for each RSCW, the mode control bits are b'001. Because staying at the last value is recommended, the no-dwell bit is 0. To form the data for each RSCW, combine these values. For RSCW0, it is 0x0100630020. For RSCW1, it is 0x0100C79021. Because the words that comprise the RSCW are not contiguous, care must be taken in calculating the RSCW. Make a chart of each of the subwords in order: address ramp rate, final address, beginning address, mode, and no dwell. Write the binary values for each subword, and then, with a copy of the register map printed out, write each of the binary bits into the map. When this is completed, the individual bytes can be read from the map. For example, Table 15 shows how RSCW1 would appear.

Table 15. RAM Mode Register Table Settings

RAM Segment Control Word No. 1 (RSCW1) (0x08)	<7:0>	RAM Segment 1 Mode Control <2:0> 001	No-Dwell Active 0	RAM Segment 1 Beginning Address <9:6> 0001
	<15:8>	RAM Segment 1 Beginning Address <5:0> 100100		RAM Segment 1 Final Address <9:8> 00
	<23:16>	RAM Segment 1 Final Address <7:0> 11000111		
	<31:24>	RAM Segment 1 Address Ramp Rate <15:8> 00000000		
	<39:32>	RAM Segment 1 Address Ramp Rate <7:0> 00010000		

The RSCW0 and RSCW1 values must be loaded into their registers before attempting to write data to RSCW0 and RSCW1; therefore, issue an I/O update.

The next step is to convert each of the intermediary frequencies into a frequency tuning word according to

$$ftw = \frac{fi}{SYSCLK} \times 2^{32}$$

where:

fi is the desired intermediary frequency.

SYSCLK is the system clock rate.

Once this is complete, the result for each profile should be a vector of 100 32-bit words. To write RAM Segment 0, select Profile 0 (PS0 = 0, PS1 = 0), and then write the instruction byte b'00001011, which indicates a RAM write operation is going to be performed. The serial port I/O controller recognizes this and polls the profile select pins, thus determining that Profile 0 is the target storage location for the data out of RSCW0 previously entered. It now knows to put the first word at Address 0, the last word at Address 99, and that there are 100 words in total. Proceed to load all 100 32-bit frequency words into the RAM. When this is done, write the data to RAM Segment 1. First, change to Profile 1 (PS0 = 1, PS1 = 0), and then write the RAM instruction byte again. The device now knows to write the first word at Address 100, the last word at Address 199, and again that there are 100 words in total. Write all 100 32-bit words of RAM Segment 1 and issue an I/O update. Whenever the PS0 pin is toggled (from 0 to 1), the part steps through the RAM segment, which is the Gaussian-shaped pattern programmed into the RAM.

SUGGESTED APPLICATION CIRCUITS

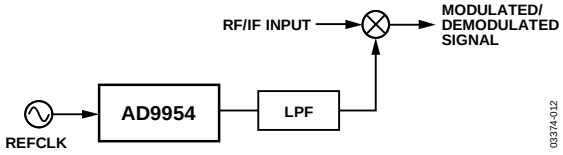


Figure 31. Synchronized LO for Upconversion/Downconversion

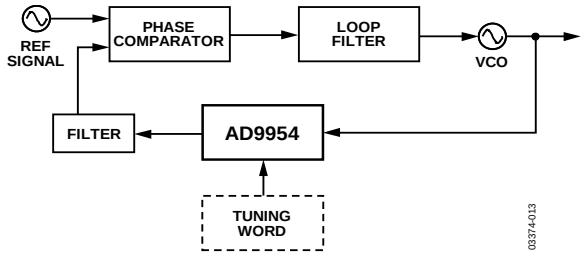


Figure 32. Digitally Programmable Divide-by-N Function in PLL

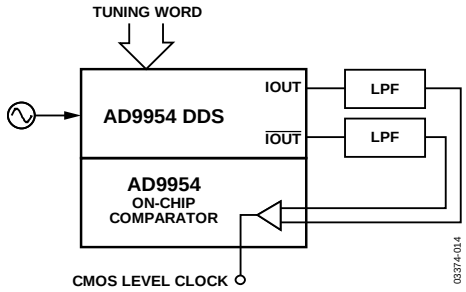


Figure 33. Frequency Agile Clock Generator

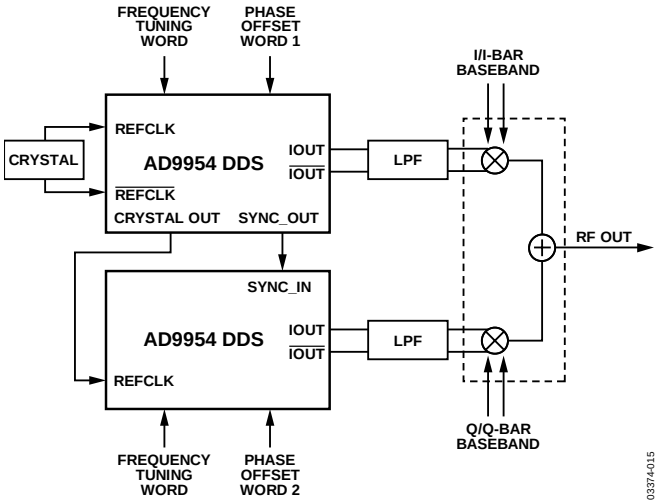


Figure 34. Two AD9954s Synchronized to Provide I and Q Carriers with Independent Phase Offsets for Nulling

EVALUATION BOARD SCHEMATICS

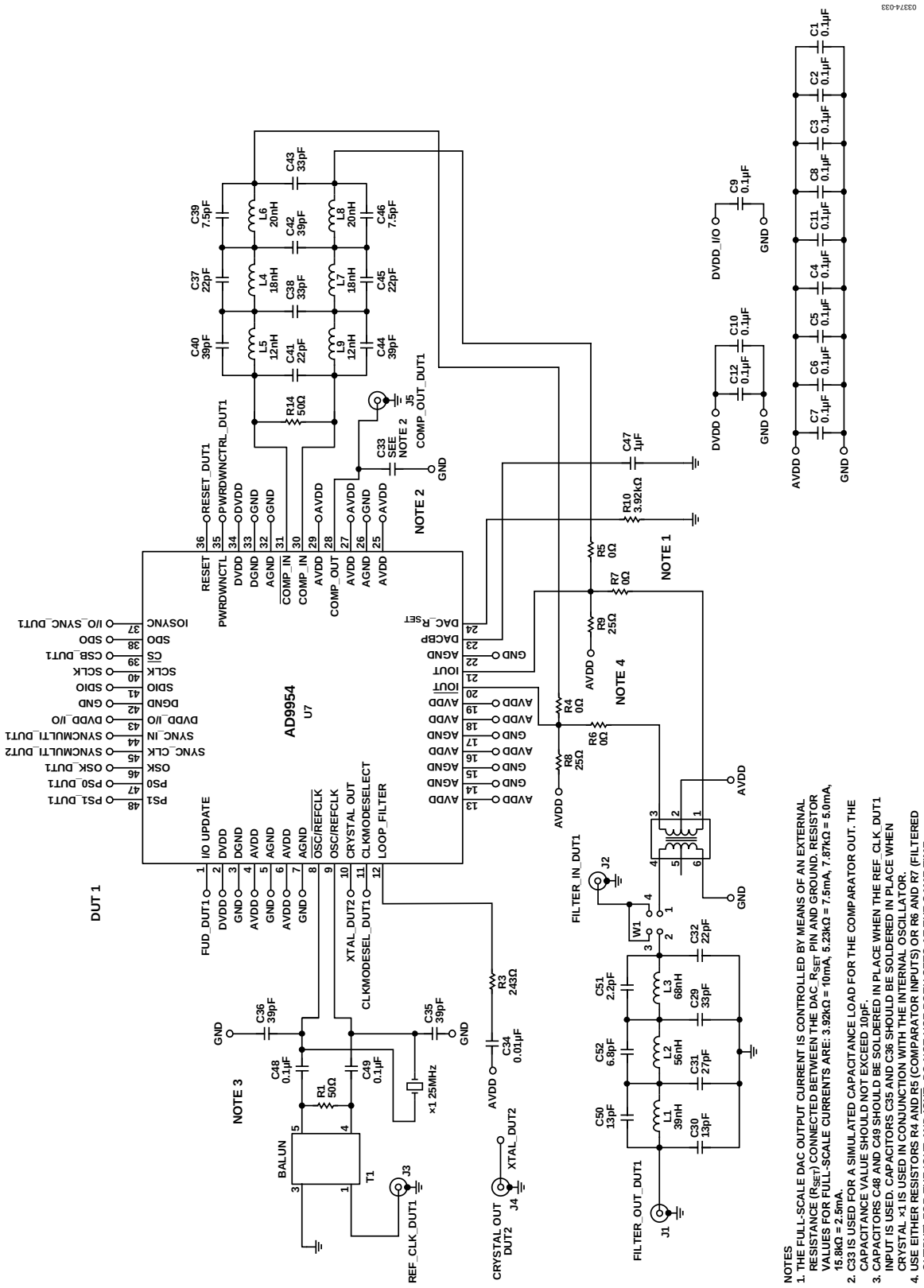


Figure 35. Evaluation Board Channel 1

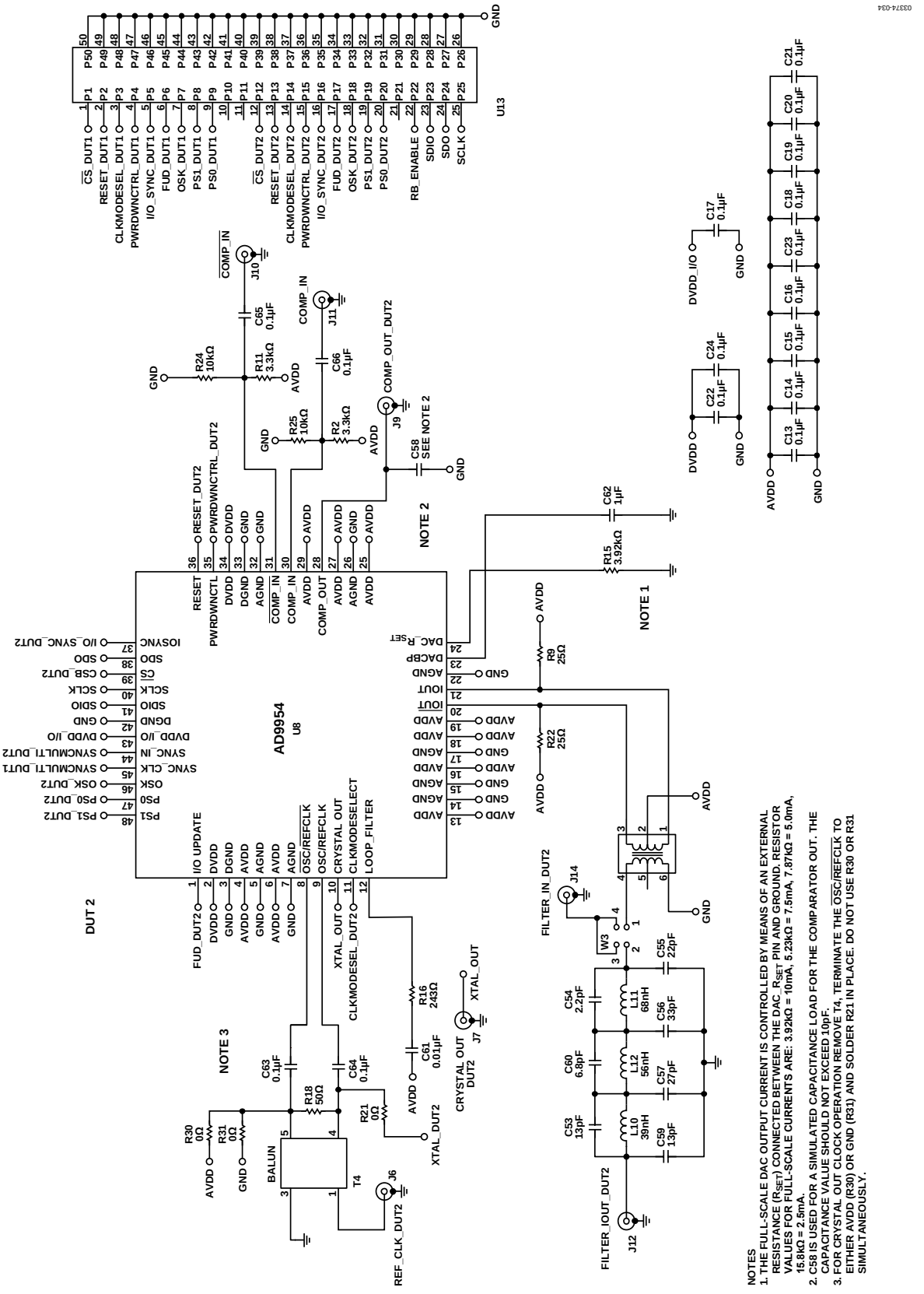


Figure 36. Evaluation Board Channel 2

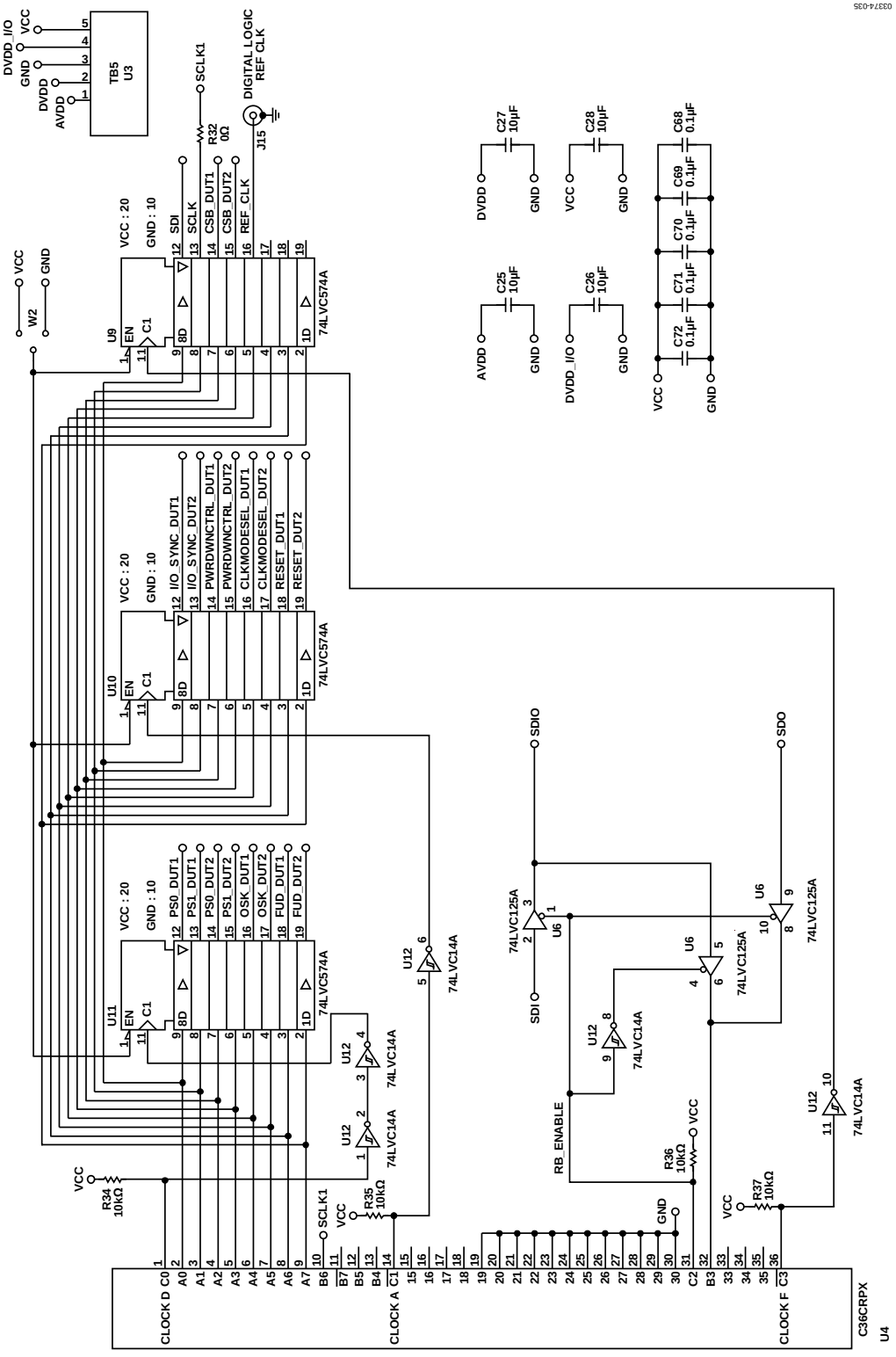
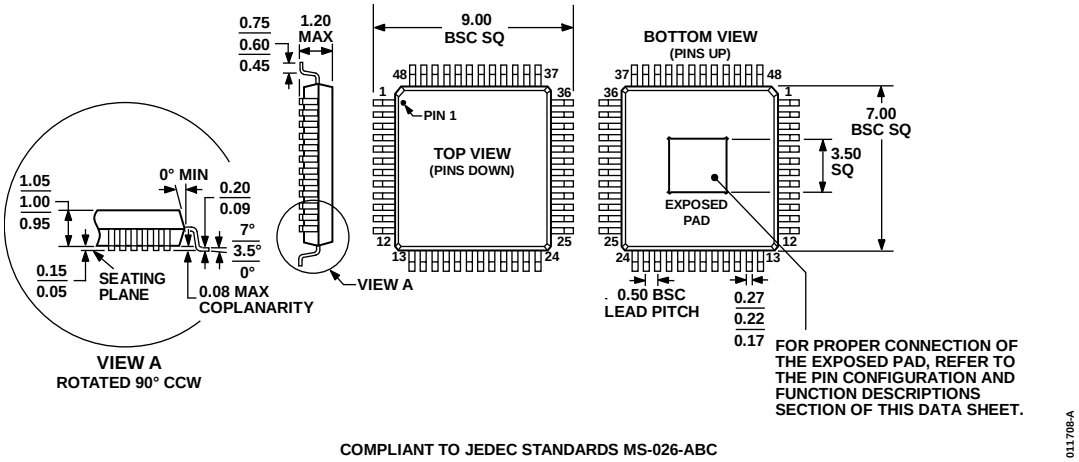


Figure 37. Evaluation Board Interface Logic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ABC

Figure 38. 48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Ordering Quantity	Package Option
AD9954YSVZ	−40°C to +105°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]		SV-48-4
AD9954YSVZ-REEL7	−40°C to +105°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	500	SV-48-4
AD9954/PCBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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