16-Channel, High Performance, 192 kHz, 24-Bit DAC

Data Sheet

ADAU1966A

FEATURES

- Differential or single-ended voltage DAC output
- 114 dB DAC dynamic range, A-weighted, differential
- –97 dB total harmonic distortion plus noise (THD + N), differential
- 110 dB DAC dynamic range, A-weighted, single-ended
- –95 dB THD + N, single-ended
- 2.5 V digital and 3.3 V analog and input/output (I/O) supplies
- 299 mW total quiescent power
- Phase-locked loop (PLL) generated or direct master clock
- Low electromagnetic interference (EMI) design
- Linear regulator driver to generate digital supply
- Supports 24-bit and 32 kHz to 192 kHz sample rates
- Low propagation 192 kHz sample rate mode
- Log volume control with autoramp function
- Temperature sensor with digital readout ±3°C accuracy
- SPI and I²C controllable for flexibility
- Software-controllable clickless mute
- Software power-down
- Right justified, left justified, I²S, and TDM modes
- Master and slave modes with up to 16-channel input/output
- 80-lead LQFP package
- Qualified for automotive applications

APPLICATIONS

- Automotive audio systems
- Home theater systems
- Digital audio effects processors

GENERAL DESCRIPTION

The ADAU1966A is a high performance, single-chip digital-to-analog converter (DAC) that provides 16 DACs with differential or single-ended outputs using the Analog Devices, Inc., patented multibit sigma-delta (Σ-Δ) architecture. A serial peripheral interface (SPI)/I²C port is included, allowing a microcontroller to adjust volume and many other parameters. The ADAU1966A operates from 2.5 V digital and 3.3 V analog supplies. A linear regulator is included to generate the digital supply voltage from the analog supply voltage. The ADAU1966A is available in an 80-lead LQFP.

The ADAU1966A is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the internal master clock from an external left-right frame clock (LRCLK), the ADAU1966A can eliminate the need for a separate high frequency master clock and can be used with or without a bit clock. The DACs are designed using the latest Analog Devices continuous time architectures to further minimize EMI. By using 2.5 V digital supplies, power consumption is minimized, and the digital waveforms are a smaller amplitude, further reducing emissions.

Note that throughout this data sheet, multifunction pins, such as SCLK/SCL, are referred to by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

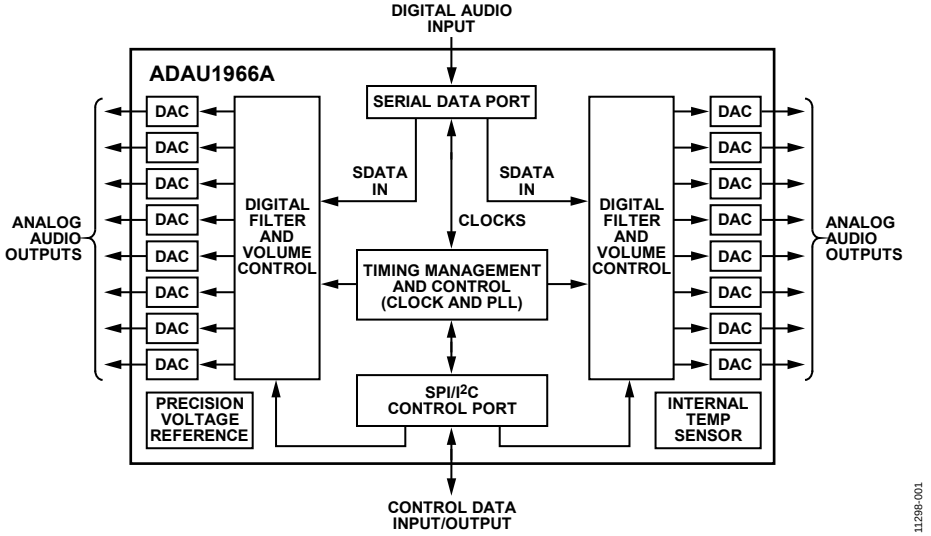


Figure 1.

Rev. A

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2013–2016 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Analog Performance Specifications: T_A = 25°C ... 3
Analog Performance Specifications: T_A = 105°C ... 4
Crystal Oscillator Specifications ... 4
Digital Input/Output Specifications ... 5
Power Supply Specifications ... 5
Digital Filters ... 6
Timing Specifications ... 6
Absolute Maximum Ratings ... 8
Thermal Resistance ... 8
ESD Caution ... 8
Pin Configuration and Function Descriptions ... 9
Typical Performance Characteristics ... 12
Typical Application Circuits ... 13
Theory of Operation ... 14
DACs ... 14
Clock Signals ... 14
Power-Up and Reset ... 16
Standalone Mode ... 16
I²C Control Port ... 16
Serial Control Port: SPI Control Mode ... 19
Power Supply and Voltage Reference ... 20
Serial Data Ports—Data Format ... 20
Time-Division Multiplexed (TDM) Modes ... 21
Temperature Sensor ... 21
Additional Modes ... 23
Register Summary ... 24
Register Details ... 25
PLL and Clock Control 0 Register ... 25
PLL and Clock Control 1 Register ... 26
Block Power-Down and Thermal Sensor Control 1 Register ... 27
Power-Down Control 2 Register ... 28
Power-Down Control 3 Register ... 29
Thermal Sensor Temperature Readout Register ... 30
DAC Control 0 Register ... 30
DAC Control 1 Register ... 31
DAC Control 2 Register ... 32
DAC Individual Channel Mutes 1 Register ... 33
DAC Individual Channel Mutes 2 Register ... 34
Master Volume Control Register ... 35
DAC 1 Volume Control Register ... 35
DAC 2 Volume Control Register ... 36
DAC 3 Volume Control Register ... 36
DAC 4 Volume Control Register ... 37
DAC 5 Volume Control Register ... 37
DAC 6 Volume Control Register ... 38
DAC 7 Volume Control Register ... 38
DAC 8 Volume Control Register ... 39
DAC 9 Volume Control Register ... 39
DAC 10 Volume Control Register ... 40
DAC 11 Volume Control Register ... 40
DAC 12 Volume Control Register ... 41
DAC 13 Volume Control Register ... 41
DAC 14 Volume Control Register ... 42
DAC 15 Volume Control Register ... 42
DAC 16 Volume Control Register ... 43
Pad Strength Register ... 43
DAC Power Adjust 1 Register ... 44
DAC Power Adjust 2 Register ... 45
DAC Power Adjust 3 Register ... 46
DAC Power Adjust 4 Register ... 47
Outline Dimensions ... 51
Ordering Guide ... 51
Automotive Products ... 51

REVISION HISTORY

3/16—Rev. 0 to Rev. A

Changes to Table 4 ... 5

8/13—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. Master clock = 12.288 MHz (48 kHz f_S, 256 × f_S mode), input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, load capacitance (digital output) = 20 pF, load current (digital output) = ±1 mA or 1.5 kΩ to ½ DVDD supply, input voltage high = 2.0 V, input voltage low = 0.8 V, analog audio output resistive load = 3100 Ω per pin, unless otherwise noted.

ANALOG PERFORMANCE SPECIFICATIONS: T_A = 25°C

Specifications guaranteed at supply voltages of AVDDx = 3.3 V, DVDD = 2.5 V, ambient temperature[1] (T_A) = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (DNR)	20 Hz to 20 kHz, −60 dB input				
No Filter (RMS)	Differential output	105.5	111		dB
With A-Weighted Filter (RMS)	Differential output	108.5	114		dB
No Filter (RMS)	Single-ended output	102.5	107		dB
With A-Weighted Filter (RMS)	Single-ended output	105.5	110		dB
Total Harmonic Distortion + Noise					
Differential Output	Two channels running −1 dBFS		−97	−85	dB
	All channels running −1 dBFS		−97	−85	dB
Single-Ended Output	Two channels running −1 dBFS		−95	−80	dB
	All channels running −1 dBFS		−95	−80	dB
Full-Scale Differential Output Voltage			2.00 (2.83)		V rms (V p-p)
Full-Scale Single-Ended Output Voltage			1.00 (1.41)		V rms (V p-p)
Gain Error		−10		+10	%
Offset Error		−25	−6	+25	mV
Gain Drift		−30		+30	ppm/°C
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-Emphasis Gain Error				±0.6	dB
Output Resistance at Each Pin			33		Ω
REFERENCE					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	1.40	1.50	1.56	V
External Reference Voltage Source	CM pin	1.40	1.50	1.56	V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	3.14	3.3	3.46	V
Regulated Output Voltage	VSENSE pin	2.25	2.50	2.59	V
TEMPERATURE SENSOR					
Temperature Accuracy		−3		+3	°C
Temperature Readout Range		−60		+140	°C
Temperature Readout Step Size			1		°C
Temperature Sample Rate		0.25		6	Hz

[1] Functionally guaranteed at −40°C to +125°C, case temperature.

ANALOG PERFORMANCE SPECIFICATIONS: T_A = 105°C

Specifications guaranteed at supply voltages of AVDDx = 3.3 V, DVDD = 2.5 V, ambient temperature[1] (T_A) = 105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (DNR)	20 Hz to 20 kHz, −60 dB input				
No Filter (RMS)	Differential output	106.5	110		dB
With A-Weighted Filter (RMS)	Differential output	109.5	113		dB
No Filter (RMS)	Single-ended output	101.5	108		dB
With A-Weighted Filter (RMS)	Single-ended output	104.5	110		dB
Total Harmonic Distortion + Noise					
Differential Output	Two channels running −1 dBFS		−92	−83	dB
	All channels running −1 dBFS		−92	−83	dB
Single-Ended Output	Two channels running −1 dBFS		−90	−80	dB
	All channels running −1 dBFS		−90	−80	dB
Full-Scale Differential Output Voltage			2.00 (2.83)		V rms (V p-p)
Full-Scale Single-Ended Output Voltage			1.00 (1.41)		V rms (V p-p)
Gain Error		−10		+10	%
Offset Error		−25	−6	+25	mV
Gain Drift		−30		+30	ppm/°C
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-Emphasis Gain Error				±0.6	dB
Output Resistance at Each Pin			33		Ω
REFERENCE					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	1.40	1.50	1.56	V
External Reference Voltage Source	CM pin	1.40	1.50	1.56	V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	3.14	3.3	3.46	V
Regulated Output Voltage	VSENSE pin	2.25	2.50	2.55	V
TEMPERATURE SENSOR					
Temperature Accuracy		−3		+3	°C
Temperature Readout Range		−60		+140	°C
Temperature Readout Step Size			1		°C
Temperature Sample Rate		0.25		6	Hz

[1] Functionally guaranteed at −40°C to +125°C, case temperature.

CRYSTAL OSCILLATOR SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
TRANSCONDUCTANCE				
T_A = 25°C	6.4	7 to 10	14	mmhos
T_A = 105°C	5.2	7.5 to 8.5	12	mmhos

DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < T_A < +105°C, IOVDD = 3.3 V ± 5%, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT					
High Level Input Voltage (V_{IH})		0.7 × IOVDD			V
Low Level Input Voltage (V_{IL})				0.3 × IOVDD	V
Input Leakage	I_{IH} at V_{IH} = 3.3 V			10	µA
	I_{IL} at V_{IL} = 0 V			10	µA
INPUT CAPACITANCE				5	pF
DIGITAL OUTPUT					
High Level Output Voltage (V_{OH})	I_{OH} = 1 mA	0.8 × IOVDD			V
Low Level Output Voltage (V_{OL})	I_{OL} = 1 mA			0.1 × IOVDD	V

POWER SUPPLY SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
Voltage	AVDDx	3.14	3.3	3.46	V
	DVDD	2.25	2.5	3.46	V
	PLLVDD	2.25	2.5	3.46	V
	IOVDD	3.14	3.3	3.46	V
	VSUPPLY	3.14	3.3	3.46	V
Analog Current	AVDDx = 3.3 V				
Normal Operation			60		mA
Power-Down			1		µA
Digital Current	DVDD = 2.5 V				
Normal Operation	f_S = 48 kHz to 192 kHz		30		mA
Power-Down	No MCLK or I^2S		4		µA
PLL Current	PLLVDD = 2.5 V				
Normal Operation	f_S = 48 kHz to 192 kHz		5		mA
Power-Down			1		µA
Input/Output Current	IOVDD = 3.3 V				
Normal Operation			4		mA
Power-Down			1		µA
QUIESCENT DISSIPATION—DITHER INPUT					
Operation	MCLK = 256 × f_S, 48 kHz				
All Supplies	AVDDx = 3.3 V, DVDD/PLLVDD = 2.5 V, IOVDD = 3.3 V		299		mW
Analog Supply	AVDDx = 3.3 V, 12.4 mW per channel		198		mW
Digital Supply	DVDD = 2.5 V		75		mW
PLL Supply	PLLVDD = 2.5 V		13		mW
I/O Supply	IOVDD = 3.3 V		13		mW
Power-Down, All Supplies			0		mW
POWER SUPPLY REJECTION RATIO					
Signal at Analog Supply Pins	1 kHz, 200 mV p-p, differential		88		dB
	20 kHz, 200 mV p-p, differential		85		dB
	1 kHz, 200 mV p-p, single-ended		85		dB
	20 kHz, 200 mV p-p, single-ended		75		dB

DIGITAL FILTERS

Table 6.

Parameter	Mode	Factor	Min	Typ	Max	Unit
DAC INTERPOLATION FILTER						
Pass Band	48 kHz mode, typical at 48 kHz	$0.4535 \times f_S$		22		kHz
	96 kHz mode, typical at 96 kHz	$0.3646 \times f_S$	35			kHz
	192 kHz mode, typical at 192 kHz	$0.3646 \times f_S$		70		kHz
Pass-Band Ripple	48 kHz mode, typical at 48 kHz				±0.01	dB
	96 kHz mode, typical at 96 kHz				±0.05	dB
	192 kHz mode, typical at 192 kHz				±0.1	dB
Transition Band	48 kHz mode, typical at 48 kHz	$0.5 \times f_S$		24		kHz
	96 kHz mode, typical at 96 kHz	$0.5 \times f_S$		48		kHz
	192 kHz mode, typical at 192 kHz	$0.5 \times f_S$		96		kHz
Stop Band	48 kHz mode, typical at 48 kHz	$0.5465 \times f_S$		26		kHz
	96 kHz mode, typical at 96 kHz	$0.6354 \times f_S$		61		kHz
	192 kHz mode, typical at 192 kHz	$0.6354 \times f_S$		122		kHz
Stop-Band Attenuation	48 kHz mode, typical at 48 kHz		68			dB
	96 kHz mode, typical at 96 kHz		68			dB
	192 kHz mode, typical at 192 kHz		68			dB
Propagation Delay	48 kHz mode, typical at 48 kHz	$25/f_S$		521		µs
	96 kHz mode, typical at 96 kHz	$11/f_S$		115		µs
	192 kHz mode, typical at 192 kHz	$8/f_S$		42		µs
	192 kHz low propagation delay mode, typical at 192 kHz	$2/f_S$		10		µs

TIMING SPECIFICATIONS

$-40°C < T_A < +105°C$, DVDD = 2.5 V ± 10%, unless otherwise noted.

Table 7.

Parameter[1]	Description	Min	Typ	Max	Unit
INPUT MASTER CLOCK (MCLKI) AND RESET					
t_{MH}	Master clock duty cycle, DAC clock source = PLL clock at $256 \times f_S$, $384 \times f_S$, $512 \times f_S$, and $768 \times f_S$	40		60	%
	DAC clock source = direct MCLKI at $512 \times f_S$ (bypass on-chip PLL)	40		60	%
f_{MCLK}	MCLKI frequency of the MCLKI/XTALI pin, PLL mode	6.9		40.5	MHz
	Direct MCLKI $512 \times f_S$ mode			27.1	MHz
f_{BCLK}	DBCLK pin frequency, PLL mode			27.0	MHz
t_{PDR}	Low	15			ns
t_{PDRR}	Recovery, reset to active output	300			ms
PLL					
Lock Time	MCLKI input of the MCLKI/XTALI pin			10	ms
	DLRCLK pin input			50	ms
Output Duty Cycle, MCLKO Pin	$256 \times f_S$ VCO clock	40		60	%

Parameter[1]	Description	Min	Typ	Max	Unit
SPI PORT	See Figure 19				
f_{SCLK}	SCLK frequency, not shown in Figure 19			10	MHz
t_{SCH}	SCLK high	35			ns
t_{SCL}	SCLK low	35			ns
t_{MOS}	MOSI setup, time to SCLK rising	10			ns
t_{MOH}	MOSI hold, time from SCLK rising	10			ns
t_{SSS}	$\overline{SS}$ setup, time to SCLK rising	10			ns
t_{SSH}	$\overline{SS}$ hold, time from SCLK falling	10			ns
t_{SSHIGH}	$\overline{SS}$ high	10			ns
t_{MIE}	MISO enable from $\overline{SS}$ falling			30	ns
t_{MID}	MISO delay from SCLK falling			30	ns
t_{MIH}	MISO hold from SCLK falling, not shown in Figure 19	30			ns
t_{MITS}	MISO tristate from $\overline{SS}$ rising			30	ns
I^2C	See Figure 2 and Figure 15				
f_{SCL}	SCL clock frequency			400	kHz
t_{SCLL}	SCL low	1.3			µs
t_{SCLH}	SCL high	0.6			µs
t_{SCS}	Setup time (start condition), relevant for repeated start condition	0.6			µs
t_{SCH}	Hold time (start condition), first clock generated after this period	0.6			µs
t_{SSH}	Setup time (stop condition)	0.6			µs
t_{DS}	Data setup time	100			ns
t_{SR}	SDA and SCL rise time			300	ns
t_{SF}	SDA and SCL fall time			300	ns
t_{BFT}	Bus-free time between stop and start	1.3			µs
DAC SERIAL PORT	See Figure 21				
t_{DBH}	DBCLK high, slave mode	10			ns
t_{DBL}	DBCLK low, slave mode	10			ns
t_{DLS}	DLRCLK setup, time to DBCLK rising, slave mode	10			ns
t_{DLH}	DLRCLK hold from DBCLK rising, slave mode	5			ns
t_{DLSK}	DLRCLK skew from DBCLK falling, master mode, not shown in Figure 21	−8		+8	ns
t_{DDS}	DSDATAx setup to DBCLK rising	10			ns
t_{DDH}	DSDATAx hold from DBCLK rising	5			ns

[1] The timing specifications may refer to single functions of multifunction pins, such as the SCL function of the SCLK/SCL pin.

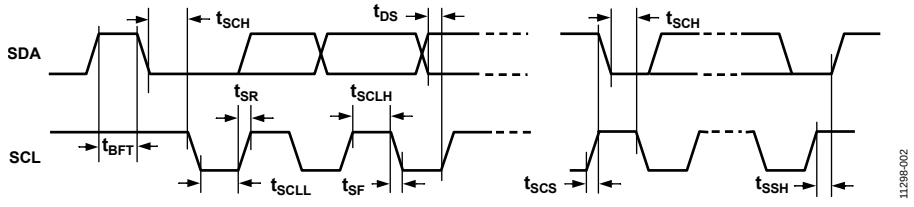


Figure 2. I^2C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Analog (AVDDx)	−0.3 V to +3.6 V
Input/Output (IOVDD)	−0.3 V to +3.6 V
Digital (DVDD)	−0.3 V to +3.6 V
PLL (PLLVDD)	−0.3 V to +3.6 V
VSUPPLY	−0.3 V to +3.6 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDDx + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to DVDD + 0.3 V
Operating Temperature Range (Case)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} represents junction-to-ambient thermal resistance, and θ_{JC} represents the junction-to-case thermal resistance. All characteristics are for a 4-layer board with a solid ground plane.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
80-Lead LQFP	42.3	10.0	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

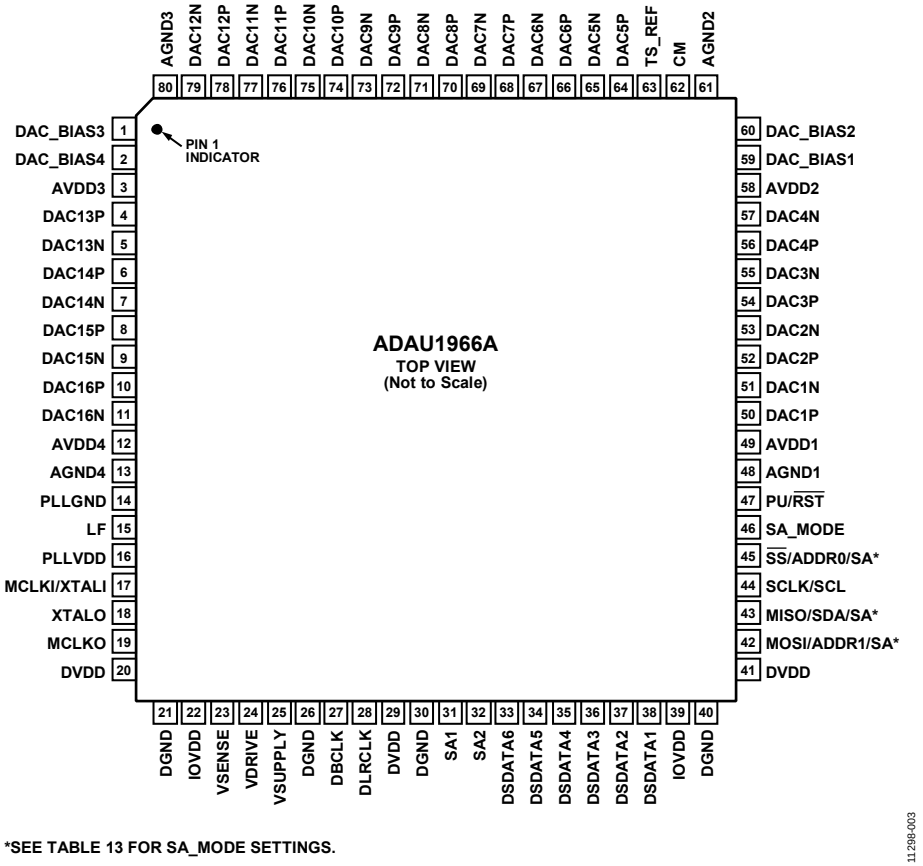


Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic[1, 2]	Type[3]	Description
1	DAC_BIAS3	I	DAC Bias 3. AC couple with a 470 nF to AGND3.
2	DAC_BIAS4	I	DAC Bias 4. AC couple with a 470 nF to AVDD3.
3	AVDD3	PWR	Analog Power.
4	DAC13P	O	DAC13 Positive Output.
5	DAC13N	O	DAC13 Negative Output.
6	DAC14P	O	DAC14 Positive Output.
7	DAC14N	O	DAC14 Negative Output.
8	DAC15P	O	DAC15 Positive Output.
9	DAC15N	O	DAC15 Negative Output.
10	DAC16P	O	DAC16 Positive Output.
11	DAC16N	O	DAC16 Negative Output.
12	AVDD4	PWR	Analog Power.
13	AGND4	GND	Analog Ground.
14	PLLGND	GND	PLL Ground.
15	LF	O	PLL Loop Filter. Reference the LF pin to PLLVDD.
16	PLLVDD	PWR	PLL Power. Apply 2.5 V to power the PLL.
17	MCLKI/XTALI	I	Master Clock Input/Input to Crystal Inverter. This is a multifunction pin.
18	XTALO	O	Output from Crystal Inverter.
19	MCLKO	O	Master Clock Output.

Pin No.	Mnemonic[1, 2]	Type[3]	Description
20, 29, 41	DVDD	PWR	Digital Power, 2.5 V.
21, 26, 30, 40	DGND	GND	Digital Ground.
22, 39	IOVDD	PWR	Power for Digital Input and Output Pins, 3.3 V.
23	VSENSE	I	2.5 V Regulator Output, Pass Transistor Collector. Bypass VSENSE with a 10 µF capacitor in parallel with a 100 nF capacitor.
24	VDRIVE	O	Pass Transistor Base Driver.
25	VSUPPLY	I	3.3 V Voltage Regulator Input , Pass Transistor Emitter . Bypass VSUPPLY with a 10 µF capacitor in parallel with a 100 nF capacitor.
27	DBCLK	I/O	Bit Clock for DACs.
28	DLRCLK	I/O	Frame Clock for DACs.
31	SA1	I	Standalone Mode, Time Domain Multiplexed (SA_MODE TDM) State. See the Standalone Mode section, Table 13, and Table 14, for more information.
32	SA2	I	Standalone Mode, Time Domain Multiplexed (SA_MODE TDM) State. See the Standalone Mode section, Table 13, and Table 14, for more information.
33	DSDATA6	I	DAC11 and DAC 12 Serial Data Input.
34	DSDATA5	I	DAC9 and DAC 10 Serial Data Input.
35	DSDATA4	I	DAC7 and DAC 8 Serial Data Input.
36	DSDATA3	I	DAC5 and DAC 6 Serial Data Input.
37	DSDATA2	I	DAC3 and DAC 4 Serial Data Input.
38	DSDATA1	I	DAC1 and DAC 2 Serial Data Input.
42	MOSI/ADDR1/SA	I	Master Output Slave Input (SPI)/Address 1 (I^2C)/SA_MODE State (see the Standalone Mode section and Table 13).
43	MISO/SDA/SA	I/O	Master Output Slave Input (SPI)/Control Data Input (I^2C)/SA_MODE State (see the Standalone Mode section and Table 13).
44	SCLK/SCL	I	Serial Clock Input (SPI)/Control Clock Input (I^2C).
45	$\overline{SS}$/ADDR0/SA	I	Slave Select (SPI) (Active Low)/Address 0 (I^2C)/SA_MODE State (see the Standalone Mode section and Table 13).
46	SA_MODE	I	Standalone Mode. This pin allows mode control of ADAU1966A using Pin 42, Pin 43, Pin 45, Pin 31, and Pin 32 (high active). See Table 13 and Table 14 for more information).
47	PU/$\overline{RST}$	I	Power-Up/Reset (Active Low). See Power-Up and Reset section for more information.
48	AGND1	GND	Analog Ground.
49	AVDD1	PWR	Analog Power.
50	DAC1P	O	DAC1 Positive Output.
51	DAC1N	O	DAC1 Negative Output.
52	DAC2P	O	DAC2 Positive Output.
53	DAC2N	O	DAC2 Negative Output.
54	DAC3P	O	DAC3 Positive Output.
55	DAC3N	O	DAC3 Negative Output.
56	DAC4P	O	DAC4 Positive Output.
57	DAC4N	O	DAC4 Negative Output.
58	AVDD2	PWR	Analog Power.
59	DAC_BIAS1	I	DAC Bias 1. AC couple Pin 59 with a 470 nF capacitor to AVDD2.
60	DAC_BIAS2	I	DAC Bias 2. AC couple Pin 60 with a 470 nF capacitor to AGND2.
61	AGND2	GND	Analog Ground.
62	CM	O	Common-Mode Reference Filter Capacitor Connection. Bypass the CM pin with a 10 µF capacitor in parallel with a 100 nF capacitor to AGND2. This reference can be shut off in the PLL_CLK_CTRL1 register (Register 0x01) and the pin can be driven with an outside voltage source.
63	TS_REF	O	Voltage Reference Filter Capacitor Connection. Bypass Pin 63 with a 10 µF capacitor in parallel with a 100 nF capacitor to AGND2.
64	DAC5P	O	DAC5 Positive Output.
65	DAC5N	O	DAC5 Negative Output.
66	DAC6P	O	DAC6 Positive Output.
67	DAC6N	O	DAC6 Negative Output.
68	DAC7P	O	DAC7 Positive Output.

Pin No.	Mnemonic[1, 2]	Type[3]	Description
69	DAC7N	O	DAC7 Negative Output.
70	DAC8P	O	DAC8 Positive Output.
71	DAC8N	O	DAC8 Negative Output.
72	DAC9P	O	DAC9 Positive Output.
73	DAC9N	O	DAC9 Negative Output.
74	DAC10P	O	DAC10 Positive Output.
75	DAC10N	O	DAC10 Negative Output.
76	DAC11P	O	DAC11 Positive Output.
77	DAC11N	O	DAC11 Negative Output.
78	DAC12P	O	DAC12 Positive Output.
79	DAC12N	O	DAC12 Negative Output.
80	AGND3	GND	Analog Ground.

[1] AVDD1, AVDD2, AVDD3, and AVDD4 are referred to elsewhere in this document as AVDDx when AVDDx means any or all of the ADVD pins.
[2] DAC Channel 1 to DAC Channel 12 pins are referred to elsewhere in this document as DACx, DACxP, or DACxN when it means any or all of the DAC channel pins.
[3] I = input, O = output, I/O = input/output, PWR = power, and GND = ground.

TYPICAL PERFORMANCE CHARACTERISTICS

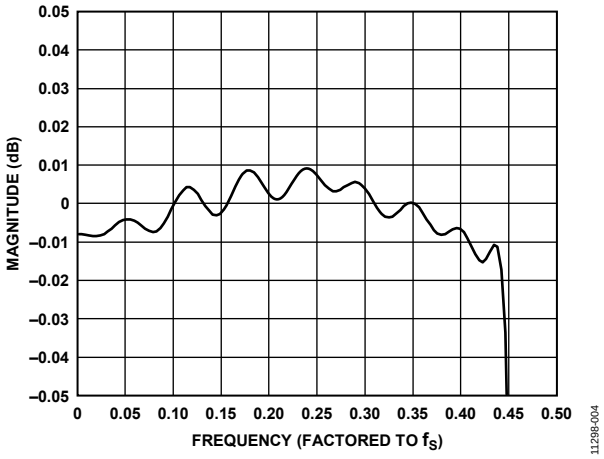


Figure 4. DAC Pass-Band Filter Response, 48 kHz

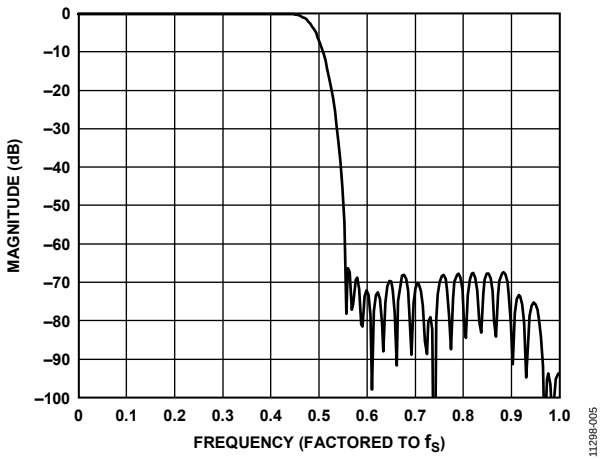


Figure 5. DAC Stop-Band Filter Response, 48 kHz

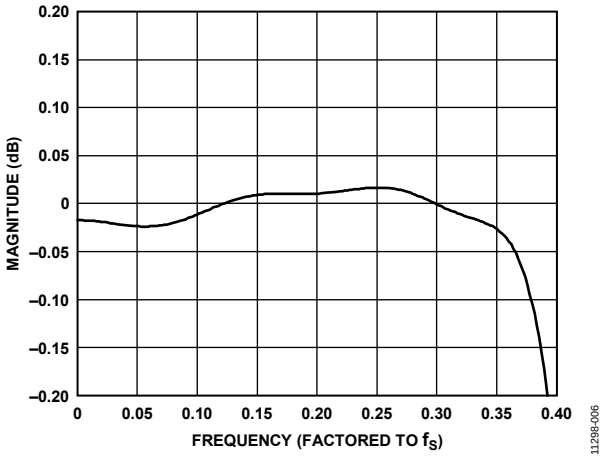


Figure 6. DAC Pass-Band Filter Response, 96 kHz

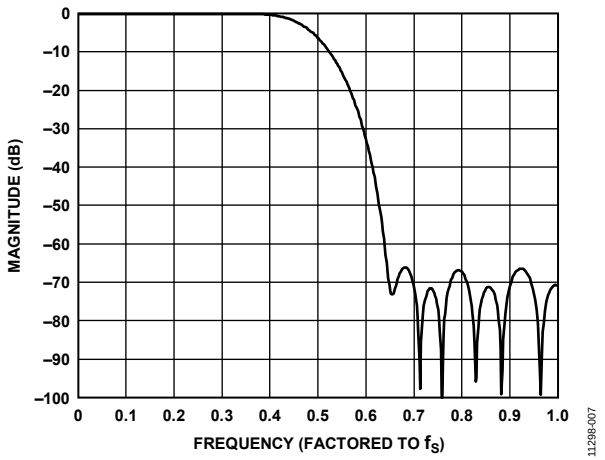


Figure 7. DAC Stop-Band Filter Response, 96 kHz

TYPICAL APPLICATION CIRCUITS

Typical application circuits are shown in Figure 8 to Figure 13. Recommended loop filters for DLRCLK and MCLKI/XTALI modes of the PLL reference are shown in Figure 8. Output filters for the DAC outputs are shown in Figure 10 to Figure 13, and an external regulator circuit is shown in Figure 9. When pins for multiple outputs are referred to generically in this datasheet, there is an x in place of the number. For example, DACxP refers to DAC1P through DAC16P.

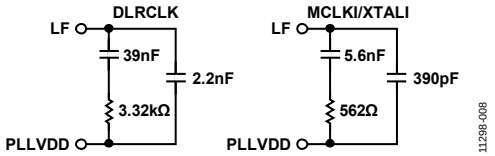


Figure 8. Recommended Loop Filters for DLRCLK and MCLKI/XTALI PLL Reference Modes

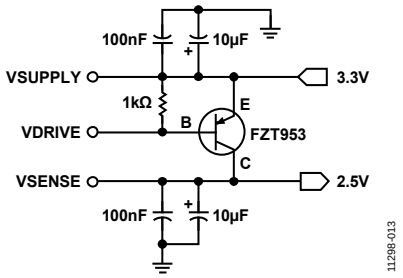


Figure 9. Recommended 2.5 V Regulator Circuit

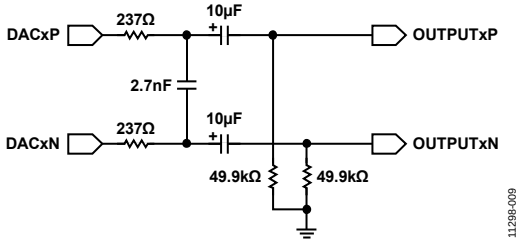


Figure 10. Typical DAC Output Passive Filter Circuit (Differential)

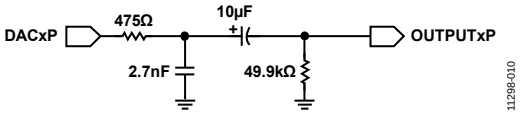


Figure 11. Typical DAC Output Passive Filter Circuit (Single-Ended)

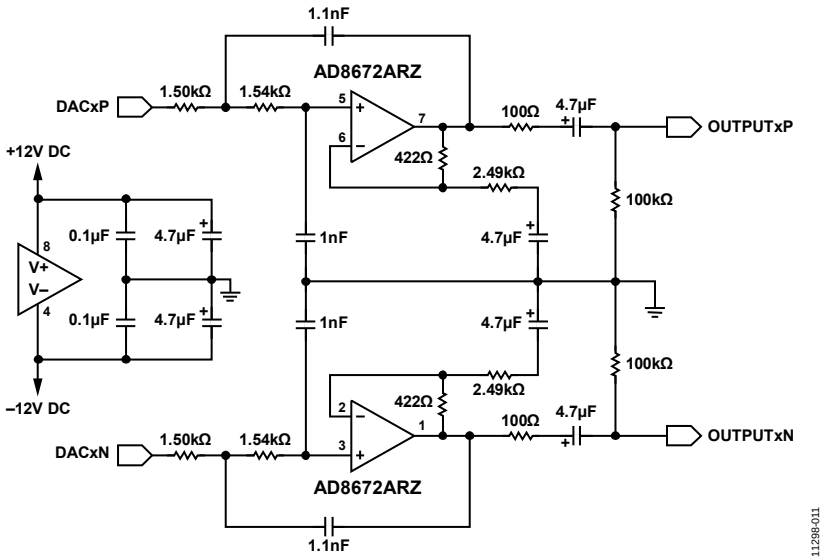


Figure 12. Typical DAC Output Active Filter Circuit (Differential)

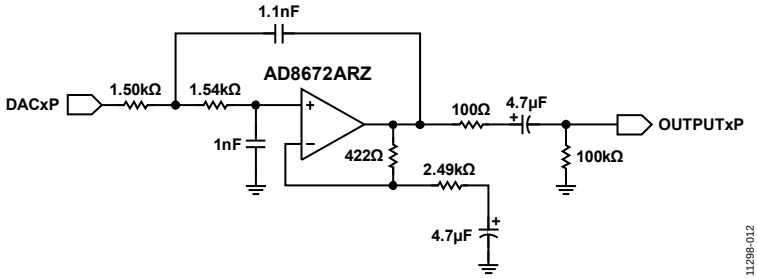


Figure 13. Typical DAC Output Active Filter Circuit (Single-Ended)

THEORY OF OPERATION

DACs

The 16 ADAU1966A DAC channels are differential for improved noise and distortion performance and are voltage output for simplified connection. The DACs include on-chip digital interpolation filters with 68 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 256× (48 kHz range), 128× (96 kHz range), or 64× (192 kHz range). Each channel has its own independently programmable attenuator, adjustable in 255 steps in increments of 0.375 dB. Digital inputs are supplied through six serial data input pins (two channels on each pin), a common frame clock (DLRCLK), and a bit clock (DBCLK). Alternatively, any one of the time domain multiplexed (TDM) modes can be used to access up to 16 channels on a single TDM data line.

The ADAU1966A has a low propagation delay mode; this mode is an option for an f_S of 192 kHz and is enabled in Register DAC_CTRL0[2:1]. By setting these bits to 0b11, the propagation delay is reduced by the amount listed in Table 6. The shorter delay is achieved by reducing the amount of digital filtering; the negative impact of selecting this mode is reduced audio frequency response and increased out-of-band energy.

Because AVDDx is supplied with 3.3 V, each analog output pin has a nominal common-mode (CM) dc level of 1.5 V. With a 0 dB full-scale digital input signal, each pin swings approximately ±1.42 V peak (2.83 V p-p and 2 V rms). Therefore, the voltage swing differentially across the two pins is 5.66 V p-p (4 V rms). The differential analog outputs require a single-order passive differential resistor-capacitor (RC) filter only to provide the specified DNR performance; see Figure 10 or Figure 11 for an example filter. The outputs can easily drive differential inputs on a separate printed circuit board (PCB) through cabling as well as differential inputs on the same PCB.

If more signal level is required, or if a more robust filter is needed, a single op amp gain stage designed as a second-order, low-pass Bessel filter can be used to remove the high frequency out-of-band noise present on each pin of the differential outputs. The choice of components and design of this circuit is critical to yield the full DNR of the DACs (see the recommended passive and active circuits in Figure 10, Figure 11, Figure 12, and Figure 13). The differential filter can be built into an active difference amplifier to provide a single-ended output with gain, if necessary. Note that the use of op amps with low slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band; exercise care when selecting these components.

The ADAU1966A offers control over the analog performance of the DACs; it is possible to program the registers to reduce the power consumption with the trade-off of lower SNR and THD + N. The reduced power consumption is the result of changing the internal bias current to the analog output amplifiers.

Register DAC_POWER1 to Register DAC_POWER4 present four basic settings for the DAC power vs. performance in each of the 16 channels: best performance, good performance, low power, and lowest power. Alternatively, in Register PLL_CLK_CTRL1[7:6], the LOPWR_MODE bits offer global control over the power and performance for all 16 channels. To select the low power or lowest power settings, set Bit 7 and Bit 6 of the DAC_POWERx registers to 0b10 or 0b11, respectively. The default setting is 0b00. This setting allows the channels to be controlled individually using the DAC_POWERx registers. The data presented in Table 11 shows the result of setting all 16 channels to each of the four settings. The SNR and THD + N specifications are shown in relation to the measured performance of a device at the best performance setting.

The voltage at CM, the common-mode reference pin, can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

CLOCK SIGNALS

Upon powering the ADAU1966A and asserting the PU/$\overline{\text{RST}}$ pin high, the part starts in either standalone mode (SA_MODE) or program mode, depending on the state of SA_MODE (Pin 46). The clock functionality of SA_MODE is described in the Standalone Mode section.

In program mode, the default for the ADAU1966A is for the MCLKO pin to feed a buffered output of the MCLKI signal on the MCLKI/XTALI pin. The default for the DLRCLK and DBCLK ports is slave mode; the DAC must be driven with a coherent set of master clock, frame clock, and bit clock signals to function.

The MCLKO pin can be programmed to provide different clock signals using Register PLL_CLK_CTRL1[5:4]. The default, 0b10, provides a buffered copy of the clock signal that is driving the MCLKI pin. Two modes, 0b00 and 0b01, provide low jitter clock signals.

The b00 setting yields a clock rate between 4 MHz and 6 MHz, and the b01 setting yields a clock rate between 8 MHz and 12 MHz. Both of these clock frequencies are scaled as ratios of the master clock automatically inside the ADAU1966A. As an example, an input to MCLKI of 8.192 MHz and a setting of 0b00 yield an MCLKO of (8.192/2) = 4.096 MHz. Alternatively, an input to MCLKI of 36.864 MHz and a setting of 0b01 yield an MCLKO frequency of (36.864/3) = 12.288 MHz. The 0b11 setting disables the MCLKO pin.

Table 11. DAC Power vs. Performance

Register Setting	Best Performance	Good Performance	Low Power	Lowest Power
Total AVDDx Current	60 mA	53 mA	47 mA	40 mA
SNR	Reference	−0.2 dB	−1.5 dB	−14.2 dB
THD + N (−1 dBFS Signal)	Reference	−1.8 dB	−3.0 dB	−5.8 dB

After the PU/$\overline{\text{RST}}$ pin is asserted high, the PLL_CLK_CTRLx registers (Register 0x00 and Register 0x01) can be programmed. The on-chip PLL can be selected to use the clock appearing at the MCLKI/XTALI pin at a frequency of 256, 384, 512, or 768 times the sample rate (f_S), referenced to the 48 kHz mode from the master clock select (MCS) setting, as described in Table 12.

In 96 kHz mode, the master clock frequency stays at the same absolute frequency; therefore, the actual multiplication rate is divided by 2. In 192 kHz mode, the actual multiplication rate is divided by 4.

For example, if the ADAU1966A is programmed in 256 × f_S mode, the frequency of the master clock input is 256 × 48 kHz = 12.288 MHz. If the ADAU1966A is then switched to 96 kHz operation (by writing to DAC_CTRL0[2:1]), the frequency of the master clock remains at 12.288 MHz, which is an MCS ratio of 128 × f_S in this example. Therefore, in 192 kHz mode, MCS becomes 64 × f_S. The internal clock for the digital core varies by mode: 512 × f_S (48 kHz mode), 256 × f_S (96 kHz mode), or 128 × f_S (192 kHz mode). By default, the on-board PLL generates this internal master clock from an external clock.

The PLL must be powered and stable before using the ADAU1966A as a source for quality audio. The PLL is enabled by reset and does not require writing to the I²C or SPI port for normal operation.

With the PLL enabled, the performance of the ADAU1966A is not affected by jitter as high as a 300 ps rms time interval error (TIE). When the internal PLL is disabled, use an independent crystal oscillator to generate the master clock.

When using the ADAU1966A in direct master clock mode, power down the PLL in the PDN_THRMSENS_CTRL_1 register. For direct master clock mode, a frequency of 512 × f_S (referenced to 48 kHz mode) must be fed into the MCLKI pin, and the CLK_SEL bit in the PLL_CLK_CTRL1 register must be set to 1. However, for the device to function, 2.5 V power must be connected to the PLLVDD pin.

The PLL of the ADAU1966A can also be programmed to run from an external LRCLK without an external master clock. Setting the PLLIN bits in the PLL_CLK_CTRL0 register to 0b01 and connecting the appropriate loop filter to the LF pin (see Figure 8), the ADAU1966A PLL generates all of the necessary internal clocks for operation with no external master clock. This mode reduces the number of high frequency signals in the design, reducing EMI emissions.

It is possible to further reduce EMI emissions of the circuit by using the internal bit clock generation setting of the BCLK_GEN bit in the DAC_CTRL1 register. Setting the BCLK_GEN bit to 1 (internal) and the SAI_MS bit to 0 (slave), the ADAU1966A generates its own bit clock; this configuration works with the PLL input register (PLL_CLK_CTRL0[7:6]) set to either MCLKI/XTALI or DLRCLK. The clock on the DLRCLK pin is the only required clock in DLRCLK PLL mode.

Table 12. MCS and f_S Modes

Frequency Sample Select DAC_CTRL0[2:1]		Master Clock Select (MCS), PLL_CLK_CTRL0[2:1]							
		Setting 0, 0b00		Setting 1, 0b01		Setting 2, 0b10		Setting 3, 0b11	
f_S (kHz)	Bit Setting	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)
32 kHz,	0b00	256 × f_S	8.192	384 × f_S	12.288	512 × f_S	16.384	768 × f_S	24.576
44.1 kHz	0b00	256 × f_S	11.2896	384 × f_S	16.9344	512 × f_S	22.5792	768 × f_S	33.8688
48 kHz	0b00	256 × f_S	12.288	384 × f_S	18.432	512 × f_S	24.576	768 × f_S	36.864
64 kHz	0b01	128 × f_S	8.192	192 × f_S	12.288	256 × f_S	16.384	384 × f_S	24.576
88.2 kHz	0b01	128 × f_S	11.2896	192 × f_S	16.9344	256 × f_S	22.5792	384 × f_S	33.8688
96 kHz	0b01	128 × f_S	12.288	192 × f_S	18.432	256 × f_S	24.576	384 × f_S	36.864
128 kHz	0b10 or 0b11	64 × f_S	8.192	96 × f_S	12.288	128 × f_S	16.384	192 × f_S	24.576
176.4 kHz	0b10 or 0b11	64 × f_S	11.2896	96 × f_S	16.9344	128 × f_S	22.5792	192 × f_S	33.8688
192 kHz	0b10 or 0b11	64 × f_S	12.288	96 × f_S	18.432	128 × f_S	24.576	192 × f_S	36.864

POWER-UP AND RESET

The power sequencing for the ADAU1966A begins with AVDDx and IOVDD, followed by DVDD. It is very important that AVDDx be settled at a regulated voltage and that IOVDD be within 10% of regulated voltage before applying DVDD. When using the internal regulator of the ADAU1966A, this timing occurs by default.

To guarantee proper startup, pull the PU/$\overline{\text{RST}}$ pin low by an external resistor and then drive it high after the power supplies have stabilized. The PU/$\overline{\text{RST}}$ can also be pulled high using a simple RC network.

Driving the PU/$\overline{\text{RST}}$ pin low puts the part into a very low power state (<3 µA). All functionality of the ADAU1966A is disabled until the PU/$\overline{\text{RST}}$ pin is asserted high. Once this pin is asserted high, the ADAU1966A requires 300 ms to stabilize. The MMUTE bit in the DAC_CTRL0 register must be toggled for operation.

The PUP (master power-up control) bit in the PLL_CLK_CTRL0 register can be used to power down the ADAU1966A. Setting the PUP bit to 0 puts the ADAU1966A in an idle state while maintaining the settings of all registers. Additionally, the power-down bits in the PDN_THRMSENS_CTRL_1 register (TS_PDN, PLL_PDN, and VREG_PDN) can be used to power down individual sections of the ADAU1966A.

The SOFT_RST bit in the PLL_CLK_CTRL0 register sets all of the control registers to their default settings while maintaining the internal clocks in default mode. The SOFT_RST bit does not power down the analog outputs; nor does toggling this bit cause audible popping sounds at the differential analog outputs.

For proper startup of the ADAU1966A, follow these steps:

1. Apply power to the ADAU1966A as described previously in this Power-Up and Reset section.
2. Assert the PU/$\overline{\text{RST}}$ pin high after power supplies are stable.
3. Set the PUP bit to 1.
4. Program all necessary registers for the desired settings.
5. Set the MMUTE bit to 0 to unmute all channels.

STANDALONE MODE

The ADAU1966A can operate without a typical I²C or SPI connection to a microcontroller. This standalone mode is available by setting SA_MODE (Pin 46) to IOVDD. All registers are set to default except for the options shown in Table 13.

Table 13. SA_MODE Settings

Pin No.	Setting	Function
42	0	Master mode serial audio interface (SAI)
	1	Slave mode SAI
43	0	MCLK = 256 × f_S, PLL on
	1	MCLK = 384 × f_S, PLL on
45	0	I²S SAI format
	1	TDM modes, determined by Pin 31 and Pin 32

When both SA_MODE (Pin 46) and $\overline{\text{SS}}$/ADDR0/SA (Pin 45) are set high, TDM mode is selected. Table 14 shows the available TDM modes; these modes are set by connecting Pin 31 (SA1) and Pin 32 (SA2) to GND or IOVDD.

Table 14. TDM Modes

Pin No.	Setting	Function
31 to 32	00	TDM4, DLRCLK pulse
	01	TDM8, DLRCLK pulse
	10	TDM16, DLRCLK pulse
	11	TDM8, DLRCLK 50% duty cycle

By powering up the ADAU1966A in SA_MODE, and asserting the PU/$\overline{\text{RST}}$ pin high, the MCLKO pin provides a buffered version of the MCLKI/XTALI pin, whether the source is a crystal or an active oscillator.

I²C CONTROL PORT

The ADAU1966A has an I²C-compatible control port that permits programming and readback of the internal control registers for the DACs and clock system. The I²C interface of the ADAU1966A is a 2-wire interface consisting of a clock line, SCL, and a data line, SDA. SDA is bidirectional, and the ADAU1966A drives SDA either to acknowledge the master (ACK) or to send data during a read operation. The SDA pin (MISO/SDA/SA) for the I²C port is an open-drain collector and requires a 2 kΩ pull-up resistor. A write or read access occurs when the SDA line is pulled low while the SCL line (SCLK/SCL) is high, indicated by a start in Figure 14 and and Figure 15.

SDA is only allowed to change when SCL is low, except when a start or stop condition occurs, as shown in Figure 14 and Figure 15. The first eight bits of the data-word consist of the device address and the R/$\overline{\text{W}}$ bit. The device address consists of an internal built-in address (0x04) and two address bits, ADDR1 and ADDR0. The two address bits allow four ADAU1966A devices to be used in a system.

Table 15. I²C Addresses

ADDR1 (AD1)	ADDR0 (AD0)	Slave Address
0	0	0x04
0	1	0x24
1	0	0x44
1	1	0x64

I²C Write

Initiating a write operation to the ADAU1966A involves the following steps (see Figure 14):

1. Send a start condition
2. Send the device address with the R/$\overline{W}$ bit set low.
   a. The ADAU1966A responds by issuing an acknowledge to indicate that it has been addressed.
3. Send a second frame directing the ADAU1966A to which register is required to be written.
   a. A second acknowledge is issued by the ADAU1966A.
4. Send a third frame with the eight data bits required to be written to the register.
   a. A third acknowledge is issued by the ADAU1966A.
5. Send a stop condition to complete the data transfer.

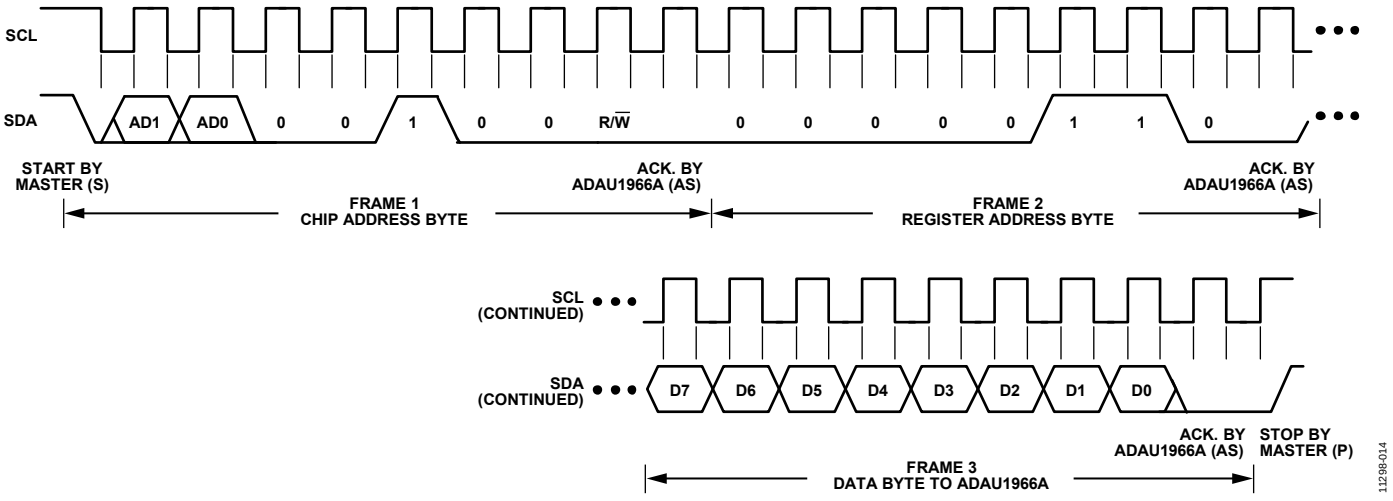


Figure 14. I²C Write Format

Table 16. I²C Abbreviations

Abbreviation	Condition
S	Start bit
P	Stop bit
AM	Acknowledge by master
AS	Acknowledge by slave

Table 17. Single Word I²C Write

S	Chip Address, R/$\overline{W}$ = 0	AS	Register Address	AS	Data-Word	AS	P

Table 18. Burst Mode I²C Write

S	Chip Address, R/$\overline{W}$ = 0	AS	Register Address	AS	Data-Word 1	AS	Data-Word 2	AS	Data-Word N	AS	P

I²C Read

A read operation requires that the user first write to the ADAU1966A to point to the correct register and then read the data. The following steps achieve this (see Figure 15):

1. Send a start condition followed by the device address frame with the R/$\overline{W}$ bit low and then the register address frame.
   a. The ADAU1966A responds with an acknowledge.
2. Issue a repeated start condition.
   a. The next frame is the device address with the R/$\overline{W}$ bit set high.
   b. On the next frame, the ADAU1966A outputs the register data on the SDA line.
3. Issue a stop condition to complete the read operation.

Table 19. Single Word I²C Read

S	Chip Address, R/$\overline{W}$ = 0	AS	Register Address	AS	S	Chip Address, R/$\overline{W}$ = 1	AS	Data-Word	AM	P

Table 20. Burst Mode I²C Read

S	Chip Address, R/$\overline{W}$ = 0	AS	Register Address	AS	S	Chip Address, R/$\overline{W}$ = 1	AS	Data-Word 1	AM	Data-Word 2	AM	Data-Word N	AM	P

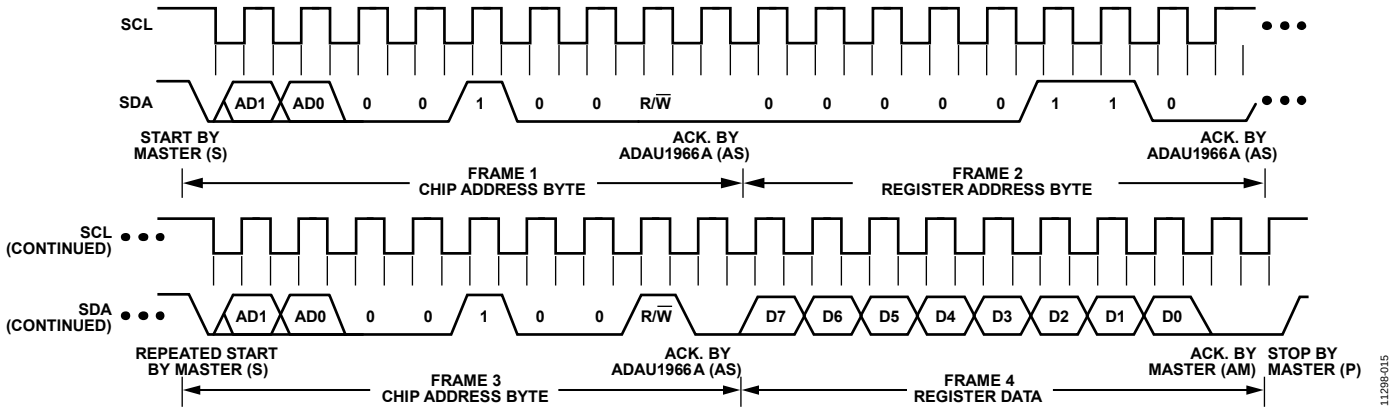


Figure 15. I²C Read Format

SERIAL CONTROL PORT: SPI CONTROL MODE

The ADAU1966A has a 4-wire SPI control port that permits the programming and reading back of the internal control registers for the DACs and clock system. A standalone mode is also available for operation without serial control; it is configured at reset using the SA_MODE pin. See the Standalone Mode section for details about the SA_MODE pin.

By default, the ADAU1966A is in I²C mode; however, it can be put into SPI control mode by pulling $\overline{SS}$ low three times. This is done by performing three dummy writes to the SPI port (the ADAU1966A does not acknowledge these three writes, see Figure 16). Beginning with the fourth SPI write, data can be written to or read from the IC. The ADAU1966A can only be taken out of SPI control mode by a full reset initiated by power cycling the device.

The format is a 24-bit wide data-word. The serial bit clock and latch can be completely asynchronous to the sample rate of the DACs. The first byte is a global address with a read/write bit. For the ADAU1966A, the address is 0x06, shifted left one bit due to the R/$\overline{W}$ bit. The second byte is the ADAU1966A register address, and the third byte is the data, as shown in Figure 17 and Figure 18. When reading data from the ADAU1966A, MISO is tristated until the third byte where it drives data out (see Figure 18). MISO is tristated at all other times, allowing it to be bused with other devices. The timing requirements are shown in Figure 19.

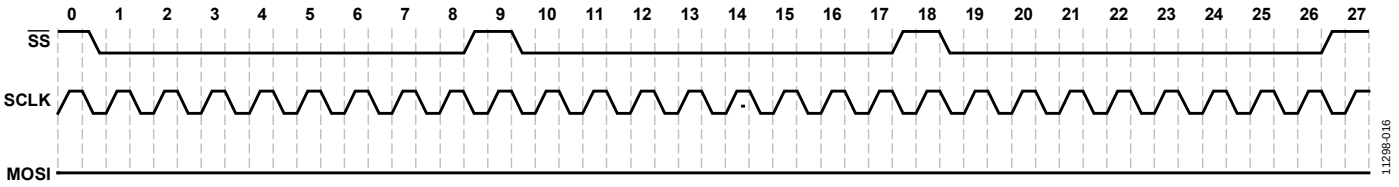


Figure 16. SPI Mode Initial Sequence

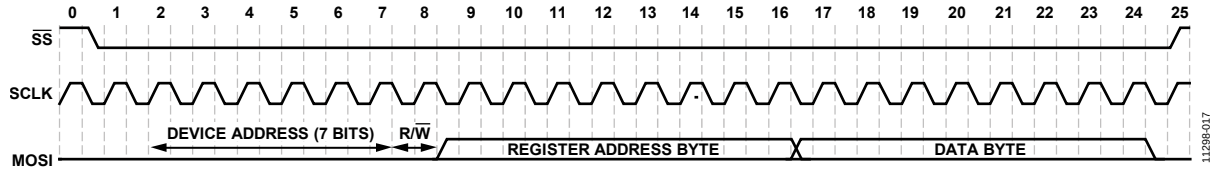


Figure 17. SPI Write to ADAU1966A Clocking

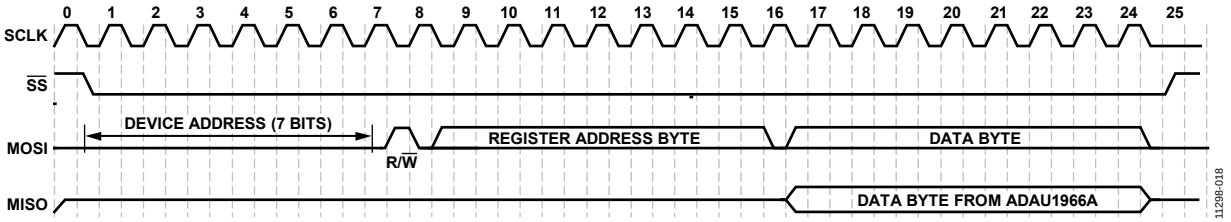


Figure 18. SPI Read from ADAU1966A Clocking

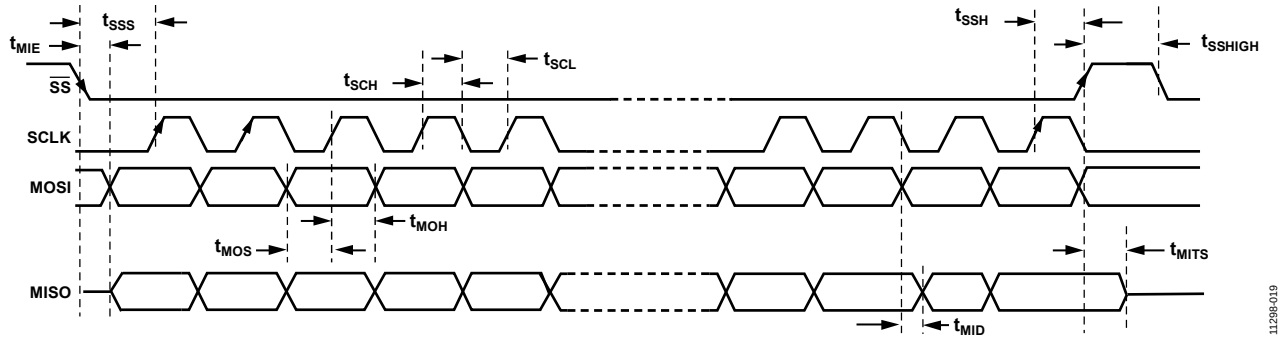


Figure 19. SPI Signal Timing

Chip Address R/$\overline{W}$

The LSB of the first byte of an SPI transaction is a R/$\overline{W}$ bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 21.

Table 21. ADAU1966A SPI Address and R/$\overline{W}$ Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	0	0	1	1	0	R/$\overline{W}$

SPI Burst Read/Write

The SPI port is capable of performing burst reads or writes by sending the chip address byte with the R/$\overline{W}$ bit followed by the first register address that needs to be read from or written to. Then, as long as the $\overline{SS}$ pin is held low, the user can sequentially read from or write to the registers by continuing to send clock pulses into the SCLK pin. An efficient way to initialize the ADAU1966A is by

- Sending out the address byte with the R/$\overline{W}$ bit low (write)
- Sending out the address of the first register
- Sending out all the register byte values
- Toggling $\overline{SS}$ to end the transfer
- Performing a burst read to verify that the register writes were successful

When referencing back to Analog Devices legacy devices, different pin names (mnemonics) were used for these SPI port functions. See Table 22 for details of the changes.

Table 22. SPI Port Pin Naming Conventions

Pin No.	Legacy Pin Mnemonic	New Pin Mnemonic
42	CDATA	MOSI
43	COUT	MISO
44	CCLK	SCLK
45	$\overline{CLATCH}$	$\overline{SS}$

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1966A is designed for 3.3 V analog and 2.5 V digital supplies. To minimize noise pickup, bypass the power supply pins with 100 nF ceramic chip capacitors placed as close to the pins as possible. Provide a bulk aluminum electrolytic capacitor of at least 22 µF for each rail on the same PCB as the codec. It is important that the analog supply be as clean as possible.

The ADAU1966A includes a 2.5 V regulator driver that requires only an external pass transistor and bypass capacitors to make a 2.5 V regulator from a 3.3 V supply. Decouple the VSUPPLY and VSENSE pins with no more than 10 µF of capacitance in parallel with 100 nF high frequency bypassing. If the regulator driver is not used, connect VSUPPLY and VDRIVE to GND and leave VSENSE unconnected.

The temperature sensor internal voltage reference (V_{TS_REF}) is connected to the TS_REF pin and must be bypassed as close as possible to the chip with a parallel combination of 10 µF and 100 nF capacitors.

The internal band gap reference can be disabled in the PLL_CLK_CTRL1 register by setting VREF_EN to 0; the CM pin can be then be driven from an external source. This can be used to scale the DAC output to the clipping level of a power amplifier based on its power supply voltage.

The CM pin is the internal common-mode reference. Bypass it as close as possible to the chip with a parallel combination of 10 µF and 100 nF capacitors. This voltage can be used to bias external op amps to the common-mode voltage of the analog input and output signal pins. It is recommended that the CM pin be isolated from the external circuitry by using a high quality buffer to provide a quiet, low impedance source for the external circuitry. Use of a quiet op amp is critical because any noise added to the reference voltage is injected into the signal path.

SERIAL DATA PORTS—DATA FORMAT

The 16 DAC channels use a common serial bit clock (DBCLK) and a common left-right framing clock (DLRCLK) in the serial data port. The clock signals are all synchronous with the sample rate. The normal stereo serial modes are shown in Figure 20.

The DAC serial data mode defaults to I^2S (1 BCLK delay) upon power-up and reset. The ports can also be programmed for left justified and right justified (24-bit and 16-bit) operation using DAC_CTRL0[7:6]. Stereo and TDM modes can be selected using DAC_CTRL0[5:3]. The polarity of DBCLK and DLRCLK is programmable according to the DAC_CTRL1[1] and DAC_CTRL1[5] bits. The serial ports are programmable as the clock masters according to the DAC_CTRL1[0] bit. By default, the serial port is in slave mode.

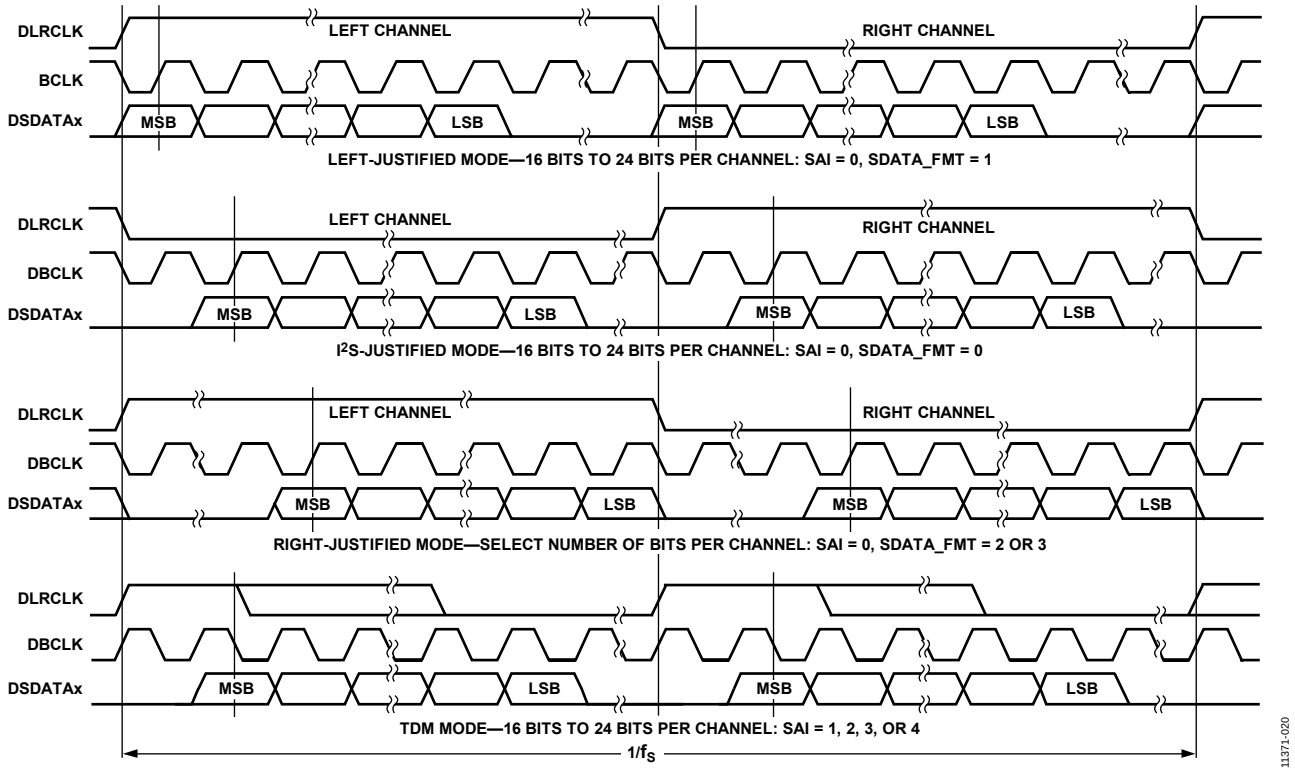


Figure 20. Stereo Serial Audio Modes

TIME-DIVISION MULTIPLEXED (TDM) MODES

The ADAU1966A serial ports also have several different TDM serial data modes. The ADAU1966A can support a single data line (TDM16), a dual data line (TDM8), a quad data line (TDM4), or eight data lines (TDM2). The DLRCLK/frame clock can operate in both single-cycle pulse mode and a 50% duty cycle mode. Both 16 DBCLKs and 32 DBCLKs per channel are selectable for each mode.

The I/O pins of the serial ports are defined according to the serial mode that is selected. For a detailed description of the function of each pin in TDM and stereo modes, see Table 23.

TEMPERATURE SENSOR

The ADAU1966A has an on-board temperature sensor that allows the user to read the temperature of the silicon inside the device. The temperature sensor readout has a range of −60°C to +140°C in 1°C steps. The PDN_THRMSENS_CTRL_1 register controls the settings of the sensor. The temperature sensor is powered on by default and can be shut off by setting the TS_PDN[2] bit to 1 in the PDN_THRMSENS_CTRL_1 register. The temperature sensor can be run in either continuous operation or one-shot mode. The temperature sensor conversion mode is modified using THRM_MODE (Bit 5); the default is THRM_MODE = 1, one-shot mode. In one-shot mode, writing a 0 followed by writing a 1 to THRM_GO (Bit 4), results in a single reset and temperature conversion, placing the resulting temperature data in the THRM_TEMP_STAT register.

In continuous operation mode, the data conversion takes place at a rate set by THRM_RATE[7:6], with a range of 0.5 sec to 4 sec between samples. Faster rates are possible using one-shot mode.

Once a temperature conversion is placed in the THRM_TEMP_STAT register, the data can be translated into degrees Celsius (°C) using the following steps:

1. Convert the binary or hexadecimal data read from THRM_TEMP_STAT into decimal form.
2. Subtract 60 from the converted THRM_TEMP_STAT data; this is the temperature of the silicon in °C.

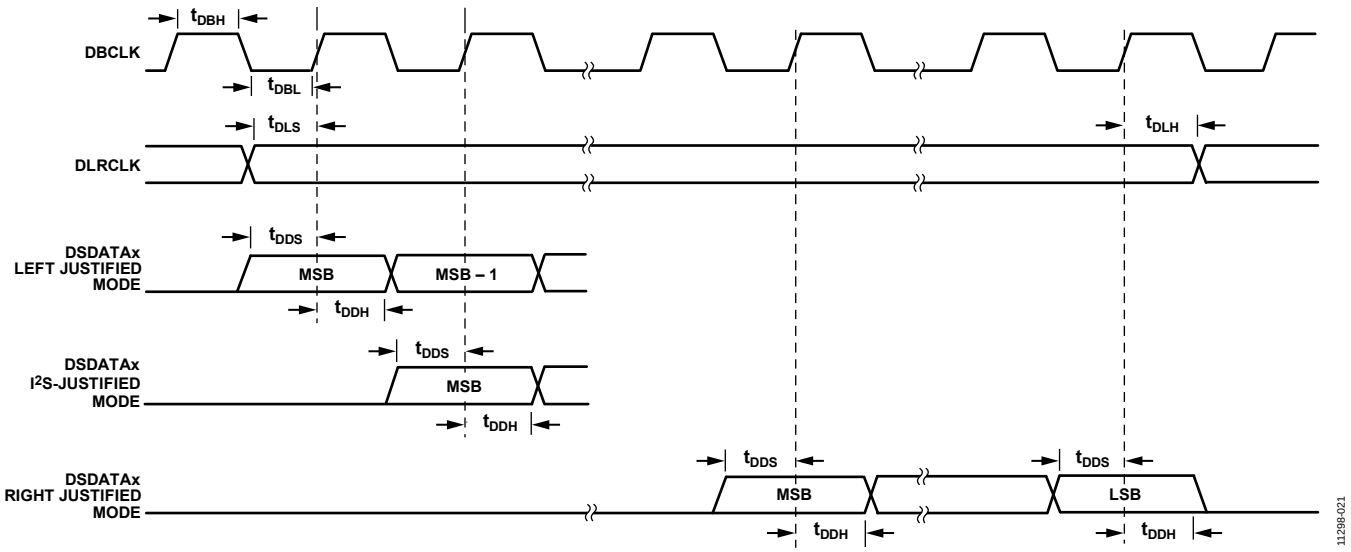


Figure 21. DAC Serial Timing

Table 23. Pin Function Changes in Different Serial Audio Interface Modes

Signal	Stereo Modes (SAI = 0 or SAI = 1)	TDM4 Mode (SAI = 2)	TDM8 Mode (SAI = 3)	TDM16 Mode (SAI = 4)
DSDATA1	Channel 1/Channel 2 data input	Channel 1 to Channel 4 data input	Channel 1 to Channel 8 data input	Channel 1 to Channel 16 data input
DSDATA2	Channel 3/Channel 4 data input	Channel 5 to Channel 8 data input	Channel 9 to Channel 16 data input	Not used
DSDATA3	Channel 5/Channel 6 data input	Channel 9 to Channel 12 data input	Not used	Not used
DSDATA4	Channel 7/Channel 8 data input	Channel 13 to Channel 16 data input	Not used	Not used
DSDATA5	Channel 9/Channel 10 data input	Not used	Not used	Not used
DSDATA6	Channel 11/Channel 12 data input	Not used	Not used	Not used
DSDATA7	Channel 13/Channel 14 data input	Not used	Not used	Not used
DSDATA8	Channel 15/Channel 16 data input	Not used	Not used	Not used
DLRCLK	DLRCLK input/DLRCLK output	TDM frame sync input/ TDM frame sync output	TDM frame sync input/ TDM frame sync output	TDM frame sync input/ TDM frame sync output
DBCLK	DBCLK input/DBCLK output	TDM DBCLK input/ TDM DBCLK output	TDM DBCLK input/ TDM DBCLK output	TDM DBCLK input/ TDM DBCLK output
Maximum Sample Rate	192 kHz	192 kHz	96 kHz	48 kHz

ADDITIONAL MODES

The ADAU1966A offers several additional modes for board level design enhancements. To reduce the EMI in board level design, serial data can be transmitted without an explicit bit clock input on the DBCLK pin. See Figure 22 for an example of a DAC TDM data transmission mode that does not require a high speed bit clock or an external master clock. This configuration is applicable when the ADAU1966A master clock is generated by the PLL with the DLRCLK pin as the PLL reference frequency.

To relax the requirement for the setup time of the ADAU1966A in cases of high speed TDM data transmission, the ADAU1966A can latch in the data using the falling edge of DBCLK pin; see the BCLK_EDGE bit in the DAC_CTRL1 register. This effectively dedicates the entire bit clock period to the setup time. This mode is useful when the source has a large delay time in the serial data driver. Figure 23 shows this inverted bit clock mode of data transmission.

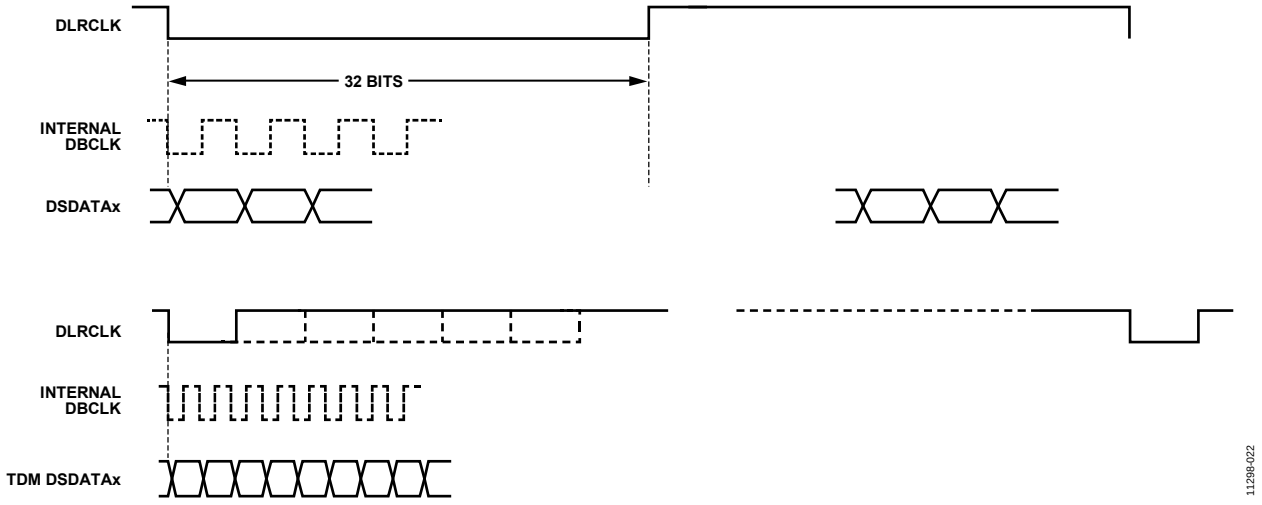


Figure 22. Serial DAC Data Transmission in TDM Format Without DBCLK (Applicable Only If PLL Locks to DLRCLK)

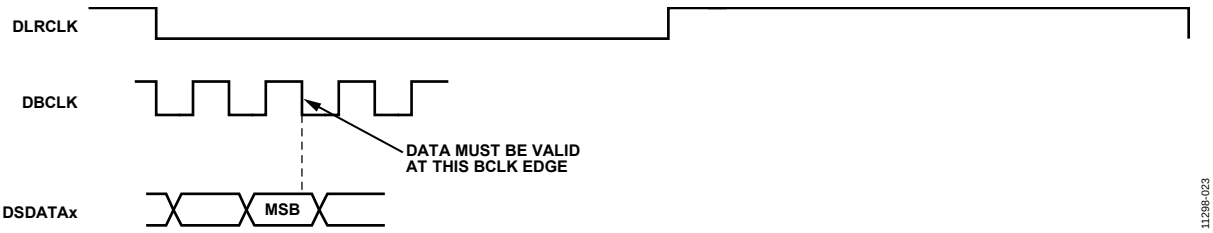


Figure 23. Inverted DBCLK Mode in DAC Serial Data Transmission (Applicable in Stereo and TDM, Useful for High Frequency TDM Transmission)

REGISTER SUMMARY

Table 24. ADAU1966A Register Summary

Reg. No.	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	PLL_CLK_CTRL0	[7:0]	PLLIN		XTAL_SET		SOFT_RST	MCS		PUP	0x00	RW
0x01	PLL_CLK_CTRL1	[7:0]	LOPWR_MODE		MCLKO_SEL		PLL_MUTE	PLL_LOCK	VREF_EN	CLK_SEL	0x2A	RW
0x02	PDN_THRMSENS_CTRL_1	[7:0]	THRM_RATE		THRM_MODE	THRM_GO	RESERVED	TS_PDN	PLL_PDN	VREG_PDN	0xA0	RW
0x03	PDN_CTRL2	[7:0]	DAC08_PDN	DAC07_PDN	DAC06_PDN	DAC05_PDN	DAC04_PDN	DAC03_PDN	DAC02_PDN	DAC01_PDN	0x00	RW
0x04	PDN_CTRL3	[7:0]	DAC16_PDN	DAC15_PDN	DAC14_PDN	DAC13_PDN	DAC12_PDN	DAC11_PDN	DAC10_PDN	DAC09_PDN	0x00	RW
0x05	THRM_TEMP_STAT	[7:0]	TEMP								0x00	R
0x06	DAC_CTRL0	[7:0]	SDATA_FMT		SAI			FS		MMUTE	0x01	RW
0x07	DAC_CTRL1	[7:0]	BCLK_GEN	LRCLK_MODE	LRCLK_POL	SAI_MSB	RESERVED	BCLK_RATE	BCLK_EDGE	SAI_MS	0x00	RW
0x08	DAC_CTRL2	[7:0]	RESERVED			BCLK_TDMC	DAC_POL	AUTO_MUTE_EN	DAC_OSR	DE_EMP_EN	0x06	RW
0x09	DAC_MUTE1	[7:0]	DAC08_MUTE	DAC07_MUTE	DAC06_MUTE	DAC05_MUTE	DAC04_MUTE	DAC03_MUTE	DAC02_MUTE	DAC01_MUTE	0x00	RW
0x0A	DAC_MUTE2	[7:0]	DAC16_MUTE	DAC15_MUTE	DAC14_MUTE	DAC13_MUTE	DAC12_MUTE	DAC11_MUTE	DAC10_MUTE	DAC09_MUTE	0x00	RW
0x0B	DACMSTR_VOL	[7:0]	DACMSTR_VOL								0x00	RW
0x0C	DAC01_VOL	[7:0]	DAC01_VOL								0x00	RW
0x0D	DAC02_VOL	[7:0]	DAC02_VOL								0x00	RW
0x0E	DAC03_VOL	[7:0]	DAC03_VOL								0x00	RW
0x0F	DAC04_VOL	[7:0]	DAC04_VOL								0x00	RW
0x10	DAC05_VOL	[7:0]	DAC05_VOL								0x00	RW
0x11	DAC06_VOL	[7:0]	DAC06_VOL								0x00	RW
0x12	DAC07_VOL	[7:0]	DAC07_VOL								0x00	RW
0x13	DAC08_VOL	[7:0]	DAC08_VOL								0x00	RW
0x14	DAC09_VOL	[7:0]	DAC09_VOL								0x00	RW
0x15	DAC10_VOL	[7:0]	DAC10_VOL								0x00	RW
0x16	DAC11_VOL	[7:0]	DAC11_VOL								0x00	RW
0x17	DAC12_VOL	[7:0]	DAC12_VOL								0x00	RW
0x18	DAC13_VOL	[7:0]	DAC13_VOL								0x00	RW
0x19	DAC14_VOL	[7:0]	DAC14_VOL								0x00	RW
0x1A	DAC15_VOL	[7:0]	DAC15_VOL								0x00	RW
0x1B	DAC16_VOL	[7:0]	DAC16_VOL								0x00	RW
0x1C	PAD_STRGTH	[7:0]	RESERVED		PAD_DRV	RESERVED					0x00	RW
0x1D	DAC_POWER1	[7:0]	DAC04_POWER		DAC03_POWER		DAC02_POWER		DAC01_POWER		0xAA	RW
0x1E	DAC_POWER2	[7:0]	DAC08_POWER		DAC07_POWER		DAC06_POWER		DAC05_POWER		0xAA	RW
0x1F	DAC_POWER3	[7:0]	DAC12_POWER		DAC11_POWER		DAC10_POWER		DAC09_POWER		0xAA	RW
0x20	DAC_POWER4	[7:0]	DAC16_POWER		DAC15_POWER		DAC14_POWER		DAC13_POWER		0xAA	RW

REGISTER DETAILS

PLL AND CLOCK CONTROL 0 REGISTER

Address: 0x00, Reset: 0x00, Name: PLL_CLK_CTRL0

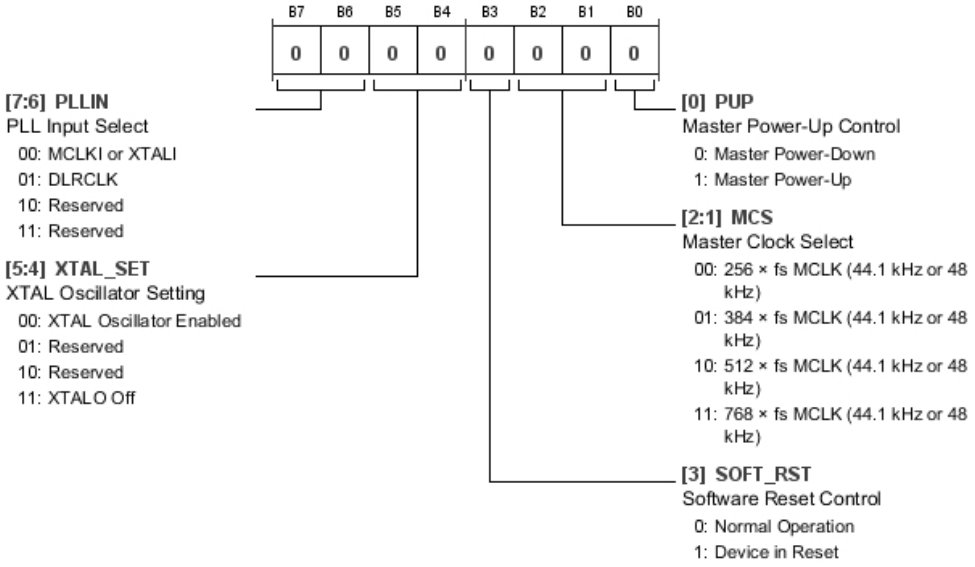


Table 25. Bit Descriptions for PLL_CLK_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	PLLIN		PLL Input Select. Selects between MCLKI/XTALI and DLRCLK as the input to the PLL.	0x0	RW
		00	MCLKI or XTALI.		
		01	DLRCLK.		
		10	Reserved.		
		11	Reserved.		
[5:4]	XTAL_SET		XTAL Oscillator Setting. XTALO pin status.	0x0	RW
		00	XTAL oscillator enabled.		
		01	Reserved.		
		10	Reserved.		
		11	XTALO Off.		
3	SOFT_RST		Software Reset Control. This bit resets all circuitry inside the IC, except I²C/SPI communications. All control registers are reset to default values, except Register 0x00 and Register 0x01. The PLL_CLK_CTRLx registers do not change state.	0x0	RW
		0	Normal Operation.		
		1	Device in Reset.		
[2:1]	MCS		Master Clock Select. MCLKI/XTALI pin functionality (PLL active), master clock rate setting. The following values are for the f_S rate range from 32 kHz to 48 kHz. See Table 12 for details when using other f_S selections.	0x0	RW
		00	256 × f_S MCLK (44.1 kHz or 48 kHz).		
		01	384 × f_S MCLK (44.1 kHz or 48 kHz).		
		10	512 × f_S MCLK (44.1 kHz or 48 kHz).		
		11	768 × f_S MCLK (44.1 kHz or 48 kHz).		
0	PUP		Master Power-Up Control. This bit must be set to 1 as the first register write to power up the IC.	0x0	RW
		0	Master Power-Down.		
		1	Master Power-Up.		

PLL AND CLOCK CONTROL 1 REGISTER

Address: 0x01, Reset: 0x2A, Name: PLL_CLK_CTRL1

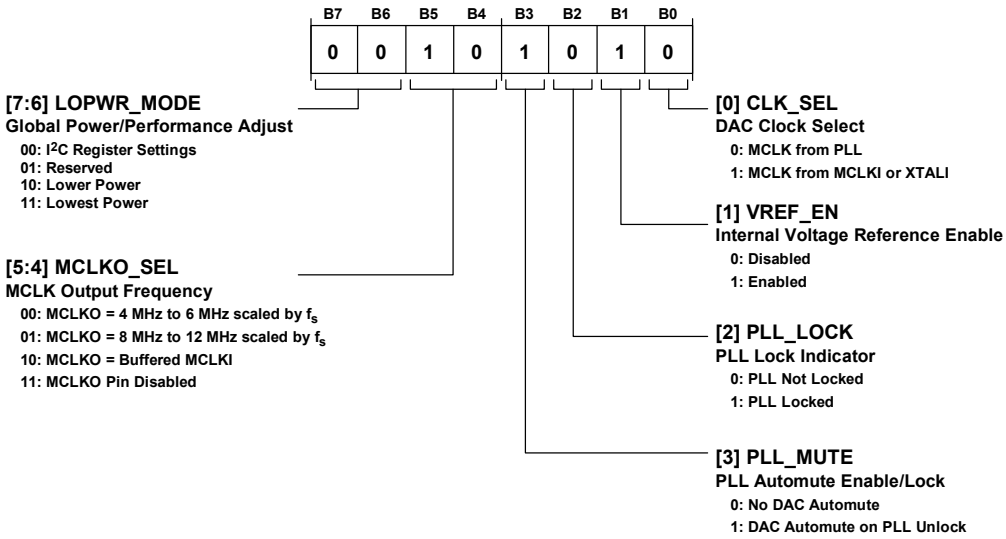


Table 26. Bit Descriptions for PLL_CLK_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LOPWR_MODE		Global Power/Performance Adjust. These bits adjust the power consumption and performance level for all 16 DAC channels at once. See the DACs section for more details.	0x0	RW
		00	I^2C Register Settings.		
		01	Reserved.		
		10	Lower Power.		
		11	Lowest Power.		
[5:4]	MCLKO_SEL		MCLK Output Frequency. Frequency selection for MCLKO pin. See the Clock Signals section for more details.	0x2	RW
		00	MCLKO = 4 MHz to 6 MHz scaled by f_S.		
		01	MCLKO = 8 MHz to 12 MHz scaled by f_S.		
		10	MCLKO = Buffered MCLKI.		
		11	MCLKO Pin Disabled.		
3	PLL_MUTE		PLL Automute Enable/Lock. This bit enables the PLL lock automute function.	0x1	RW
		0	No DAC Automute.		
		1	DAC Automute on PLL Unlock.		
2	PLL_LOCK		PLL Lock Indicator.	0x0	R
		0	PLL Not Locked.		
		1	PLL Locked.		
1	VREF_EN		Internal Voltage Reference Enable. The internal voltage reference powers the common mode for the ADAU1966A. Disabling this bit allows the user to drive the CM pin with an outside voltage source.	0x1	RW
		0	Disabled.		
		1	Enabled.		
0	CLK_SEL		DAC Clock Select. Selects between PLL and direct MCLK mode.	0x0	RW
		0	MCLK from PLL.		
		1	MCLK from MCLKI or XTALI.		

BLOCK POWER-DOWN AND THERMAL SENSOR CONTROL 1 REGISTER

Address: 0x02, Reset: 0xA0, Name: PDN_THRMSENS_CTRL_1

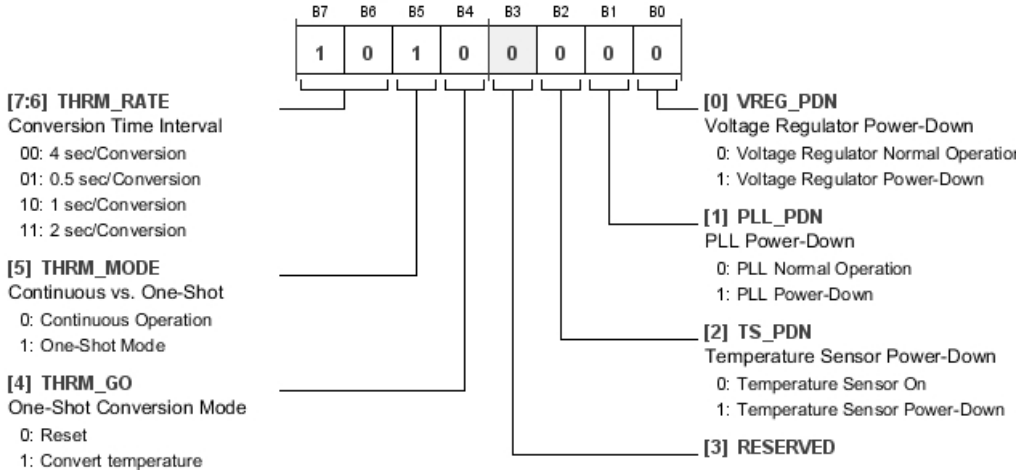


Table 27. Bit Descriptions for PDN_THRMSENS_CTRL_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	THRM_RATE		Conversion Time Interval. When THRM_MODE = 0, the THRM_RATE bits control the time interval between temperature conversions.	0x2	RW
		00	4 sec/Conversion.		
		01	0.5 sec/Conversion.		
		10	1 sec/Conversion.		
		11	2 sec/Conversion.		
5	THRM_MODE		Continuous vs. One-Shot. Determines if the temperature conversions occur continuously or only when commanded. To perform one-shot temperature conversions, set this bit to 1.	0x1	RW
		0	Continuous Operation.		
		1	One-Shot Mode.		
4	THRM_GO		One-Shot Conversion Mode. When in one-shot conversion mode, THRM_MODE = 1, the THRM_GO bit must be set to 0 followed by a write of 1. This sequence results in a single temperature conversion. The temperature data is available 120 ms after writing a 1 to this bit.	0x0	RW
		0	Reset.		
		1	Convert Temperature.		
2	TS_PDN		Temperature Sensor Power-Down.	0x0	RW
		0	Temperature Sensor On.		
		1	Temperature Sensor Power-Down.		
1	PLL_PDN		PLL Power-Down.	0x0	RW
		0	PLL Normal Operation.		
		1	PLL Power-Down.		
0	VREG_PDN		Voltage Regulator Power-Down.	0x0	RW
		0	Voltage Regulator Normal Operation.		
		1	Voltage Regulator Power-Down.		

POWER-DOWN CONTROL 2 REGISTER

Address: 0x03, Reset: 0x00, Name: PDN_CTRL2

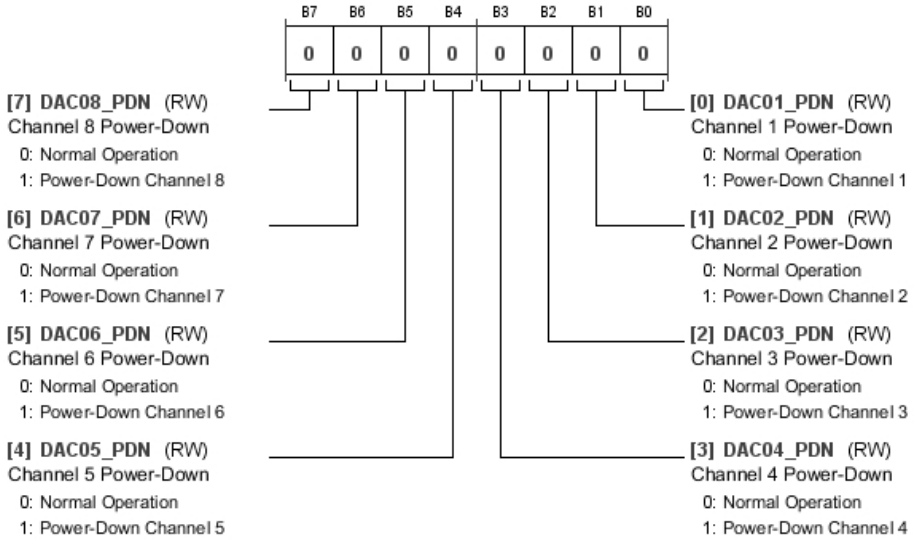


Table 28. Bit Descriptions for PDN_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC08_PDN		Channel 8 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 8		
6	DAC07_PDN		Channel 7 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 7		
5	DAC06_PDN		Channel 6 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 6		
4	DAC05_PDN		Channel 5 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 5		
3	DAC04_PDN		Channel 4 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 4		
2	DAC03_PDN		Channel 3 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 3		
1	DAC02_PDN		Channel 2 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 2		
0	DAC01_PDN		Channel 1 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 1		

POWER-DOWN CONTROL 3 REGISTER

Address: 0x04, Reset: 0x00, Name: PDN_CTRL3

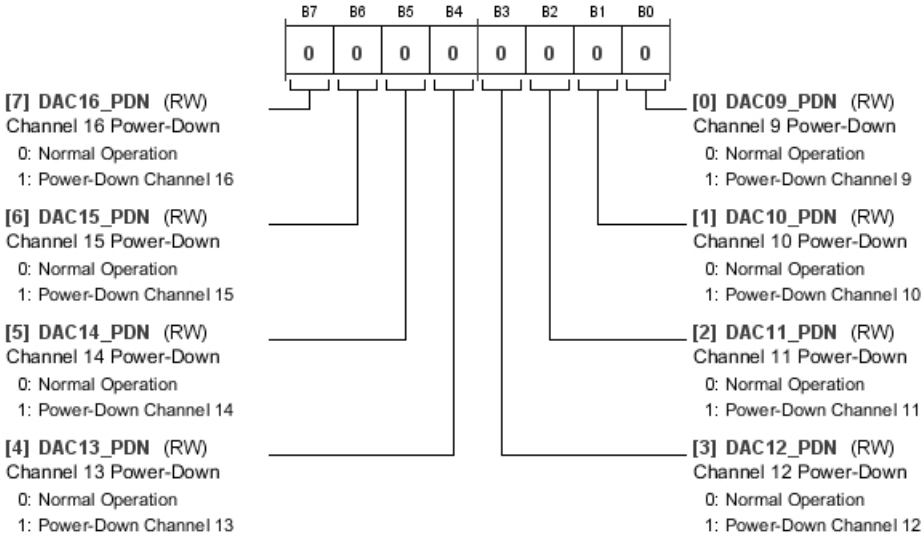


Table 29. Bit Descriptions for PDN_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC16_PDN		Channel 16 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 16		
6	DAC15_PDN		Channel 15 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 15		
5	DAC14_PDN		Channel 14 Power-Down.	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 14		
4	DAC13_PDN		Channel 13 Power-Down.	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 13		
3	DAC12_PDN		Channel 12 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 12		
2	DAC11_PDN		Channel 11 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 11		
1	DAC10_PDN		Channel 10 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 10		
0	DAC09_PDN		Channel 9 Power-Down	0x0	RW
		0	Normal Operation		
		1	Power-Down Channel 9		

THERMAL SENSOR TEMPERATURE READOUT REGISTER

Address: 0x05, Reset: 0x00, Name: THRM_TEMP_STAT

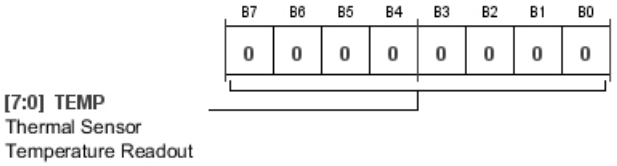


Table 30. Bit Descriptions for THRM_TEMP_STAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP		Thermal Sensor Temperature Readout. −60°C to +140°C range, 1°C step size. To convert the hexadecimal or binary TEMP value into decimal form, use the following equation: (TEMP − 60). The result is the temperature in degrees Celsius.	0x00	R

DAC CONTROL 0 REGISTER

Address: 0x06, Reset: 0x01, Name: DAC_CTRL0

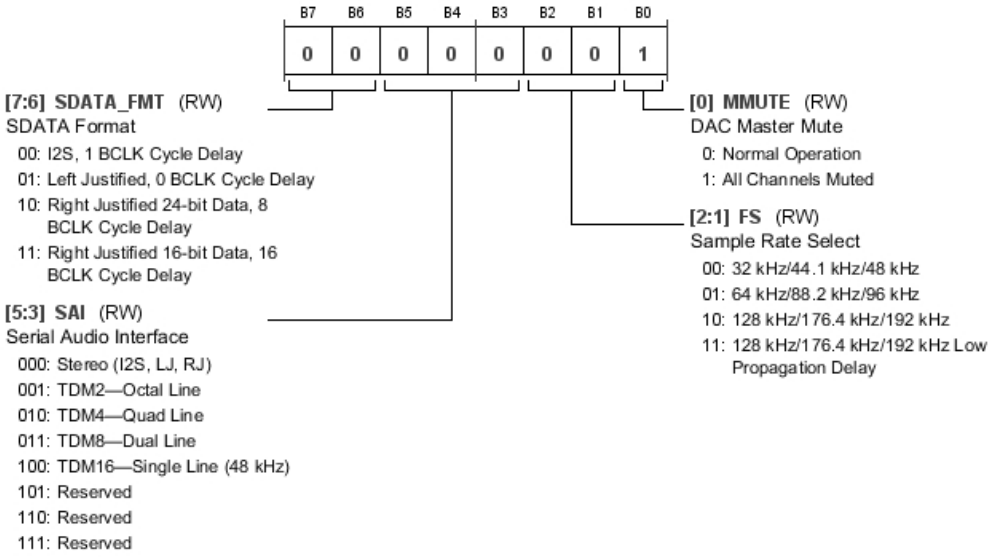


Table 31. Bit Descriptions for DAC_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT		SDATA Format. Only used when SAI = 000.	0x0	RW
		00	I^2S, 1 BCLK Cycle Delay.		
		01	Left Justified, 0 BCLK Cycle Delay.		
		10	Right Justified, 24-Bit Data, 8 BCLK Cycle Delay.		
		11	Right Justified, 16-Bit Data, 16 BCLK Cycle Delay.		
[5:3]	SAI		Serial Audio Interface. When SAI = 000, the SDATA_FMT bits control stereo SDATA format.	0x0	RW
		000	Stereo (I^2S, LJ, RJ).		
		001	TDM2—Octal Line.		
		010	TDM4—Quad Line.		
		011	TDM8—Dual Line.		
		100	TDM16—Single Line (48 kHz).		
		101	Reserved.		
		110	Reserved.		
		111	Reserved.		

Bits	Bit Name	Settings	Description	Reset	Access
[2:1]	FS		Sample Rate Select.	0x0	RW
		00	32 kHz/44.1 kHz/48 kHz.		
		01	64 kHz/88.2 kHz/96 kHz.		
		10	128 kHz/176.4 kHz/192 kHz.		
		11	128 kHz/176.4 kHz/192 kHz Low Propagation Delay.		
0	MMUTE		DAC Master Mute.	0x1	RW
		0	Normal Operation.		
		1	All Channels Muted.		

DAC CONTROL 1 REGISTER

Address: 0x07, Reset: 0x00, Name: DAC_CTRL1

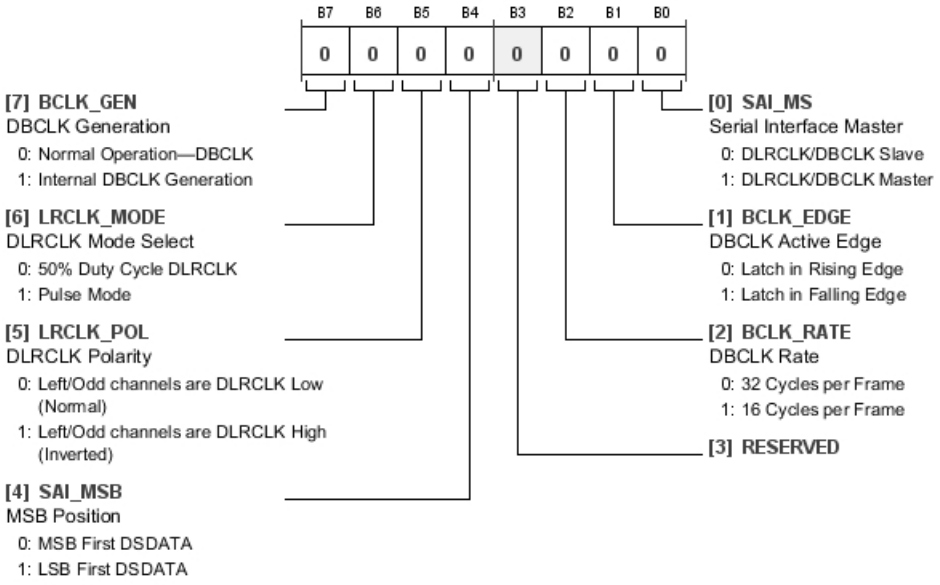


Table 32. Bit Descriptions for DAC_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLK_GEN		DBCLK Generation. When the PLL is locked to DLRCLK, it is possible to run the ADAU1966A without an external DBCLK.	0x0	RW
		0	Normal Operation—DBCLK.		
		1	Internal DBCLK Generation.		
6	LRCLK_MODE		DLRCLK Mode Select. Only Valid for TDM modes.	0x0	RW
		0	50% Duty Cycle DLRCLK.		
		1	Pulse Mode.		
5	LRCLK_POL		DLRCLK Polarity. Allows the swapping of data between channels.	0x0	RW
		0	Left/Odd channels are DLRCLK Low (Normal).		
		1	Left/Odd channels are DLRCLK High (Inverted).		
4	SAI_MSB		MSB Position.	0x0	RW
		0	MSB First DSDATA.		
		1	LSB First DSDATA.		
2	BCLK_RATE		DBCLK Rate. Number of DBCLK cycles per DLRCLK frame. Used only for generating DBCLK in master mode operation (SAI_MS = 1).	0x0	RW
		0	32 Cycles per Frame.		
		1	16 Cycles per Frame.		

Bits	Bit Name	Settings	Description	Reset	Access
1	BCLK_EDGE		DBCLK Active Edge. Adjust the polarity of the DBCLK leading edge.	0x0	RW
		0	Latch in Rising Edge.		
		1	Latch in Falling Edge.		
0	SAI_MS		Serial Interface Master. Both DLRCLK and DBCLK become the master when enabled.	0x0	RW
		0	DLRCLK/DBCLK Slave.		
		1	DLRCLK/DBCLK Master.		

DAC CONTROL 2 REGISTER

Address: 0x08, Reset: 0x06, Name: DAC_CTRL2

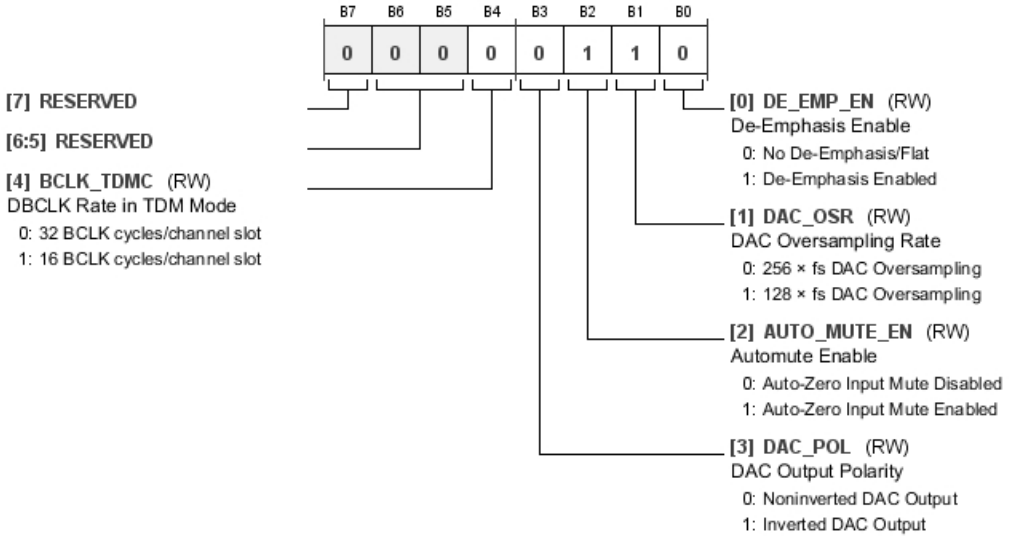


Table 33. Bit Descriptions for DAC_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
4	BCLK_TDMC		DBCLK Rate in TDM Mode. Number of DBCLK cycles per channel slot when in TDM mode.	0x0	RW
		0	32 BCLK cycles/channel slot.		
		1	16 BCLK cycles/channel slot.		
3	DAC_POL		DAC Output Polarity. This is a global switch of DAC polarity.	0x0	RW
		0	Noninverted DAC Output.		
		1	Inverted DAC Output.		
2	AUTO_MUTE_EN		Automute Enable. Automatically mutes the DACs when 1024 consecutive zero input samples are received. This is independent per channel.	0x1	RW
		0	Auto-Zero Input Mute Disabled.		
		1	Auto-Zero Input Mute Enabled.		
1	DAC_OSR		DAC Oversampling Rate. OSR selection.	0x1	RW
		0	256 × f_S DAC Oversampling.		
		1	128 × f_S DAC Oversampling.		
0	DE_EMP_EN		De-Emphasis Enable.	0x0	RW
		0	No De-Emphasis/Flat.		
		1	De-Emphasis Enabled.		

DAC INDIVIDUAL CHANNEL MUTES 1 REGISTER

Address: 0x09, Reset: 0x00, Name: DAC_MUTE1

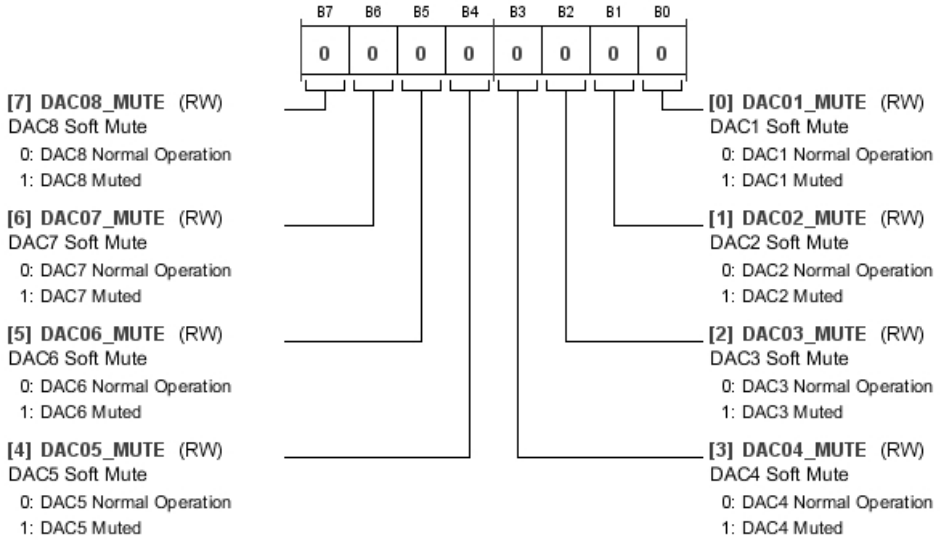


Table 34. Bit Descriptions for DAC_MUTE1

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC08_MUTE		DAC8 Soft Mute	0x0	RW
		0	DAC8 Normal Operation		
		1	DAC8 Muted		
6	DAC07_MUTE		DAC7 Soft Mute	0x0	RW
		0	DAC7 Normal Operation		
		1	DAC7 Muted		
5	DAC06_MUTE		DAC6 Soft Mute	0x0	RW
		0	DAC6 Normal Operation		
		1	DAC6 Muted		
4	DAC05_MUTE		DAC5 Soft Mute	0x0	RW
		0	DAC5 Normal Operation		
		1	DAC5 Muted		
3	DAC04_MUTE		DAC4 Soft Mute	0x0	RW
		0	DAC4 Normal Operation		
		1	DAC4 Muted		
2	DAC03_MUTE		DAC3 Soft Mute	0x0	RW
		0	DAC3 Normal Operation		
		1	DAC3 Muted		
1	DAC02_MUTE		DAC2 Soft Mute	0x0	RW
		0	DAC2 Normal Operation		
		1	DAC2 Muted		
0	DAC01_MUTE		DAC1 Soft Mute	0x0	RW
		0	DAC1 Normal Operation		
		1	DAC1 Muted		

DAC INDIVIDUAL CHANNEL MUTES 2 REGISTER

Address: 0x0A, Reset: 0x00, Name: DAC_MUTE2

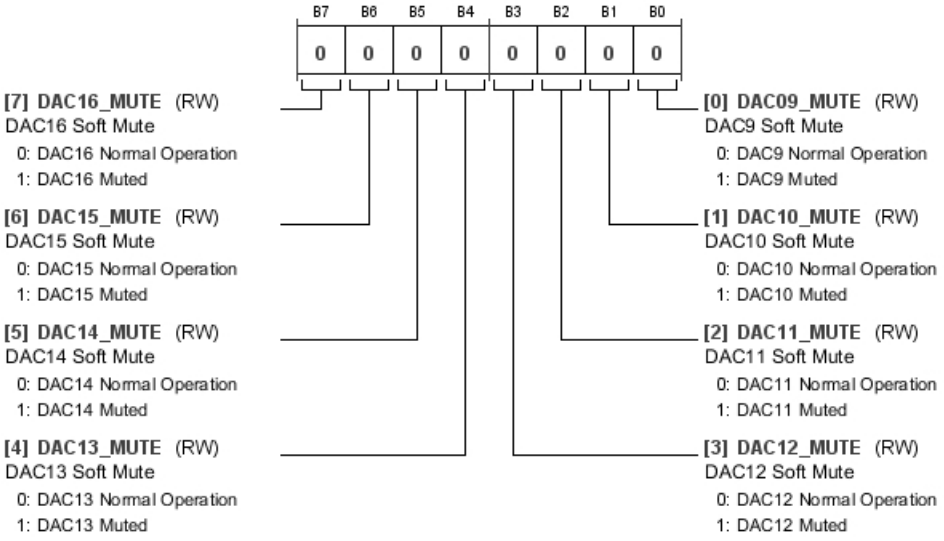


Table 35. Bit Descriptions for DAC_MUTE2

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC16_MUTE		DAC16 Soft Mute	0x0	RW
		0	DAC16 Normal Operation		
		1	DAC16 Muted		
6	DAC15_MUTE		DAC15 Soft Mute	0x0	RW
		0	DAC15 Normal Operation		
		1	DAC15 Muted		
5	DAC14_MUTE		DAC14 Soft Mute	0x0	RW
		0	DAC14 Normal Operation		
		1	DAC14 Muted		
4	DAC13_MUTE		DAC13 Soft Mute	0x0	RW
		0	DAC13 Normal Operation		
		1	DAC13 Muted		
3	DAC12_MUTE		DAC12 Soft Mute	0x0	RW
		0	DAC12 Normal Operation		
		1	DAC12 Muted		
2	DAC11_MUTE		DAC11 Soft Mute	0x0	RW
		0	DAC11 Normal Operation		
		1	DAC11 Muted		
1	DAC10_MUTE		DAC10 Soft Mute	0x0	RW
		0	DAC10 Normal Operation		
		1	DAC10 Muted		
0	DAC09_MUTE		DAC9 Soft Mute	0x0	RW
		0	DAC9 Normal Operation		
		1	DAC9 Muted		

MASTER VOLUME CONTROL REGISTER

Address: 0x0B, Reset: 0x00, Name: DACMSTR_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

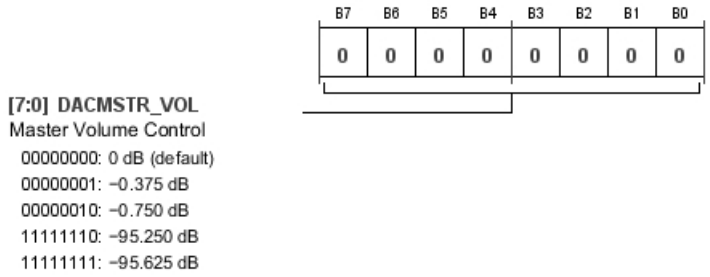


Table 36. Bit Descriptions for DACMSTR_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DACMSTR_VOL		Master Volume Control	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 1 VOLUME CONTROL REGISTER

Address: 0x0C, Reset: 0x00, Name: DAC01_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

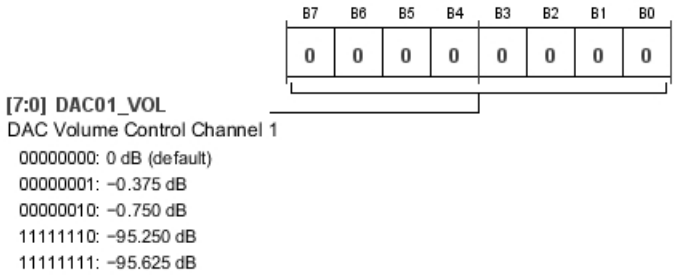


Table 37. Bit Descriptions for DAC01_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC01_VOL		DAC Volume Control Channel 1	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 2 VOLUME CONTROL REGISTER

Address: 0x0D, Reset: 0x00, Name: DAC02_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

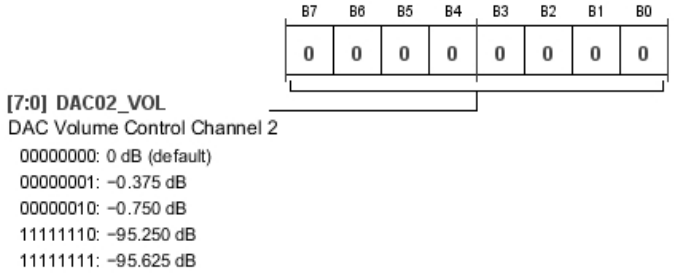


Table 38. Bit Descriptions for DAC02_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC02_VOL		DAC Volume Control Channel 2	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 3 VOLUME CONTROL REGISTER

Address: 0x0E, Reset: 0x00, Name: DAC03_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

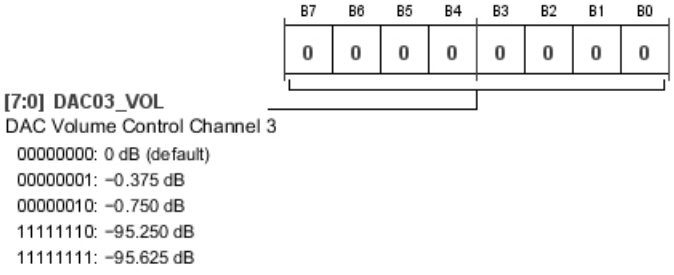


Table 39. Bit Descriptions for DAC03_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC03_VOL		DAC Volume Control Channel 3	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 4 VOLUME CONTROL REGISTER

Address: 0x0F, Reset: 0x00, Name: DAC04_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

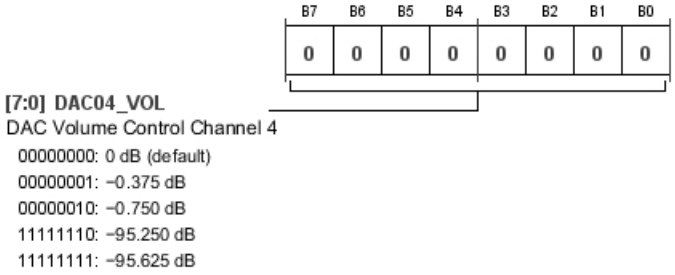


Table 40. Bit Descriptions for DAC04_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC04_VOL		DAC Volume Control Channel 4	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 5 VOLUME CONTROL REGISTER

Address: 0x10, Reset: 0x00, Name: DAC05_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

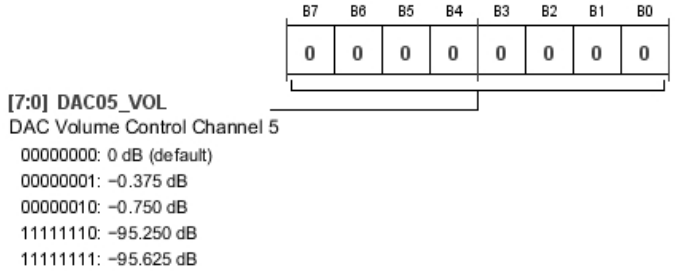


Table 41. Bit Descriptions for DAC05_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC05_VOL		DAC Volume Control Channel 5	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 6 VOLUME CONTROL REGISTER

Address: 0x11, Reset: 0x00, Name: DAC06_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

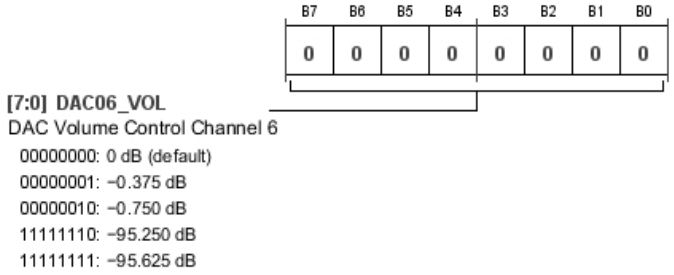


Table 42. Bit Descriptions for DAC06_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC06_VOL		DAC Volume Control Channel 6	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 7 VOLUME CONTROL REGISTER

Address: 0x12, Reset: 0x00, Name: DAC07_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

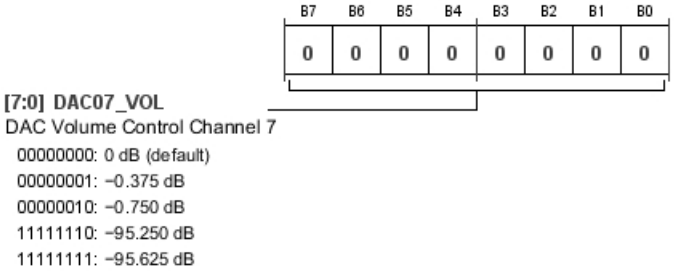


Table 43. Bit Descriptions for DAC07_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC07_VOL		DAC Volume Control Channel 7	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 8 VOLUME CONTROL REGISTER

Address: 0x13, Reset: 0x00, Name: DAC08_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

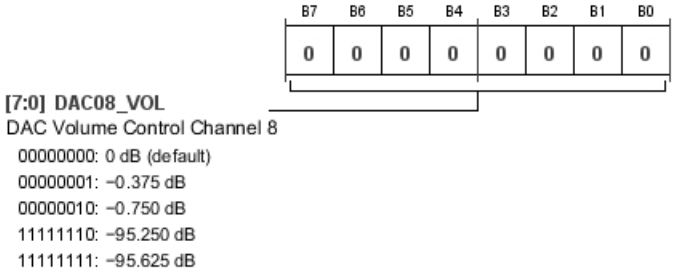


Table 44. Bit Descriptions for DAC08_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC08_VOL		DAC Volume Control Channel 8	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 9 VOLUME CONTROL REGISTER

Address: 0x14, Reset: 0x00, Name: DAC09_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

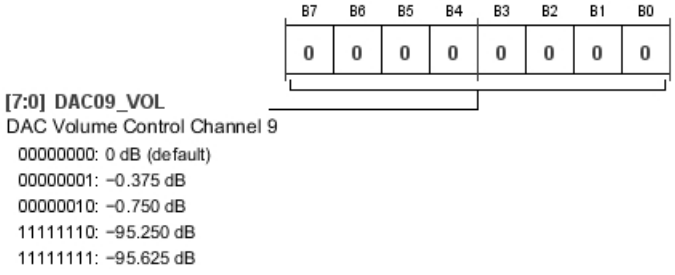


Table 45. Bit Descriptions for DAC09_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC09_VOL		DAC Volume Control Channel 9	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 10 VOLUME CONTROL REGISTER

Address: 0x15, Reset: 0x00, Name: DAC10_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

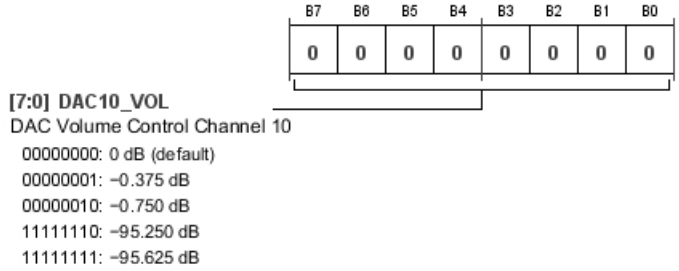


Table 46. Bit Descriptions for DAC10_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC10_VOL		DAC Volume Control Channel 10	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 11 VOLUME CONTROL REGISTER

Address: 0x16, Reset: 0x00, Name: DAC11_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

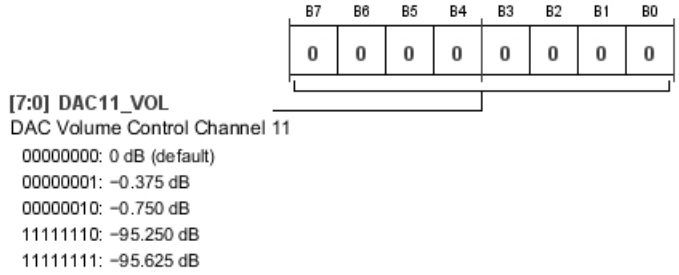


Table 47. Bit Descriptions for DAC11_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC11_VOL		DAC Volume Control Channel 11	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 12 VOLUME CONTROL REGISTER

Address: 0x17, Reset: 0x00, Name: DAC12_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

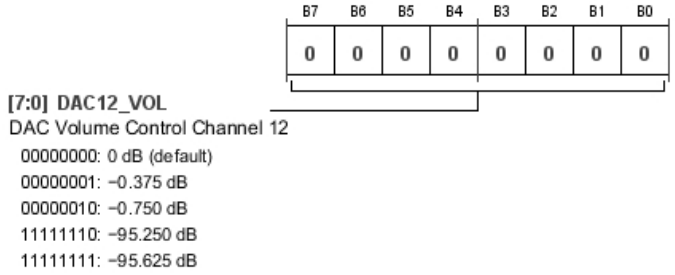


Table 48. Bit Descriptions for DAC12_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC12_VOL		DAC Volume Control Channel 12	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 13 VOLUME CONTROL REGISTER

Address: 0x18, Reset: 0x00, Name: DAC13_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

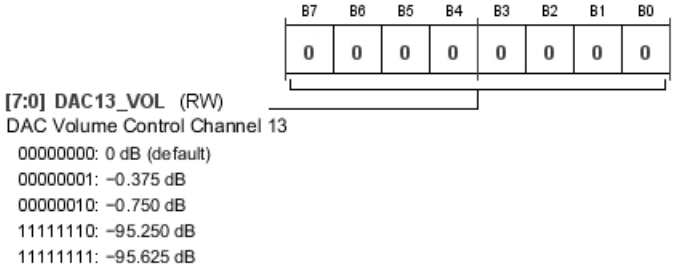


Table 49. Bit Descriptions for DAC13_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC13_VOL		DAC Volume Control Channel 13	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 14 VOLUME CONTROL REGISTER

Address: 0x19, Reset: 0x00, Name: DAC14_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

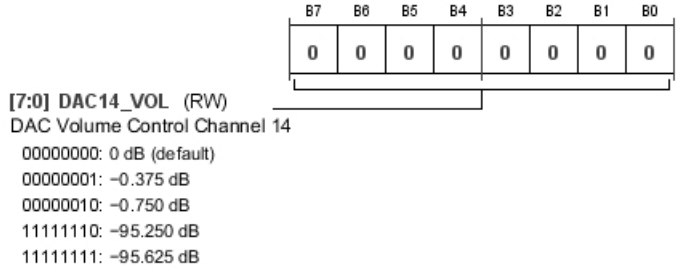


Table 50. Bit Descriptions for DAC14_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC14_VOL		DAC Volume Control Channel 14	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 15 VOLUME CONTROL REGISTER

Address: 0x1A, Reset: 0x00, Name: DAC15_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

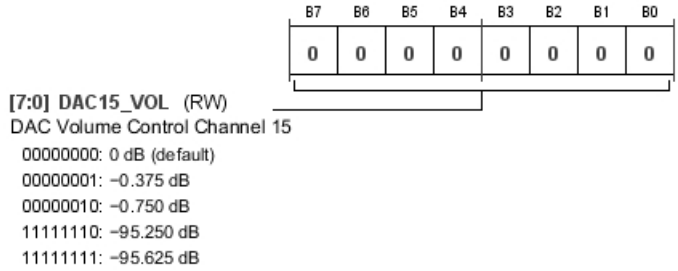


Table 51. Bit Descriptions for DAC15_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC15_VOL		DAC Volume Control Channel 15	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

DAC 16 VOLUME CONTROL REGISTER

Address: 0x1B, Reset: 0x00, Name: DAC16_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 58 for a complete list of the volume settings.

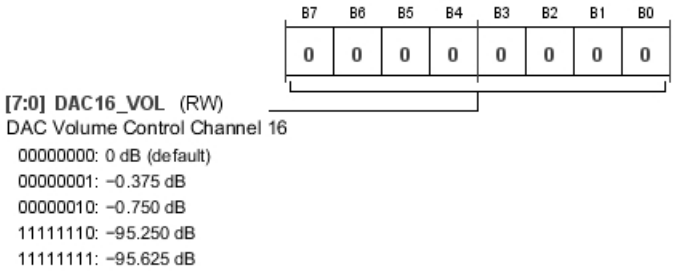


Table 52. Bit Descriptions for DAC16_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC16_VOL		DAC Volume Control Channel 16	0x00	RW
		00000000	0 dB (default)		
		00000001	−0.375 dB		
		00000010	−0.750 dB		
		11111110	−95.250 dB		
		11111111	−95.625 dB		

PAD STRENGTH REGISTER

Address: 0x1C, Reset: 0x00, Name: PAD_STRGTH

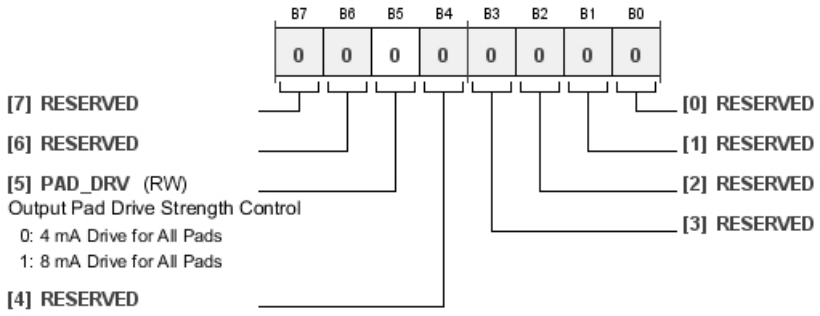


Table 53. Bit Descriptions for PAD_STRGTH

Bits	Bit Name	Settings	Description	Reset	Access
5	PAD_DRV		Output Pad Drive Strength Control	0x0	RW
		0	4 mA Drive for All Pads		
		1	8 mA Drive for All Pads		

DAC POWER ADJUST 1 REGISTER

Address: 0x1D, Reset: 0xAA, Name: DAC_POWER1

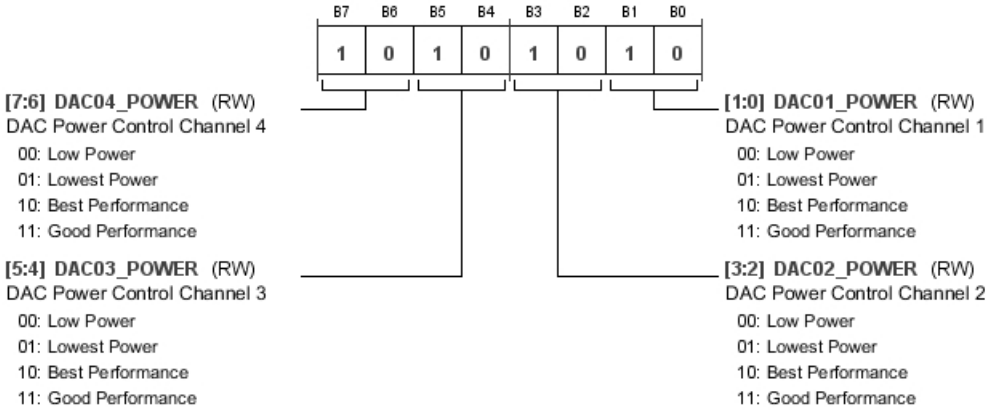


Table 54. Bit Descriptions for DAC_POWER1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC04_POWER		DAC Power Control Channel 4	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[5:4]	DAC03_POWER		DAC Power Control Channel 3	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[3:2]	DAC02_POWER		DAC Power Control Channel 2	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[1:0]	DAC01_POWER		DAC Power Control Channel 1	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		

DAC POWER ADJUST 2 REGISTER

Address: 0x1E, Reset: 0xAA, Name: DAC_POWER2

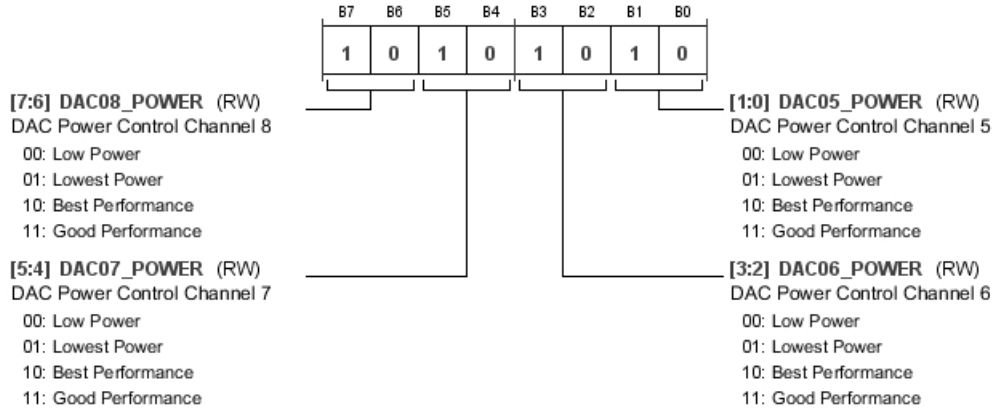


Table 55. Bit Descriptions for DAC_POWER2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC08_POWER		DAC Power Control Channel 8	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[5:4]	DAC07_POWER		DAC Power Control Channel 7	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[3:2]	DAC06_POWER		DAC Power Control Channel 6	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[1:0]	DAC05_POWER		DAC Power Control Channel 5	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		

DAC POWER ADJUST 3 REGISTER

Address: 0x1F, Reset: 0xAA, Name: DAC_POWER3

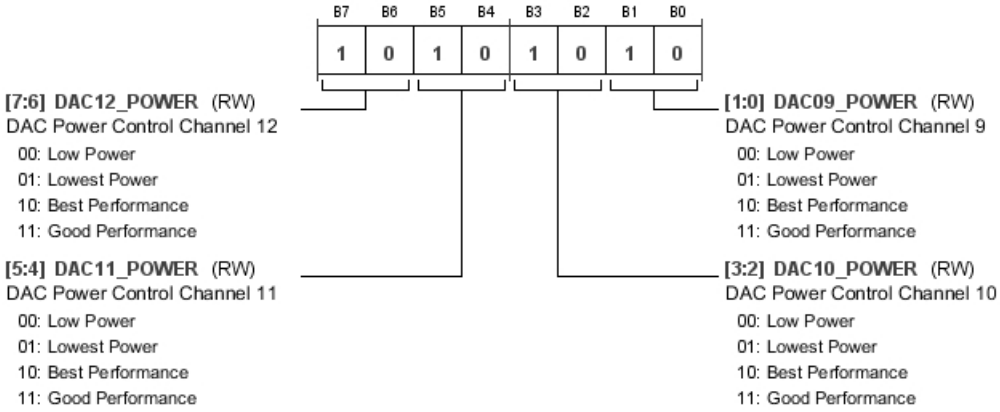


Table 56. Bit Descriptions for DAC_POWER3

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC12_POWER		DAC Power Control Channel 12	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[5:4]	DAC11_POWER		DAC Power Control Channel 11	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[3:2]	DAC10_POWER		DAC Power Control Channel 10	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[1:0]	DAC09_POWER		DAC Power Control Channel 9	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		

DAC POWER ADJUST 4 REGISTER

Address: 0x20, Reset: 0xAA, Name: DAC_POWER4

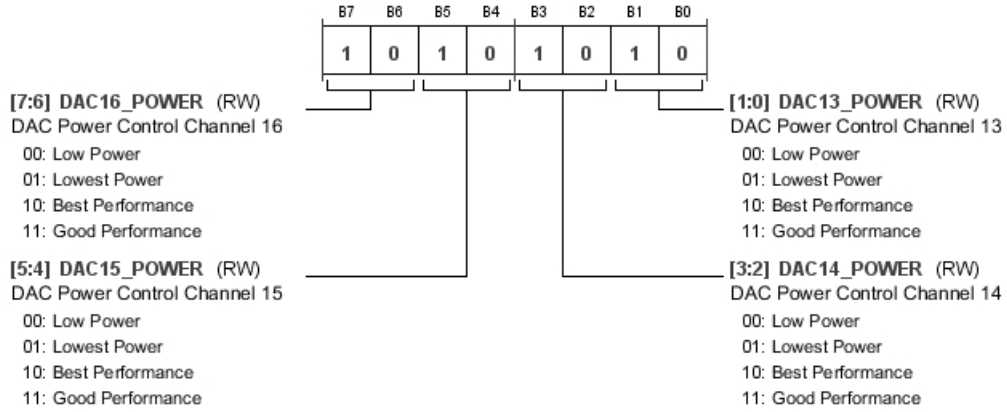


Table 57. Bit Descriptions for DAC_POWER4

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC16_POWER		DAC Power Control Channel 16	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[5:4]	DAC15_POWER		DAC Power Control Channel 15	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[3:2]	DAC14_POWER		DAC Power Control Channel 14	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		
[1:0]	DAC13_POWER		DAC Power Control Channel 13	0x2	RW
		00	Low Power		
		01	Lowest Power		
		10	Best Performance		
		11	Good Performance		

Table 58. Volume Settings

Binary Value	Hex Value	Volume Attenuation (dB)
00000000	00	0
00000001	01	−0.375
00000010	02	−0.75
00000011	03	−1.125
00000100	04	−1.5
00000101	05	−1.875
00000110	06	−2.25
00000111	07	−2.625
00001000	08	−3
00001001	09	−3.375
00001010	0A	−3.75
00001011	0B	−4.125
00001100	0C	−4.5
00001101	0D	−4.875
00001110	0E	−5.25
00001111	0F	−5.625
00010000	10	−6
00010001	11	−6.375
00010010	12	−6.75
00010011	13	−7.125
00010100	14	−7.5
00010101	15	−7.875
00010110	16	−8.25
00010111	17	−8.625
00011000	18	−9
00011001	19	−9.375
00011010	1A	−9.75
00011011	1B	−10.125
00011100	1C	−10.5
00011101	1D	−10.875
00011110	1E	−11.25
00011111	1F	−11.625
00100000	20	−12
00100001	21	−12.375
00100010	22	−12.75
00100011	23	−13.125
00100100	24	−13.5
00100101	25	−13.875
00100110	26	−14.25
00100111	27	−14.625
00101000	28	−15
00101001	29	−15.375
00101010	2A	−15.75
00101011	2B	−16.125
00101100	2C	−16.5
00101101	2D	−16.875
00101110	2E	−17.25
00101111	2F	−17.625
00110000	30	−18
00110001	31	−18.375
00110010	32	−18.75
00110011	33	−19.125
00110100	34	−19.5
00110101	35	−19.875
00110110	36	−20.25
00110111	37	−20.625
00111000	38	−21
00111001	39	−21.375
00111010	3A	−21.75
00111011	3B	−22.125
00111100	3C	−22.5
00111101	3D	−22.875
00111110	3E	−23.25
00111111	3F	−23.625
01000000	40	−24
01000001	41	−24.375
01000010	42	−24.75
01000011	43	−25.125
01000100	44	−25.5
01000101	45	−25.875
01000110	46	−26.25
01000111	47	−26.625
01001000	48	−27
01001001	49	−27.375
01001010	4A	−27.75
01001011	4B	−28.125
01001100	4C	−28.5
01001101	4D	−28.875
01001110	4E	−29.25
01001111	4F	−29.625
01010000	50	−30
01010001	51	−30.375
01010010	52	−30.75
01010011	53	−31.125
01010100	54	−31.5
01010101	55	−31.875
01010110	56	−32.25
01010111	57	−32.625
01011000	58	−33
01011001	59	−33.375
01011010	5A	−33.75
01011011	5B	−34.125
01011100	5C	−34.5
01011101	5D	−34.875
01011110	5E	−35.25
01011111	5F	−35.625

Binary Value	Hex Value	Volume Attenuation (dB)
01100000	60	−36
01100001	61	−36.375
01100010	62	−36.75
01100011	63	−37.125
01100100	64	−37.5
01100101	65	−37.875
01100110	66	−38.25
01100111	67	−38.625
01101000	68	−39
01101001	69	−39.375
01101010	6A	−39.75
01101011	6B	−40.125
01101100	6C	−40.5
01101101	6D	−40.875
01101110	6E	−41.25
01101111	6F	−41.625
01110000	70	−42
01110001	71	−42.375
01110010	72	−42.75
01110011	73	−43.125
01110100	74	−43.5
01110101	75	−43.875
01110110	76	−44.25
01110111	77	−44.625
01111000	78	−45
01111001	79	−45.375
01111010	7A	−45.75
01111011	7B	−46.125
01111100	7C	−46.5
01111101	7D	−46.875
01111110	7E	−47.25
01111111	7F	−47.625
10000000	80	−48
10000001	81	−48.375
10000010	82	−48.75
10000011	83	−49.125
10000100	84	−49.5
10000101	85	−49.875
10000110	86	−50.25
10000111	87	−50.625
10001000	88	−51
10001001	89	−51.375
10001010	8A	−51.75
10001011	8B	−52.125
10001100	8C	−52.5
10001101	8D	−52.875
10001110	8E	−53.25
10001111	8F	−53.625

Binary Value	Hex Value	Volume Attenuation (dB)
10010000	90	−54
10010001	91	−54.375
10010010	92	−54.75
10010011	93	−55.125
10010100	94	−55.5
10010101	95	−55.875
10010110	96	−56.25
10010111	97	−56.625
10011000	98	−57
10011001	99	−57.375
10011010	9A	−57.75
10011011	9B	−58.125
10011100	9C	−58.5
10011101	9D	−58.875
10011110	9E	−59.25
10011111	9F	−59.625
10100000	A0	−60
10100001	A1	−60.375
10100010	A2	−60.75
10100011	A3	−61.125
10100100	A4	−61.5
10100101	A5	−61.875
10100110	A6	−62.25
10100111	A7	−62.625
10101000	A8	−63
10101001	A9	−63.375
10101010	AA	−63.75
10101011	AB	−64.125
10101100	AC	−64.5
10101101	AD	−64.875
10101110	AE	−65.25
10101111	AF	−65.625
10110000	B0	−66
10110001	B1	−66.375
10110010	B2	−66.75
10110011	B3	−67.125
10110100	B4	−67.5
10110101	B5	−67.875
10110110	B6	−68.25
10110111	B7	−68.625
10111000	B8	−69
10111001	B9	−69.375
10111010	BA	−69.75
10111011	BB	−70.125
10111100	BC	−70.5
10111101	BD	−70.875
10111110	BE	−71.25
10111111	BF	−71.625

Binary Value	Hex Value	Volume Attenuation (dB)
11000000	C0	−72
11000001	C1	−72.375
11000010	C2	−72.75
11000011	C3	−73.125
11000100	C4	−73.5
11000101	C5	−73.875
11000110	C6	−74.25
11000111	C7	−74.625
11001000	C8	−75
11001001	C9	−75.375
11001010	CA	−75.75
11001011	CB	−76.125
11001100	CC	−76.5
11001101	CD	−76.875
11001110	CE	−77.25
11001111	CF	−77.625
11010000	D0	−78
11010001	D1	−78.375
11010010	D2	−78.75
11010011	D3	−79.125
11010100	D4	−79.5
11010101	D5	−79.875
11010110	D6	−80.25
11010111	D7	−80.625
11011000	D8	−81
11011001	D9	−81.375
11011010	DA	−81.75
11011011	DB	−82.125
11011100	DC	−82.5
11011101	DD	−82.875
11011110	DE	−83.25
11011111	DF	−83.625

Binary Value	Hex Value	Volume Attenuation (dB)
11100000	E0	−84
11100001	E1	−84.375
11100010	E2	−84.75
11100011	E3	−85.125
11100100	E4	−85.5
11100101	E5	−85.875
11100110	E6	−86.25
11100111	E7	−86.625
11101000	E8	−87
11101001	E9	−87.375
11101010	EA	−87.75
11101011	EB	−88.125
11101100	EC	−88.5
11101101	ED	−88.875
11101110	EE	−89.25
11101111	EF	−89.625
11110000	F0	−90
11110001	F1	−90.375
11110010	F2	−90.75
11110011	F3	−91.125
11110100	F4	−91.5
11110101	F5	−91.875
11110110	F6	−92.25
11110111	F7	−92.625
11111000	F8	−93
11111001	F9	−93.375
11111010	FA	−93.75
11111011	FB	−94.125
11111100	FC	−94.5
11111101	FD	−94.875
11111110	FE	−95.25
11111111	FF	−95.625

OUTLINE DIMENSIONS

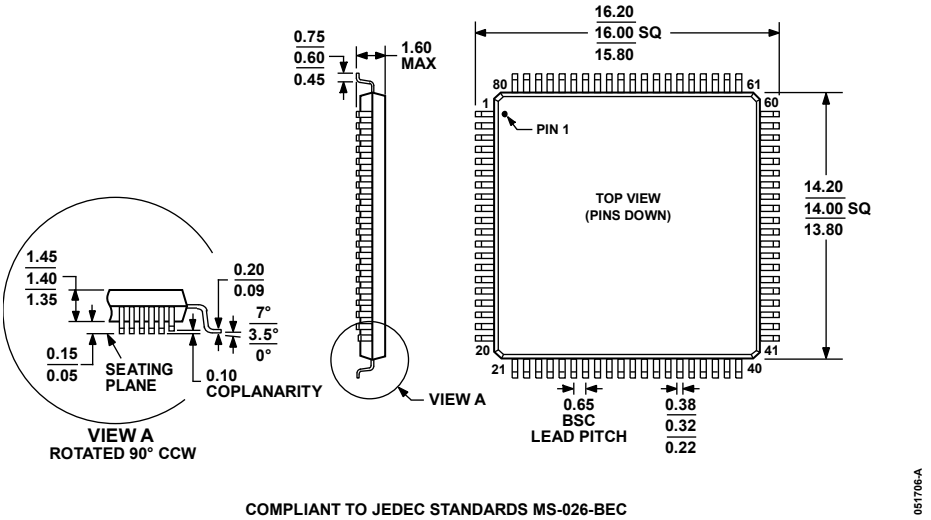


Figure 24. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADAU1966AWBSTZ	−40°C to +105°C	80-Lead LQFP	ST-80-2
ADAU1966AWBSTZ-RL	−40°C to +105°C	80-Lead LQFP, 13" Tape and Reel	ST-80-2
EVAL-ADAU1966AZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1966AW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

©2013–2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D11298-0-3/16(A)