ADC0831-N/ADC0832-N/ADC0834-N/ADC0838-N 8-Bit Serial I/O A/D Converters with Multiplexer Options

Check for Samples: ADC0831-N, ADC0832-N, ADC0834-N, ADC0838-N

FEATURES

- TI MICROWIRE Compatible—Direct Interface to COPS Family Processors
- Easy Interface to All Microprocessors, or Operates "Stand-Alone"
- Operates Ratiometrically or with 5 V_{DC} Voltage Reference
- No Zero or Full-Scale Adjust Required
- 2-, 4- or 8-Channel Multiplexer Options with Address Logic
- Shunt Regulator Allows Operation with High Voltage Supplies
- 0V to 5V Input Range with Single 5V Power Supply
- Remote Operation with Serial Digital Data Link
- TTL/MOS Input/Output Compatible
- 0.3 in. Standard Width, 8-, 14- or 20-Pin PDIP Package
- 20 Pin PLCC Package (ADC0838-N Only)
- SOIC Package

KEY SPECIFICATIONS

- Resolution: 8 Bits
- Total Unadjusted Error: ±½ LSB and ±1 LSB
- Single Supply: 5 V_{DC}
- Low Power: 15 mW
- Conversion Time: 32 µs

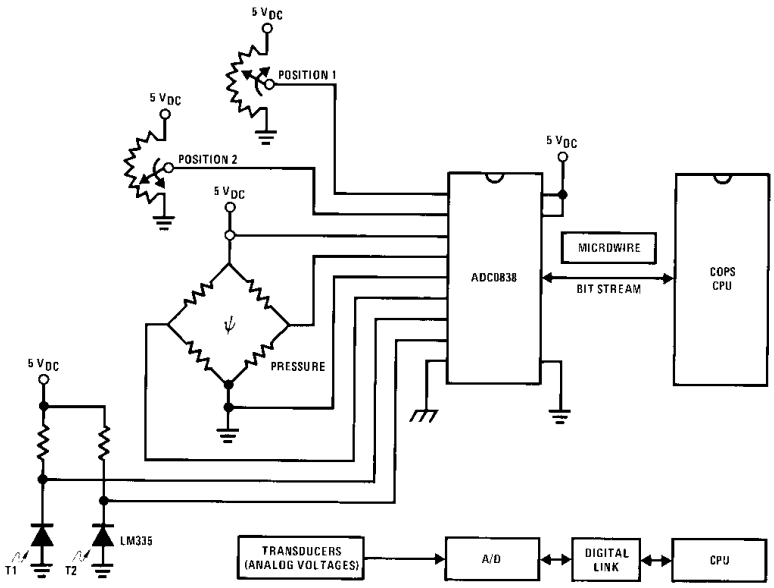
DESCRIPTION

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the TI MICROWIRE serial data exchange standard for easy interface to the COPS family of processors, and can interface with standard shift registers or µPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Typical Application



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Connection Diagrams

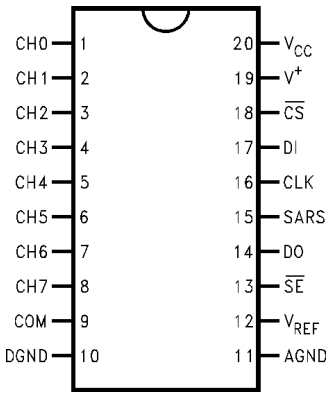


Figure 1. ADC0838-N 8-Channel Mux SOIC/PDIP Package (DW or NFH) Top View

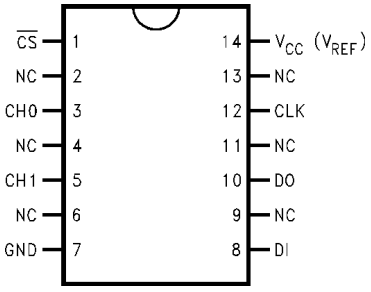
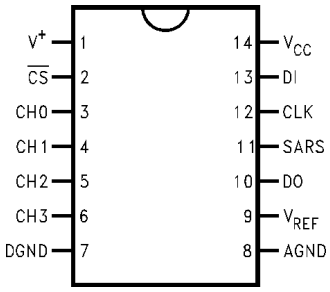


Figure 2. ADC0832-N 2-Channel MUX SOIC Package (NPA) Top View



COM internally connected to A GND
Top View

Figure 3. ADC0834-N 4-Channel MUX SOIC/PDIP (NPA or NFF) Top View

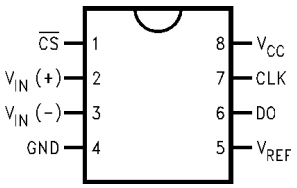
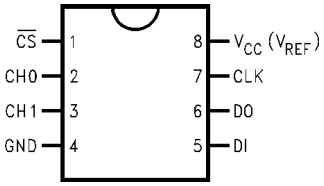


Figure 4. ADC0831-N Single Differential Input PDIP Package (P) Top View



COM internally connected to GND.
V_{REF} internally connected to V_{CC}.
Top View

Figure 5. ADC0832-N 2-Channel MUX PDIP Package (P) Top View

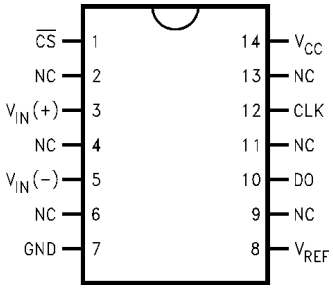


Figure 6. ADC0831-N Single Differential Input SOIC Package (NPA) Top View

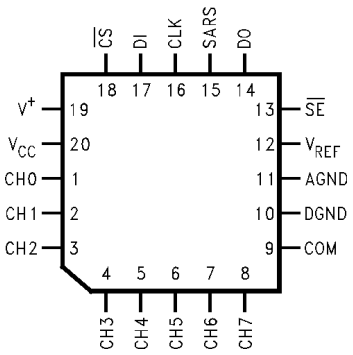


Figure 7. ADC0838-N 8-Channel MUX PLCC Package (FN)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2) (3)

Current into V^+ (4)		15 mA
Supply Voltage, V_{CC} (4)		6.5V
Voltage	Logic Inputs	−0.3V to V_{CC} + 0.3V
	Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per	Pin (5)	±5 mA
	Package	±20 mA
Storage Temperature		−65°C to +150°C
Package Dissipation	at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	PDIP Package	260°C
PLCC Package	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
ESD Susceptibility (6)		2000V

(1) All voltages are measured with respect to the ground plugs.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore ensured for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See Figure 24 in Functional Description)
(5) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Ratings (1) (2)

Supply Voltage, V_{CC}		4.5 V_{DC} to 6.3 V_{DC}
Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	ADC0832/8CIWM ADC0834BCN, ADC0838BCV, ADC0831/2/4/8CCN, ADC0838CCV	−40°C to +85°C
	ADC0831/2/4/8CCWM	0°C to +70°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to the ground plugs.

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Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \le V_{CC}$ +0.1V, $T_A = T_j$ = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter		Conditions	CIWM Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
			Typ(1)	Tested Limit(2)	Design Limit(3)	Typ(1)	Tested Limit(2)	Design Limit(3)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Total Unadjusted Error	ADC0838BCV	V_{REF} = 5.00 V(4)					±½	**±½**	LSB (Max)
	ADC0834BCN						±½	**±½**	
	ADC0838CCV						±1	**±1**	
	ADC0831/2/4/8CCN						±1	**±1**	
	ADC0831/2/4/8CCWM						±1	**±1**	
	ADC0832/8CIWM			**±1**					
Minimum Reference Input Resistance(5)			3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance(5)			3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range(6)				**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Range(6)				**GND −0.05**			GND −0.05	**GND −0.05**	V
DC Common-Mode Error			±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Change in zero error from V_{CC}=5V to internal zener operation(7)		15 mA into V+, V_{CC} = N.C., V_{REF} = 5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V+)(7)	MIN	15 mA into V+		**6.3**			6.3	**6.3**	V
	MAX			**8.5**			8.5	**8.5**	
Power Supply Sensitivity		V_{CC} = 5V ± 5%	±1/16	**±¼**	±¼	±1/16	±¼	**±¼**	LSB
I_{OFF}, Off Channel Leakage Current(8)		On Channel = 5V		−0.2			−0.2	**−1**	µA
		Off Channel = 0V		**−1**					
		On Channel = 0V		+0.2			+0.2	**+1**	µA
		Off Channel = 5V		**+1**					
I_{ON}, On Channel Leakage Current(8)		On Channel = 0V		−0.2			−0.2	**−1**	µA
		Off Channel = 5V		**−1**					
		On Channel = 5V		+0.2			+0.2	**+1**	µA
		Off Channel = 0V		**+1**					

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(3) Ensured but not 100% production tested. These limits are not used to calculate outgoing quality levels.
(4) Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
(5) Cannot be tested for ADC0832-N.
(6) For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Functional Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.
(7) Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore ensured for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See Figure 24 in Functional Description)
(8) Leakage current is measured with the clock not switching.

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Converter and Multiplexer Electrical Characteristics (continued)

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \le V_{CC}$ +0.1V, $T_A = T_j$ = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter		Conditions	CIWM Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
			Typ(1)	Tested Limit(2)	Design Limit(3)	Typ(1)	Tested Limit(2)	Design Limit(3)	
DIGITAL AND DC CHARACTERISTICS									
$V_{IN(1)}$, Logical "1" Input Voltage (Min)		V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)		V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)		V_{IN} = 5.0V	0.005	**1**		0.005	1	**1**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)		V_{IN} = 0V	−0.005	**−1**		−0.005	−1	**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)		V_{CC} = 4.75V I_{OUT} = −360 µA		**2.4**			2.4	**2.4**	V
		I_{OUT} = −10 µA		**4.5**			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)		V_{CC} = 4.75V, I_{OUT} = 1.6 mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)		V_{OUT} = 0V	−0.1	**−3**		−0.1	−3	**−3**	µA
		V_{OUT} = 5V	0.1	**3**		0.1	+3	**+3**	µA
I_{SOURCE}, Output Source Current (Min)		V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)		V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	ADC0831-N, ADC0834-N, ADC0838-N		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832-N		Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

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AC Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f$ = 20 ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ(1)	Tested Limit(2)	Design Limit(3)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle(4)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid(5)		C_L=100 pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi–Z		C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits and Waveforms)	125		250	ns
		C_L=100 pf, R_L=2k		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(3) Ensured but not 100% production tested. These limits are not used to calculate outgoing quality levels.
(4) A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 µs. The maximum time the clock can be high is 60 µs. The clock can be stopped when low so long as the analog input voltage remains stable.
(5) Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see ADC0838-N Functional Block Diagram) to allow for comparator response time.

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Typical Performance Characteristics

Unadjusted Offset Error vs. V_{REF} Voltage

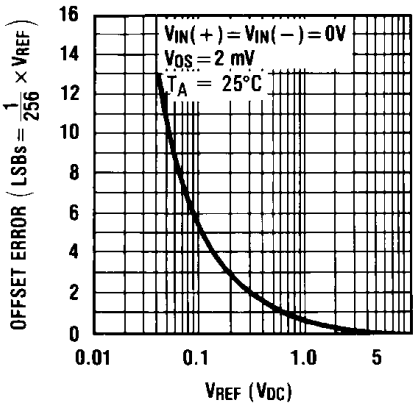


Figure 8.

Linearity Error vs. V_{REF}Voltage

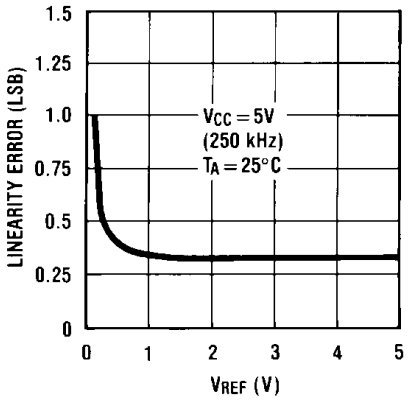


Figure 9.

Linearity Error vs. Temperature

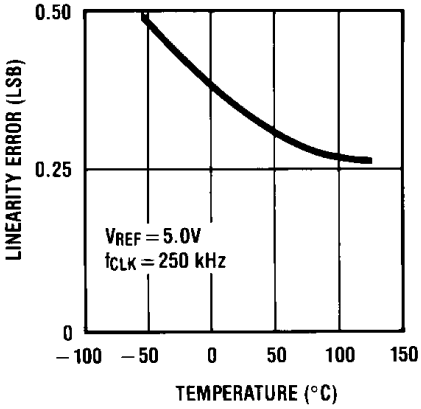


Figure 10.

Linearity Error vs. f_{CLK}

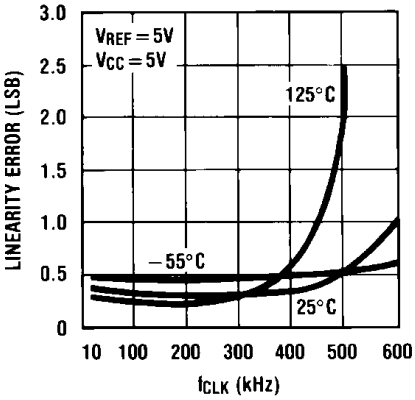
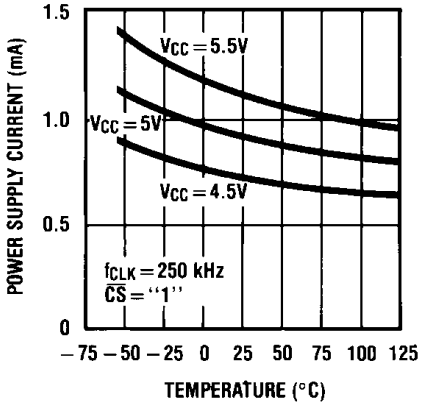


Figure 11.

Power Supply Current vs. Temperature (ADC0838-N, ADC0831-N, ADC0834-N)



Note: For ADC0832-N add I_{REF}.

Figure 12.

Output Current vs. Temperature

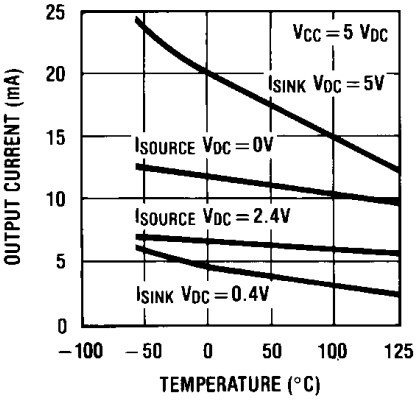


Figure 13.

Typical Performance Characteristics (continued)

Power Supply Current vs. f_{CLK}

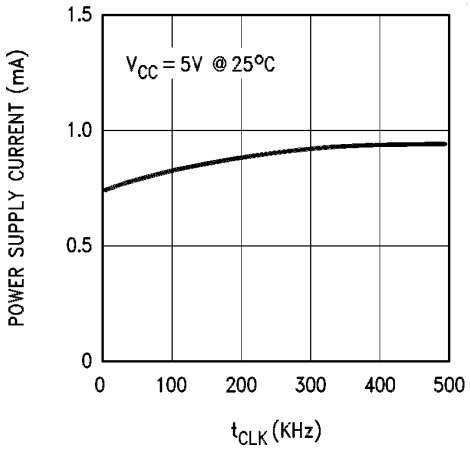
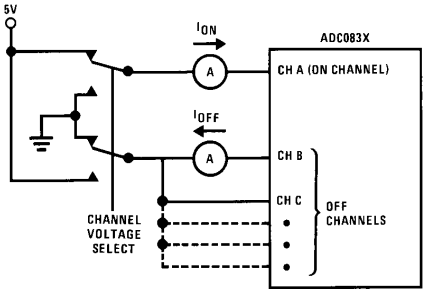
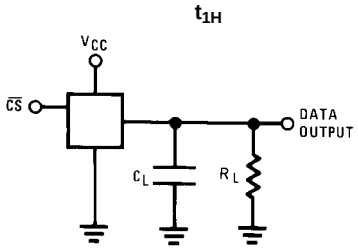


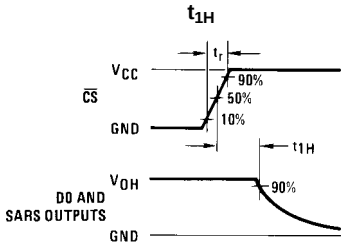
Figure 14.

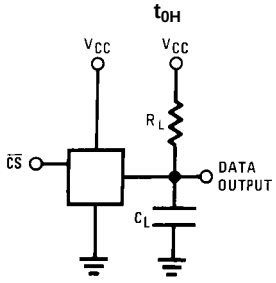
Leakage Current Test Circuit

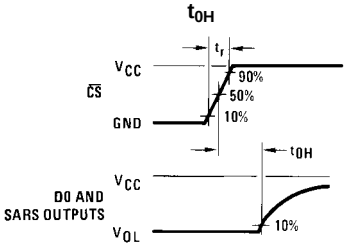


TRI-STATE Test Circuits and Waveforms









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Timing Diagrams

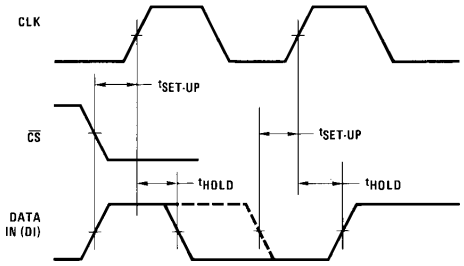


Figure 15. Data Input Timing

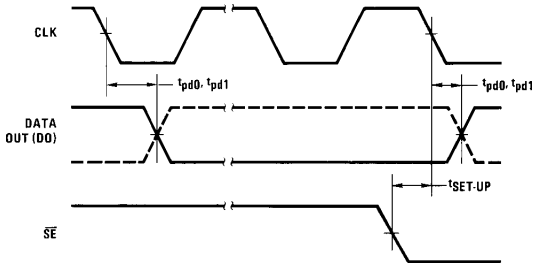


Figure 16. Data Output Timing

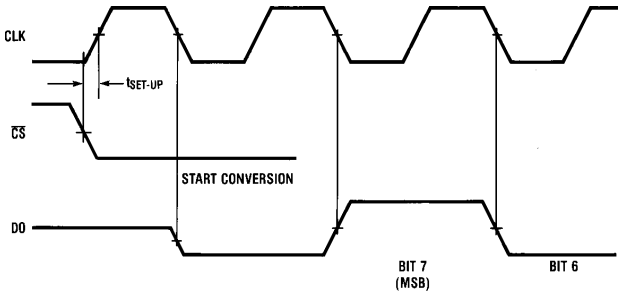
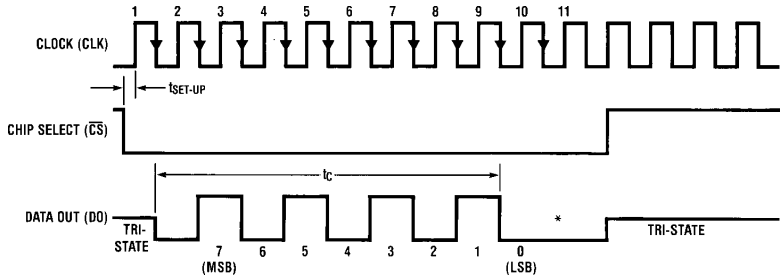


Figure 17. ADC0831-N Start Conversion Timing



*LSB first output not available on ADC0831-N.

Figure 18. ADC0831-N Timing

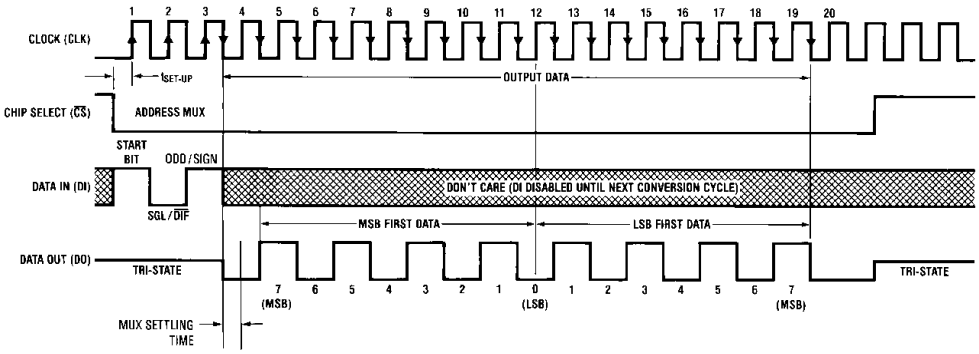


Figure 19. ADC0832-N Timing

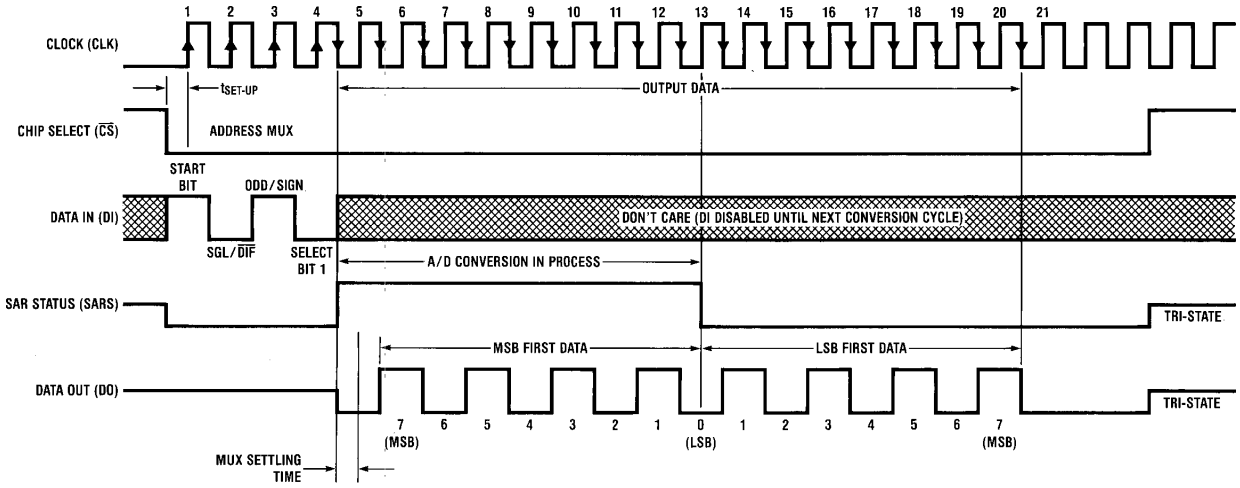
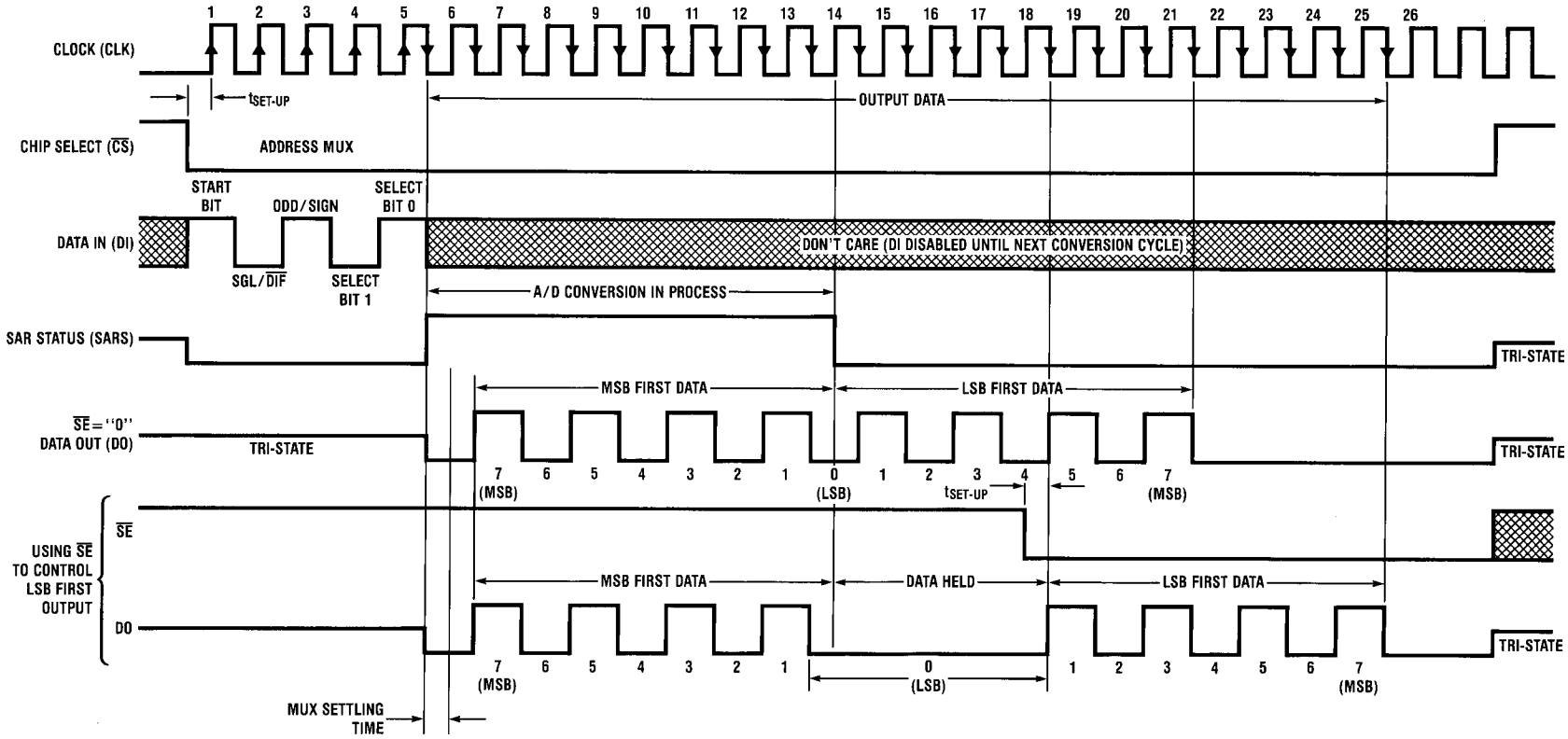


Figure 20. ADC0834-N Timing

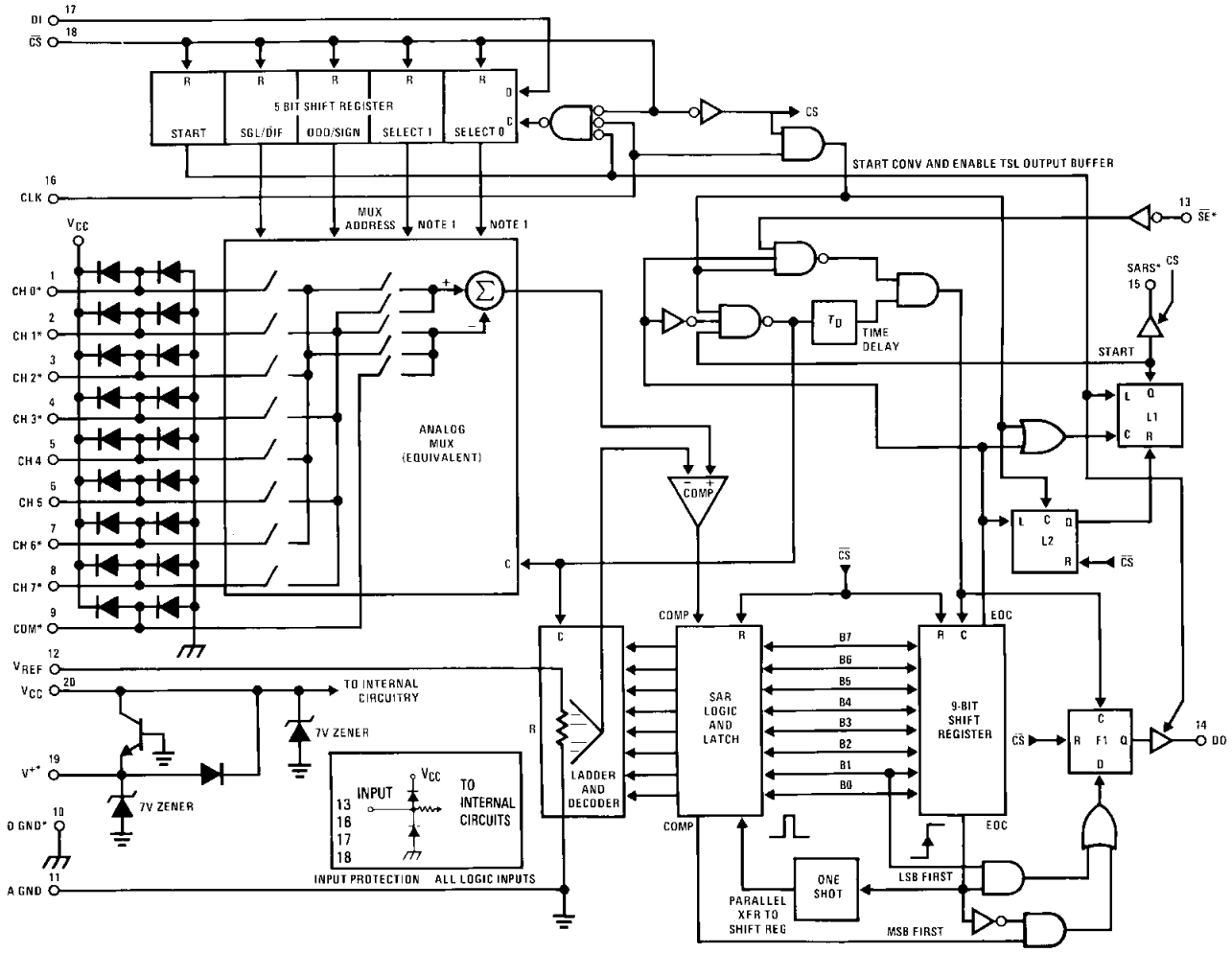
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*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

Figure 21. ADC0838-N Timing

ADC0838-N Functional Block Diagram



*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834-N, D1 is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832-N, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

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Functional Description

Multiplexer Addressing

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831-N contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838-N can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

Table 1. Multiplexer/Package Options Single-Ended MUX Mode

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC0831-N	1	1	8
ADC0832-N	2	1	8
ADC0834-N	4	2	14
ADC0838-N	8	4	20

Table 2. MUX Addressing: ADC0838-N Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

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Table 3. MUX Addressing: ADC0838-N Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0		1		2		3	
		1	0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

Table 4. MUX Addressing: ADC0834-N Single-Ended MUX Mode

MUX Address			Channel #			
SGL / DIF	ODD / SIGN	SELECT	0	1	2	3
		1				
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

Table 5. MUX Addressing: ADC0834-N Differential MUX Mode

MUX Address			Channel #			
SGL / DIF	ODD / SIGN	SELECT	0	1	2	3
		1				
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

Table 6. MUX Addressing: ADC0832-N Single-Ended MUX Mode

MUX Address		Channel #	
SGL / $\overline{\text{DIF}}$	ODD / SIGN	0	1
1	0	+	
1	1		+

Table 7. MUX Addressing: ADC0832-N Differential MUX Mode

MUX Address		Channel #	
SGL / $\overline{\text{DIF}}$	ODD / SIGN	0	1
0	0	+	−
0	1	−	+

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. Figure 22 illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

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THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

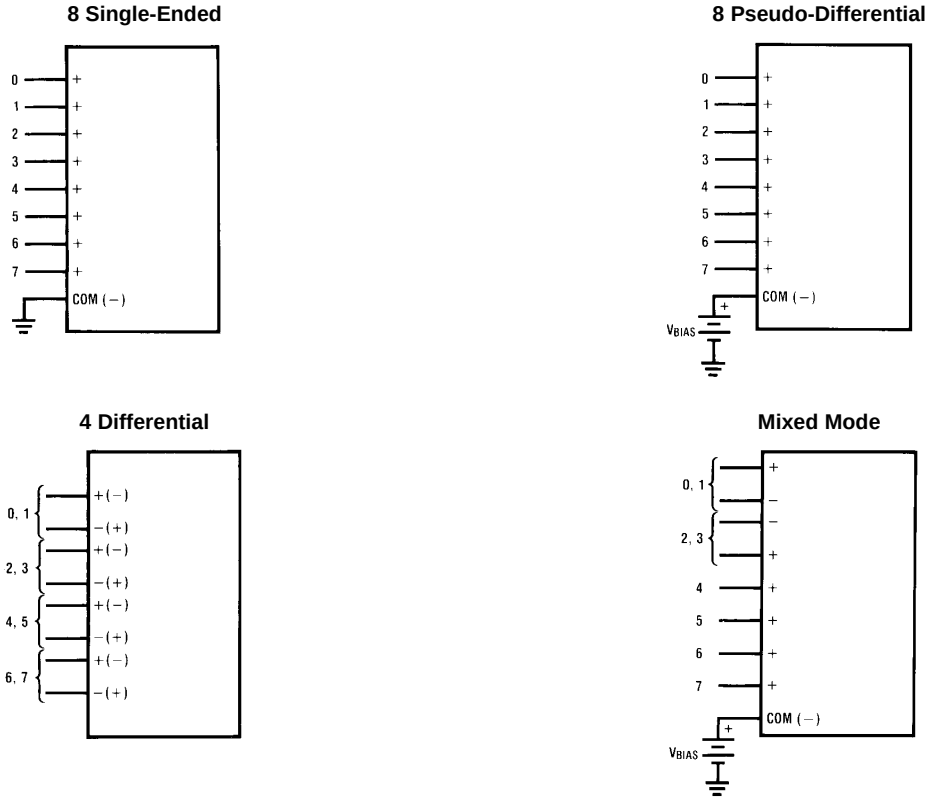


Figure 22. Analog Input Multiplexer Options for the ADC0838-N

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic “1” that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

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7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838-N the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831-N is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

Reference Considerations

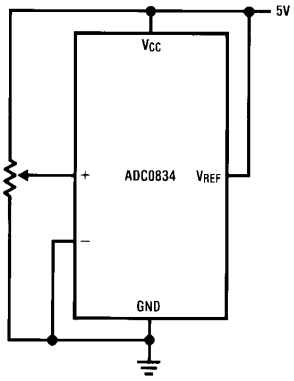
The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 3.5 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832-N). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

a) Ratiometric



b) Absolute with a reduced Span

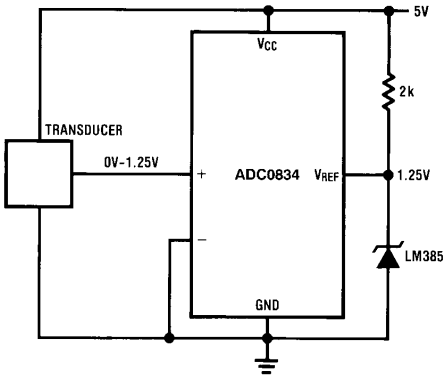


Figure 23. Reference Examples

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The Analog Inputs

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}} \right) \quad (1)$$

where

- f_{CM} is the frequency of the common-mode signal
- V_{PEAK} is its peak voltage value
- f_{CLK}, is the A/D clock frequency

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 µA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

Optional Adjustments

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN}(−) input and applying a small magnitude positive voltage to the V_{IN}(+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB=9.8 mV for V_{REF}=5.000 V_{DC}).

Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input (or V_{CC} for the ADC0832) for a digital output code which is just changing from 1111 1110 to 1111 1111.

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Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB= analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN}(−) voltage applied] by forcing a voltage to the V_{IN}(+) input which is given by:

$$V_{IN}(+)\,\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right] \quad (2)$$

where

- V_{MAX} = the high end of the analog input range
- V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

Power Supply

A unique feature of the ADC0838-N and ADC0834-N is the inclusion of a zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in Figure 24(1).

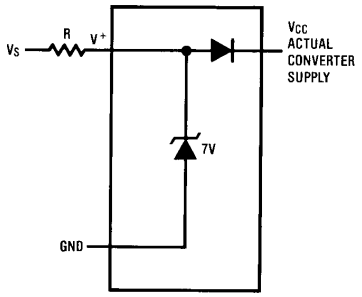


Figure 24. An On-Chip Shunt Regulator Diode

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. Figure 25 and Figure 27 illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V^+ and V_{CC} is shown in Figure 26 and Figure 28. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V^+ pin.

(1) Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore ensured for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See Figure 24 in Functional Description)

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APPLICATIONS

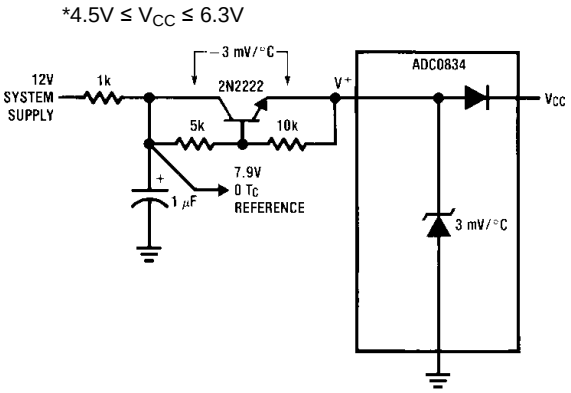


Figure 25. Operating with a Temperature Compensated Reference

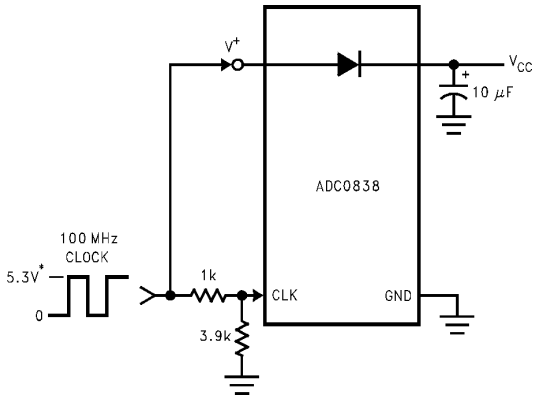


Figure 26. Generating V_{CC} from the Converter Clock

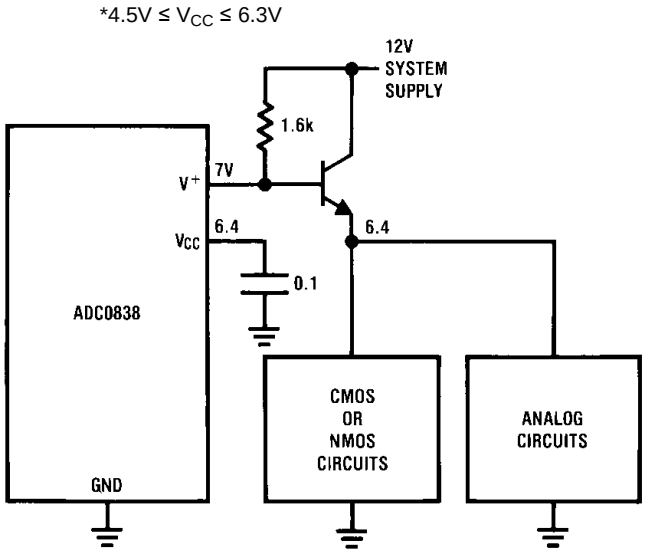


Figure 27. Using the A/D as the System Supply Regulator

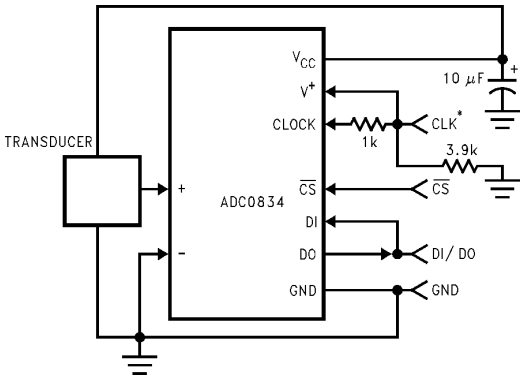


Figure 28. Remote Sensing— Clock and Power on 1 Wire

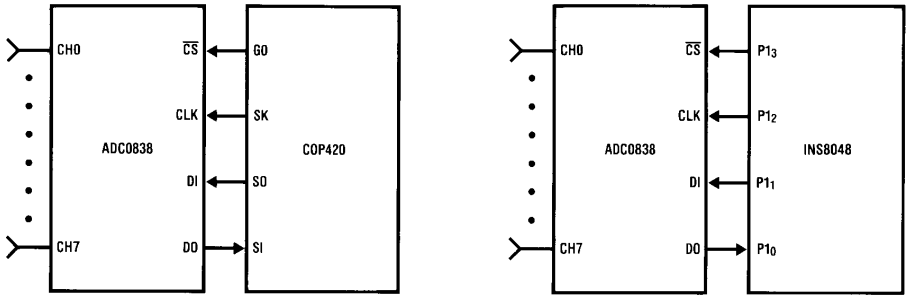


Figure 29. Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048

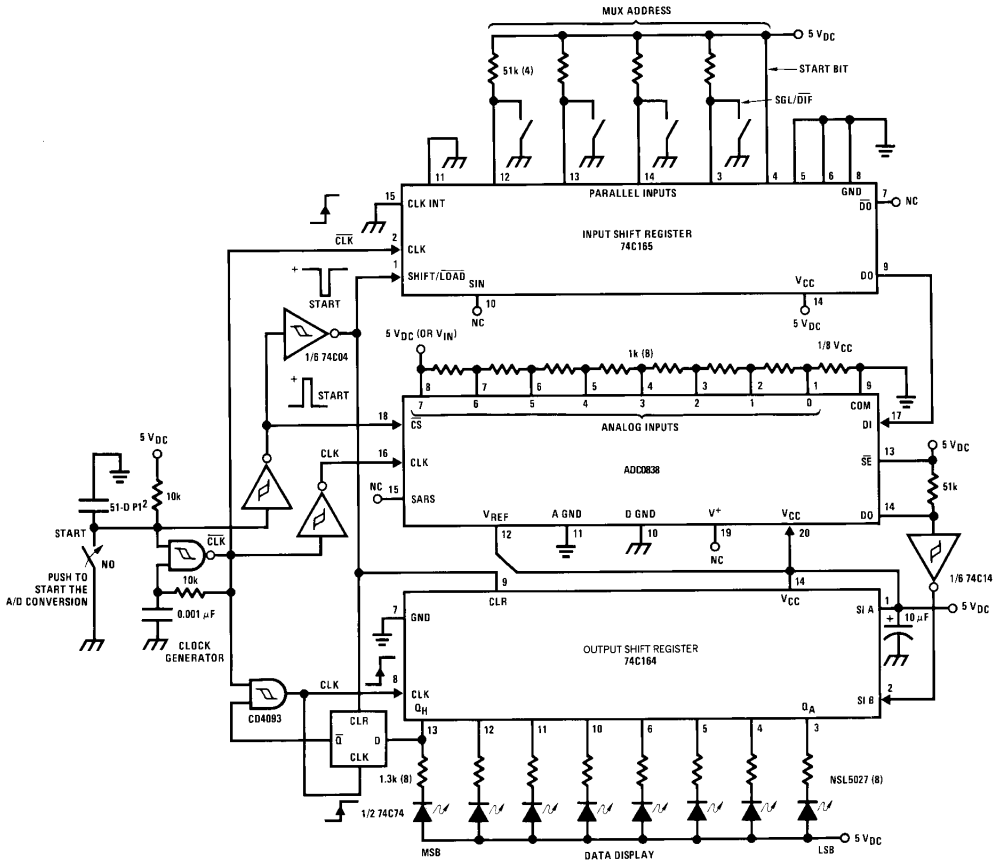
Cop Coding Example

```
   Mnemonic                Instruction
LEI                 ENABLES SIO's INPUT AND OUTPUT
SC                  C = 1
OGI                 G0 = 0 (CS = 0)
CLR A               CLEARS ACCUMULATOR
AISC 1              LOADS ACCUMULATOR WITH 1
XAS                 EXCHANGES SIO WITH ACCUMULATOR
                    AND STARTS SK CLOCK
LDD                 LOADS MUX ADDRESS FROM RAM
                    INTO ACCUMULATOR
NOP                 -
XAS                 LOADS MUX ADDRESS FROM
                    ACCUMULATOR
                          ↑
                    8 INSTRUCTIONS
                          ↓
XAS                 READS HIGH ORDER NIBBLE (4 BITS)
                    INTO ACCUMULATOR
XIS                 PUTS HIGH ORDER NIBBLE INTO RAM
CLER A              CLEARS ACCUMULATOR
RC                  C = 0
XAS                 READS LOW ORDER NIBBLE INTO
                    ACCUMULATOR AND STOPS SK
XIS                 PUTS LOW ORDER NIBBLE INTO RAM
OGI                 G0 = 1 (CS = 1)
LEI                 DISABLES SIO's INPUT AND OUTPUT
```

8048 Coding Example

```
    Mnemonic       Instruction
START:   ANL   P1, #0F7H  ;SELECT A/D (CS = 0)
         MOV   B, #5      ;BIT COUNTER←5
         MOV   A, #ADDR   ;A←MUX ADDRESS
LOOP 1:  RRC   A          ;CY←ADDRESS BIT
         JC    ONE        ;TEST BIT
                          ;BIT=0
ZERO:    ANL   P1, #0FEH  ;DI←0
         JMP   CONT       ;CONTINUE
                          ;BIT=1
ONE:     ORL   P1, #1     ;DI←1
CONT:    CALL  PULSE      ;PULSE SK 0→1→0
         DJNZ  B, LOOP 1  ;CONTINUE UNTIL
                          DONE
         CALL  PULSE      ;EXTRA CLOCK FOR
                          SYNC
         MOV   B, #8      ;BIT COUNTER←8
LOOP 2:  CALL  PULSE      ;PULSE SK 0→1→0
         IN    A, P1      ;CY←DO
         RRC   A
         RRC   A
         MOV   A, C       ;A←RESULT
         RLC   A          ;A(0)←BIT AND SHIFT
         MOV   C, A       ;C←RESULT
         DJNZ  B, LOOP 2  ;CONTINUE UNTIL
                          DONE
RETR
                          ;PULSE SUBROUTINE
PULSE:   ORL   P1, #04    ;SK←1
         NOP              ;DELAY
         ANL   P1, #0FBH  ;SK←0
         RET
```


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*Pinouts shown for ADC0838-N.
For all other products tie to
pin functions as shown.

Figure 30. A "Stand-Alone" Hook-Up for ADC0838-N Evaluation

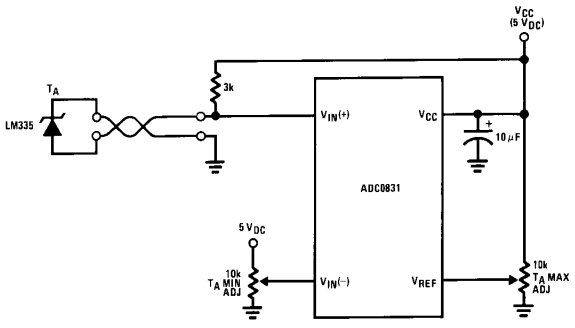


Figure 31. Low-Cost Remote Temperature Sensor

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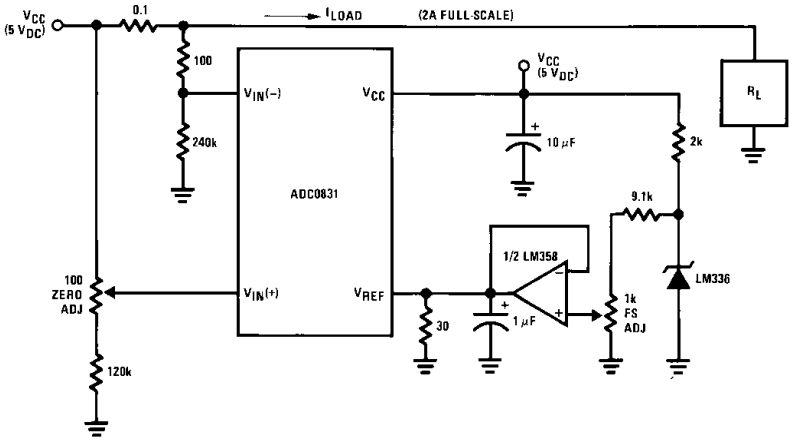
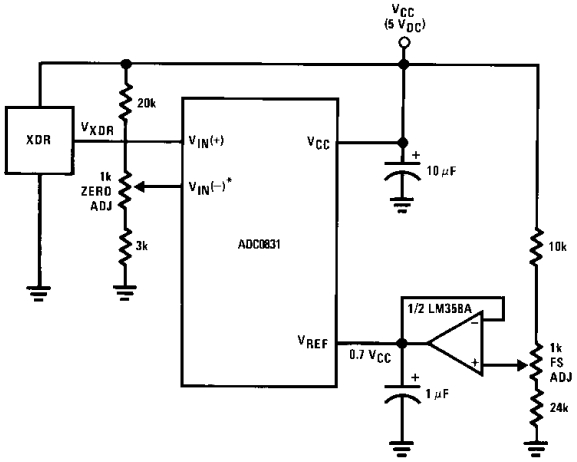


Figure 32. Digitizing a Current Flow



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

Figure 33. Operating with Ratiometric Transducers

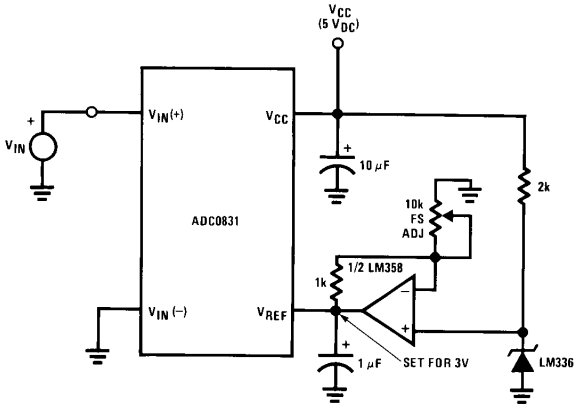


Figure 34. Span Adjust: $0V \le V_{IN} \le 3V$

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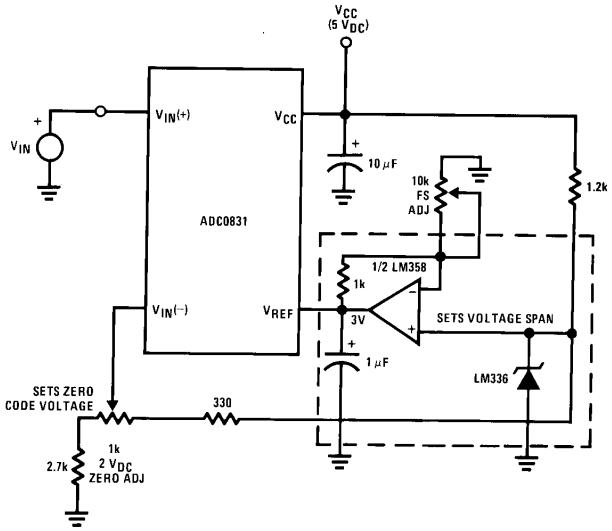


Figure 35. Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

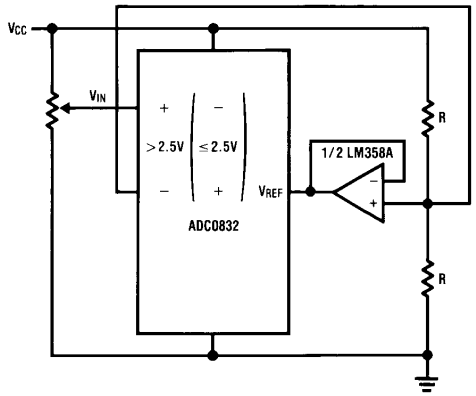
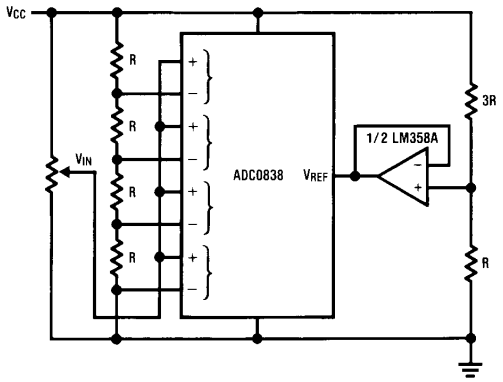
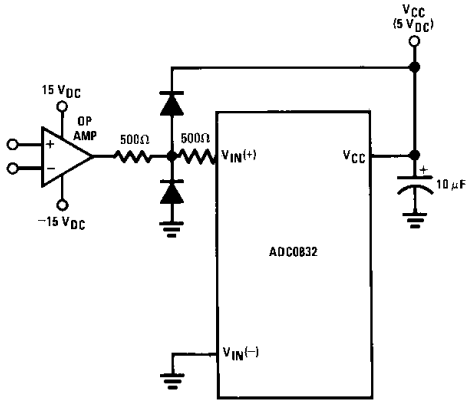


Figure 36. Obtaining Higher Resolution - 9-Bit A/D



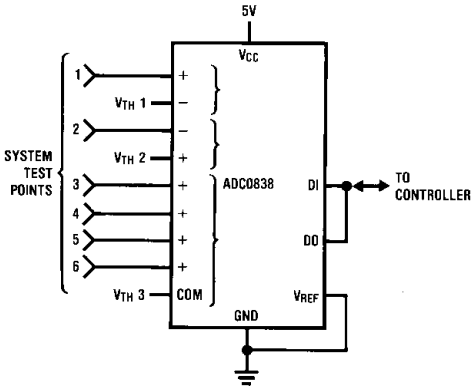
Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

Figure 37. Obtaining Higher Resolution - 10-Bit A/D



Diodes are 1N914

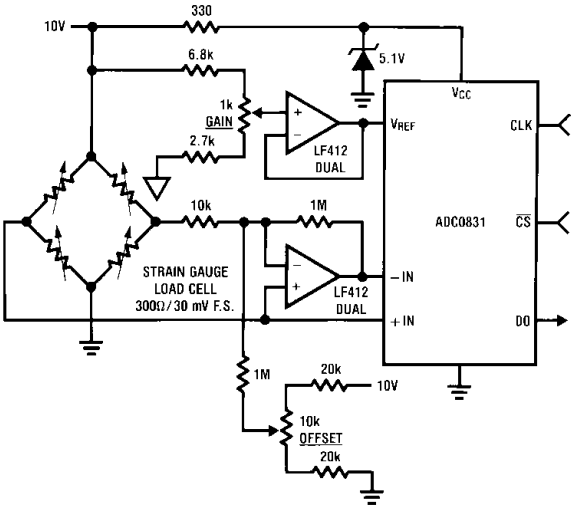
Figure 38. Protecting the Input



DO = all 1s if $+V_{IN} > -V_{IN}$
DO = all 0s if $+V_{IN} < -V_{IN}$

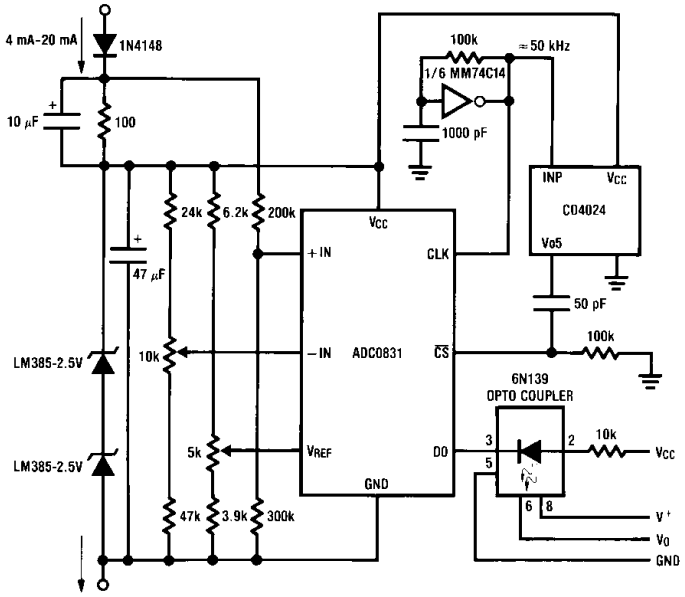
Figure 39. High Accuracy Comparators

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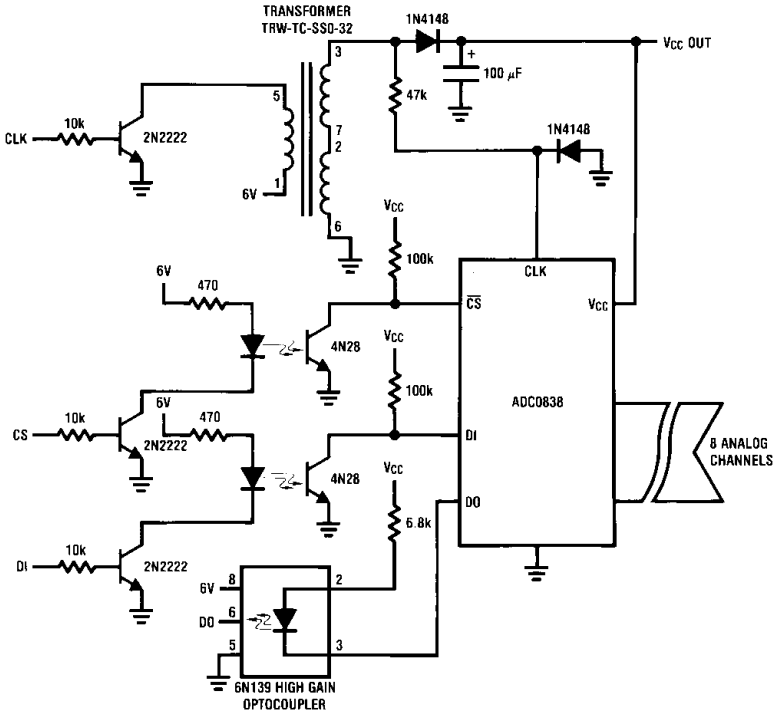
- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

Figure 40. Digital Load Cell



- All power supplied by loop
- 1500V isolation at output

Figure 41. 4 mA-20 mA Current Loop Converter



•No power required remotely
•1500V isolation

Figure 42. Isolated Data Converter

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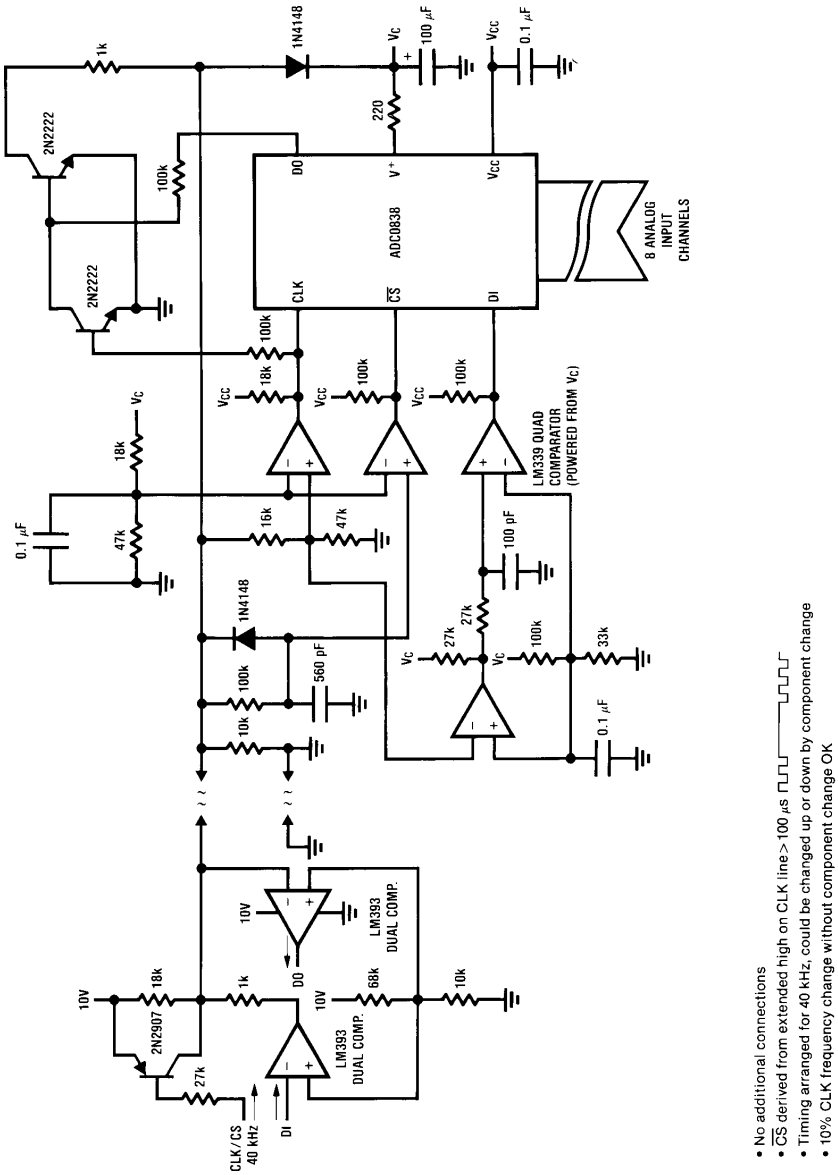


Figure 43. Two Wire Interface for 8 Channels

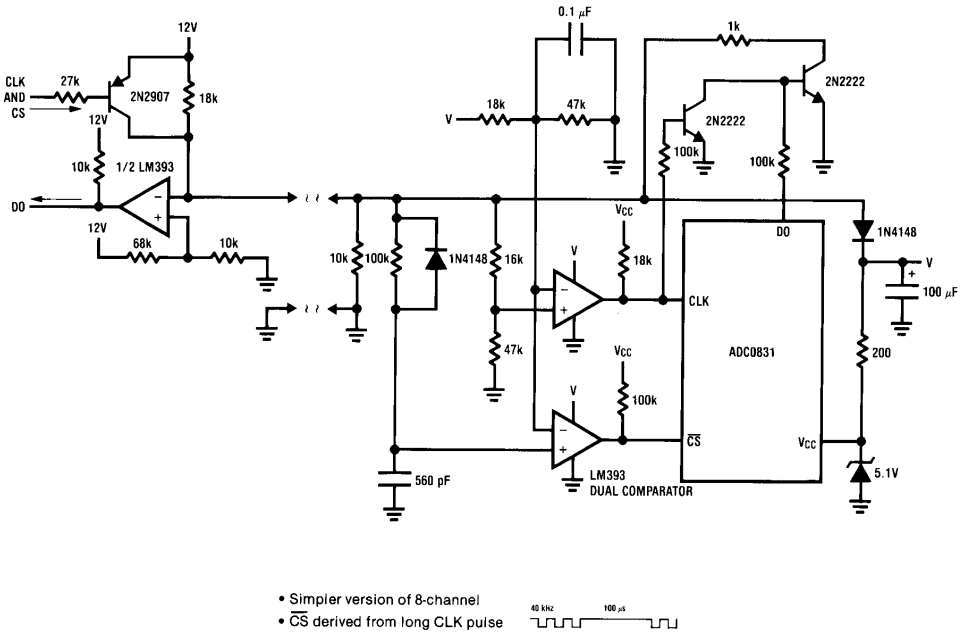


Figure 44. Two Wire 1-Channels Interface

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	28

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC0831CCN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	ADC 0831CCN
ADC0831CCWM/NOPB	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0831CCWM/NOPB.A	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0831CCWM/NOPB.B	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0831CCWMX/NOPB	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0831CCWMX/NOPB.A	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0831CCWMX/NOPB.B	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0831 CCWM
ADC0832CCN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	ADC 0832CCN
ADC0832CCWM/NOPB	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0832CCWM/NOPB.A	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0832CCWM/NOPB.B	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0832CCWMX/NOPB	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0832CCWMX/NOPB.A	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0832CCWMX/NOPB.B	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0832 CCWM
ADC0834CCN/NOPB	Obsolete	Production	PDIP (N) | 14	-	-	Call TI	Call TI	-40 to 85	ADC0834CCN
ADC0834CCWM/NOPB	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM
ADC0834CCWM/NOPB.A	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC0834CCWM/NOPB.B	Active	Production	SOIC (NPA) | 14	50 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM
ADC0834CCWMX/NOPB	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM
ADC0834CCWMX/NOPB.A	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM
ADC0834CCWMX/NOPB.B	Active	Production	SOIC (NPA) | 14	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0834 CCWM
ADC0838CCWM/NOPB	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CCWM/NOPB.A	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CCWM/NOPB.B	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CCWMX/NOPB	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CCWMX/NOPB.A	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CCWMX/NOPB.B	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CCWM
ADC0838CIWM/NOPB	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM
ADC0838CIWM/NOPB.A	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM
ADC0838CIWM/NOPB.B	Active	Production	SOIC (DW) | 20	36 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM
ADC0838CIWMX/NOPB	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM
ADC0838CIWMX/NOPB.A	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM
ADC0838CIWMX/NOPB.B	Active	Production	SOIC (DW) | 20	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC0838 CIWM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

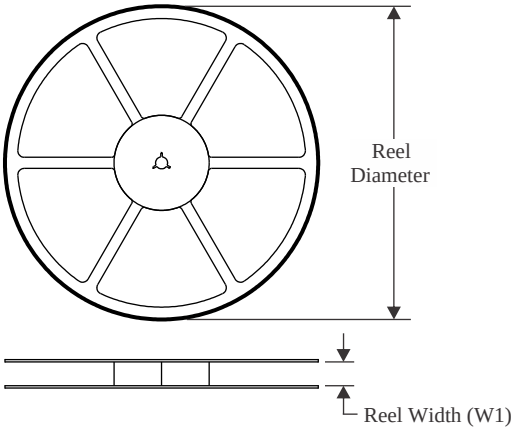
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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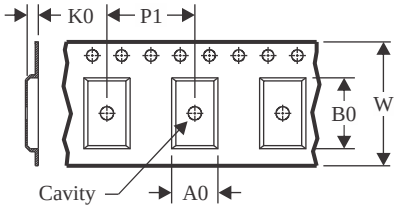
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

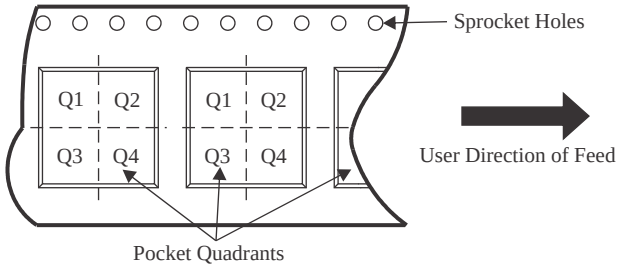


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

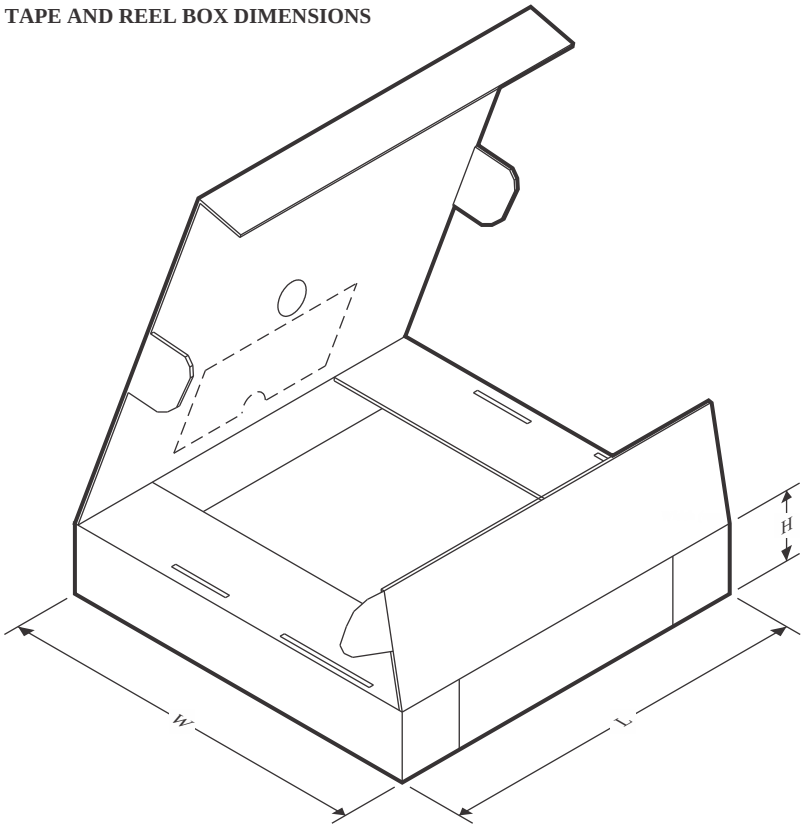
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC0831CCWMX/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1
ADC0832CCWMX/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1
ADC0834CCWMX/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1
ADC0838CCWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1
ADC0838CIWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

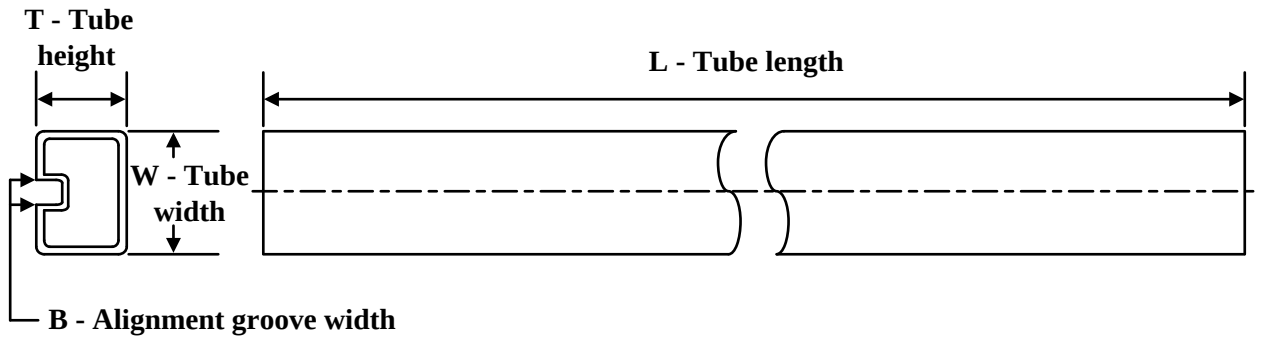
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC0831CCWMX/NOPB	SOIC	NPA	14	1000	356.0	356.0	36.0
ADC0832CCWMX/NOPB	SOIC	NPA	14	1000	356.0	356.0	36.0
ADC0834CCWMX/NOPB	SOIC	NPA	14	1000	356.0	356.0	36.0
ADC0838CCWMX/NOPB	SOIC	DW	20	1000	356.0	356.0	45.0
ADC0838CIWMX/NOPB	SOIC	DW	20	1000	356.0	356.0	45.0

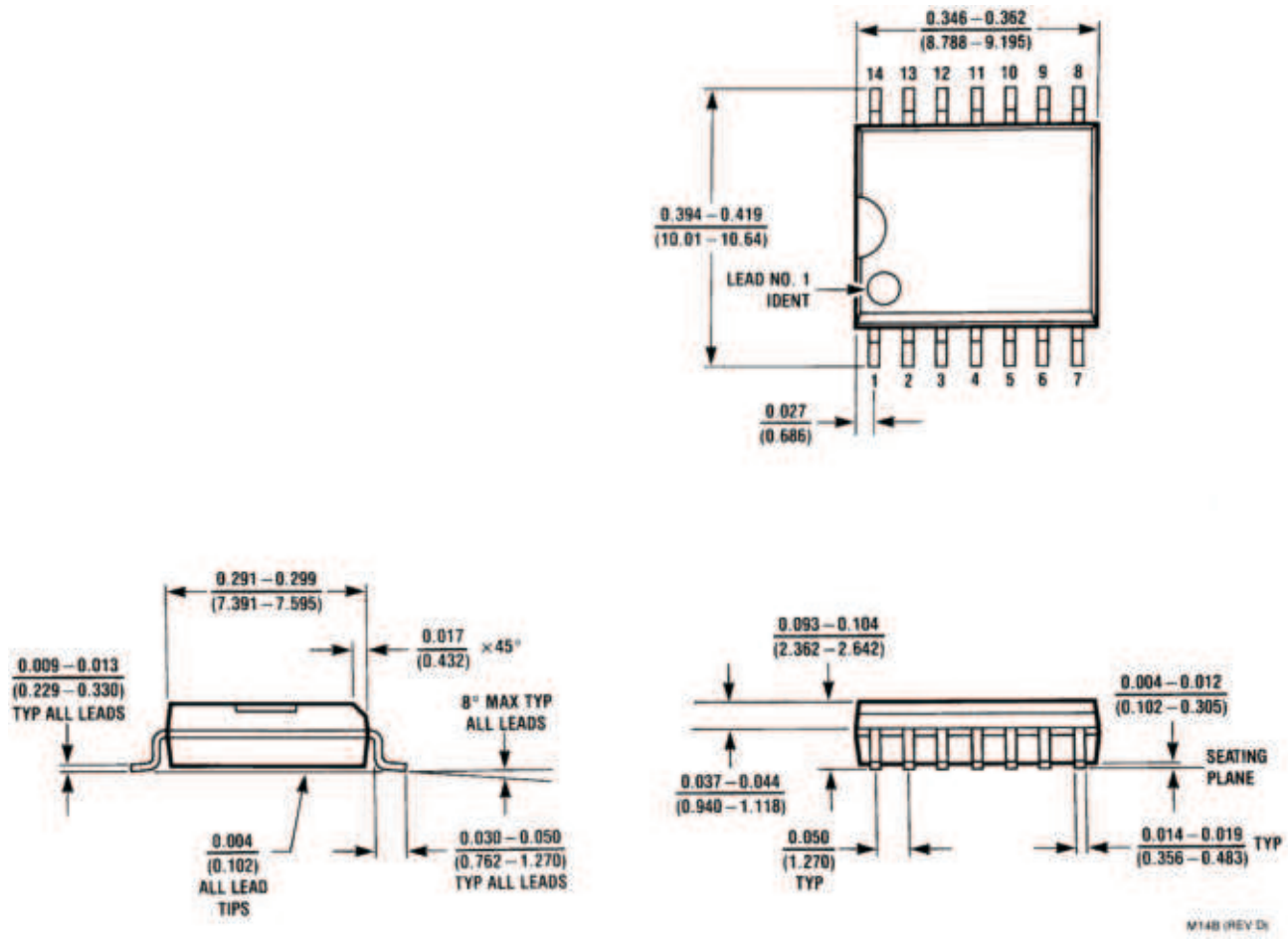
TUBE



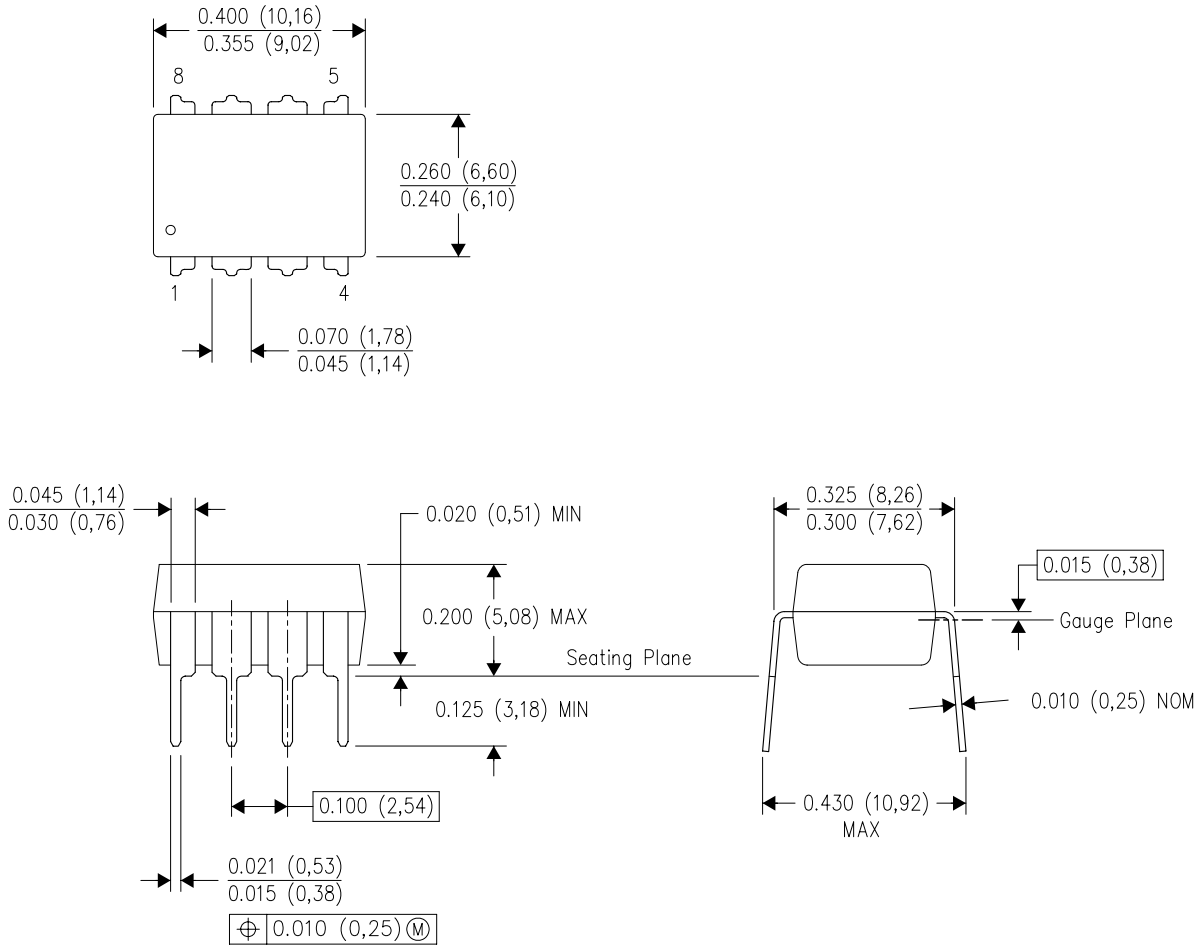
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADC0831CCWM/NOPB	NPA	SOIC	14	50	495	15	5842	7.87
ADC0831CCWM/NOPB.A	NPA	SOIC	14	50	495	15	5842	7.87
ADC0831CCWM/NOPB.B	NPA	SOIC	14	50	495	15	5842	7.87
ADC0832CCWM/NOPB	NPA	SOIC	14	50	495	15	5842	7.87
ADC0832CCWM/NOPB.A	NPA	SOIC	14	50	495	15	5842	7.87
ADC0832CCWM/NOPB.B	NPA	SOIC	14	50	495	15	5842	7.87
ADC0834CCWM/NOPB	NPA	SOIC	14	50	495	15	5842	7.87
ADC0834CCWM/NOPB.A	NPA	SOIC	14	50	495	15	5842	7.87
ADC0834CCWM/NOPB.B	NPA	SOIC	14	50	495	15	5842	7.87
ADC0838CCWM/NOPB	DW	SOIC	20	36	495	15	5842	7.87
ADC0838CCWM/NOPB.A	DW	SOIC	20	36	495	15	5842	7.87
ADC0838CCWM/NOPB.B	DW	SOIC	20	36	495	15	5842	7.87
ADC0838CIWM/NOPB	DW	SOIC	20	36	495	15	5842	7.87
ADC0838CIWM/NOPB.A	DW	SOIC	20	36	495	15	5842	7.87
ADC0838CIWM/NOPB.B	DW	SOIC	20	36	495	15	5842	7.87

NPA0014B


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV D)

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

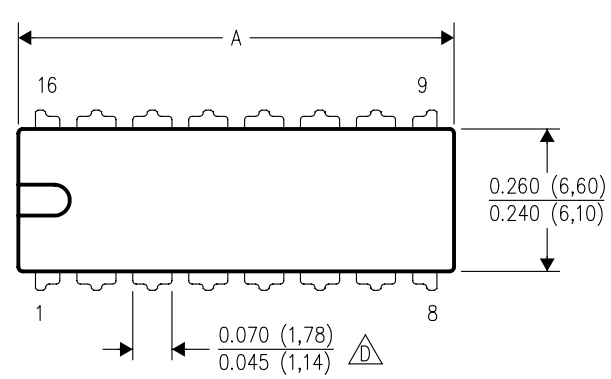


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

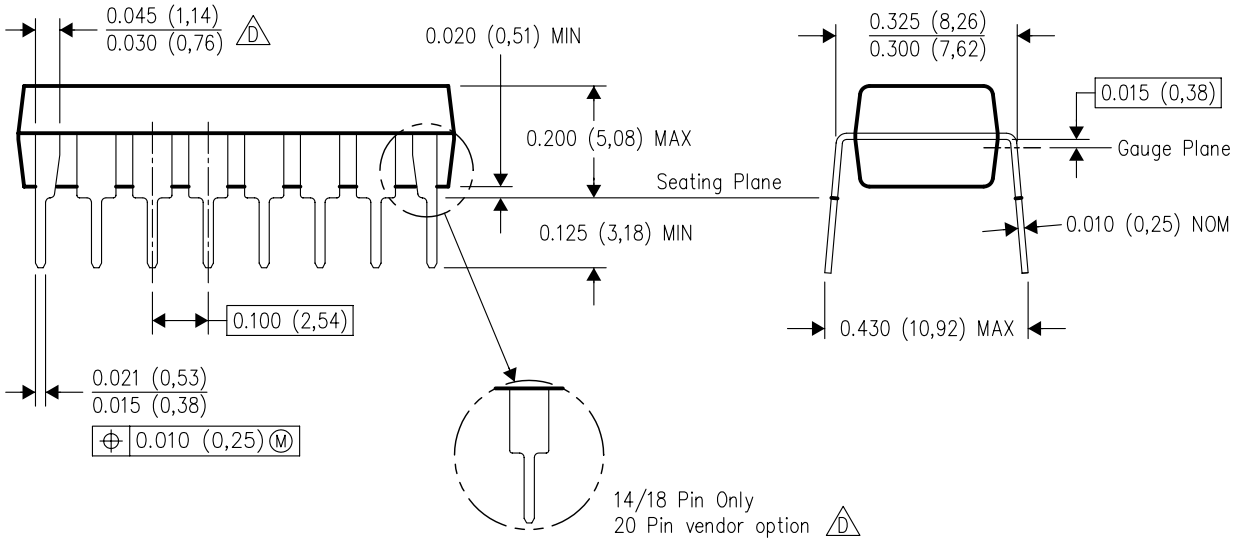
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

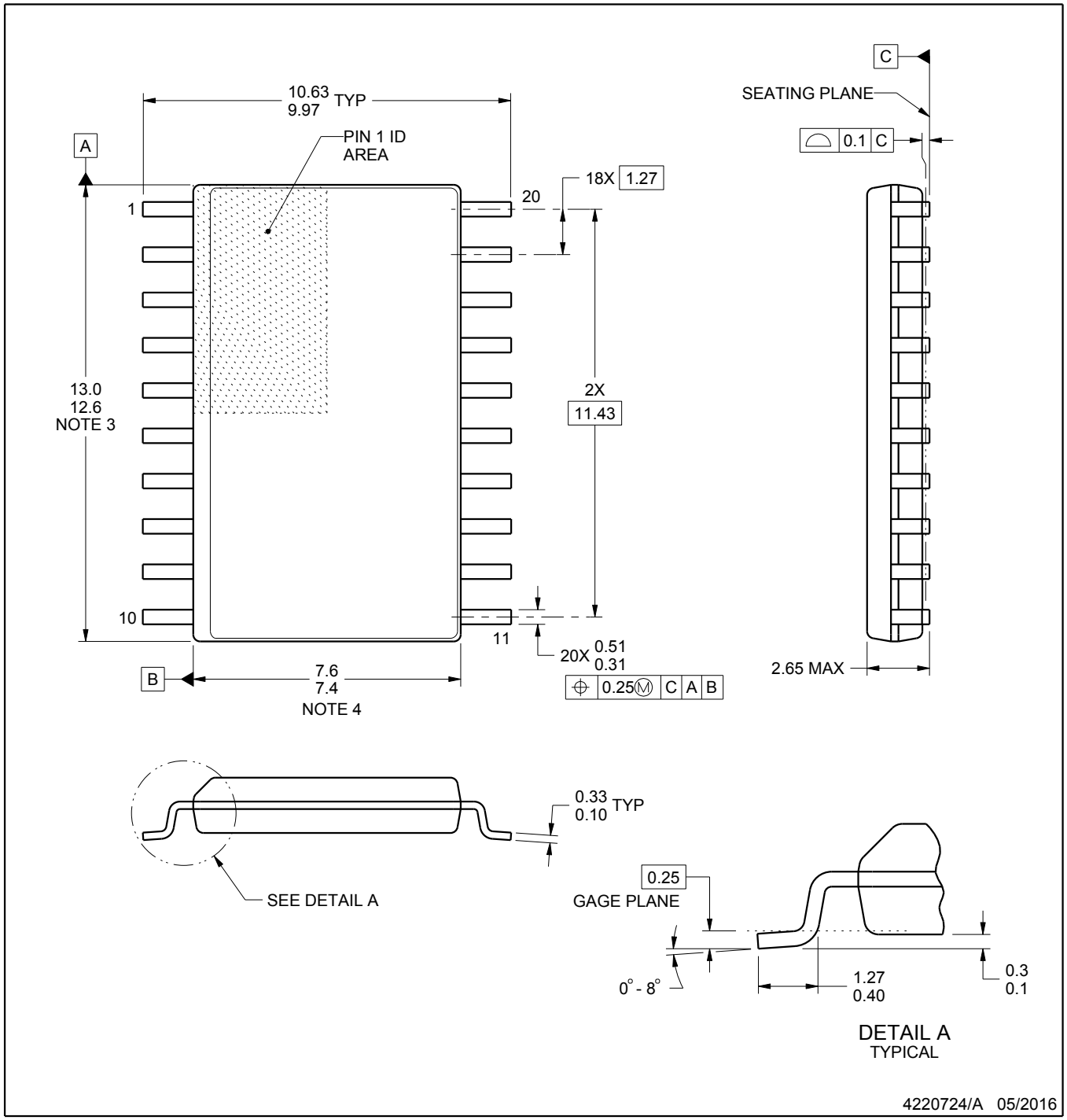


PACKAGE OUTLINE

DW0020A

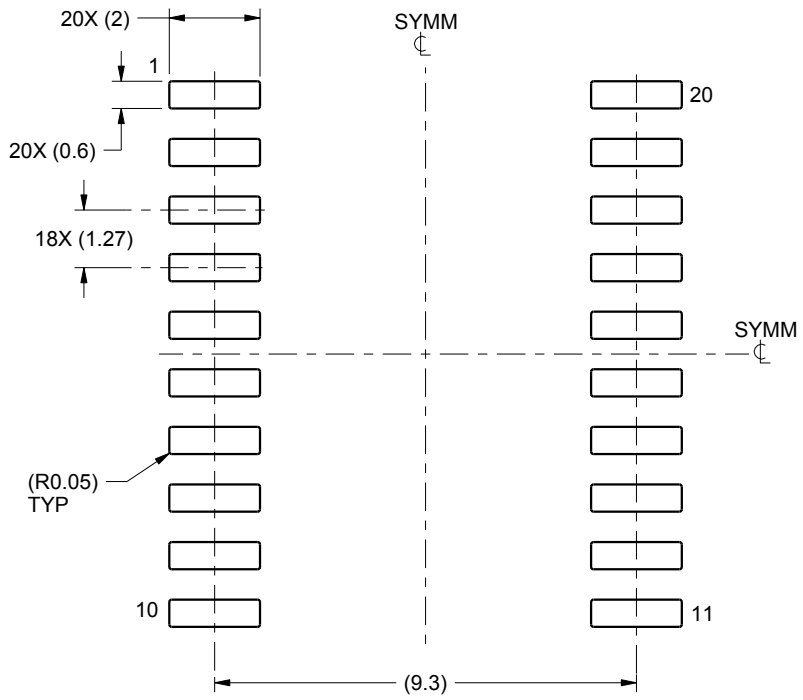
SOIC - 2.65 mm max height

SOIC

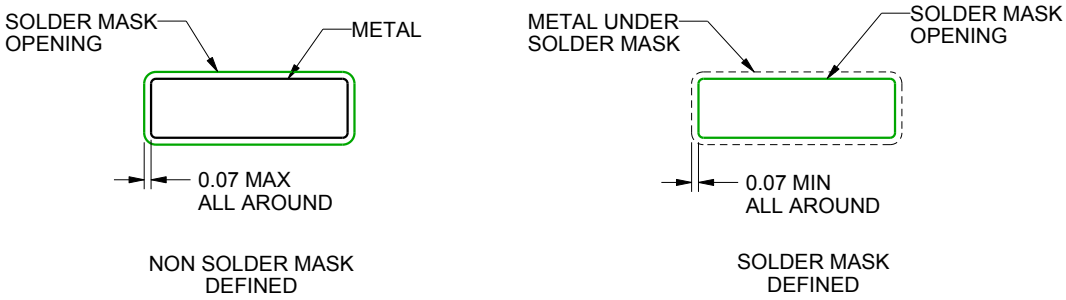


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

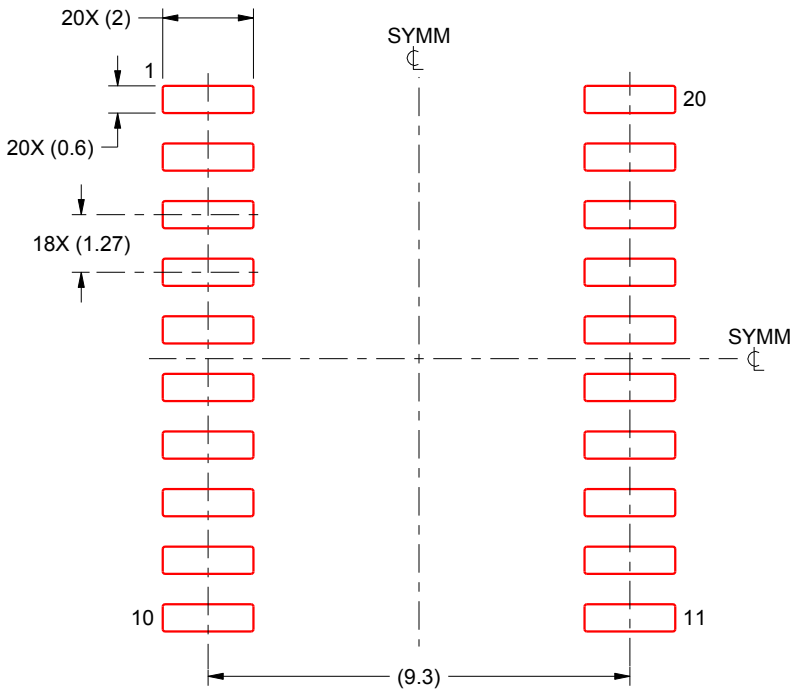


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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