ADC08351 8-Bit, 42 MSPS, 40 mW A/D Converter

Check for Samples: ADC08351

FEATURES

- **Low Input Capacitance**
- **Internal Sample-and-Hold Function**
- **Single +3V Operation**
- **Power Down Feature**
- **TRI-STATE Outputs**

KEY SPECIFICATIONS

- **Resolution: 8 Bits**
- **Maximum Sampling Frequency: 42MSPS (min)**
- **ENOB @ f_{CLK} = 42 MHz, f_{IN} = 4.4 MHz: 7.2 Bits (typ)**
- **Ensured No Missing Codes**
- **Power Consumption: 40 mW (typ); 48 mW (max) (Excluding Reference Current)**

APPLICATIONS

- **Video Digitization**
- **Digital Still Cameras**
- **Set Top Boxes**
- **Digital Camcorders**
- **Communications**
- **Medical Imaging**
- **Personal Computer Video**
- **CCD Imaging**
- **Electro-Optics**

DESCRIPTION

The ADC08351 is an easy to use low power, low cost, small size, 42 MSPS analog-to-digital converter that digitizes signals to 8 bits. The ADC08351 uses an unique architecture that achieves 7.2 Effective Bits with a 4.4 MHz input and 42 MHz clock frequency and 6.8 Effective Bits with a 21 MHz input and 42 MHz clock frequency. Output formatting is straight binary coding.

To minimize system cost and power consumption, the ADC08351 requires minimal external components and includes input biasing to allow optional a.c. input signal coupling. The user need only provide a +3V supply and a clock. Many applications require no separate reference or driver components.

The excellent dc and ac characteristics of this device, together with its low power consumption and +3V single supply operation, make it ideally suited for many video and imaging applications, including use in portable equipment. Total power consumption is reduced to less than 7 mW in the power-down mode. Furthermore, the ADC08351 is resistant to latch-up and the outputs are short-circuit proof.

Fabricated on a 0.35 micron CMOS process, the ADC08351 is offered in TSSOP and WQFN (a molded lead frame-based chip-scale package), and is designed to operate over the industrial temperature range of −40°C to +85°C.

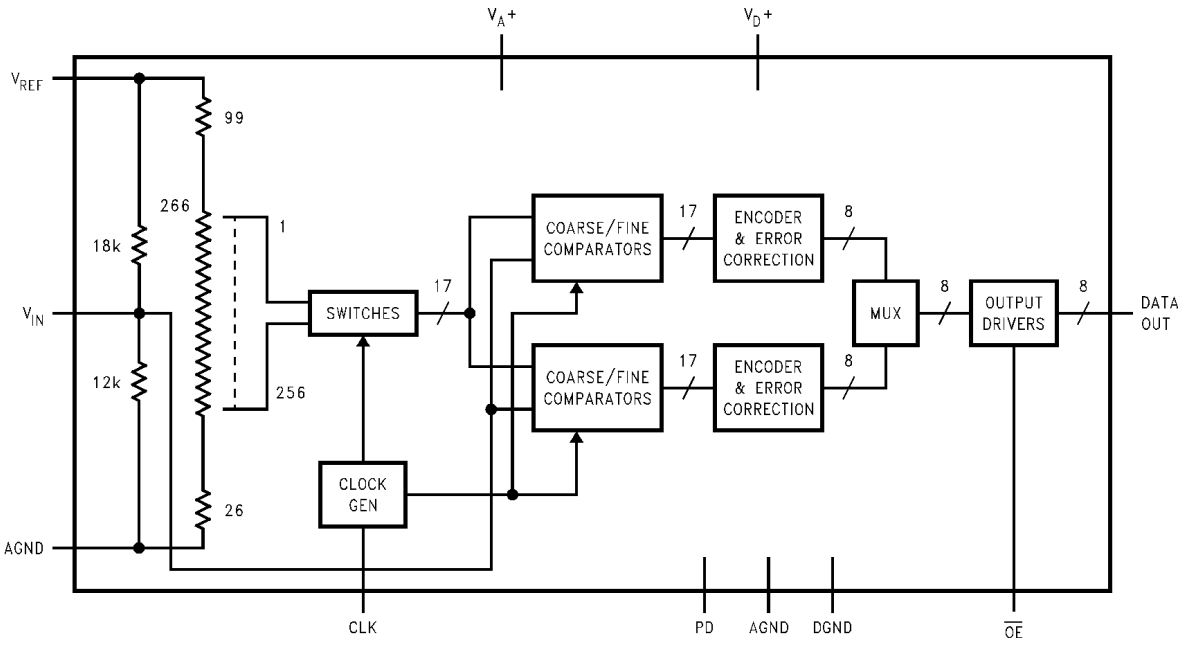
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000–2013, Texas Instruments Incorporated

ADC08351 Block Diagram



Pin Configuration

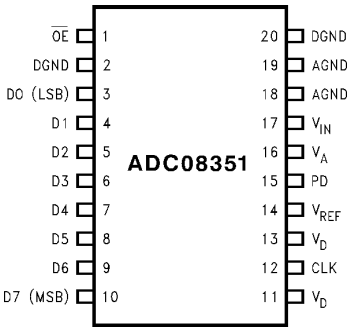


Figure 1. 20-Pin TSSOP - Top View

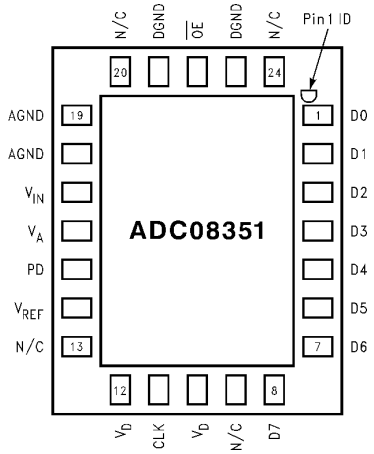
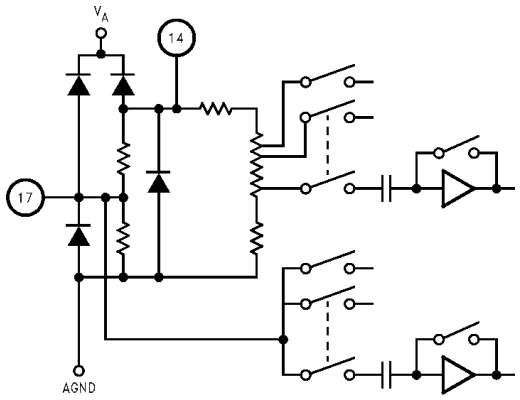
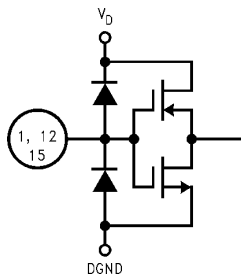
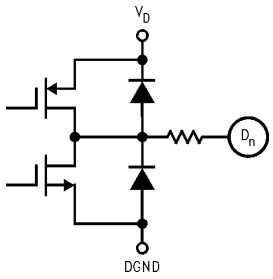


Figure 2. 24-Pin WQFN (CSP) - Bottom View

Copyright © 2000–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS(1)

Pin No.	Symbol	Equivalent Circuit	Description
17 (17)	V_{IN}		Analog signal input. Conversion range is 0.5 V_{P-P} to 0.68 V_A.
14 (14)	V_{REF}		Positive reference voltage input. Operating range of this voltage is 0.75V to V_A. This pin should be bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor.
1 (22)	$\overline{OE}$		CMOS/TTL compatible digital input that, when low, enables the digital outputs of the ADC08351. When high, the outputs are in a high impedance state.
12 (11)	CLK		CMOS/TTL compatible digital clock input. V_{IN} is sampled on the falling edge of CLK input.
15 (15)	PD		CMOS/TTL compatible digital input that, when high, puts the ADC08351 into the power down mode, where it consumes minimal power. When this pin is low, the ADC08351 is in the normal operating mode.
3 thru 10 (1 thru 8)	D0–D7		Conversion data digital output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the $\overline{OE}$ pin low.
11, 13 (10, 12)	V_D		Positive digital supply pin. Connect to a clean, quiet voltage source of +3V. V_A and V_D should have a common supply and be separately bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor. See Layout and Grounding for more information.
2, 20 (21, 23)	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC08351.
16 (16)	V_A		Positive analog supply pin. Connected to a clean, quiet voltage source of +3V. V_A and V_D should have a common supply and be separately bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor. See Layout and Grounding for more information.
18, 19 (18, 19)	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC08351 package.

(1) WQFN pins in parentheses

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2000–2013, Texas Instruments Incorporated

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_A, V_D)		4.2V
Voltage on Any Input or Output Pin		−0.3V to 4.2V
Ground Difference (AGND–DGND)		±100 mV
CLK, $\overline{OE}$ Voltage Range		−0.5 to (V_A + 0.5V)
Digital Output Voltage (V_{OH}, V_{OL})		V_D to DGND
Input Current at Any Pin[4]		±25 mA
Package Input Current[4]		±50 mA
Package Dissipation at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	4000V
	Machine Model	200V
Soldering Temp., Infrared, 10 sec.[7]		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DGND, or greater than V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. For the 20-pin TSSOP, θ_{JA} is 135°C/W, so P_DMAX = 926 mW at 25°C and 481 mW at the maximum operating ambient temperature of 85°C. Note that the power dissipation of this device under normal operation will typically be about 68 mW (40 mW quiescent power + 23 mW reference ladder power + 5 mW due to 1 TTL loan on each digital output). The values for maximum power dissipation listed above will be reached only when the ADC08351 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.
(7) See AN-450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 Texas Instruments Linear Data Book, for other methods of soldering surface mount devices.

Operating Ratings[1][2]

Operating Temperature Range	−40°C T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+2.7V to +3.6V
Ground Difference |DGND–AGND|	0V to 100 mV
V_{IN} Voltage Range (V_{P-P})	0.5V to 0.68 V_A

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Copyright © 2000–2013, Texas Instruments Incorporated

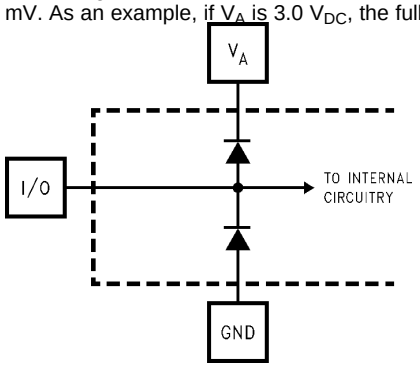
Converter Electrical Characteristics

The following specifications apply for $V_A = V_D = +3.0\ V_{DC}$, $V_{REF} = 2.4V$, $V_{IN} = 1.63\ V_{P-P}$, $\overline{OE} = 0V$, $C_L = 20\ pF$, $f_{CLK} = 42\ MHz$, 50% duty cycle, unless otherwise specified.

Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits $T_A = 25°C$ (1)(2)

Symbol	Parameter	Conditions		Typical (3)	Limits (3)	Units (Limits)
DC Accuracy						
INL	Integral Non Linearity Error			±0.7	**±1.4**	LSB (max)
DNL	Differential Non Linearity			±0.6	**+1.3** **−1.0**	LSB (max) LSB (min)
	Missing Codes				**0**	(max)
E_Z	Zero Scale Offset Error			−17		mV
E_{FS}	Full Scale Offset Error			−7		mV
Video Accuracy						
DP	Differential Phase Error	f_{CLK} = 20 MHz, Video Ramp Input		1.0		Degree
DG	Differential Gain Error	f_{CLK} = 20 MHz, Video Ramp Input		1.5		%
Analog Input and Reference Characteristics						
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 1.5V + 0.7 Vrms	(CLK LOW)	4		pF
			(CLK HIGH)	11		pF
R_{IN}	R_{IN} Input Resistance			7.2		kΩ
FPBW	Full-Power Bandwidth			120		MHz
V_{REF}	Reference Input Voltage	At pin 14		0.735 V_A		V V
I_{REF}	Reference Input Current			7.7		mA
Power Supply Characteristics						
I_A	Analog Supply Current	PD = Low		10.5		mA
		PD = High		1		mA
I_D	Digital Supply Current	PD = Low, No Digital Output Load		2.9		mA
		PD = High		0.5		mA
	Total Operating Current	Excluding Reference Current, $V_{IN} = 0\ V_{DC}$		13.4	**16**	mA (max)
	Power Consumption (active)	PD = Low (excluding reference current)		40.2	**48**	mW (max)
	Power Consumption (power down)	PD = High (excluding reference current)		<7		mW

(1) All inputs are protected as shown below. Input voltage magnitudes up to 500 mV above the supply voltage or 500 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_A or below AGND by more than 300 mV. As an example, if V_A is 3.0 V_{DC}, the full-scale input voltage must be ≤3.3 V_{DC} to ensure accurate conversions.



(2) To ensure accuracy, it is required that V_A and V_D be well bypassed. Each V_A and V_D pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to TI's AOQL (Average Outgoing Quality Level).

Copyright © 2000–2013, Texas Instruments Incorporated

Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = V_D = +3.0\ V_{DC}$, $V_{REF} = 2.4V$, $V_{IN} = 1.63\ V_{P-P}$, $\overline{OE} = 0V$, $C_L = 20\ pF$, $f_{CLK} = 42\ MHz$, 50% duty cycle, unless otherwise specified.

Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits $T_A = 25°C$[1][2]

Symbol	Parameter	Conditions	Typical[3]	Limits[3]	Units (Limits)
CLK, $\overline{OE}$ Digital Input Characteristics					
V_{IH}	Logical High Input Voltage	$V_D = V_A = 3V$		**2.0**	V (min)
V_{IL}	Logical Low Input Voltage	$V_D = V_A = 3V$		**1.0**	V (max)
I_{IH}	Logical High Input Current	$V_{IH} = V_D = V_A = 3.3V$	10		µA
I_{IL}	Logic Low Input Current	$V_{IL} = 0V$, $V_D = V_A = 3.3V$	−10		µA
C_{IN}	Logic Input Capacitance		10		pF
Digital Output Characteristics					
I_{OH}	High Level Output Current	$V_D = 2.7V$, $V_{OH} = V_D - 0.5V$		**−1.1**	mA (min)
I_{OL}	Low Level Output Current	$V_D = 2.7V$, $\overline{OE}$ = DGND, $V_{OL} = 0.4V$		**1.8**	mA (min)
V_{OH}	High Level Output Voltage	$V_D = 2.7V$, $I_{OH} = -360\ µA$	2.65		V
V_{OL}	Low Level Output Voltage	$V_D = 2.7V$, $I_{OL} = 1.6\ mA$	0.2		V
I_{OZH}, I_{OZL}	TRI-STATE Output Current	$\overline{OE} = V_D = 3.3V$, $V_{OH} = 3.3V$ or $V_{OL} = 0V$	±10		µA
AC Electrical Characteristics					
f_{C1}	Maximum Conversion Rate			**42**	MHz (min)
f_{C2}	Minimum Conversion Rate		2		MHz
t_{OD}	Output Delay	CLK High to Data Valid	14	**19**	ns (max)
	Pipline Delay (Latency)		2.5		Clock Cycles
t_{DS}	Sampling (Aperture) Delay	CLK Low to Acquisition of Data	2		ns
t_{OH}	Output Hold Time	CLK High to Data Invalid	9		ns
t_{EN}	$\overline{OE}$ Low to Data Valid	Loaded as in Figure 20	14		ns
t_{DIS}	$\overline{OE}$ High to High Z State	Loaded as in Figure 20	10		ns
ENOB	Effective Number of Bits	$f_{CLK} = 30\ MHz$, $f_{IN} = 1\ MHz$	7.2		Bits
		$f_{CLK} = 42\ MHz$, $f_{IN} = 4.4\ MHz$	7.2		Bits
		$f_{CLK} = 42\ MHz$, $f_{IN} = 21\ MHz$	6.8	**6.1**	Bits (min)
SINAD	Signal-to-Noise & Distortion	$f_{CLK} = 30\ MHz$, $f_{IN} = 1\ MHz$	45		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 4.4\ MHz$	45		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 21\ MHz$	43	**38.5**	dB (min)
SNR	Signal-to-Noise Ratio	$f_{CLK} = 30\ MHz$, $f_{IN} = 1\ MHz$	44		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 4.4\ MHz$	45		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 21\ MHz$	44	**41**	dB (min)
THD	Total Harmonic Distortion	$f_{CLK} = 30\ MHz$, $f_{IN} = 1\ MHz$	−57		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 4.4\ MHz$	−51		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 21\ MHz$	−46	**−41**	dB (min)
SFDR	Spurious Free Dynamic Range	$f_{CLK} = 30\ MHz$, $f_{IN} = 1\ MHz$	57		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 4.4\ MHz$	54		dB
		$f_{CLK} = 42\ MHz$, $f_{IN} = 21\ MHz$	49	**41**	dB (min)

Copyright © 2000–2013, Texas Instruments Incorporated

Typical Performance Characteristics

$V_A = V_D = V_D$ I/O = 3V, f_{CLK} = 42 MHz, unless otherwise specified

DNL @ 42 MSPS

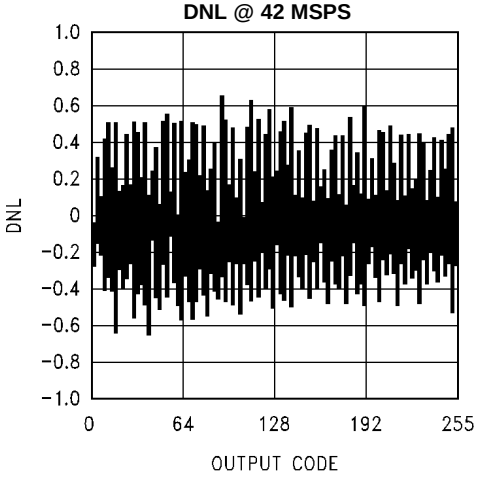


Figure 3.

DNL vs Sample Rate

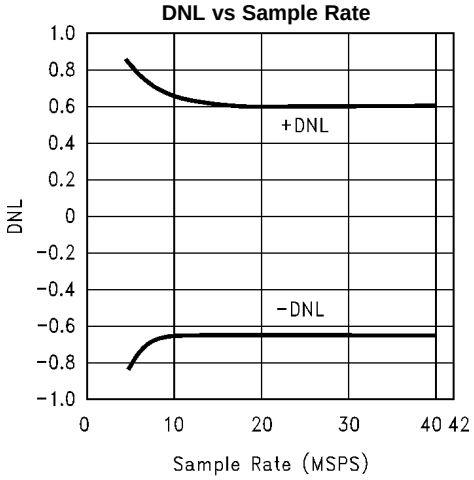


Figure 4.

DNL vs V_A

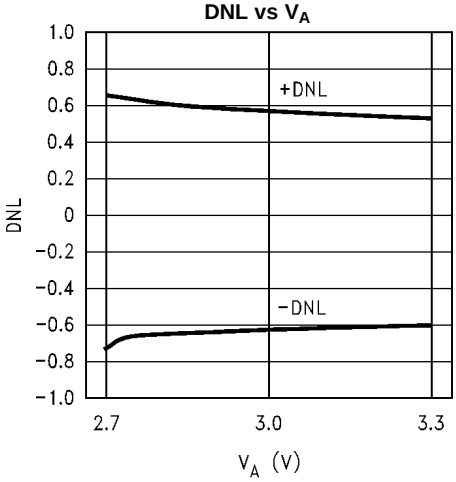


Figure 5.

DNL vs Temperature

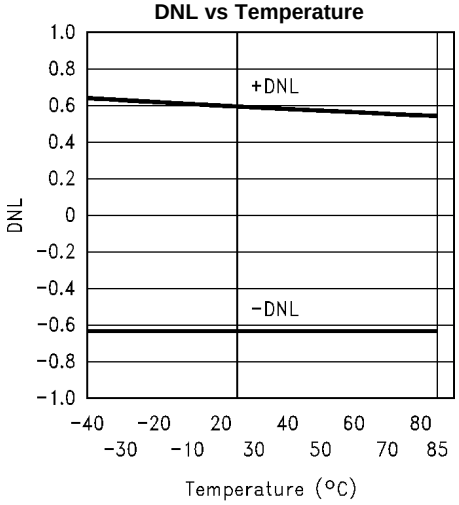


Figure 6.

INL @ 42 MSPS

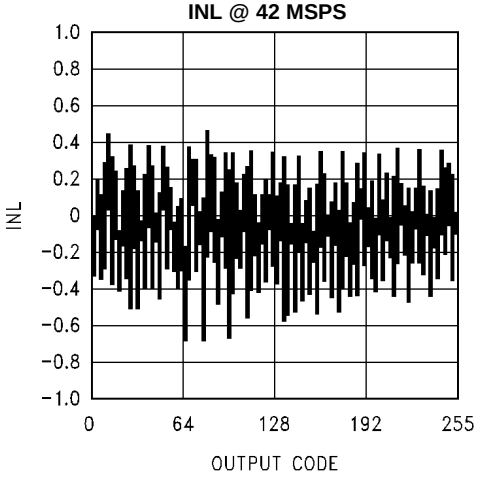


Figure 7.

INL vs Sample Rate

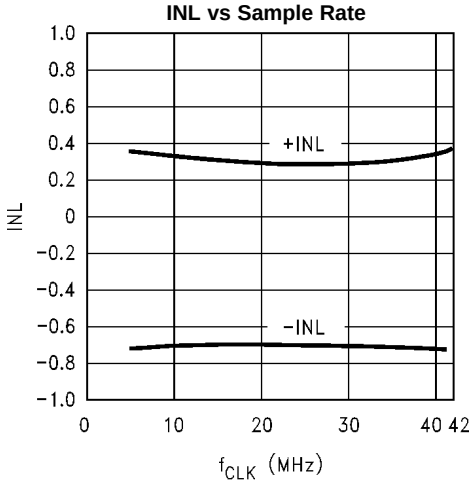


Figure 8.

Copyright © 2000–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

$V_A = V_D = V_D$ I/O = 3V, f_{CLK} = 42 MHz, unless otherwise specified

INL vs V_A

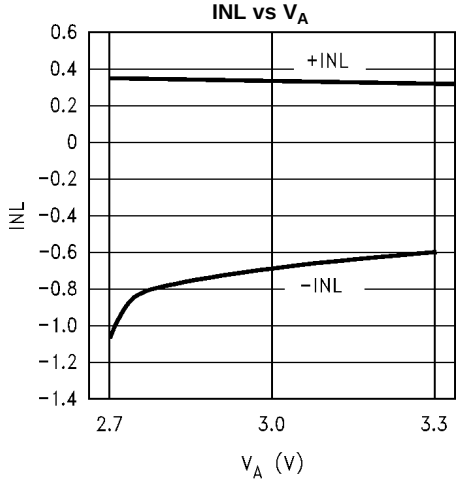


Figure 9.

INL vs Temperature

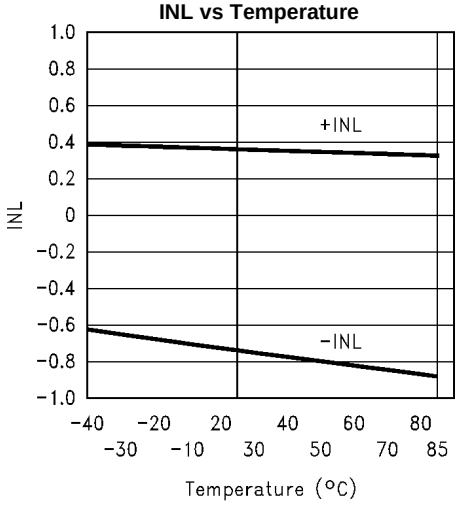


Figure 10.

SINAD and ENOB vs f_{IN}

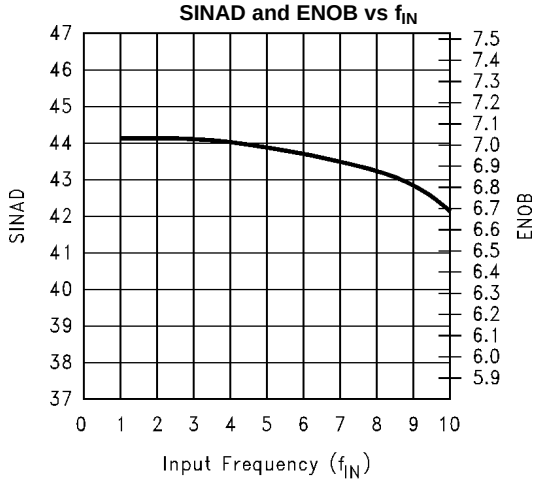


Figure 11.

SINAD and ENOB vs f_{CLK}

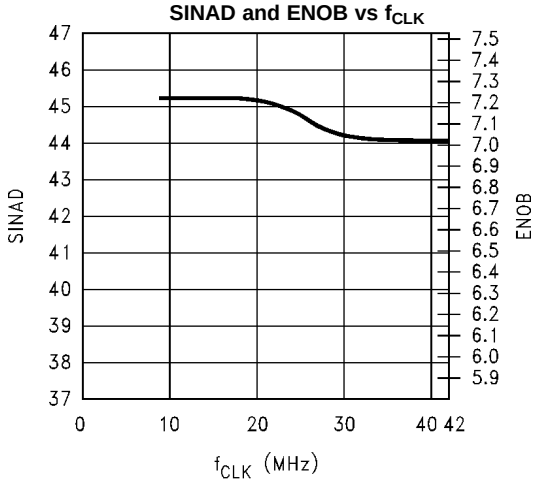


Figure 12.

SINAD and ENOB vs Clock Duty Cycle

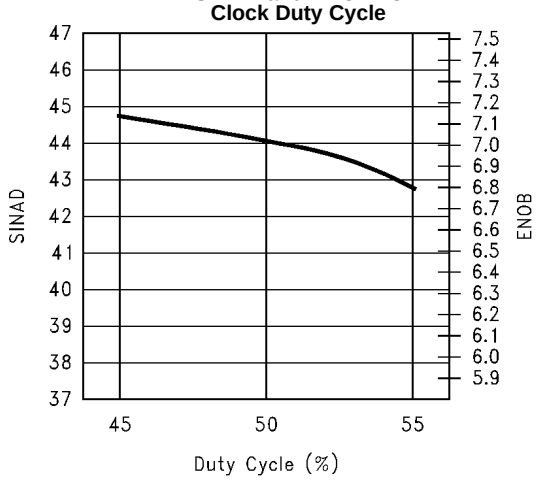


Figure 13.

SNR vs f_{IN}

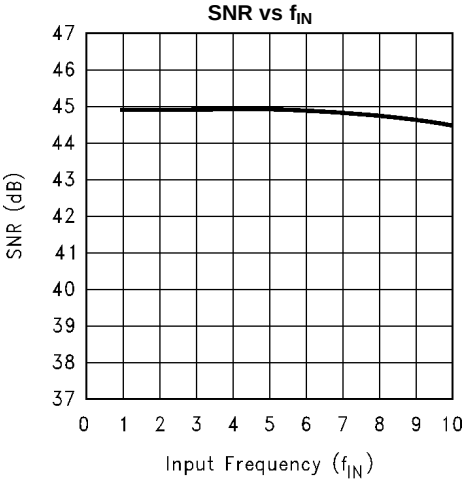


Figure 14.

Copyright © 2000–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

$V_A = V_D = V_D$ I/O = 3V, f_{CLK} = 42 MHz, unless otherwise specified

THD vs f_{IN}

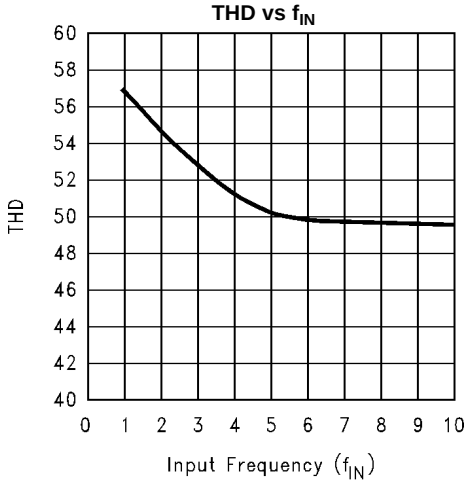


Figure 15.

(I_D) + (I_A) vs f_{CLK}

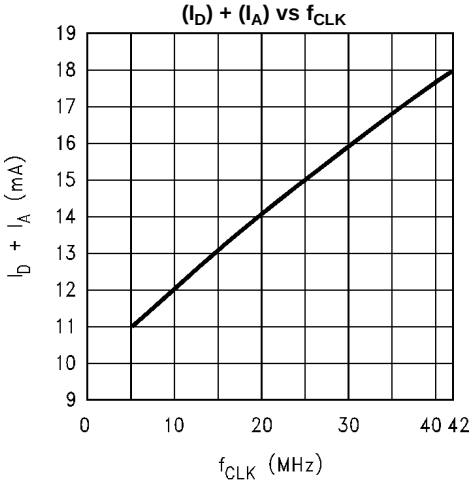


Figure 16.

t_{OD} vs V_D

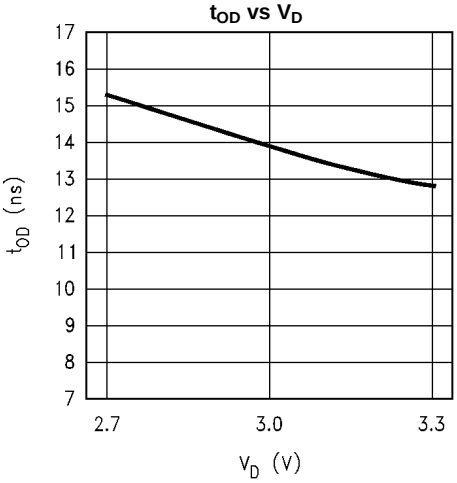


Figure 17.

Spectral Response @ 42 MSPS

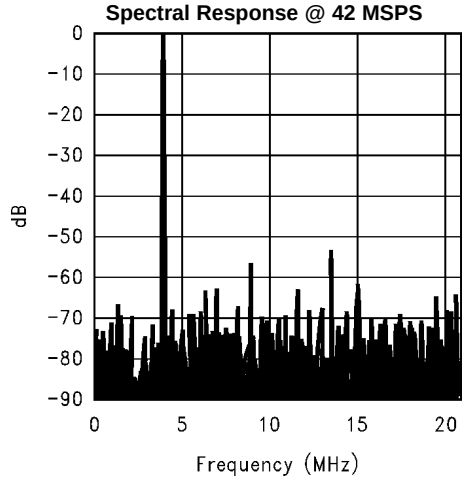


Figure 18.

Specification Definitions

ANALOG INPUT BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

DIFFERENTIAL GAIN ERROR is the percentage difference between the output amplitudes of a high frequency reconstructed sine wave at two different dc input levels.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DIFFERENTIAL PHASE ERROR is the difference in the output phase of a reconstructed small signal sine wave at two different dc input levels.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD - 1.76)/6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100KHz plus integer multiples of f_{CLK} The input frequency at which the output is —3 dB relative to the low frequency input signal is the full power bandwidth.

FULL SCALE OFFSET ERROR is the difference between the analog input voltage that just causes the output code to transition to the full scale code (all 1's in the case of the ADC08351) and the ideal value of 1½ LSB below the value of V_{REF}.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and the availability of that conversion result at the output. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

SAMPLING (APERTURE) DELAY is that time required after the fall of the clock input for the sampling switch to open. The sample is effectively taken this amount of time after the fall of the clock input.

SIGNAL TO NOISE RATIO (SNR) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first six harmonic components to the rms value of the input signal.

ZERO SCALE OFFSET ERROR is the difference between the analog input voltage that just causes the output code to transition to the first code and the ideal value of ½ LSB for that transition.

Copyright © 2000–2013, Texas Instruments Incorporated

Timing Diagram

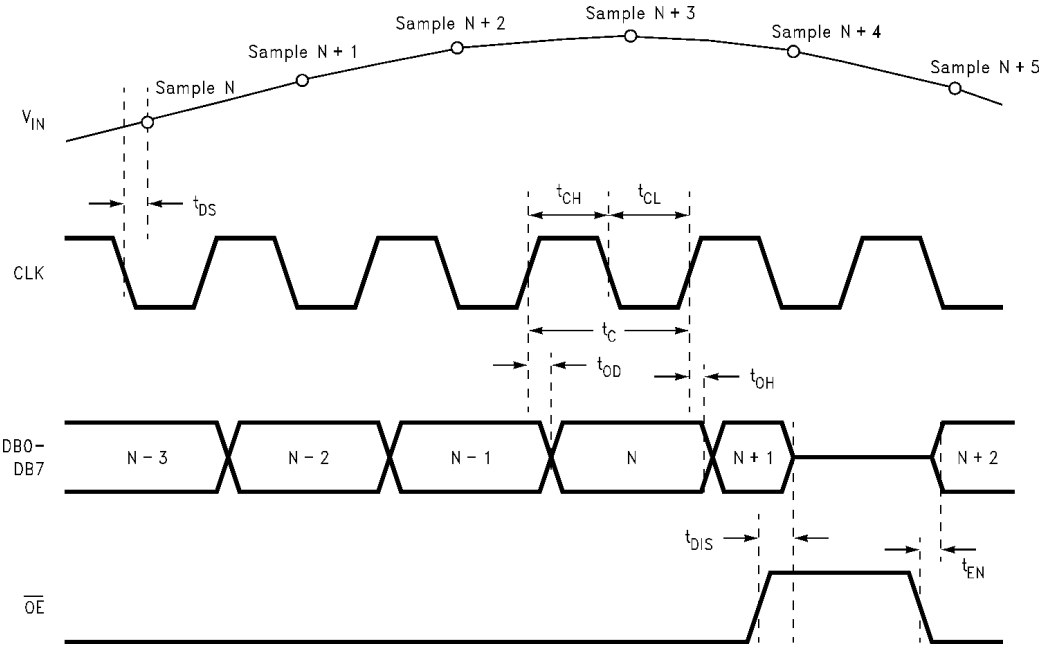


Figure 19. ADC08351 Timing Diagram

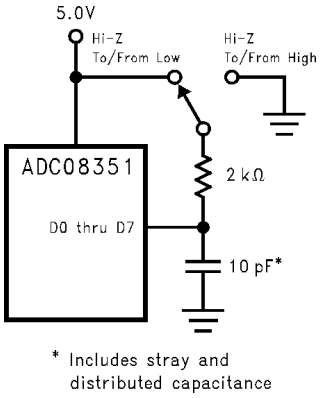


Figure 20. t_{EN}, t_{DIS} Test Circuit

FUNCTIONAL DESCRIPTION

The ADC08351 achieves 6.8 effective bits at 21 MHz input frequency with 42 MHz clock frequency digitizing to eight bits the analog signal at V_{IN} that is within the nominal voltage range of 0.5 V_{P-P} to 0.68 V_A.

Input voltages below 0.0665 times the reference voltage will cause the output word to consist of all zeroes, while input voltages above ¾ of the reference voltage will cause the output word to consist of all ones. For example, with a V_{REF} of 2.4V, input voltages below 160 mV will result in an output word of all zeroes, while input voltages above 1.79V will result in an output word of all ones.

The output word rate is the same as the clock frequency. Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC08351 will convert as long as the clock signal is present at the CLK pin, but the data will not appear at the outputs unless the $\overline{OE}$ pin is low. The digital outputs are in the high impedance state when the $\overline{OE}$ pin or when the PD pin is high.

Copyright © 2000–2013, Texas Instruments Incorporated

APPLICATIONS INFORMATION

(All schematic pin numbers refer to the TSSOP.)

THE ADC REFERENCE AND THE ANALOG INPUT

The capacitance seen at the input changes with the clock level, appearing as 4 pF when the clock is low, and 11 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than is a fixed capacitance, choose an amplifier that can drive this type of load. The CLC409, CLC440, LM6152, LM6154, LM6181 and LM6182 are good devices for driving analog input of the ADC08351. Do not drive the input beyond the supply rails.

The maximum peak-to-peak input level without clipping of the reconstructed output is determined by the values of the resistor string between V_{REF} and AGND. The bottom of the reference ladder has a voltage of 0.0665 times V_{REF}, while the top of the reference ladder has a voltage of 0.7468 times V_{REF}. The maximum peak-to-peak input level works out to be about 68% of the value of V_{REF}. The relationship between the input peak-to-peak voltage and V_{REF} is

$$V_{REF} = \frac{391 \times V_{IN\ (P-P)}}{266} \quad (1)$$

We do not recommend opertaing with input levels below 1 V_{P-P} because the signal-to-noise ratio will degrade considerably due to the quantization noise. However, the ADC08351 will give adequate results in many applications with signal levels down to about 0.5 V_{P-P} (V_{REF} = 0.735V). Very good performance can be obtained with reference voltages up to the supply voltage (V_A = V_{REF} = 3V, 2.04 V_{P-P}).

As with all sampling ADCs, the opening and closing of the switches associated with the sampling causes an output of energy from the analog input, V_{IN}. The reference ladder also has switches associated with it, so the reference source must be able to supply sufficient current to hold V_{REF} steady.

The analog input of the ADC08351 is self-biased with an 18 kΩ pull-up resistor to V_{REF} and a 12 kΩ pull-down resistor to AGND. This allows for either a.c. or d.c. coupling of the input signal. These two resistors provide a convenient way to ensure a signal that is less than full scale will be centered within the input common mode range of the converter. However, the high values of these resistors and the energy coming from this input means that performance will be improved with d.c. coupling.

The driving circuit at the signal input must be able to sink and source sufficient current at the signal frequency to prevent distortion from being introduced at the input.

POWER SUPPLY CONSIDERATIONS

A tantalum or aluminum electrolytic capacitor of 5 µF to 10 µF should be placed within a centimeter of each of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed within ½ centimeter of each of the power pins. Leadless chip capacitors are preferred because they provide lower lead inductance than do their leaded counterparts.

While a single voltage source should be used for the analog and digital supplies of the ADC08351, these supply pins should be decoupled from each other to prevent any digital noise from being coupled to the analog power pins. A ferrite bead between the analog and digital supply pins would help to isolate the two supplies.

The converter digital supply should **not** be the supply that is used for other digital circuitry on the board. It should be the same supply used for the A/D analog supply, decoupled from the A/D analog supply pin, as described above. A common analog supply should be used for both V_A and V_D, and each of these pins should be separately bypassed with a 0.1 µF ceramic capacitor and with low ESR a 10 µF capacitor.

As is the case with all high speed converters, the ADC08351 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be minimized, keeping it below 200 mV_{P-P} at 100 kHz. Of course, higher frequency noise on the power supply should be even more severely limited.

No pin should ever have a voltage on it that is in excess of the supply voltages. This can be a problem upon application of power to a circuit. Be sure that the supplies to circuits driving the CLK, $\overline{OE}$, analog input and reference pins do not come up any faster than does the voltage at the ADC08351 power pins.

Copyright © 2000–2013, Texas Instruments Incorporated

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC08351 are required to meet data sheet limits. The analog and digital grounds may be in the same layer, but should be separated from each other and should **never** overlap each other.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry and from the digital ground plane.

The back of the WQFN package has a large metal area inside the area bounded by the pins. This metal area is connected to the die substrate (ground). This pad may be left floating if desired. If it is connected to anything, it should be to ground near the connection between analog and digital ground planes. Soldering this metal pad to ground will help keep the die cooler and could yield improved performance because of the lower impedance between die and board grounds. However, a poor layout could compromise performance.

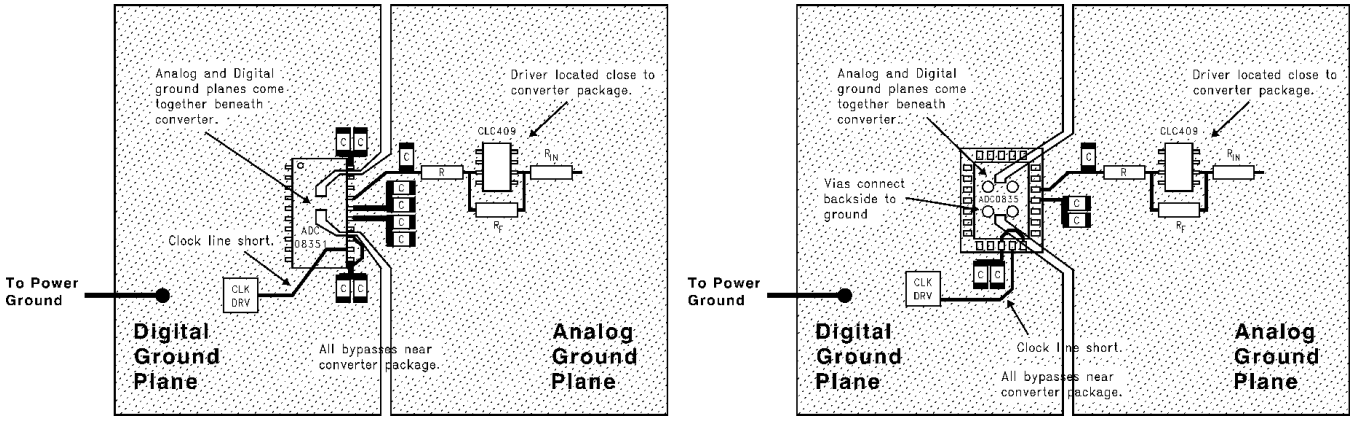


Figure 21. Layout examples showing separate analog and digital ground planes connected below the ADC08351.

Generally, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. To maximize accuracy in video (high frequency) systems, however, avoid crossing analog and digital lines altogether. Furthermore, it is important to keep any clock lines isolated from ALL other lines, including other digital lines. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane.

Figure 21 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be placed over the digital ground plane.

All ground connections should have a low inductance path to ground.

DYNAMIC PERFORMANCE

The ADC08351 is ac tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best ac performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 22.

Copyright © 2000–2013, Texas Instruments Incorporated

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

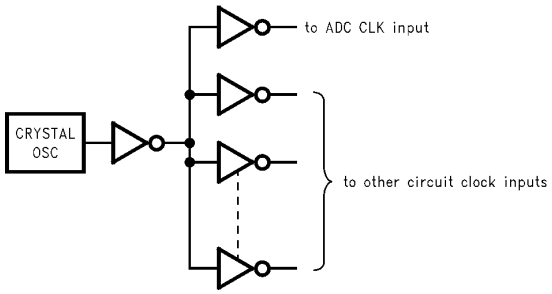


Figure 22. Isolating the ADC Clock from Digital Circuitry

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families. In general, slower logic families, such as 74LS and 74HC(T) will produce less high frequency noise than do high speed logic families, such as the 74F and 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by connecting the analog and digital ground planes together beneath the ADC with a copper trace that is narrow compared with the rest of the ground plane. This narrowing beneath the converter provides a fairly high impedance to the high frequency components of the digital switching currents, directing them away from the analog pins. The relatively lower frequency analog ground currents do not create a significant variation across the impedance of this relatively narrow ground connection.

TYPICAL APPLICATION CIRCUITS

Figure 23 shows a simple interface for a low impedance source located close to the converter. As discussed in The ADC Reference and The Analog Input, the series capacitor is optional. Notice the isolation of the ADC clock signal from the clock signals going elsewhere in the system. The reference input of this circuit is shown connected to the 3V supply.

Video ADCs tend to have input current transients that can upset a driving source, causing distortion of the driving signal. The resistor at the ADC08351 input isolates the amplifier's output from the current transients at the input to the converter.

When the signal source is not located close to the converter, the signal should be buffered. Figure 24 shows an example of an appropriate buffer. The amplifier provides a gain of two to compensate for transmission losses.

Operational amplifiers have better linearity when they operate with gain, so the input is attenuated with the 68Ω and 30Ω resistors at the non-inverting input. The 330Ω resistor in parallel with these two resistors provides for a 75Ω cable termination. Replacing this 330Ω resistor with one of 100Ω will provide a 50Ω termination.

The circuit shown has a nominal gain of two. You can provide a gain adjustment by changing the 110Ω feedback resistor to a 100Ω resistor in series with a 20Ω potentiometer.

The offset adjustment is used to bring the input signal within the common mode range of the converter. If a fixed offset is desired, the potentiometer and the 3.3k resistor may be replaced with a single resistor of 3k to 4k to the appropriate supply. The resistor value and the supply polarity used will depend upon the amount and polarity of offset needed.

The CLC409 shown in Figure 24 was chosen for a low cost solution with good overall performance.

Copyright © 2000–2013, Texas Instruments Incorporated

Figure 25 shows an inverting DC coupled circuit. The above comments regarding Figure 24 generally apply to this circuit as well.

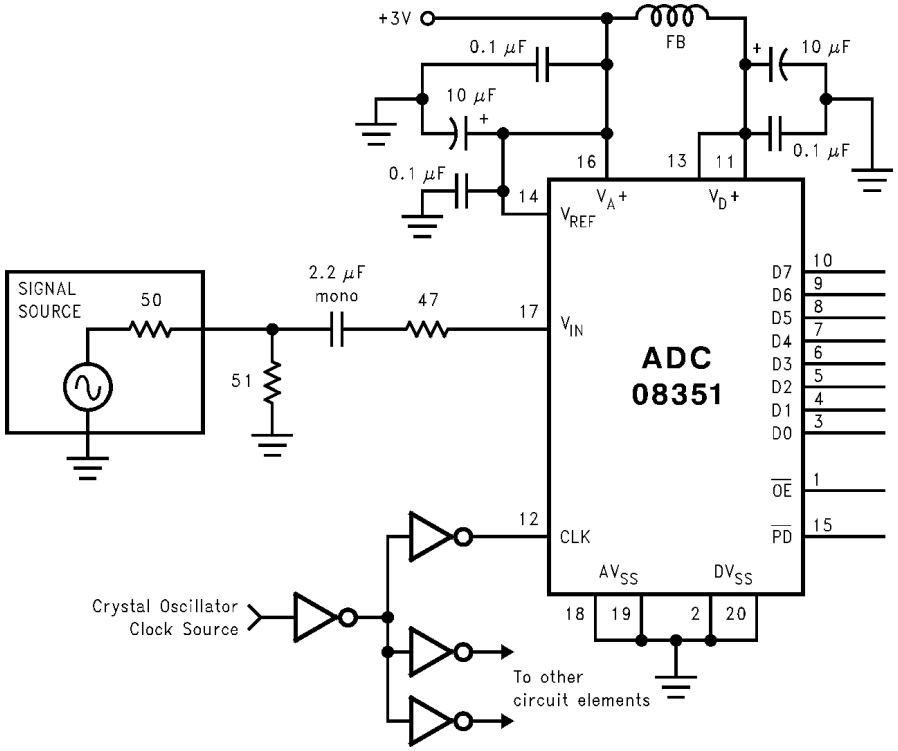


Figure 23. AC Coupled Circuit for a Low Impedance Source Located Near the Converter

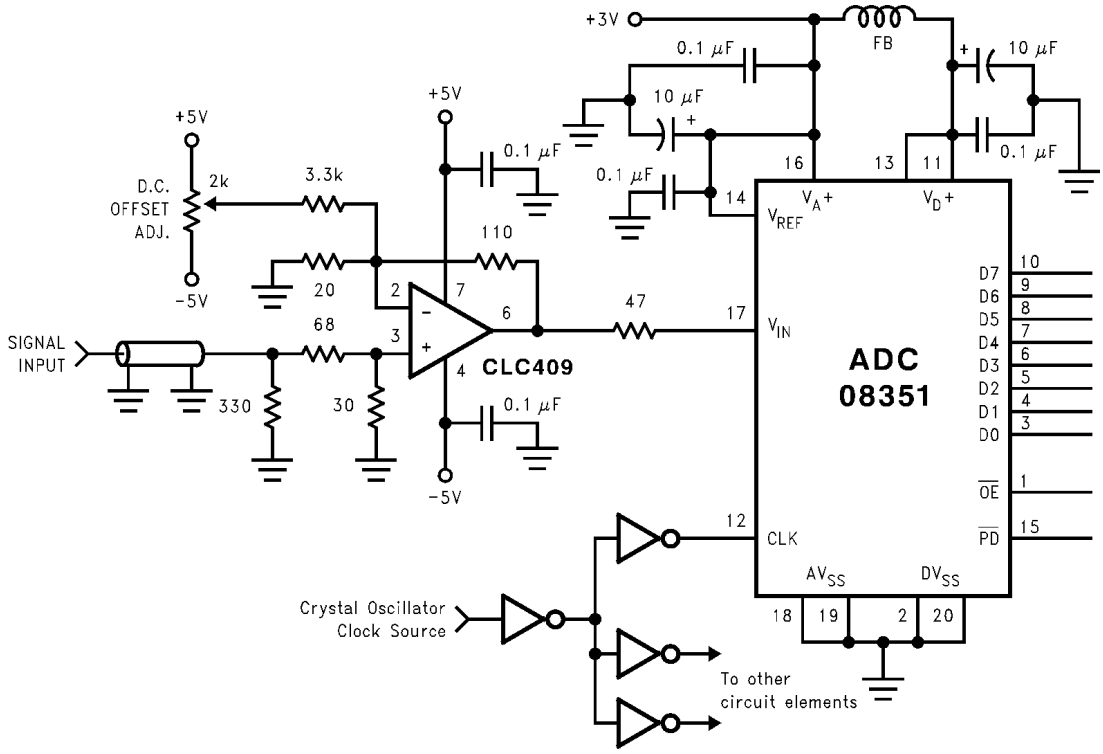


Figure 24. Non-inverting Input Circuit for Remote Signal Source

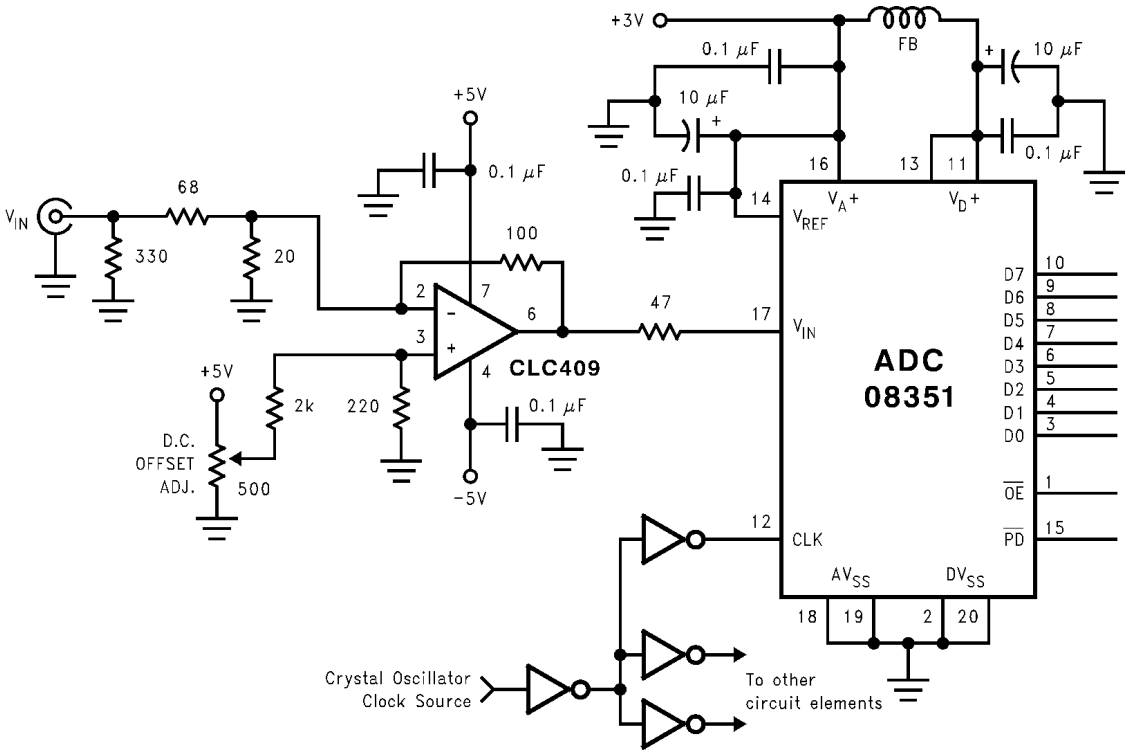
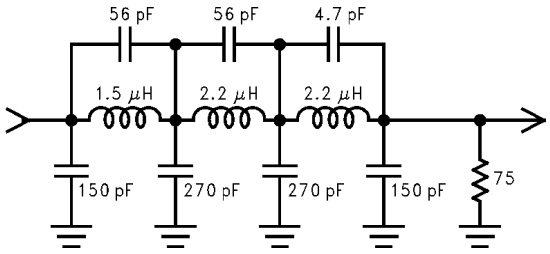


Figure 25. Inverting Circuit with Bias Adjust

ACCURATELY EVALUATING THE ADC

If a signal that is spectrally impure is presented to the ADC, the output from the ADC cannot be pure. Nearly all signal generators in use today produce signals that are not spectrally pure enough to adequately evaluate present-day ADCs. This is especially true at higher frequencies and at high resolutions.

To ensure that the signal you are presenting to the ADC being evaluated is spectrally pure, use a bandpass filter between the signal generator and the ADC input. One such possible filter is the elliptic filter shown in Figure 26.



This elliptic filter has a cutoff frequency of about 11MHz and is suitable for input frequencies of 5MHz to 10MHz. It should be driven by a generator of 75Ω source impedance and teminated with 75Ω. This termination may be provided by the ADC evaluation circuit.

Figure 26. Elliptic Filter

In addition to being used to eliminate undesired frequencies from a desired signal, this filter can be used to filter a square wave, reducing 3rd and higher harmonics to negligible levels.

When evaluating dynamic performance of an ADC, repeatability of measurements could be a problem unless coherent sampling is used.

and ADC08351 evaluation system is available that can simplify evaluation of this product.

Copyright © 2000–2013, Texas Instruments Incorporated

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV beyond the supply rails. That is, more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground or above the power supply. Since these conditions are of very short duration with very fast rise and fall times, they can inject noise into the system and may be difficult to detect with an oscilloscope. A resistor of about 50Ω to 100Ω in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08351 (or any device) with a device that is powered from supplies outside the range of the ADC08351 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers have to charge for each conversion, the more instantaneous digital current is required from V_D and DGND. These large charging current spikes can couple into the analog section, degrading dynamic performance. While adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem on the board, this coupling can still occur on the ADC08351 die. Buffering the digital data outputs (with a 74ACQ541, for example) may be necessary if the data bus to be driven is heavily loaded.

Dynamic performance can also be improved by adding series resistors at each digital output, reducing the energy coupled back into the converter output pins by limiting the output slew rate. A reasonable value for these resistors is about 47Ω.

Using an inadequate amplifier to drive the analog input. As explained in Power Supply Considerations, the capacitance seen at the input alternates between 4 pF and 11 pF with the clock. This dynamic capacitance is more difficult to drive than a fixed capacitance, so care should be taken in choosing a driving device. The CLC409, CLC440, LM6152, LM6154, LM6181 and LM6182 are good devices for driving the ADC08351. Also, an amplifier with insufficient gain-bandwidth may limit the overall frequency response of the overall circuit.

Using an operational amplifier in an insufficient gain configuration to drive the analog input. Operational amplifiers, while some may be unity gain stable, generally exhibit more distortion at low in-circuit gains than at higher gains.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. Simple gates with RC timing is generally inadequate.

Not considering the timing relationships, especially t_{OD}. Timing is always important and gets more critical with higher speeds. If the output data is latched or looked at when that data is in transition, you may see excessive noise and distortion of the output signal.

Copyright © 2000–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	17

Copyright © 2000–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08351CILQX/NOPB	ACTIVE	WQFN	NHW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-20 to 85	08351	Samples
ADC08351CIMTCX	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-20 to 85	ADC08351 CIMTC	Samples
ADC08351CIMTCX/NOPB	ACTIVE	TSSOP	PW	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	ADC08351 CIMTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

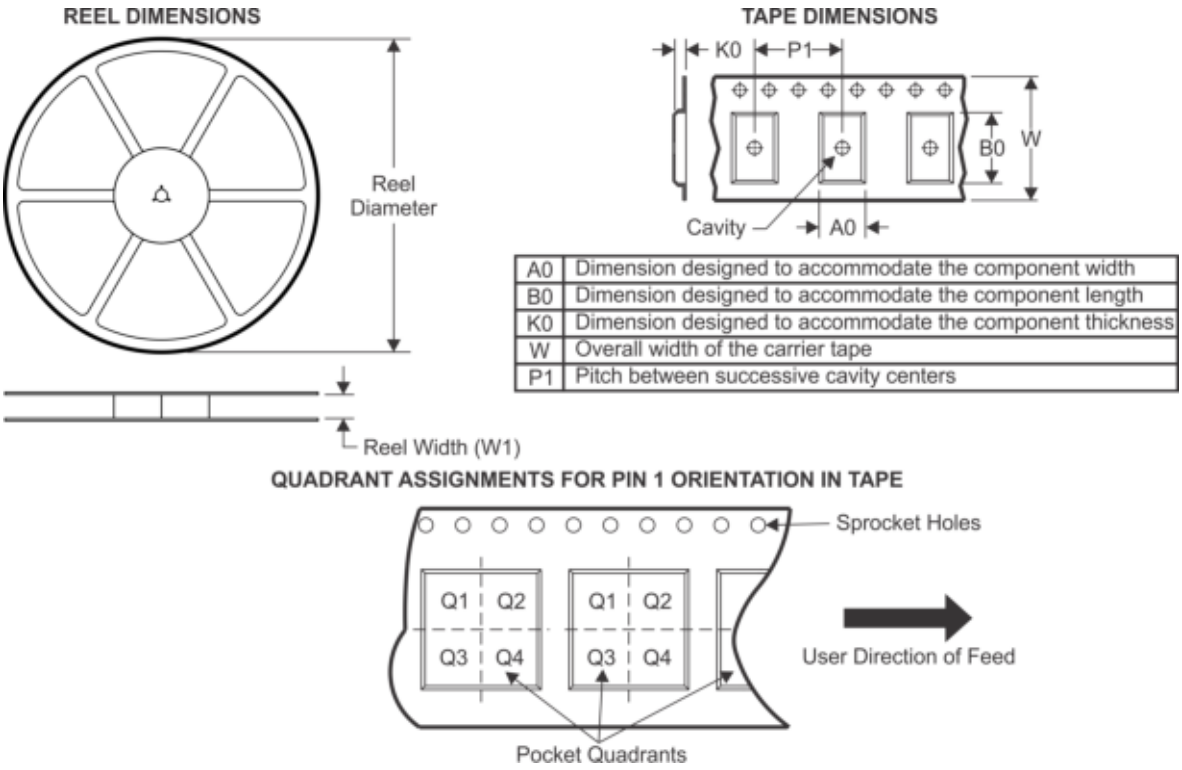
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

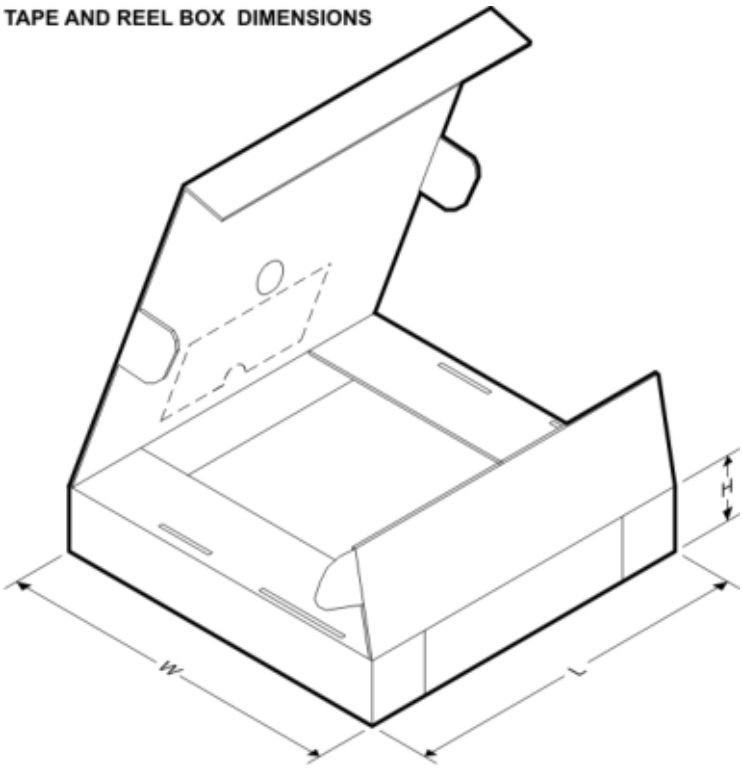


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC08351CILQX/NOPB	WQFN	NHW	24	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADC08351CIMTCX/NOPB	TSSOP	PW	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

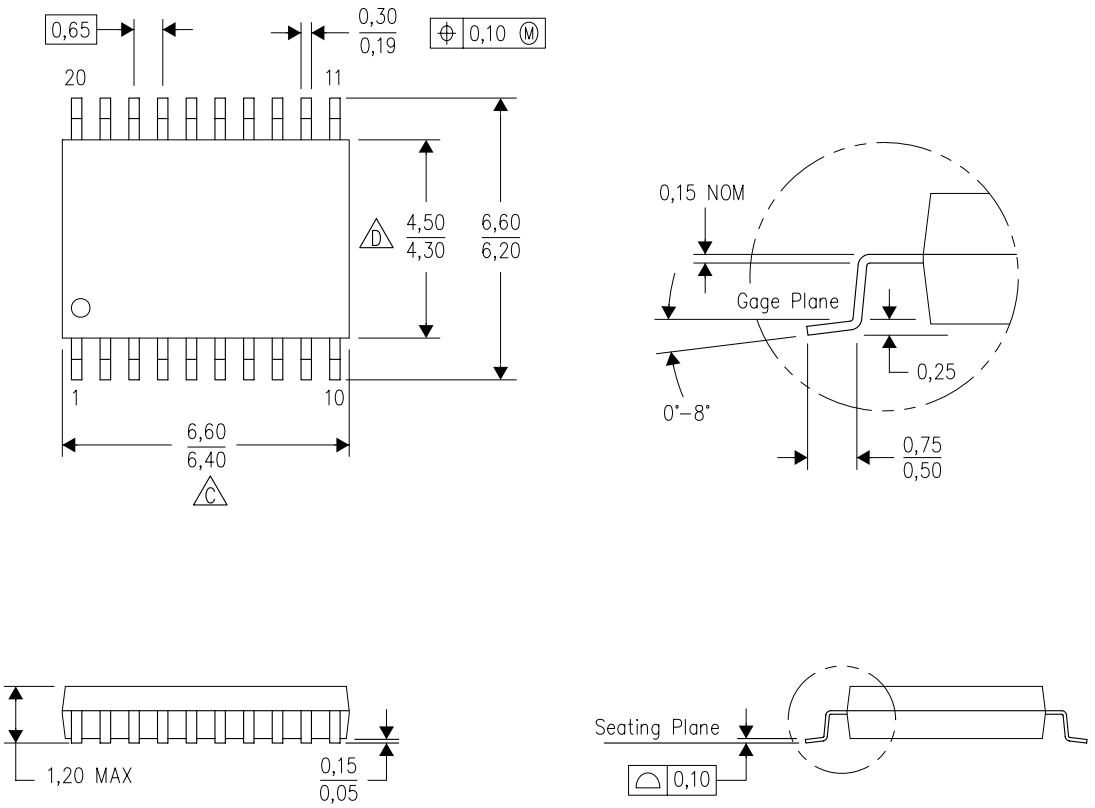
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC08351CILQX/NOPB	WQFN	NHW	24	4500	367.0	367.0	35.0
ADC08351CIMTCX/NOPB	TSSOP	PW	20	2500	367.0	367.0	35.0

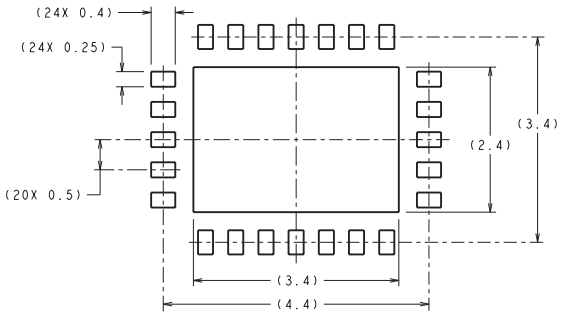
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



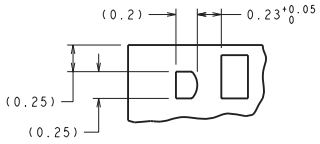
4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

NHW0024B

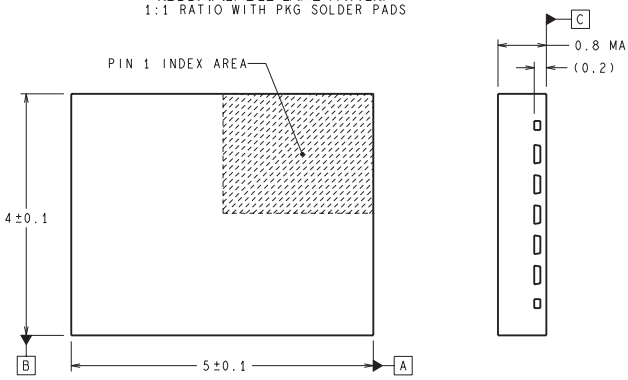


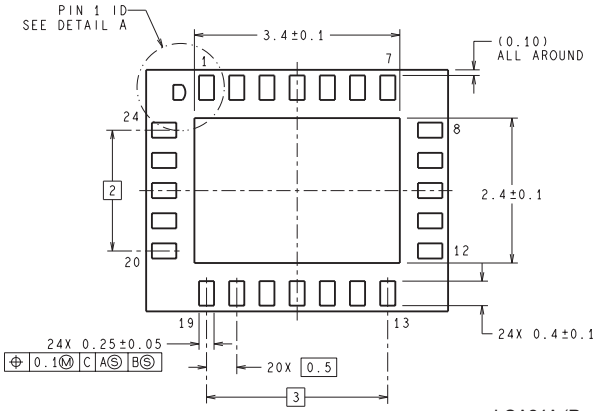
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



DETAIL A

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





LQA24A (Rev B)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated