# ADC084S051 4 Channel, 200 ksps to 500 ksps, 8-Bit A/D Converter

**Check for Samples: ADC084S051**

## FEATURES

- **Specified Over a Range of Sample Rates.**
- **Four Input Channels**
- **Variable Power Management**
- **Single Power Supply with 2.7V - 5.25V Range**

## KEY SPECIFICATIONS

- **DNL: ±0.09 LSB (typ)**
- **INL: + 0.12/−-0.062 LSB (typ)**
- **SNR: 49.6 dB (typ)**
- **Power Consumption:**
  - **3V Supply: 2.2 mW (typ)**
  - **5V Supply: 7.1 mW (typ)**

## APPLICATIONS

- **Portable Systems**
- **Remote Data Acquisition**
- **Instrumentation and Control Systems**

## DESCRIPTION

The ADC084S051 is a low-power, four-channel CMOS 8-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC084S051 is fully specified over a sample rate range of 500 ksps to 1 Msps. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to four input signals at inputs IN1 through IN4.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC084S051 operates with a single supply, that can range from +2.7V to +5.25V. Normal power consumption using a +3V or +5V supply is 2.2 mW and 7.1 mW, respectively. The power-down feature reduces the power consumption to just 0.12 µW using a +3V supply, or 0.35 µW using a +5V supply.

The ADC084S051 is packaged in a 10-lead VSSOP package. Operation over the industrial temperature range of −40°C to +85°C is ensured.

**Table 1. Pin-Compatible Alternatives by Resolution and Speed(1)**

| Resolution | Specified for Sample Rate Range of: | | |
|---|---|---|---|
| | 50 to 200 ksps | 200 to 500 ksps | 500 ksps to 1Msps |
| 12-bit | ADC124S021 | ADC124S051 | ADC124S101 |
| 10-bit | ADC104S021 | ADC104S051 | ADC104S101 |
| 8-bit | ADC084S021 | **ADC084S051** | ADC084S101 |

(1) All devices are fully pin compatible.

## Connection Diagram

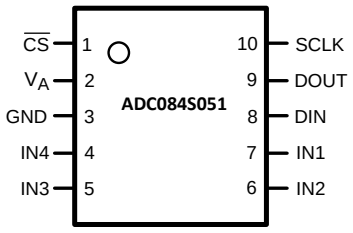



**Figure 1. VSSOP Package**
**See Package Number DGS0010A**

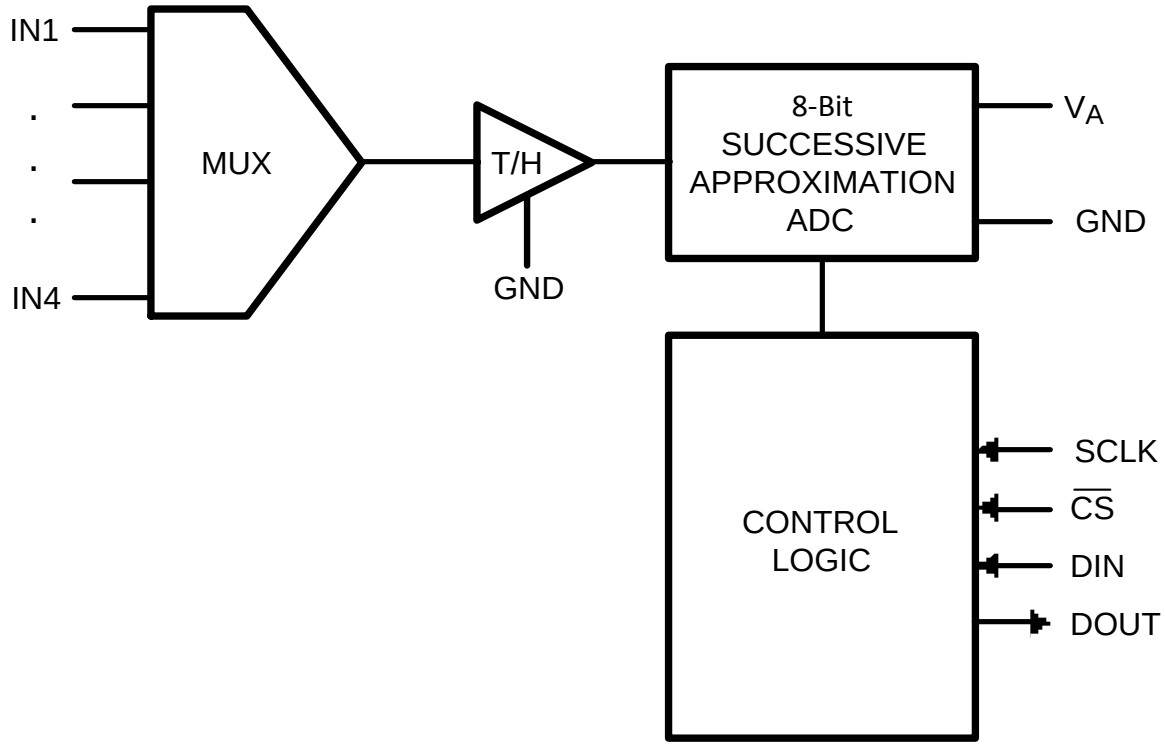
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## Block Diagram




### Pin Descriptions and Equivalent Circuits

| Pin No. | Pin Name | Description |
|---|---|---|
| **ANALOG I/O** | | |
| 4-7 | IN1 to IN4 | Analog inputs. These signals can range from 0V to $V_A$. |
| **DIGITAL I/O** | | |
| 10 | SCLK | Digital clock input. This clock directly controls the conversion and readout processes. |
| 9 | DOUT | Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin. |
| 8 | DIN | Digital data input. The ADC084S051's Control Register is loaded through this pin on rising edges of the SCLK pin. |
| 1 | $\overline{CS}$ | Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low. |
| **POWER SUPPLY** | | |
| 2 | $V_A$ | Positive supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 µF capacitor and a 0.1 µF monolithic capacitor located within 1 cm of the power pin. |
| 3 | GND | The ground return for supply and signals. |


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)(3)

| | | |
|---|---|---|
| Supply Voltage $V_A$ | | −0.3V to 6.5V |
| Voltage on Any Pin to GND | | −0.3V to $V_A$ +0.3V |
| Input Current at Any Pin(4) | | ±10 mA |
| Package Input Current(4) | | ±20 mA |
| Power Consumption at $T_A$ = 25°C | | See (5) |
| ESD Susceptibility(6) | Human Body Model | 2500V |
| | Machine Model | 250V |
| Junction Temperature | | +150°C |
| Storage Temperature | | −65°C to +150°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(4) When the input voltage at any pin exceeds the power supply (that is, $V_{IN}$ < GND or $V_{IN}$ > $V_A$), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Rating specification does not apply to the $V_A$ pin. The current into the $V_A$ pin is limited by the Analog Supply Voltage specification.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($\theta_{JA}$), and the ambient temperature ($T_A$), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through zero ohms.

## Operating Ratings(1)(2)

| | |
|---|---|
| Operating Temperature Range | −40°C ≤ $T_A$ ≤ +85°C |
| $V_A$ Supply Voltage | +2.7V to +5.25V |
| Digital Input Pins Voltage Range | −0.3V to $V_A$ |
| Clock Frequency | 50 kHz to 16 MHz |
| Analog Input Voltage | 0V to $V_A$ |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

## Package Thermal Resistance(1)

| Package | $\theta_{JA}$ |
|---|---|
| 10-lead VSSOP | 190°C / W |

(1) Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. Reflow temperature profiles are different for lead-free and non-lead-free packages.

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## ADC084S051 Converter Electrical Characteristics(1)

The following specifications apply for $V_A$ = +2.7V to 5.25V, GND = 0V, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $C_L$ = 50 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$**: all other limits $T_A$ = 25°C.

| Parameter | | Test Conditions | Typical | Limits (2) | Units |
|---|---|---|---|---|---|
| **STATIC CONVERTER CHARACTERISTICS** | | | | | |
| | Resolution with No Missing Codes | | | **8** | Bits |
| INL | Integral Non-Linearity | | +0.12 | **+0.4** | LSB (max) |
| | | | −0.062 | **−0.3** | LSB (min) |
| DNL | Differential Non-Linearity | | ±0.09 | **±0.3** | LSB (max) |
| $V_{OFF}$ | Offset Error | | +0.53 | **±0.7** | LSB (max) |
| OEM | Channel to Channel Offset Error Match | | +0.005 | **±0.3** | LSB (max) |
| FSE | Full-Scale Error | | +0.52 | **±0.7** | LSB (max) |
| FSEM | Channel to Channel Full-Scale Error Match | | +0.006 | **±0.3** | LSB (max) |
| **DYNAMIC CONVERTER CHARACTERISTICS** | | | | | |
| SINAD | Signal-to-Noise Plus Distortion Ratio | $V_A$ = +2.7V to 5.25V<br>$f_{IN}$ = 40.2 kHz, −0.02 dBFS | 49.5 | **49.1** | dB (min) |
| SNR | Signal-to-Noise Ratio | $V_A$ = +2.7V to 5.25V<br>$f_{IN}$ = 40.2 kHz, −0.02 dBFS | 49.5 | **49.2** | dB (min) |
| THD | Total Harmonic Distortion | $V_A$ = +2.7V to 5.25V<br>$f_{IN}$ = 40.2 kHz, −0.02 dBFS | −76 | **−62** | dB (max) |
| SFDR | Spurious-Free Dynamic Range | $V_A$ = +2.7V to 5.25V<br>$f_{IN}$ = 40.2 kHz, −0.02 dBFS | 68 | **63** | dB (min) |
| ENOB | Effective Number of Bits | $V_A$ = +2.7V to 5.25V | 7.93 | **7.9** | Bits (min) |
| | Channel-to-Channel Crosstalk | $V_A$ = +2.7V to 5.25V<br>$f_{IN}$ = 40.2 kHz | −73 | | dB |
| IMD | Intermodulation Distortion, Second Order Terms | $V_A$ = 5.25V<br>$f_a$ = 40.161 kHz, $f_b$ = 41.015 kHz | −78 | | dB |
| | Intermodulation Distortion, Third Order Terms | $V_A$ = 5.25V<br>$f_a$ = 40.161 kHz, $f_b$ = 41.015 kHz | −73 | | dB |
| FPBW | -3 dB Full Power Bandwidth | $V_A$ = +5V | 11 | | MHz |
| | | $V_A$ = +3V | 8 | | MHz |
| **ANALOG INPUT CHARACTERISTICS** | | | | | |
| $V_{IN}$ | Input Range | | 0 to $V_A$ | | V |
| $I_{DCL}$ | DC Leakage Current | | | **±1** | µA (max) |
| $C_{INA}$ | Input Capacitance | Track Mode | 33 | | pF |
| | | Hold Mode | 3 | | pF |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | |
| $V_{IH}$ | Input High Voltage | $V_A$ = +5.25V | | **2.4** | V (min) |
| | | $V_A$ = +3.6V | | **2.1** | V (min) |
| $V_{IL}$ | Input Low Voltage | | | **0.8** | V (max) |
| $I_{IN}$ | Input Current | $V_{IN}$ = 0V or $V_A$ | | **±10** | µA (max) |
| $C_{IND}$ | Digital Input Capacitance | | 2 | **4** | pF (max) |

(1) Min/max specification limits are specified by design, test, or statistical analysis.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).


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## ADC084S051 Converter Electrical Characteristics(1) (continued)

The following specifications apply for $V_A$ = +2.7V to 5.25V, GND = 0V, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $C_L$ = 50 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$**: all other limits $T_A$ = 25°C.

| Parameter | | Test Conditions | Typical | Limits (2) | Units |
|---|---|---|---|---|---|
| **DIGITAL OUTPUT CHARACTERISTICS** | | | | | |
| $V_{OH}$ | Output High Voltage | $I_{SOURCE}$ = 200 µA | $V_A$ − 0.03 | **$V_A$ − 0.5** | V (min) |
| | | $I_{SOURCE}$ = 1 mA | $V_A$ − 0.1 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{SINK}$ = 200 µA | 0.03 | **0.4** | V (max) |
| | | $I_{SINK}$ = 1 mA | 0.1 | | V |
| $I_{OZH}$, $I_{OZL}$ | TRI-STATE Leakage Current | | 0.005 | **±1** | µA (max) |
| $C_{OUT}$ | TRI-STATE Output Capacitance | | 2 | **4** | pF (max) |
| | Output Coding | | Straight (Natural) Binary | | |
| **POWER SUPPLY CHARACTERISTICS** ($C_L$ = 10 pF) | | | | | |
| $V_A$ | Supply Voltage | | | **2.7** | V (min) |
| | | | | **5.25** | V (max) |
| $I_A$ | Supply Current, Normal Mode (Operational, $\overline{CS}$ low) | $V_A$ = +5.25V, $f_{SAMPLE}$ = 500 ksps, $f_{IN}$ = 40 kHz | 1.35 | **1.9** | mA (max) |
| | | $V_A$ = +3.6V, $f_{SAMPLE}$ = 500 ksps, $f_{IN}$ = 40 kHz | 0.62 | **0.9** | mA (max) |
| | Supply Current, Shutdown ($\overline{CS}$ high) | $V_A$ = +5.25V, $f_{SAMPLE}$ = 0 ksps | 200 | | nA |
| | | $V_A$ = +3.6V, $f_{SAMPLE}$ = 0 ksps | 200 | | nA |
| $P_D$ | Power Consumption, Normal Mode (Operational, $\overline{CS}$ low) | $V_A$ = +5.25V | 7.1 | **10** | mW (max) |
| | | $V_A$ = +3.6V | 2.23 | **3.2** | mW (max) |
| | Power Consumption, Shutdown ($\overline{CS}$ high) | $V_A$ = +5.25V | 0.35 | | µW |
| | | $V_A$ = +3.6V | 0.12 | | µW |
| **AC ELECTRICAL CHARACTERISTICS** | | | | | |
| $f_{SCLK}$ | Clock Frequency | See (3) | | **3.2** | MHz (min) |
| | | | | **8** | MHz (max) |
| $f_S$ | Sample Rate | See (3) | | **200** | ksps (min) |
| | | | | **500** | ksps (max) |
| $t_{CONV}$ | Conversion Time | | | **13** | SCLK cycles |
| DC | SCLK Duty Cycle | | 50 | **30** | % (min) |
| | | | | **70** | % (max) |
| $t_{ACQ}$ | Track/Hold Acquisition Time | Full-Scale Step Input | | **3** | SCLK cycles |
| | Throughput Time | Acquisition Time + Conversion Time | | **16** | SCLK cycles |

(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified under Operating Ratings.

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## ADC104S051 Timing Specifications

The following specifications apply for $V_A$ = +2.7V to 5.25V, GND = 0V, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{SAMPLE}$ = 200 to 500 ksps, $C_L$ = 50 pF, **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$**: all other limits $T_A$ = 25°C.

| Parameter | | Test Conditions | | Typical | Limits (1) | Units |
|---|---|---|---|---|---|---|
| $t_{CSU}$ | Setup Time SCLK High to $\overline{CS}$ Falling Edge | See (2) | $V_A$ = +3.0V | −3.5 | **10** | ns (min) |
| | | | $V_A$ = +5.0V | −0.5 | | |
| $t_{CLH}$ | Hold time SCLK Low to $\overline{CS}$ Falling Edge | See (2) | $V_A$ = +3.0V | +4.5 | **10** | ns (min) |
| | | | $V_A$ = +5.0V | +1.5 | | |
| $t_{EN}$ | Delay from $\overline{CS}$ Until DOUT active | | $V_A$ = +3.0V | +4 | **30** | ns (max) |
| | | | $V_A$ = +5.0V | +2 | | |
| $t_{ACC}$ | Data Access Time after SCLK Falling Edge | | $V_A$ = +3.0V | +16.5 | **30** | ns (max) |
| | | | $V_A$ = +5.0V | +15 | | |
| $t_{SU}$ | Data Setup Time Prior to SCLK Rising Edge | | | +3 | **10** | ns (min) |
| $t_H$ | Data Valid SCLK Hold Time | | | +3 | **10** | ns (min) |
| $t_{CH}$ | SCLK High Pulse Width | | | 0.5 x $t_{SCLK}$ | **0.3 x $t_{SCLK}$** | ns (min) |
| $t_{CL}$ | SCLK Low Pulse Width | | | 0.5 x $t_{SCLK}$ | **0.3 x $t_{SCLK}$** | ns (min) |
| $t_{DIS}$ | $\overline{CS}$ Rising Edge to DOUT High-Impedance | Output Falling | $V_A$ = +3.0V | 1.7 | **20** | ns (max) |
| | | | $V_A$ = +5.0V | 1.2 | | |
| | | Output Rising | $V_A$ = +3.0V | 1.0 | | |
| | | | $V_A$ = +5.0V | 1.0 | | |

(1) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(2) Clock may be either high or low when $\overline{CS}$ is asserted as long as setup and hold times $t_{CSU}$ and $t_{CLH}$ are strictly observed.


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## Timing Diagrams

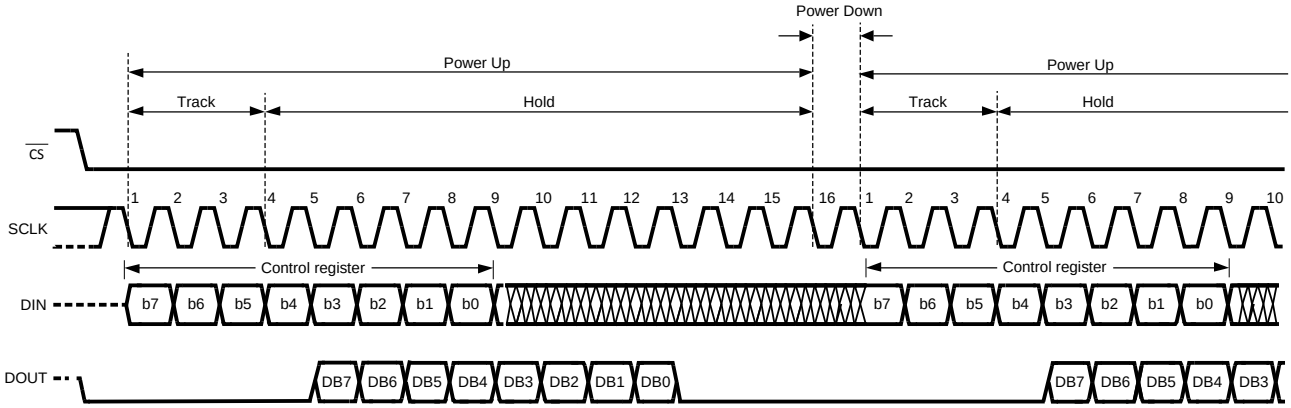



**Figure 2. ADC084S051 Operational Timing Diagram**

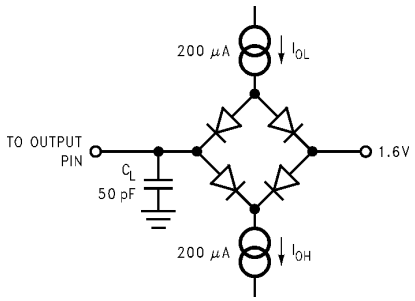



**Figure 3. Timing Test Circuit**

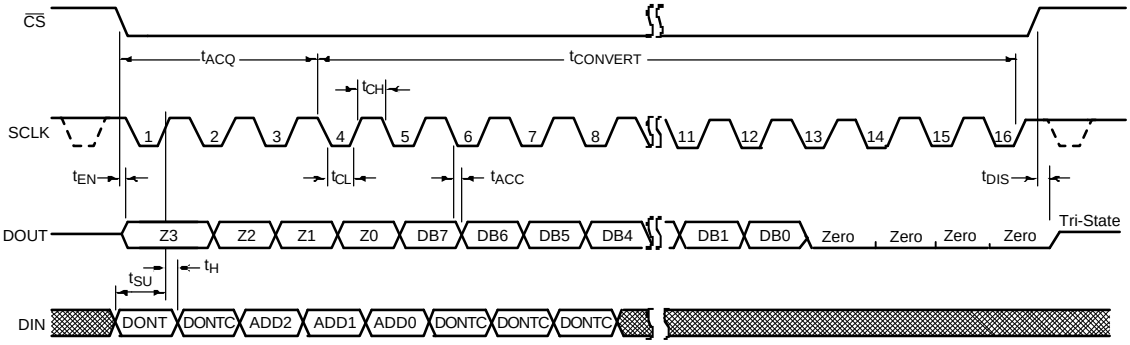



**Figure 4. ADC084S051 Serial Timing Diagram**

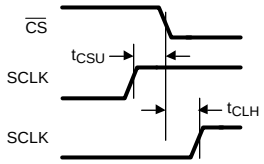



**Figure 5. SCLK and $\overline{CS}$ Timing Parameters**

## Specification Definitions

**ACQUISITION TIME** is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage.

**APERTURE DELAY** is the time between the fourth falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

**CONVERSION TIME** is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

**CROSSTALK** is the coupling of energy from one channel into the other channel, or the amount of signal energy from one analog input that appears at the measured analog input.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**DUTY CYCLE** is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**FULL SCALE ERROR (FSE)** is a measure of how far the last code transition is from the ideal 1½ LSB below $V_{REF^+}$ and is defined as:

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+} \quad (1)$$

where

- $V_{max}$ is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range.

**GAIN ERROR** is the deviation of the last code transition (111...110) to (111...111) from the ideal ($V_{REF}$ − 1.5 LSB), after adjusting for offset error.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dB.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. These codes cannot be reached with any input value. The ADC084S051 is ensured not to have any missing codes.

**OFFSET ERROR** is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.


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**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}} \quad (2)$$

where

- $Af_1$ is the RMS power of the input frequency at the output and $Af_2$ through $Af_6$ are the RMS power in the first 5 harmonic frequencies.

**THROUGHPUT TIME** is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion and read out times. In the case of the ADC084S051, this is 16 SCLK periods.

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## Typical Performance Characteristics

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**DNL - $V_A$ = 3.0V**

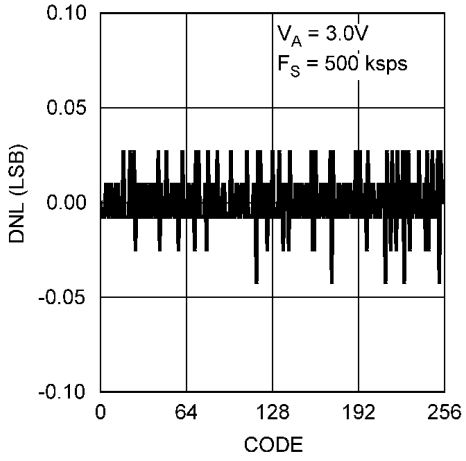



**Figure 6.**

**INL - $V_A$ = 3.0V**

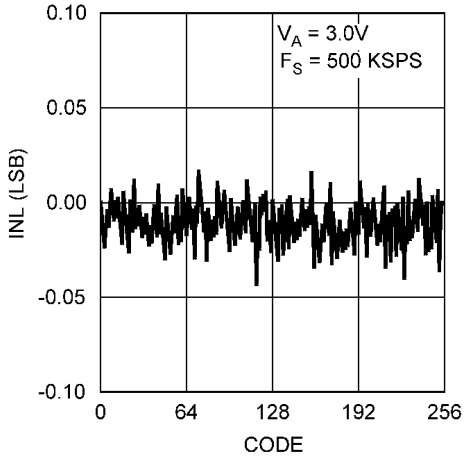



**Figure 7.**

**DNL - $V_A$ = 5.0V**

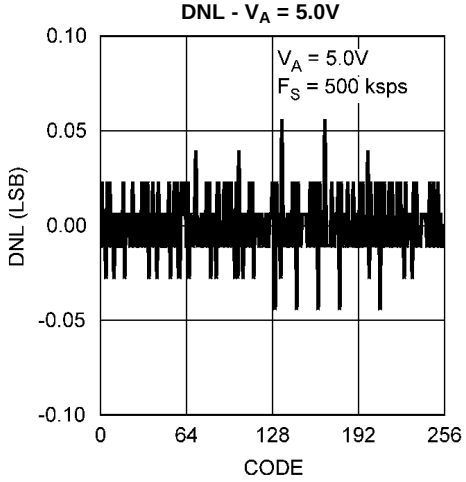



**Figure 8.**

**INL - $V_A$ = 5.0V**

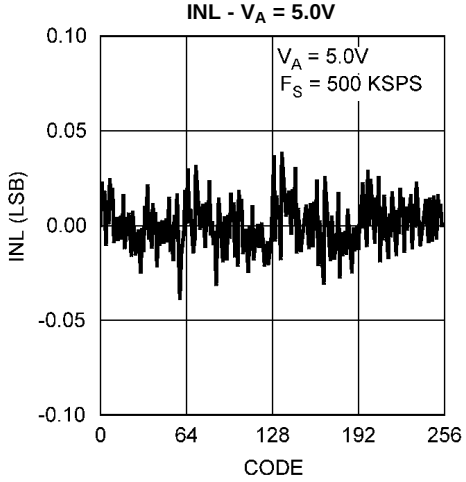



**Figure 9.**

**DNL vs. Supply**

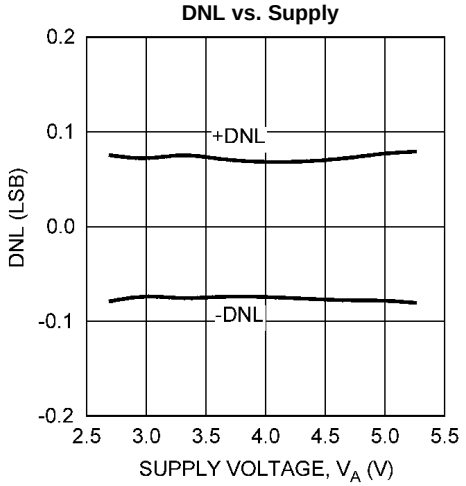



**Figure 10.**

**INL vs. Supply**

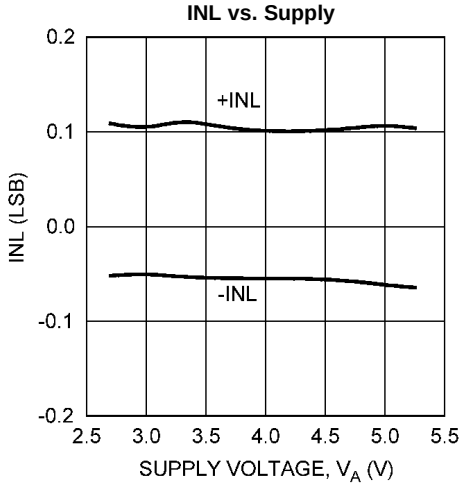



**Figure 11.**


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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**DNL vs. Clock Frequency**

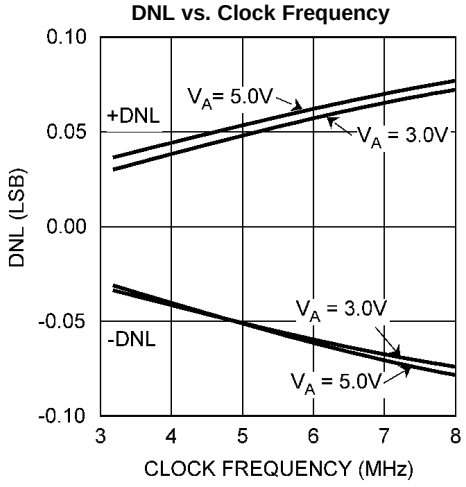



**Figure 12.**

**INL vs. Clock Frequency**

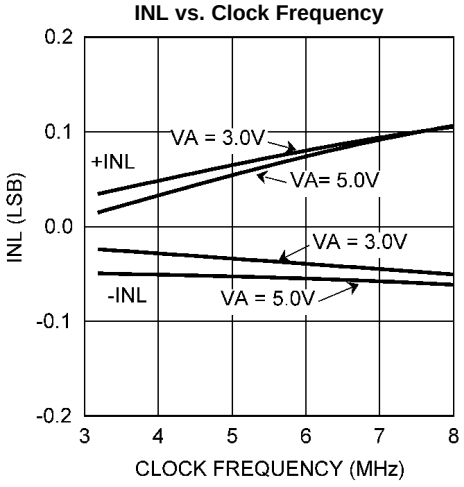



**Figure 13.**

**DNL vs. Clock Duty Cycle**

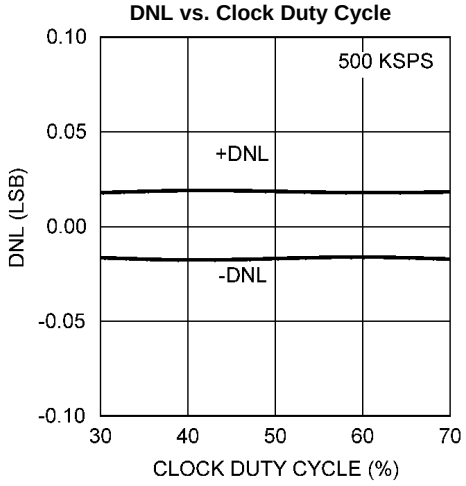



**Figure 14.**

**INL vs. Clock Duty Cycle**

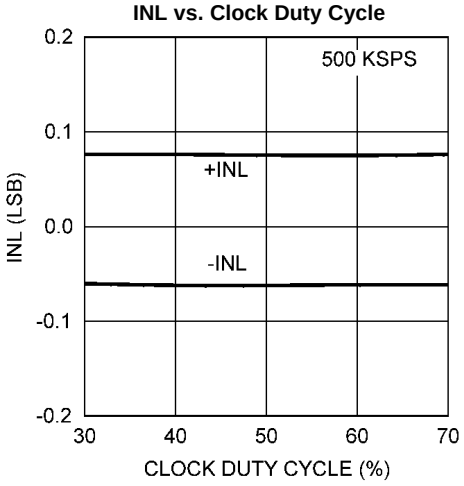



**Figure 15.**

**DNL vs. Temperature**

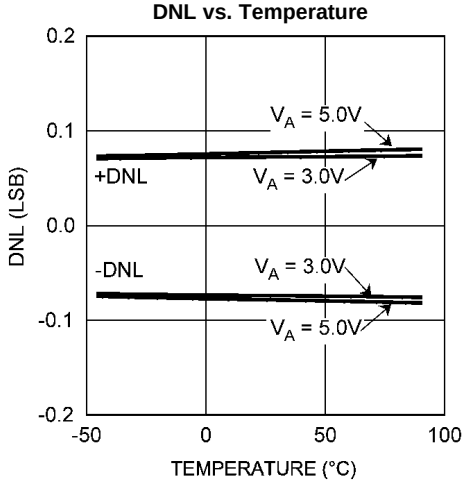



**Figure 16.**

**INL vs. Temperature**

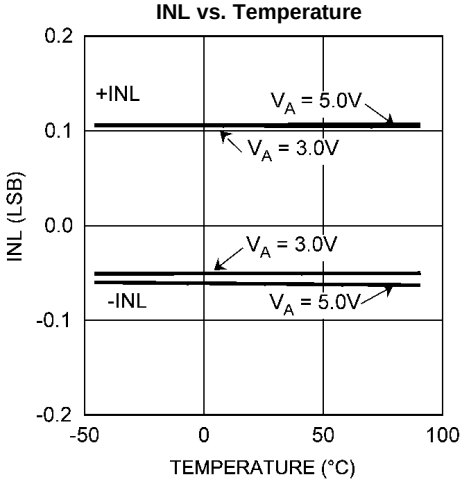



**Figure 17.**

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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**SNR vs. Supply**

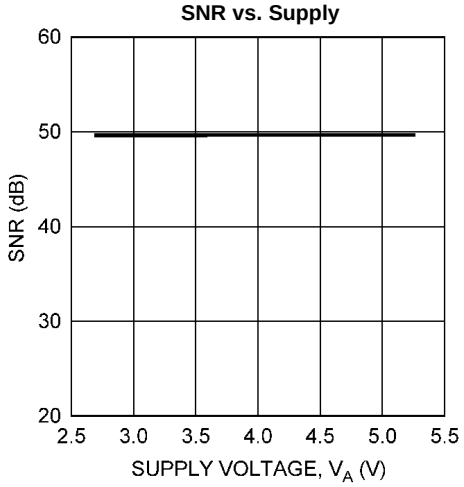



**Figure 18.**

**THD vs. Supply**

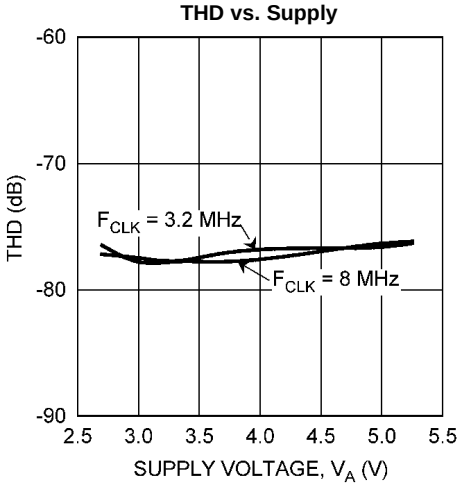



**Figure 19.**

**SNR vs. Clock Frequency**

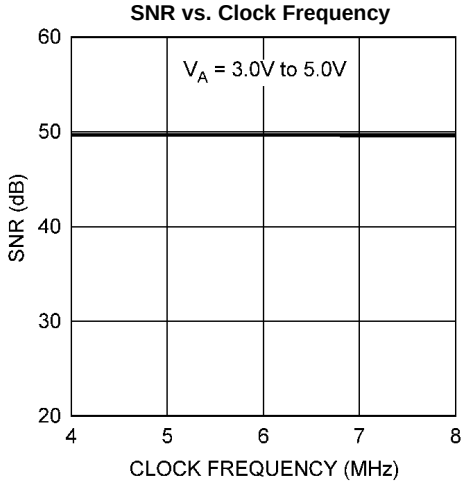



**Figure 20.**

**THD vs. Clock Frequency**

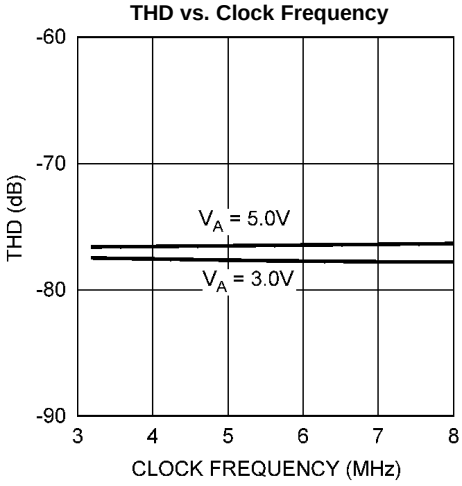



**Figure 21.**

**SNR vs. Clock Duty Cycle**

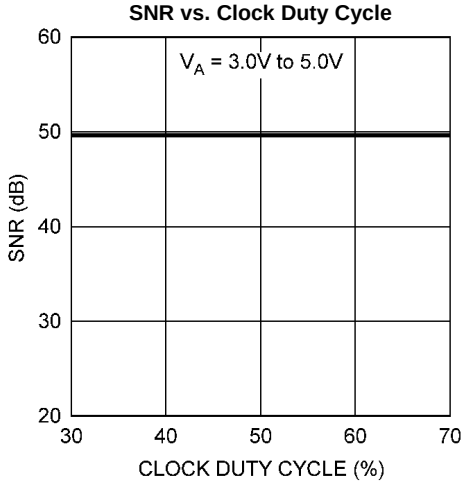



**Figure 22.**

**THD vs. Clock Duty Cycle**

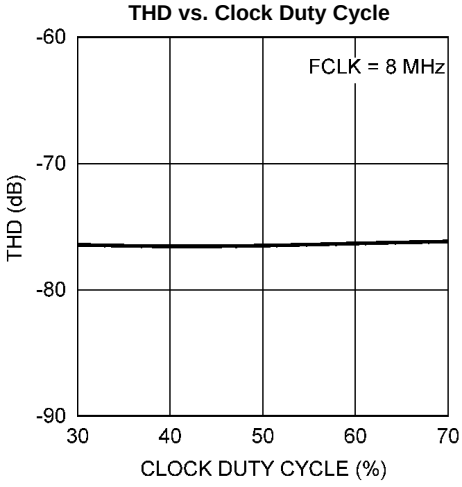



**Figure 23.**


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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**SNR vs. Input Frequency**

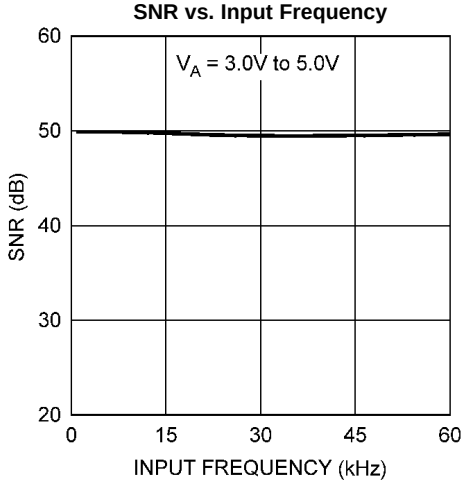



**Figure 24.**

**THD vs. Input Frequency**

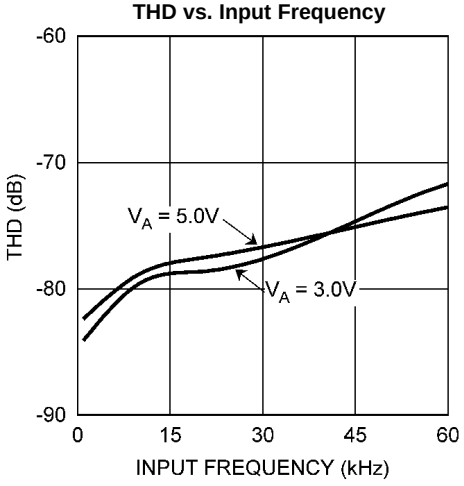



**Figure 25.**

**SNR vs. Temperature**

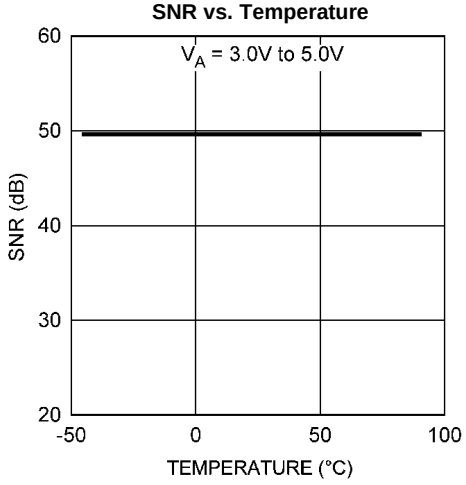



**Figure 26.**

**THD vs. Temperature**

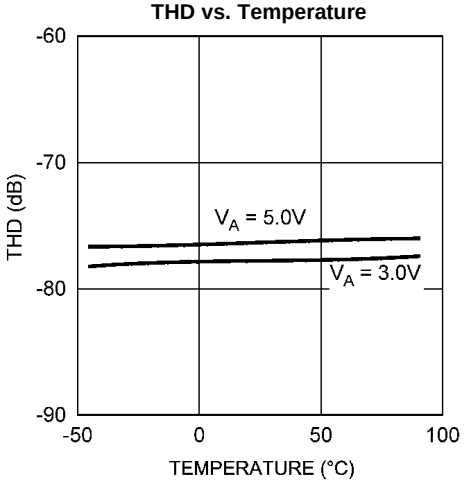



**Figure 27.**

**SFDR vs. Supply**

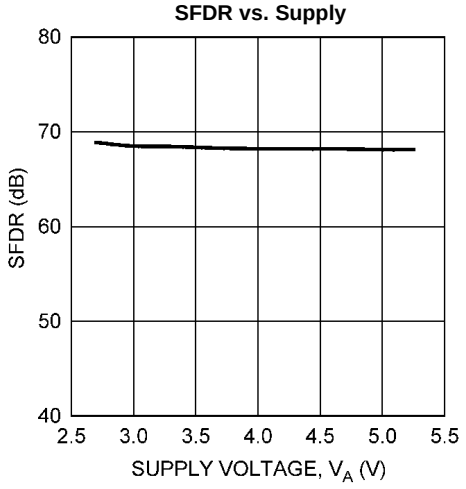



**Figure 28.**

**SINAD vs. Supply**

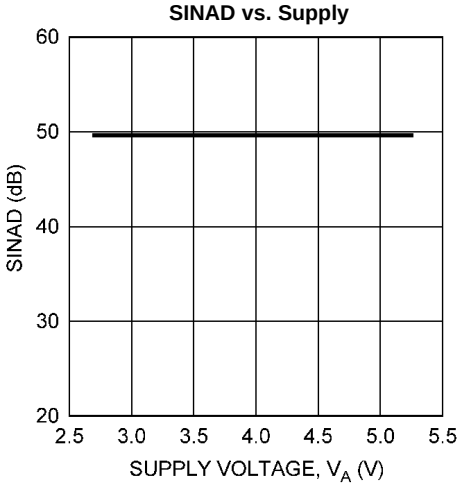



**Figure 29.**

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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**SFDR vs. Clock Frequency**

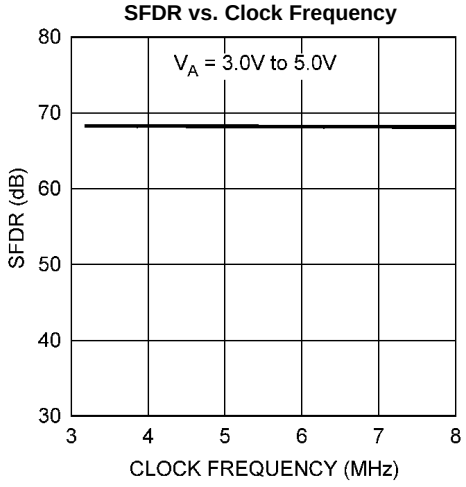



**Figure 30.**

**SINAD vs. Clock Frequency**

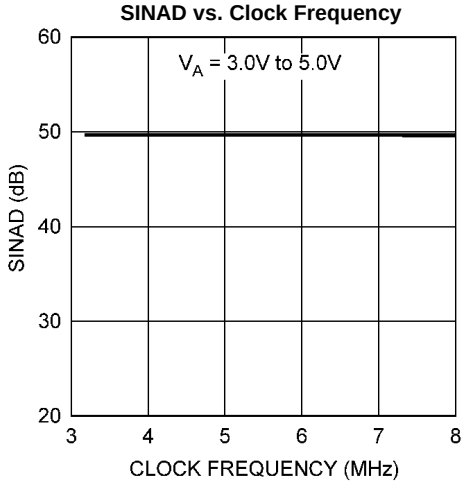



**Figure 31.**

**SFDR vs. Clock Duty Cycle**

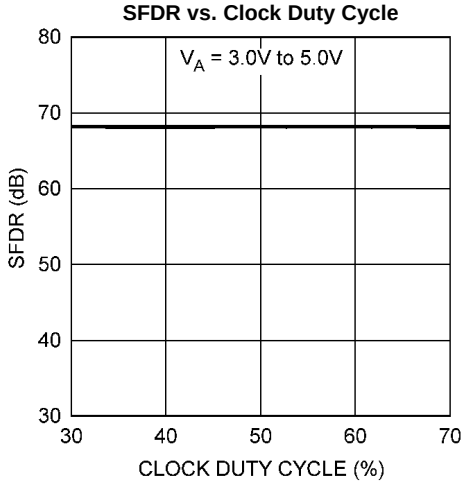



**Figure 32.**

**SINAD vs. Clock Duty Cycle**

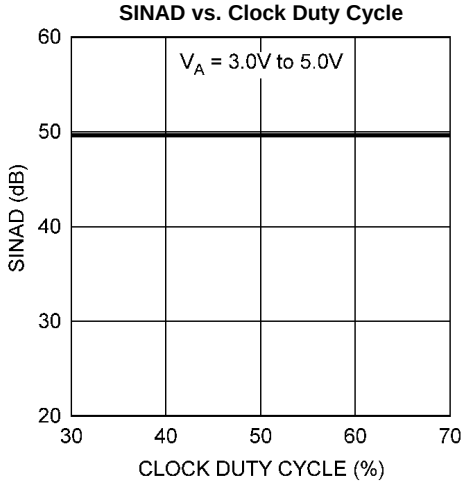



**Figure 33.**

**SFDR vs. Input Frequency**

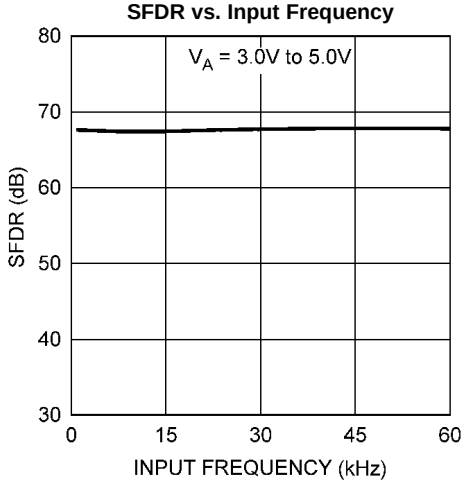



**Figure 34.**

**SINAD vs. Input Frequency**

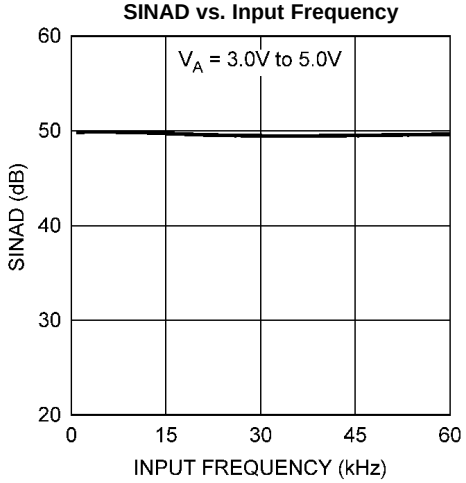



**Figure 35.**


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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**SFDR vs. Temperature**

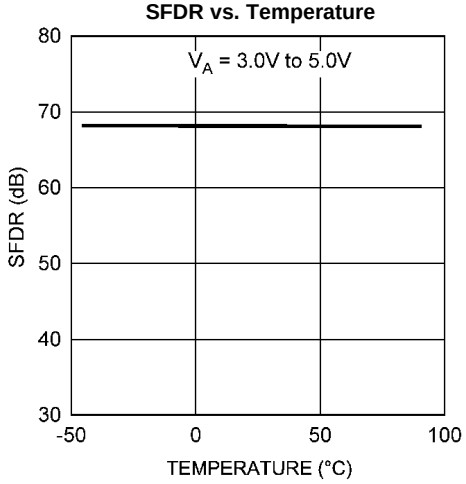



**Figure 36.**

**SINAD vs. Temperature**

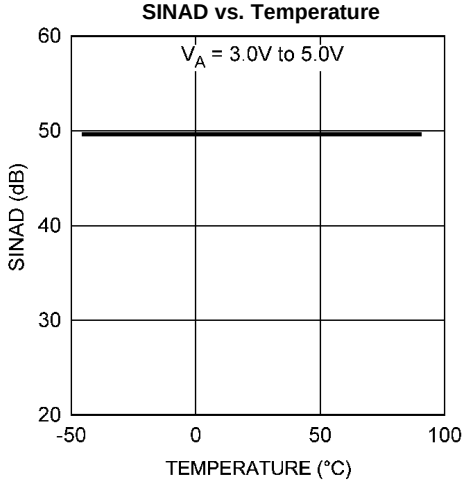



**Figure 37.**

**ENOB vs. Supply**

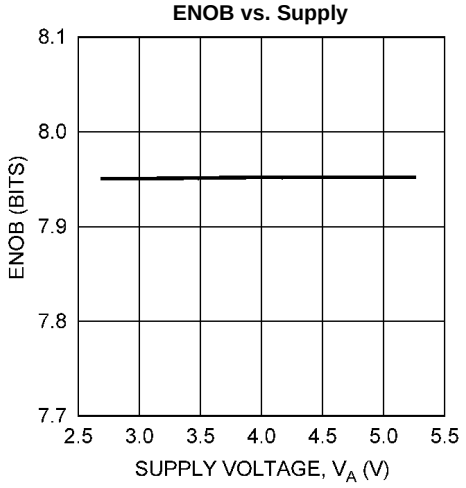



**Figure 38.**

**ENOB vs. Clock Frequency**

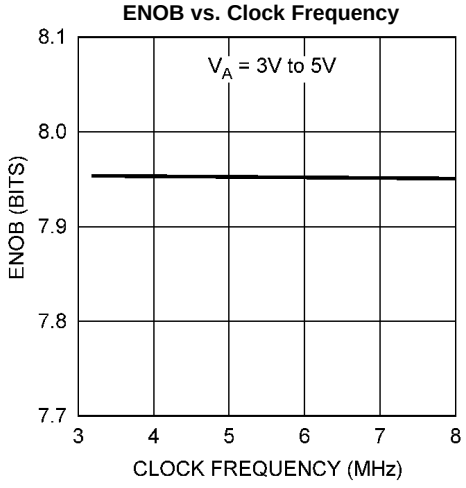



**Figure 39.**

**ENOB vs. Clock Duty Cycle**

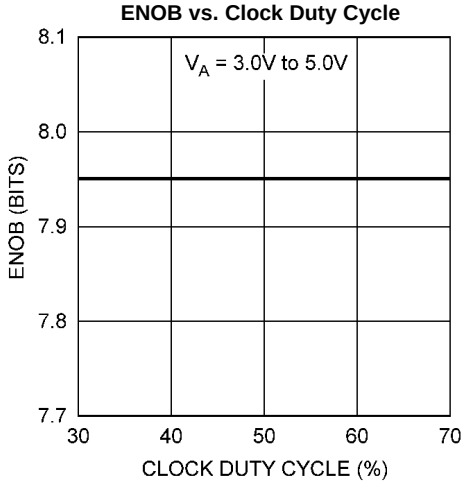



**Figure 40.**

**ENOB vs. Input Frequency**

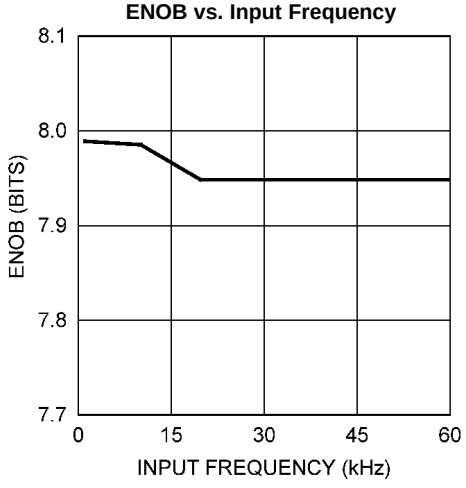



**Figure 41.**

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## Typical Performance Characteristics (continued)

$T_A$ = +25°C, $f_{SAMPLE}$ = 200 ksps to 500 ksps, $f_{SCLK}$ = 3.2 MHz to 8 MHz, $f_{IN}$ = 40.2 kHz unless otherwise stated.

**ENOB vs. Temperature**

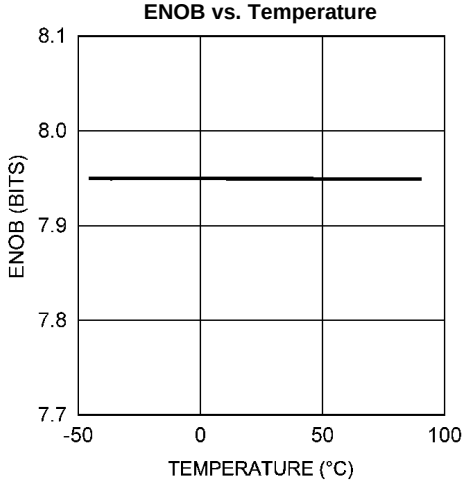



**Figure 42.**

**Spectral Response - 3V, 200 ksps**

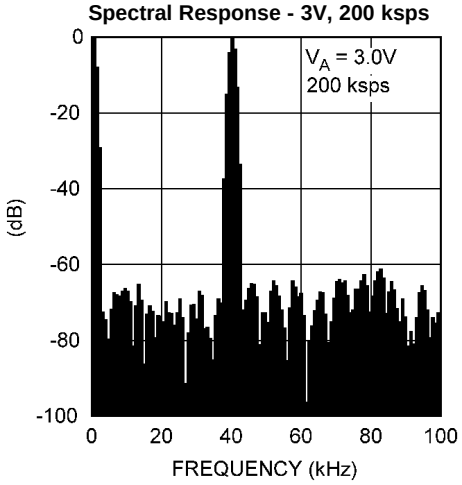



**Figure 43.**

**Spectral Response - 5V, 200 ksps**

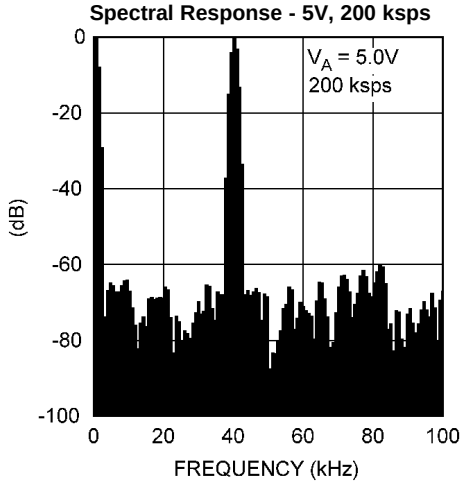



**Figure 44.**

**Spectral Response - 3V, 500 ksps**

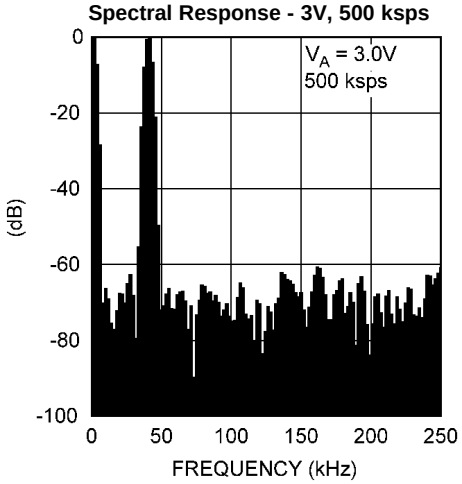



**Figure 45.**

**Spectral Response - 5V, 500 ksps**

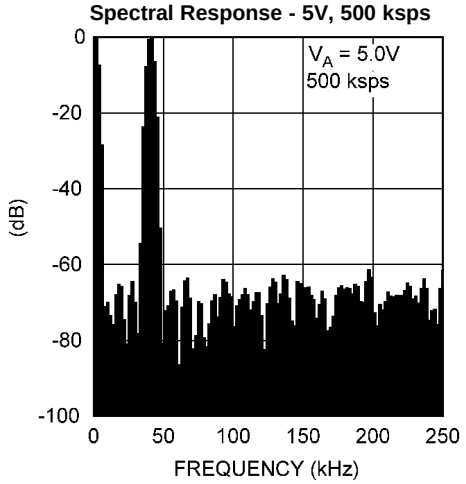



**Figure 46.**

**Power Consumption vs. Throughput**

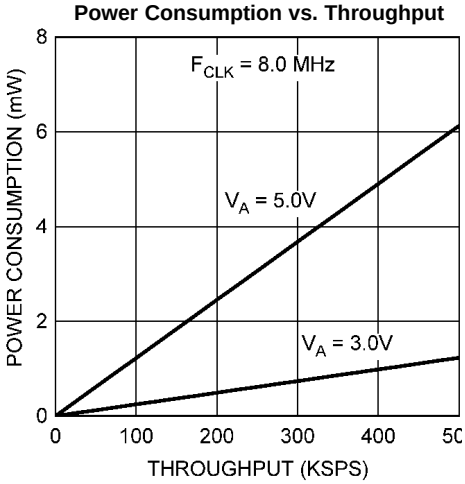



**Figure 47.**


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# APPLICATIONS INFORMATION

## ADC084S051 OPERATION

The ADC084S051 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADC084S051 in both track and hold modes are shown in Figure 48 and Figure 49, respectively. In Figure 48, the ADC084S051 is in track mode: switch SW1 connects the sampling capacitor to one of four analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC084S051 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 49 shows the ADC084S051 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add fixed amounts of charge to the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC084S051 is in this state for the fourth through sixteenth SCLK cycles after $\overline{CS}$ is brought low.

The time when $\overline{CS}$ is low is considered a serial frame. Each of these frames should contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

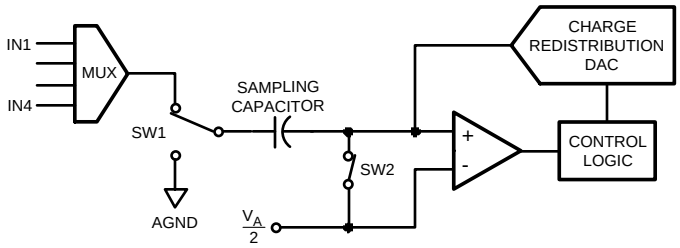



**Figure 48. ADC084S051 in Track Mode**

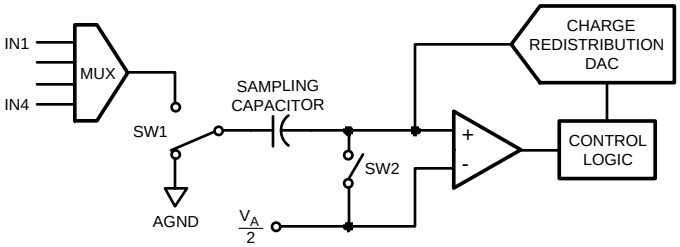



**Figure 49. ADC084S051 in Hold Mode**

## USING THE ADC084S051

An ADC084S051 timing diagram and a serial interface timing diagram for the ADC084S051 are shown in the Timing Diagrams section. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC084S051's Control Register is placed at DIN, the serial data input pin. New data is written to the ADC at DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Additionally, the device goes into a power down state when $\overline{CS}$ is high, and also between continuous conversion cycles.

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During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first, starting with the 5th clock. If there is more than one conversion in a frame, the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK, where "N" is an integer.

When $\overline{CS}$ is brought high, SCLK is internally gated off. If SCLK is stopped in the low state while $\overline{CS}$is high, the subsequent fall of $\overline{CS}$ will generate a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode on the first falling edge of SCLK after the falling edge of $\overline{CS}$.

During each conversion, data is clocked into the ADC at DIN on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. For each conversion, it is necessary to clock in the data indicating the input that is selected for the conversion after the current one. See Table 2, Table 3, and Table 4.

If $\overline{CS}$ and SCLK go low within the times defined by $t_{CSU}$ and $t_{CLH}$, the rising edge of SCLK that begins clocking data in at DIN may be one clock cycle later than expected. It is, therefore, best to strictly observe the minimum $t_{CSU}$ and $t_{CLH}$ times given in the Timing Specifications.

There are no power-up delays or dummy conversions required with the ADC084S051. The ADC is able to sample and convert an input to full conversion immediately following power up. The first conversion result after power-up will be that of IN1.

**Table 2. Control Register Bits**

| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| **DONTC** | **DONTC** | **ADD2** | **ADD1** | **ADD0** | **DONTC** | **DONTC** | **DONTC** |

**Table 3. Control Register Bit Descriptions**

| Bit #: | Symbol: | Description |
|---|---|---|
| 7 - 6, 2 - 0 | DONTC | Don't care. The value of these bits do not affect device operation. |
| 5 | ADD2 | These three bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in Table 4. |
| 4 | ADD1 | |
| 3 | ADD0 | |

**Table 4. Input Channel Selection**

| ADD2 | ADD1 | ADD0 | Input Channel |
|---|---|---|---|
| x | 0 | 0 | IN1 (Default) |
| x | 0 | 1 | IN2 |
| x | 1 | 0 | IN3 |
| x | 1 | 1 | IN4 |


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## ADC084S051 TRANSFER FUNCTION

The output format of the ADC084S051 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC084S051 is $V_A$/256. The ideal transfer characteristic is shown in Figure 50. The transition from an output code of 0000 0000 to a code of 0000 0001 is at 1/2 LSB, or a voltage of $V_A$/512. Other code transitions occur at steps of one LSB.

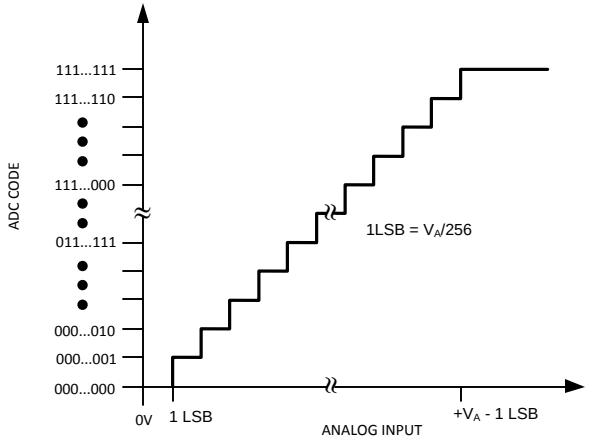



**Figure 50. Ideal Transfer Characteristic**

## TYPICAL APPLICATION CIRCUIT

A typical application of the ADC084S051 is shown in Figure 52. Power is provided, in this example, by the TI LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC084S051.

Because the reference for the ADC084S051 is the supply voltage, any noise on the supply will degrade device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC084S051 supply pin. Because of the ADC084S051's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. Because of the ADC084S051's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is shown connected to a microprocessor or DSP.

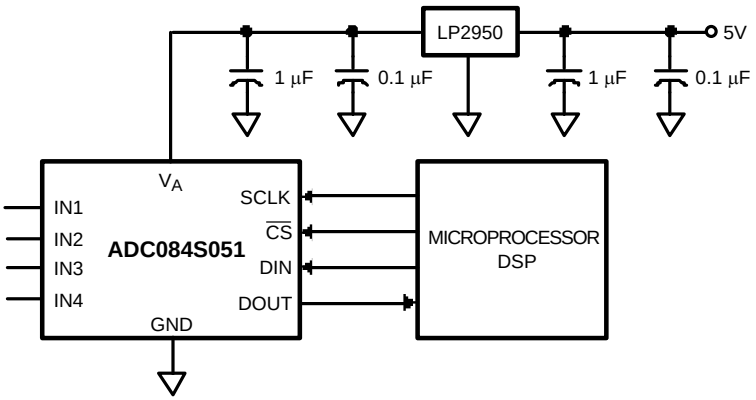



**Figure 51. Typical Application Circuit**

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## ANALOG INPUTS

An equivalent circuit for one of the ADC084S051's input channels is shown in Figure 52. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should any input go beyond ($V_A$ + 300 mV) or (GND − 300 mV), as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, these ESD diodes should NOT be used to clamp the input signal.

The capacitor C1 in Figure 52 has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch, and is typically 500 ohms. Capacitor C2 is the ADC084S051 sampling capacitor, and is typically 30 pF. The ADC084S051 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC084S051 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

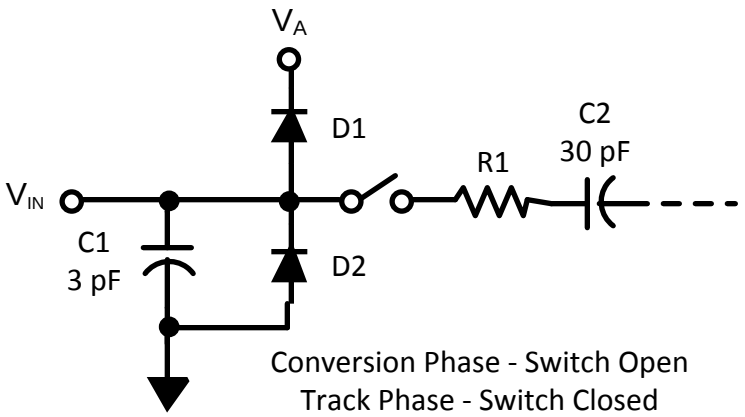



**Figure 52. Equivalent Input Circuit**

## DIGITAL INPUTS AND OUTPUTS

The ADC084S051's digital output DOUT is limited by, and cannot exceed, the supply voltage, $V_A$. The digital input pins are not prone to latch-up and, and although not recommended, SCLK, $\overline{CS}$ and DIN may be asserted before $V_A$ without any latchup risk.

## POWER SUPPLY CONSIDERATIONS

The ADC084S051 is fully powered-up whenever $\overline{CS}$ is low, and fully powered-down whenever $\overline{CS}$ is high, with one exception: the ADC084S051 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see Timing Diagrams).

The ADC084S051 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC084S051 will perform conversions continuously as long as $\overline{CS}$ is held low.

The user may trade off throughput for power consumption by simply performing fewer conversions per unit time. The Power Consumption vs. Sample Rate curve in the Typical Performance Characteristics section shows the typical power consumption of the ADC084S051 versus throughput. To calculate the power consumption, simply multiply the fraction of time spent in the normal mode by the normal mode power consumption , and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power dissipation.


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### Power Management

When the ADC084S051 is operated continuously in normal mode, the maximum throughput is $f_{SCLK}/16$. Throughput may be traded for power consumption by running $f_{SCLK}$ at its maximum 8 MHz and performing fewer conversions per unit time, putting the ADC084S051 into shutdown mode between conversions. A plot of typical power consumption versus throughput is shown in the Typical Performance Characteristics section. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Generally, the user will put the part into normal mode and then put the part back into shutdown mode. Note that the curve of power consumption vs. throughput is nearly linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

### Power Supply Noise Considerations

The charging of any output load capacitance requires current from the power supply, $V_A$. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and maintain noise performance.

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## REVISION HISTORY

| Changes from Revision E (March 2013) to Revision F | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 21 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC084S051CIMM/NOPB | ACTIVE | VSSOP | DGS | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | X10C | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

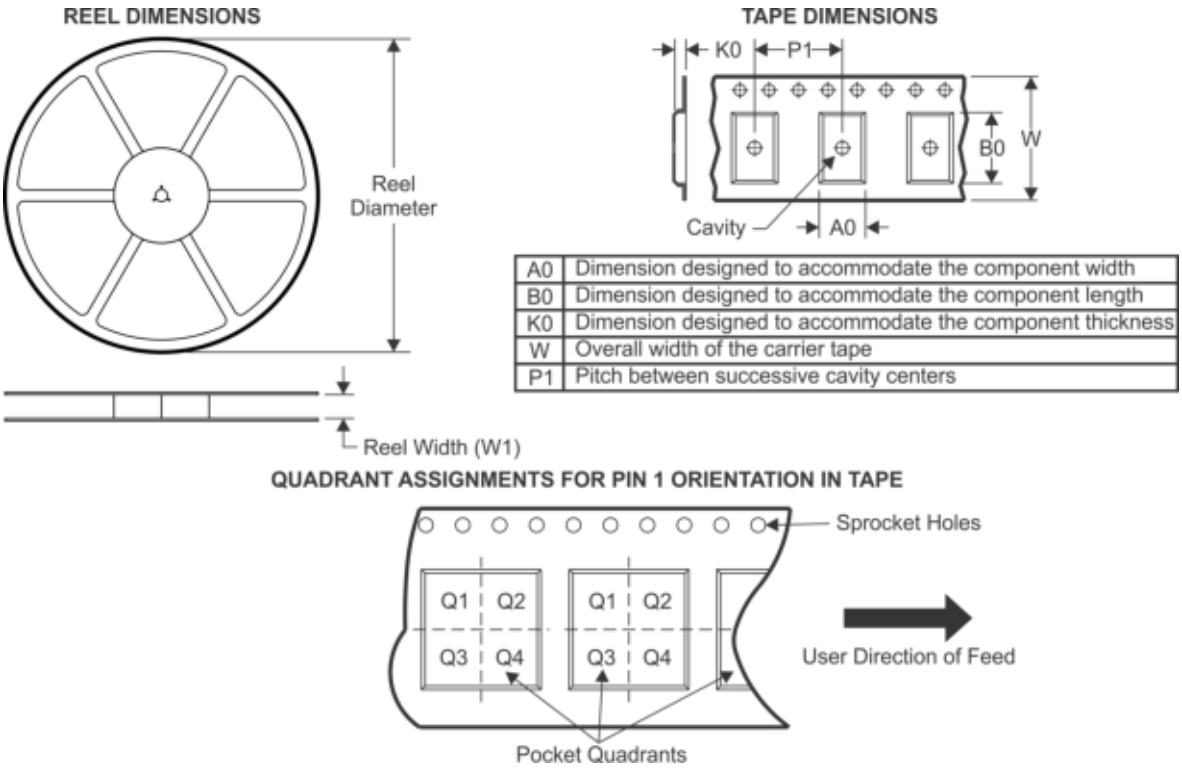
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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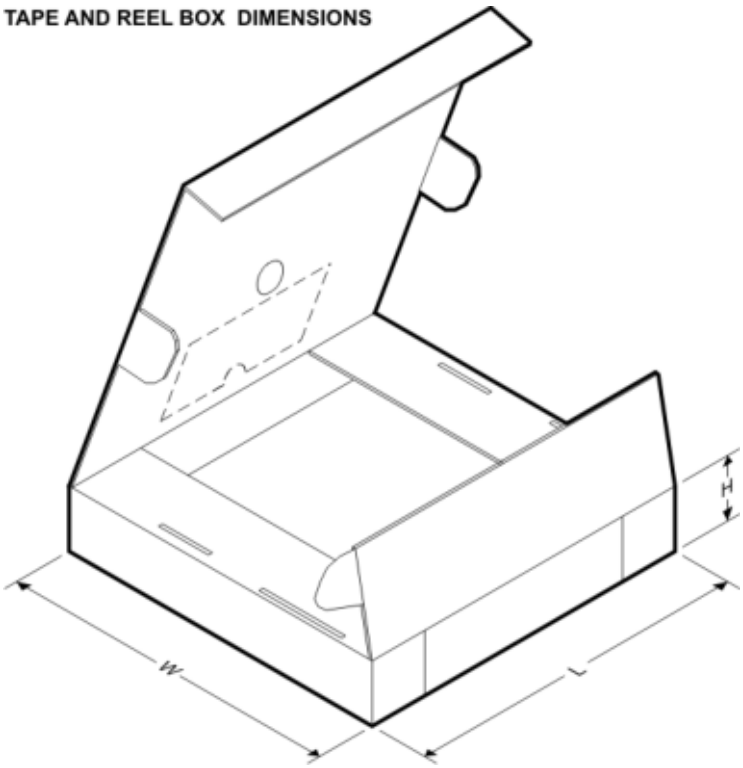



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC084S051CIMM/NOPB | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

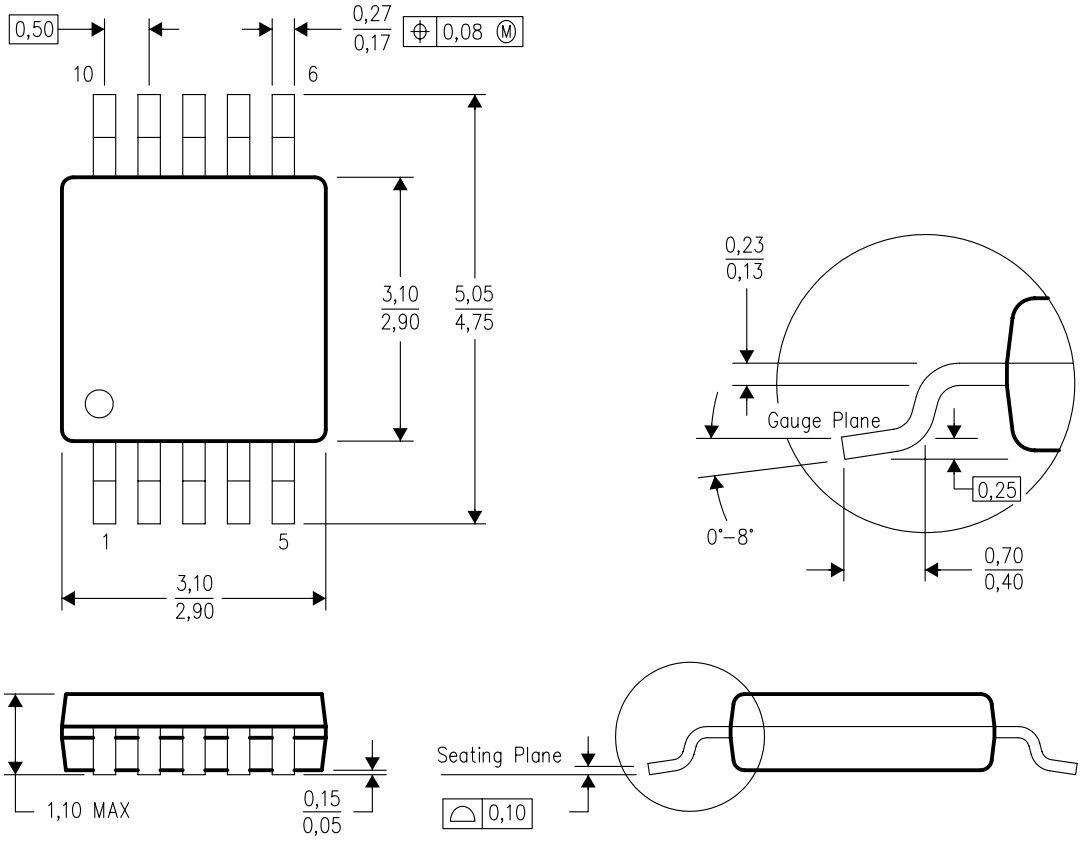
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADC084S051CIMM/NOPB | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |

## DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE




4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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