ADC121S625 12-Bit, 50 ksps to 200 ksps, Differential Input, Micro Power Sampling A/D Converter

Check for Samples: ADC121S625

FEATURES

- **True Differential Inputs**
- **Ensured Performance from 50ksps to 200ksps**
- **External Reference**
- **High AC Common-Mode Rejection**
- **SPI™/QSPI™/MICROWIRE/DSP Compatible Serial Interface**

APPLICATIONS

- **Automotive Navigation**
- **Portable Systems**
- **Medical Instruments**
- **Instrumentation and Control Systems**
- **Motor Control**
- **Direct Sensor Interface**

KEY SPECIFICATIONS

- **Conversion Rate 50 to 200 ksps**
- **Offset Error 0.4 LSB (typ)**
- **Gain Error 0.05 LSB (typ)**
- **INL ± 1 LSB (max)**
- **DNL ± 0.75 LSB (max)**
- **CMRR 82 dB (typ)**
- **Power Consumption**
  - **Active, 200 ksps 2.25 mW (typ)**
  - **Active, 50 ksps 1.33 mW (typ)**
  - **Power Down 60 nW (typ)**

DESCRIPTION

The ADC121S625 is a 12-bit, 50 ksps to 200 ksps sampling Analog-to-Digital (A/D) converter that features a fully differential, high impedance analog input and an external reference. While best performance is achieved with reference voltage between 500mV and 2.5V, the reference voltage can be varied from 100mV to 2.5V, with a corresponding resolution between 49µV and 1.22mV.

The output serial data is binary 2's complement, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and with many common DSP serial interfaces. The differential input, low power, automatic power down, and small size make the ADC121S625 ideal for direct connection to transducers in battery operated systems or remote data acquisition applications.

Operating from a single +5V supply, the normal power consumption is reduced to a few nanowatts in the power-down mode. The ADC121S625 is a pin-compatible superior replacement for the ADS7817 and is available in the VSSOP-8 package. Operation is ensured over the industrial temperature range of −40°C to +85°C and clock rates of 800 kHz to 3.2 MHz.

Connection Diagram

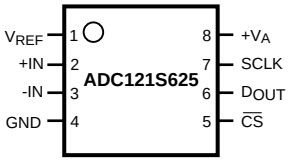


Figure 1. 8-Lead VSSOP
See DGK Package

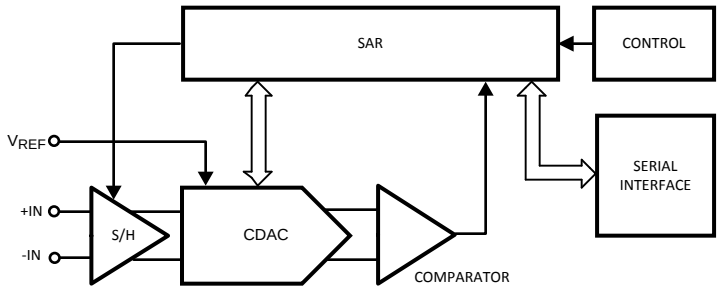
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Block Diagram



PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	DESCRIPTION
1	V_{REF}	Reference Voltage input.
2	+IN	Non-inverting input.
3	−IN	Inverting input.
4	GND	Ground pin.
5	$\overline{CS}$	The ADC is in the active move when this pin is LOW and in the Power-Down Mode when this pin is HIGH. A conversion begins at the fall of $\overline{CS}$.
6	D_{OUT}	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of SCLK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 SCLK edges.
7	SCLK	Serial Clock used to control data transfer. Also serves as the conversion clock.
8	V_A	Power Supply input.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2) (3)

Analog Supply Voltage V_A	−0.3V to 6.5V
Voltage on Any Pin to GND	−0.3V to (V_A +0.3V)
Input Current at Any Pin (4)	±10 mA
Package Input Current (4)	±50 mA
Power Consumption at T_A = 25°C	See (5)
ESD Susceptibility (6) Human Body Model Machine Model	 2500V 250V
Charge Device Modeling (CDM)	750V
Soldering Temperature, Infrared, 10 seconds (7)	 260°C
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C

(1) Absolute maximum ratings are limiting values which indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC121S625 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms.
(7) See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 Texas Instruments Linear Data Book, for other methods of soldering surface mount devices.

Operating Ratings (1) (2)

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage, V_A	+4.5V to +5.5V
Reference Voltage, V_{REF}	+0.1V to 2.5V
Input Common-Mode Voltage, V_{CM}	See Figure 51
Digital Input Pins Voltage Range	0 to V_A
Clock Frequency	0.8 MHz to 3.2 MHz
Differential Analog Input Voltage	$-V_{REF}$ to $+V_{REF}$

(1) Absolute maximum ratings are limiting values which indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

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Package Thermal Resistance

Package	θ_{JA}
8-lead VSSOP	20°C / W

ADC121S625 Converter Electrical Characteristics(1)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 0.8 to 3.2 MHz, f_{IN} = 20 kHz, C_L = 100 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limits	Units (2)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non-Linearity			+0.5 −0.3	**+1.0** **-1.0**	LSB (max) LSB (min)
DNL	Differential Non-Linearity			±0.4	**±0.75**	LSB (max)
OE	Offset Error			0.4	**±4**	LSB (max)
FSE	Positive Full-Scale Error			+0.2		LSB
	Negative Full-Scale Error			+0.2		LSB
GE	Gain Error			-0.05	**±4**	LSB
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 20 kHz, −0.1 dBFS		72.6	**68.5**	dBc (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 20 kHz, −0.1 dBFS		72.9	**70**	dBc (min)
THD	Total Harmonic Distortion	f_{IN} = 20 kHz, −0.1 dBFS		−84	**−74**	dBc (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 20 kHz, −0.1 dBFS		85.2	**74**	dBc (min)
ENOB	Effective Number of Bits	f_{IN} = 20 kHz, −0.1 dBFS		11.8	**11.1**	bits (min)
FPBW	−3 dB Full Power Bandwidth	Output at 70.7%FS with FS Input	Differential Input	26		MHz
			Single-Ended Input	22		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Differential Input Range				**$-V_{REF}$**	V (min)
					$+V_{REF}$	V (max)
I_{DCL}	DC Leakage Current			±0.04	**±2**	µA (max)
C_{INA}	Input Capacitance	In Track Mode		17		pF
		In Hold Mode		3		pF
CMRR	Common Mode Rejection Ratio			82		dB
V_{REF}	Reference Voltage Range				**0.1**	V (min)
					2.5	V (max)
I_{REF}	Reference Current	$\overline{CS}$ low, f_{SCLK} = 3.2 MHz, f_S = 200 ksps, output = FF8h		12		µA
		$\overline{CS}$ low, f_{SCLK} = 3.2 MHz, f_S = 50 ksps, output = FF8h		3		µA
		$\overline{CS}$ low, f_{SCLK} = 3.2 MHz, 12.5 ksps, output = FF8h		0.7		µA
		$\overline{CS}$ high, f_{SCLK} = 0		0.3		µA
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage	V_A = 4.5V to 5.5V			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_A = 4.5V to 5.5V			**0.8**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_A		±0.03	**1**	µA (max)
C_{IND}	Input Capacitance			2	**4**	pF (max)

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

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ADC121S625 Converter Electrical Characteristics(1) (continued)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 0.8 to 3.2 MHz, f_{IN} = 20 kHz, C_L = 100 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units (2)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	V_A = 4.5V to 5.5V, I_{SOURCE} = 250 µA	V_A − 0.05	**V_A − 0.2**	V (min)
		V_A = 4.5V to 5.5V, I_{SOURCE} = 2 mA	V_A − 0.1		V
V_{OL}	Output Low Voltage	V_A = 4.5V to 5.5V, I_{SINK} = 250 µA	0.02	**0.4**	V (max)
		V_A = 4.5V to 5.5V, I_{SOURCE} = 2 mA	0.1		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current		±0.03	**±1**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Binary 2'S Complement		
POWER SUPPLY CHARACTERISTICS					
V_A	Analog Supply Voltage			**4.5**	V (min)
				5.5	V (max)
I_A Active	Supply Current, Normal Mode (Operational)	f_{SCLK} = 3.2 MHz, f_{SMPL} = 200 ksps, f_{IN} = 20 kHz, C_L = 15pF	410	**510**	µA (max)
		f_{SCLK} = 3.2 MHz, f_{SMPL} = 12.5 ksps, C_L = 15pF, Power Down between conversions	31		µA
		f_{SCLK} = 0.8 MHz, f_{SMPL} = 50 ksps, C_L = 15pF	242		µA
		f_{SCLK} = 0.2 MHz, f_{SMPL} = 12.5 ksps, C_L = 15pF (3)	200		µA
I_A Shutdown	Supply Current, Shutdown ($\overline{CS}$ high)	f_{SCLK} = 0	0.01	**2**	µA (max)
		f_{SCLK} = 3.2 MHz	6		µA
PWR Active	Power Consumption, Normal Mode (Operational)	f_{SCLK} = 3.2 MHz, f_{SMPL} = 200 ksps, f_{IN} = 20 kHz, C_L = 15pF	2.25	**2.8**	mW (max)
		f_{SCLK} = 3.2 MHz, f_{SMPL} = 12.5 ksps, C_L = 15pF, Power Down between conversions	0.18		mW
		f_{SCLK} = 0.8 MHz, f_{SMPL} = 50 ksps, C_L = 15pF	1.33		mW
		f_{SCLK} = 0.2 MHz, f_{SMPL} = 12.5 ksps, C_L = 15pF (3)	1.1		mW
PWR Shutdown	Power Consumption, Shutdown ($\overline{CS}$ high)	f_{SCLK} = 0	0.06	**11**	µW (max)
		f_{SCLK} = 3.2 MHz	33		µW
PSRR	Power Supply Rejection Ratio	Offset Change with 1.0V change in V_A	71		dB
		Gain Error Change with 1.0V change in V_A	83		dB
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Maximum Clock Frequency		4.8	**3.2**	MHz (min)
f_{SCLK}	Minimum Clock Frequency		200	**800**	kHz (max)
f_S	Maximum Sample Rate		300	**200**	ksps (min)
t_{ACQ}	Track/Hold Acquisition Time			**1.5**	SCLK cycles (min)
				2.0	SCLK cycles (max)
t_{CONV}	Conversion Time		12	**12**	SCLK cycles

(3) While the maximum sample rate is f_{SCLK}/16, the actual sample rate may be lower than this by having the $\overline{CS}$ rate being slower than f_{SCLK}/16.

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ADC121S625 Converter Electrical Characteristics(1) (continued)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 0.8 to 3.2 MHz, f_{IN} = 20 kHz, C_L = 100 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units (2)
t_{CYC}	Throughput Time	Normal Operation		**16**	SCLK cycles
		Short Cycled		**14**	SCLK cycles (min)
f_{RATE}	Throughput Rate			**200**	ksps (max)
t_{AD}	Aperture Delay		6		ns

ADC121S625 Timing Specifications(1)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 0.8 MHz to 3.2 MHz, C_L = 100 pF, **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
t_{CFCS}	SCLK Fall to $\overline{CS}$ Fall			**0**	ns (min)
t_{CSCR}	$\overline{CS}$ Fall to SCLK Rise	See (2)		**0**	ns (min)
t_{CHLD}	SCLK Fall to Data Change Hold Time	See (2)		**10**	ns (min)
t_{CDV}	SCLK Fall to Next D_{OUT} Valid		38	**100**	ns (max)
t_{DIS}	Rising Edge of $\overline{CS}$ To D_{OUT} Disabled		38	**50**	ns (max)
t_{EN}	2nd SCLK Fall after $\overline{CS}$ Fall to D_{OUT} Enabled		6	**50**	ns (max)
t_{CH}	SCLK High Time		42	**60**	ns (min)
t_{CL}	SCLK Low Time		42	**60**	ns (min)
t_r	D_{OUT} Rise Time		5	**50**	ns (max)
t_f	D_{OUT} Fall Time		13	**50**	ns (max)

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Clock should be in low when $\overline{CS}$ is asserted, as indicated by the t_{CSCR} and t_{CFCS} specifications.

Timing Diagrams

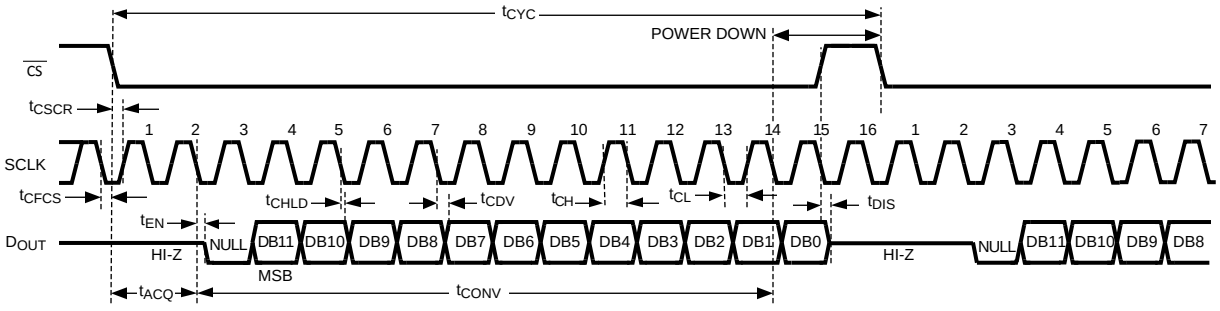


Figure 2. ADC121S625 Single Cycle Timing Diagram

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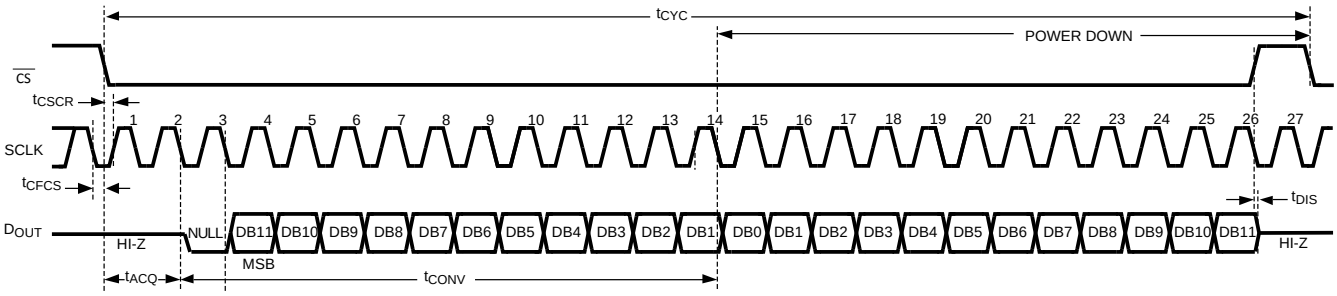


Figure 3. ADC121S625 Double Cycle Timing Diagram

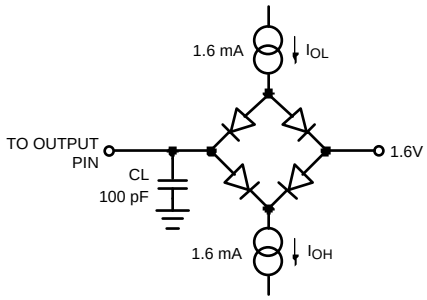


Figure 4. Timing Test Circuit

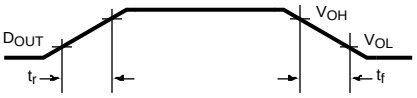


Figure 5. Voltage Waveform for D_{OUT}, t_r, t_f

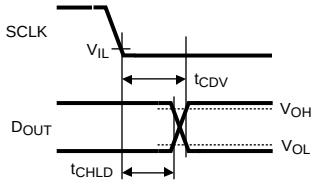


Figure 6. Voltage Waveforms for d_{OUT} delay time, t_{CDV}

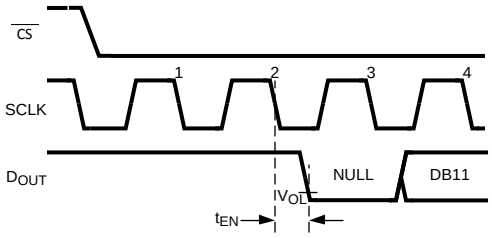


Figure 7. Voltage Waveform for t_{EN}

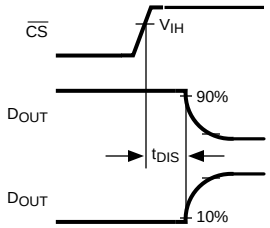


Figure 8. Voltage Waveform for t_{DIS}

Specification Definitions

APERTURE DELAY is the time between the second falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

CMRR = 20 LOG (ΔCommon Input / ΔOutput) (1)

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the difference between Positive Full Scale Error and Negative Full Scale Error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC121S625 is ensured not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from negative full scale and the next code and $-V_{REF}$ + 0.5 LSB

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 000h to 001h and 1/2 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale V_{REF} minus 1.5 LSB.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the supply voltage is rejected. It is the ratio of the change in Full-Scale Gain Error or the Offset Error that results from a change in the d.c. power supply voltage, expressed in dB.

PSRR = 20 LOG (ΔV_A / ΔOffset) (2)

PSRR = 20 LOG (ΔV_A / ΔGain) (3)

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

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SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^{\,2} + \cdots + A_{f6}^{\,2}}{A_{f1}^{\,2}}} \tag{4}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

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Typical Performance Characteristics

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

DNL - 50 ksps

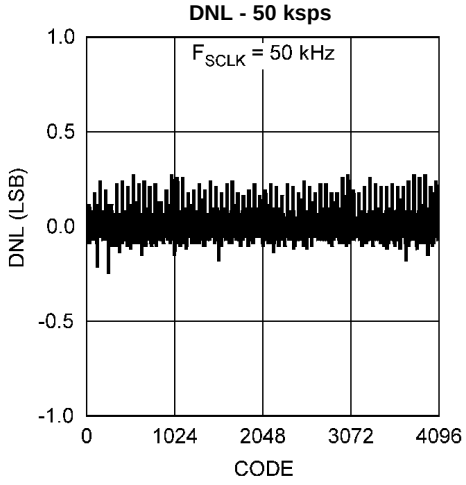


Figure 9.

INL - 50 ksps

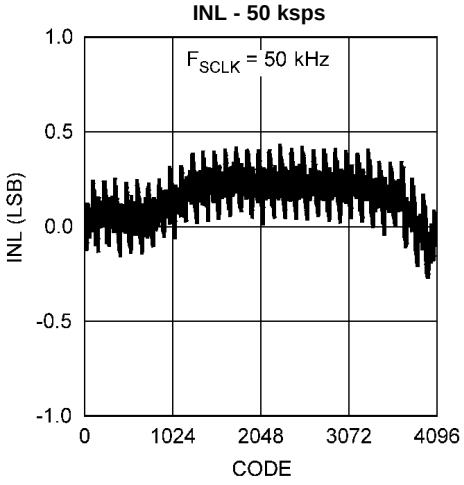


Figure 10.

DNL - 200 ksps

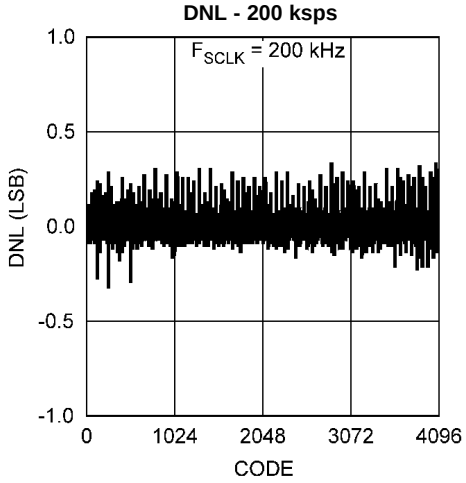


Figure 11.

INL - 200 ksps

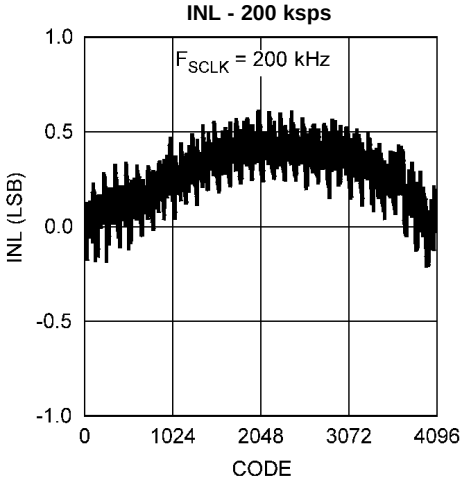


Figure 12.

DNL vs. V_A

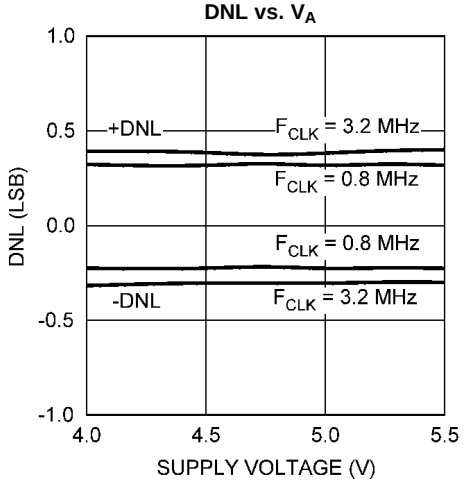


Figure 13.

INL vs. V_A

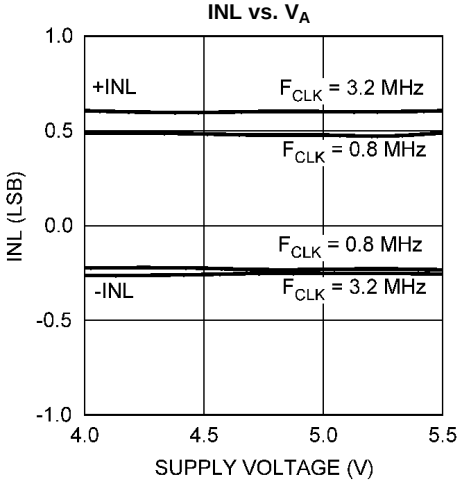


Figure 14.

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Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

DNL vs. f_{SCLK}

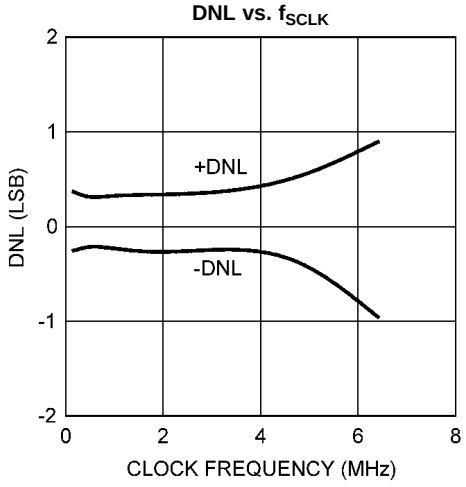


Figure 15.

INL vs. f_{SCLK}

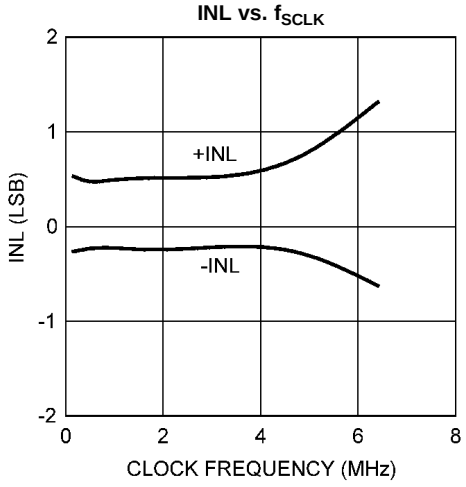


Figure 16.

DNL vs. SCLK DUTY CYCLE

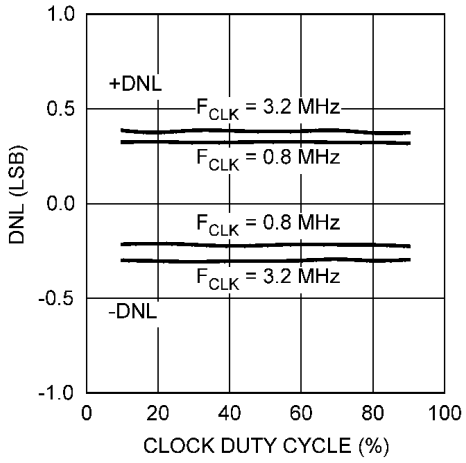


Figure 17.

INL vs. SCLK DUTY CYCLE

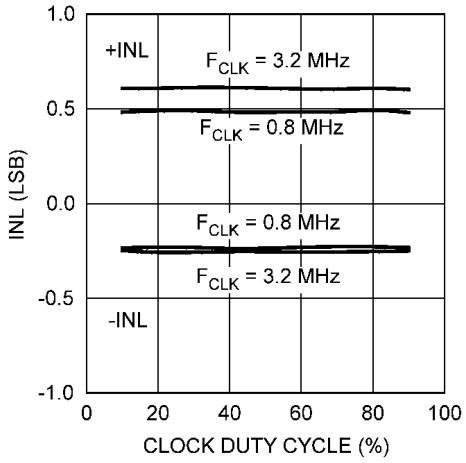


Figure 18.

DNL vs. TEMPERATURE

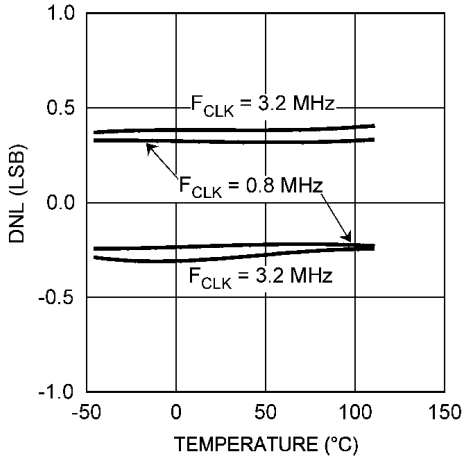


Figure 19.

INL vs. TEMPERATURE

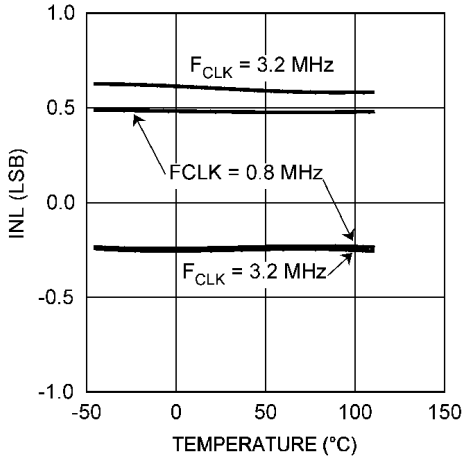


Figure 20.

Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

SNR vs. V_A

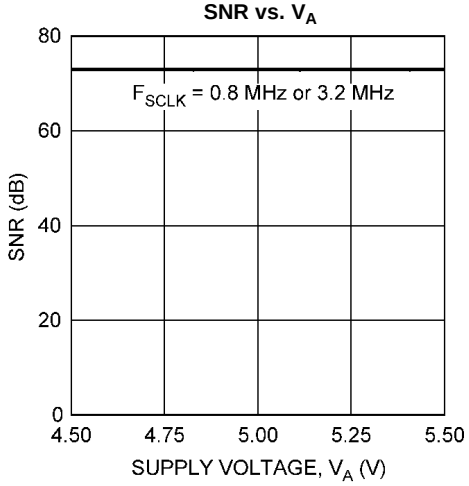


Figure 21.

THD vs. V_A

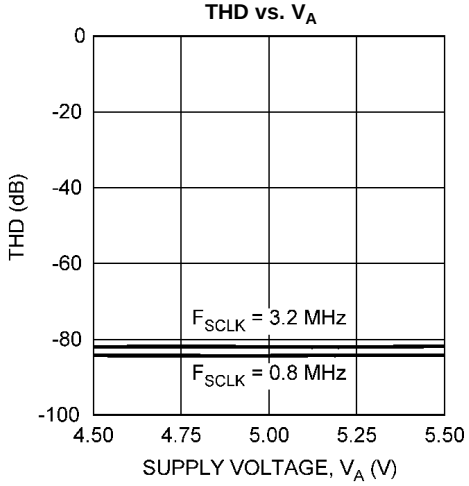


Figure 22.

SINAD vs. V_A

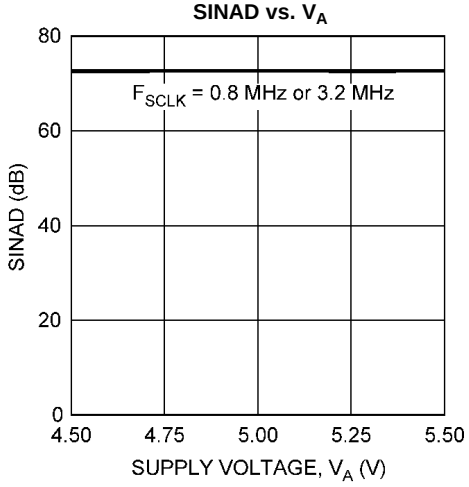


Figure 23.

SFDR vs. V_A

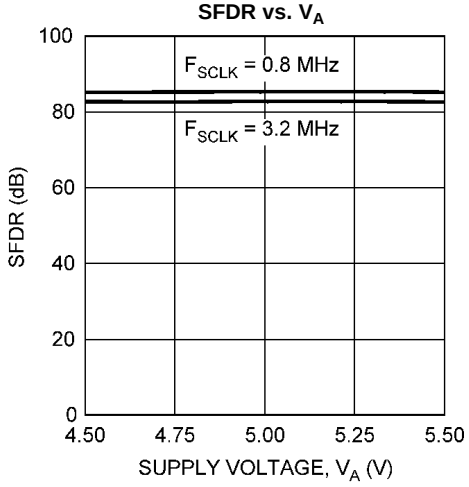


Figure 24.

SNR vs. V_{REF}

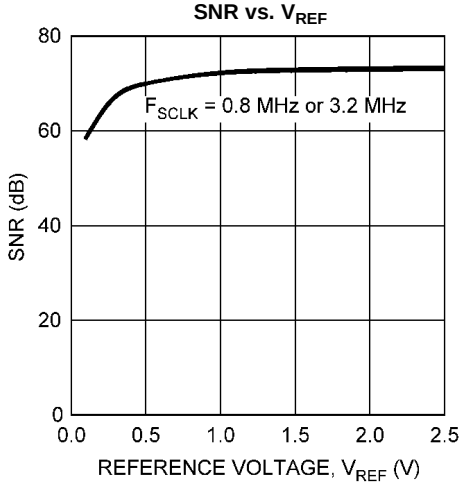


Figure 25.

THD vs. V_{REF}

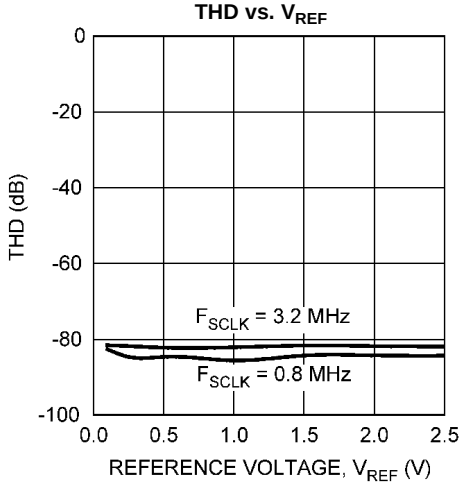


Figure 26.

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Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

SINAD vs. V_{REF}

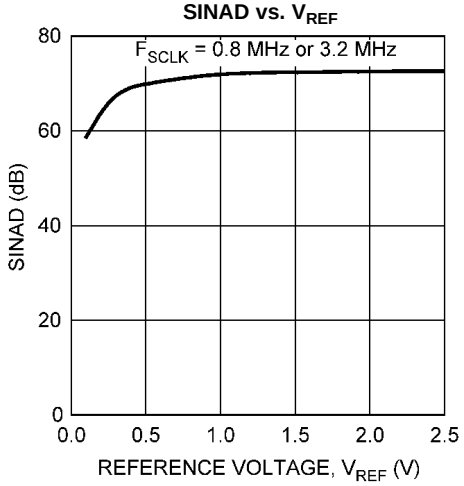


Figure 27.

SFDR vs. V_{REF}

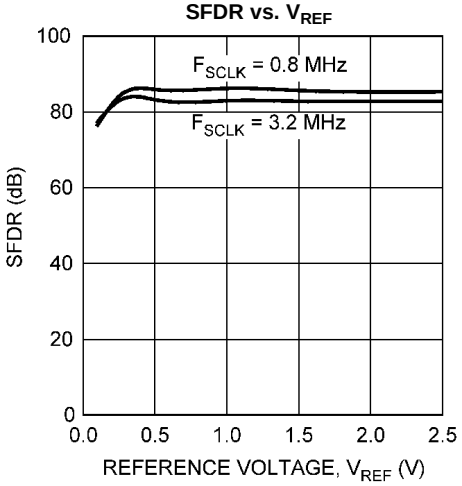


Figure 28.

SNR vs. CLOCK FREQUENCY

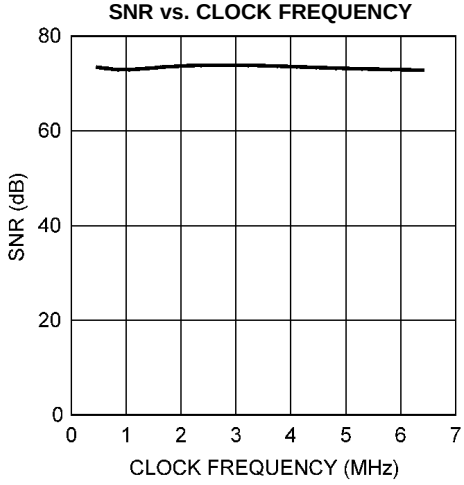


Figure 29.

THD vs. CLOCK FREQUENCY

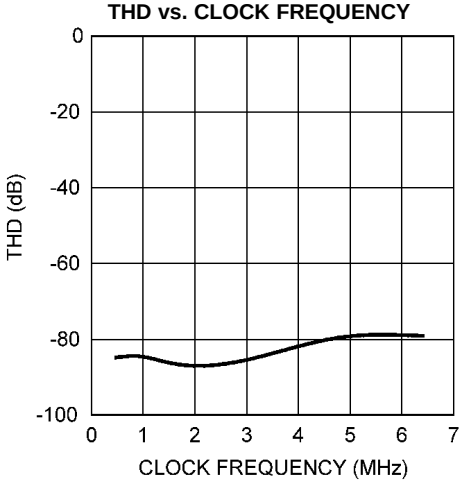


Figure 30.

SINAD vs. CLOCK FREQUENCY

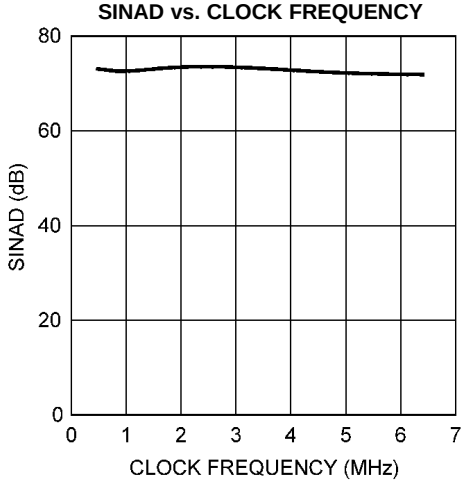


Figure 31.

SFDR vs. CLOCK FREQUENCY

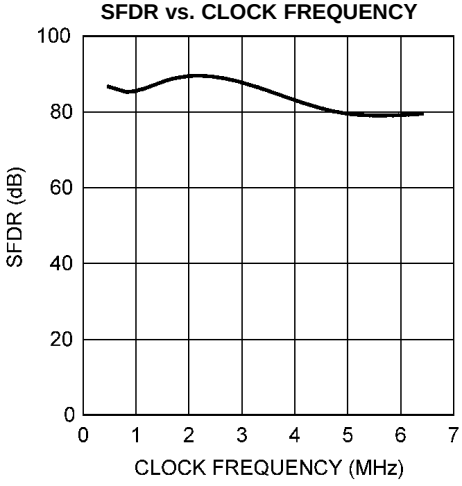


Figure 32.

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Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

SNR vs. SCLK DUTY CYCLE

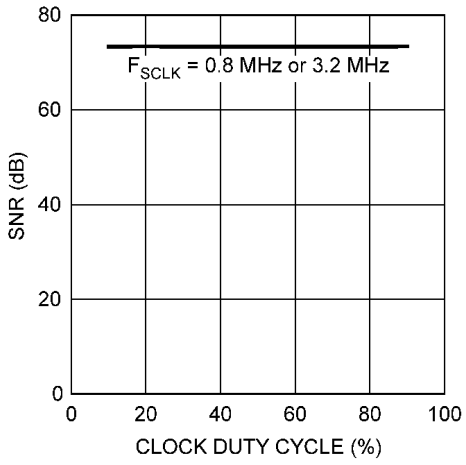


Figure 33.

THD vs. SCLK DUTY CYCLE

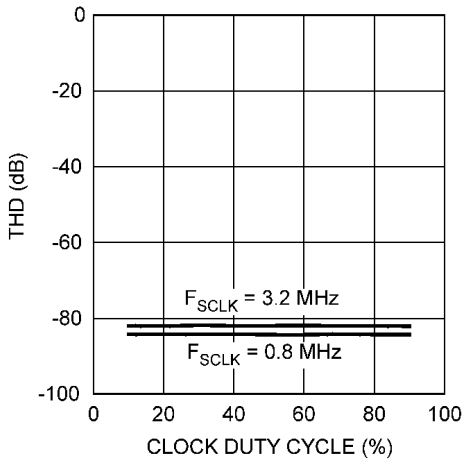


Figure 34.

SINAD vs. SCLK DUTY CYCLE

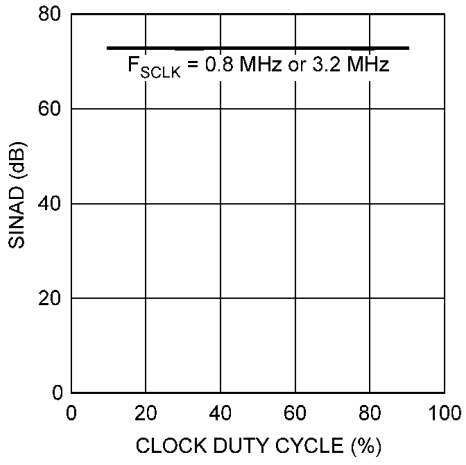


Figure 35.

SFDR vs. SCLK DUTY CYCLE

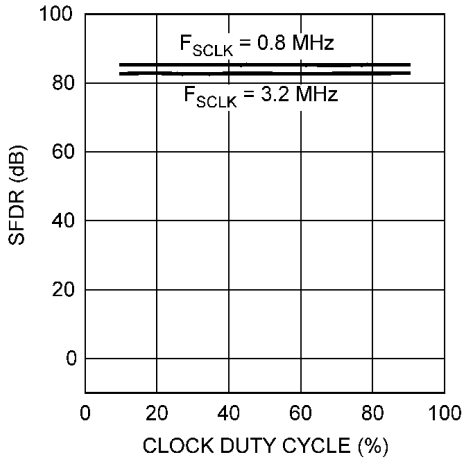


Figure 36.

SNR vs. INPUT FREQUENCY

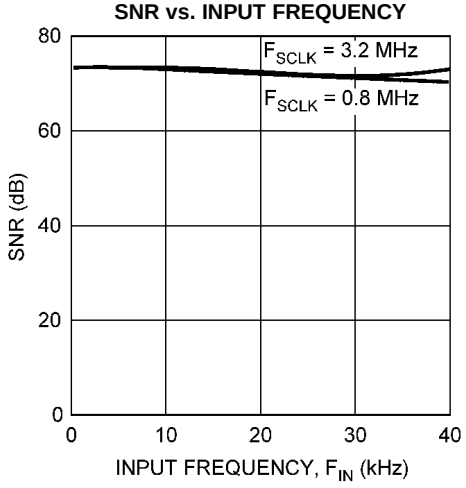


Figure 37.

THD vs. INPUT FREQUENCY

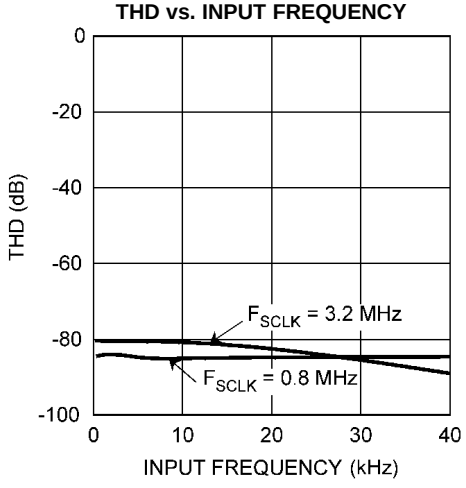


Figure 38.

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Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

SINAD vs. INPUT FREQUENCY

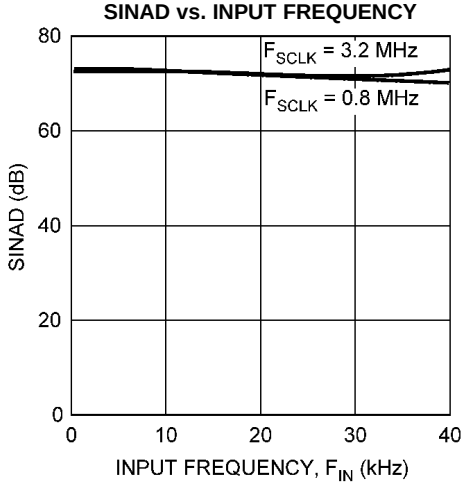


Figure 39.

SFDR vs. INPUT FREQUENCY

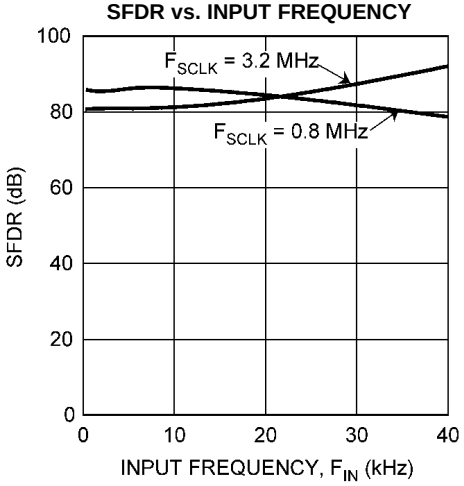


Figure 40.

REF. CURRENT vs. TEMPERATURE (Output = FF8h)

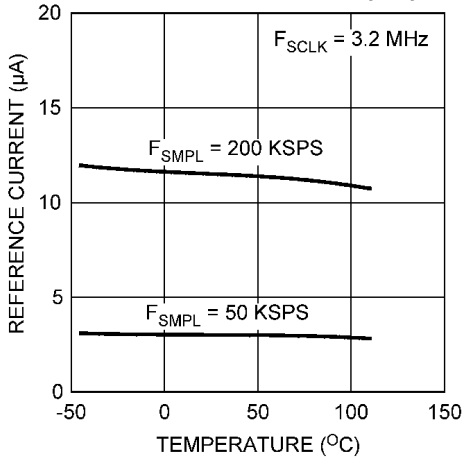


Figure 41.

REF. CURRENT vs. SAMPLE RATE (Output = FF8h)

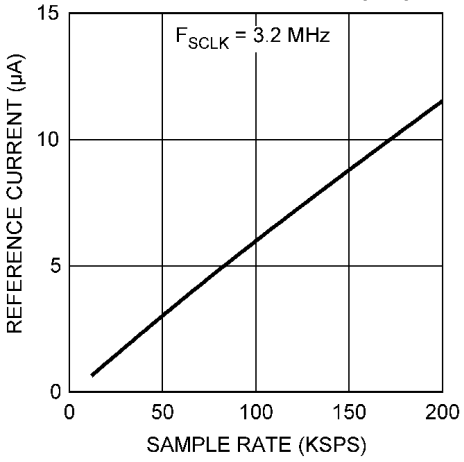


Figure 42.

SUPPLY CURRENT vs. TEMPERATURE

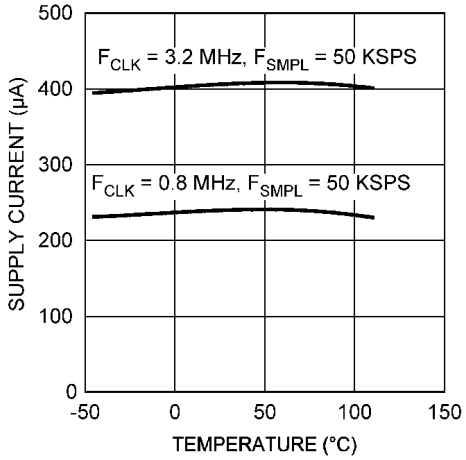


Figure 43.

POWER DOWN CURRENT vs. TEMPERATURE

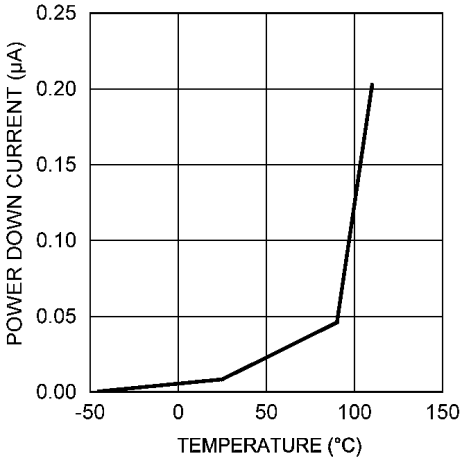


Figure 44.

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Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, f_{IN} = 20 kHz unless otherwise stated.

OFFSET ERROR vs. V_{REF}

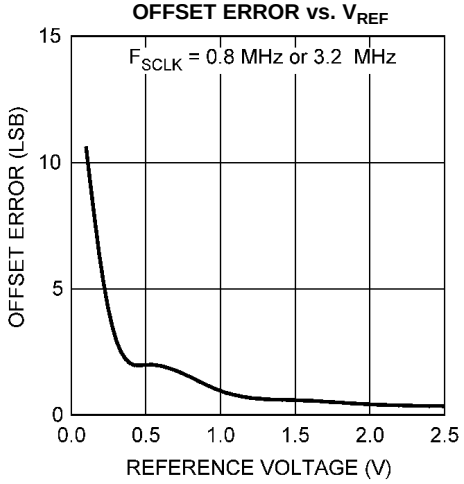


Figure 45.

OFFSET ERROR vs. TEMPERATURE

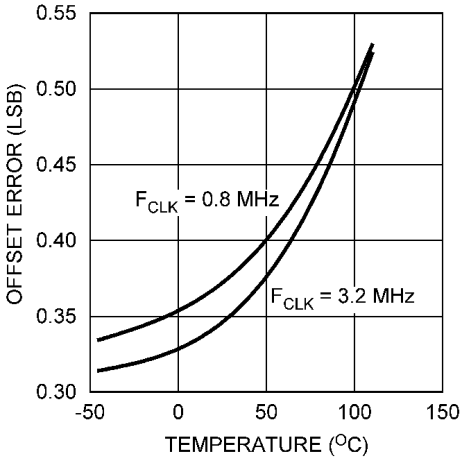


Figure 46.

GAIN ERROR vs. V_{REF}

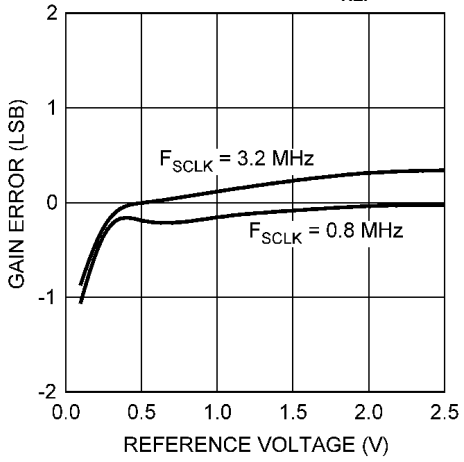


Figure 47.

GAIN ERROR vs. TEMPERATURE

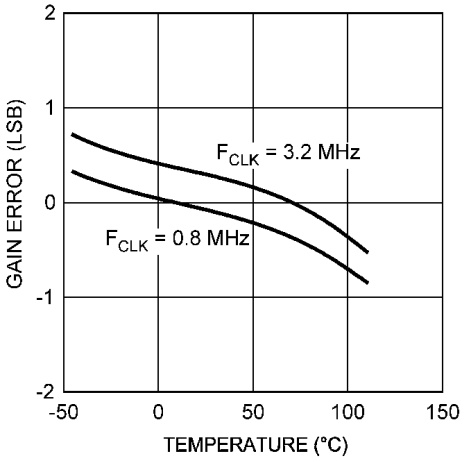


Figure 48.

Spectral Response - 50 ksps

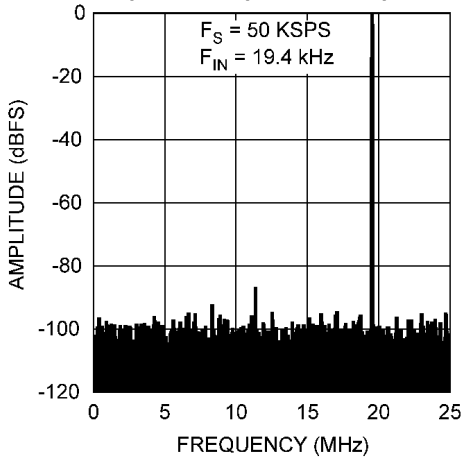


Figure 49.

Spectral Response - 200 ksps

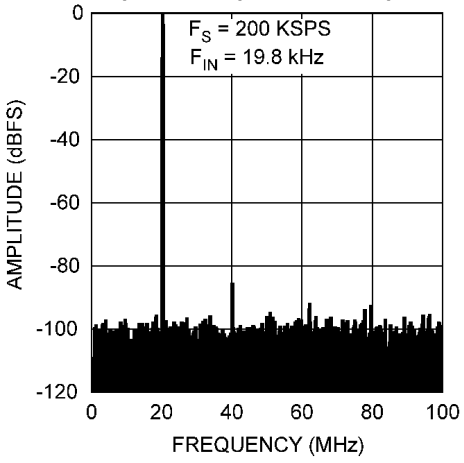


Figure 50.

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FUNCTIONAL DESCRIPTION

The ADC121S625 analog-to-digital converter uses a successive approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample/hold function. The architecture and process allow the ADC121S625 to acquire and convert an analog signal at sample rates up to 200,000 conversions per second while consuming very little power.

The ADC121S625 requires an external reference and external clock, and a single +5V power source that can be as low as +4.5V. The external reference can be any voltage between 100mV and 2.5V. The value of the reference voltage determines the range of the analog input, while the reference input current depends on the conversion rate.

The external clock can take on values as indicated in the ADC121S625 Converter Electrical Characteristics section of this data sheet. The duty cycle of the clock is essentially unimportant, provided the minimum clock high and low times are met. The minimum clock frequency is set by internal capacitor leakage. Each conversion requires 16 SCLK cycles to complete. Short cycling can reduce this to 14 or 15 SCLK cycles, depending upon whether the clock edge after the fall of $\overline{CS}$ is a rise or a fall. See the Timing Diagrams.

The analog input is presented to the two input pins: +IN and –IN. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from internal circuitry while a conversion is in progress.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit first, at the D_{OUT} pin. The digital data that is provided at the D_{OUT} pin is that of the conversion currently in progress. It is possible to continue to clock the ADC121S625 after the conversion is complete and to obtain the serial data least significant bit first. Each bit of the data word (including the leading null bit) is clocked out on subsequent falling edges of SCLK and can be clocked into the receiving device on the rising edges. See SERIAL DIGITAL INTERFACE and timing diagram for more information.

REFERENCE INPUT

The externally supplied reference voltage sets the analog input range. The ADC121S625 will operate with a reference voltage in the range of 100mV to 2.5V. However, care must be exercised when the reference voltage is less than 500 millivolts.

As the reference voltage is reduced, the range of input voltages corresponding to each digital output code is reduced. That is, a smaller analog input range corresponds to one LSB (Least Significant Bit). The size of one LSB is equal to twice the reference voltage divided by 4096. When the LSB size goes below the noise floor of the ADC121S625, the noise will span an increasing number of codes and overall noise performance will suffer. That is, for dynamic signals the SNR will degrade and for d.c. measurements the code uncertainty will increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, since offset and gain errors are specified in LSB, any offset and/or gain errors inherent in the A/D converter will increase in terms of LSB size as the reference voltage is reduced.

The ADC121S625 is more sensitive to nearby signals and EMI (electromagnetic interference) when a low reference voltage is used. For this reason, extra care should be exercised in planning a clean layout, a low noise reference and a clean power supply when using low reference voltages.

The reference input and the analog inputs are connected to the capacitor array through a switch matrix when the input is sampled. Hence, the only current required at the reference and at the analog inputs is only a series of transient spikes. The amount of these current spikes will depend, to some degree, upon the conversion code, but will not vary a great deal.

The current required to recharge the input capacitance at the reference and analog signal inputs will cause voltage spikes at these pins. Do not try to filter our these noise spikes. Rather, ensure that the transient settles out during the sample period (1.5 clock cycles after the fall at the $\overline{CS}$ input).

Lower reference voltages will decrease the current pulses at the reference input and, therefore, will slightly decrease the average input current there because the internal capacitance is required to take on a lower charge at lower reference voltages. The reference current changes only slightly with temperature. See the curves, “Reference Current vs. Sample Rate”, “Reference Current vs. Temperature” and “SNR vs. V_{REF}” in the Typical Performance Characteristics section.

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ANALOG SIGNAL INPUTS

The ADC121S625 has a differential input. As such, the effective input voltage that is digitized is (+IN) − (−IN). As is the case with any differential input A/D converter, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. Yet, the ADC121S625 can be presented with a single-ended input.

Differential Input Operation

With a fully differential input voltage or signal, a positive full scale output code (0111 1111 1111b or 7FFh) will be obtained when (+IN) − (−IN) ≥ V_{REF} − 1.5 LSB and a negative full scale code (1000 0000 0000b or 800h) will be obtained when (+IN) − (−IN) ≤ −V_{REF} + 0.5 LSB. This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code.

Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC121S625 should be driven with a signal or voltages that have a maximum to minimum value range that is equal to or less than twice the reference voltage. The inverting input (−IN) should be biased to a stable voltage that is half way between these maximum and minimum values. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

Input Common Mode Voltage

The allowable input common mode voltage (V_{CM}) range depends upon the supply and reference voltages used for the ADC121S625 and are depicted in Figure 51 and Figure 52. The minimum and maximum common mode voltages for differential and single-ended operation are shown in Table 1.

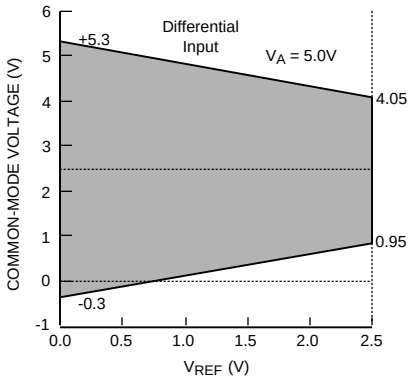


Figure 51. V_{CM} range for differential input operation

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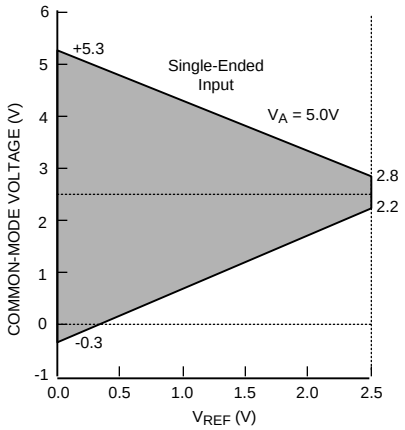


Figure 52. V_{CM} range for single-ended operation

Table 1. Allowable V_{CM} Range

Input Signal	Minimum V_{CM}	Maximum V_{CM}
Differential	V_{REF} / 2 − 0.3V	V_A + 0.3V − (V_{REF} / 2)
Single-Ended	V_{REF} − 0.3V	V_A + 0.3V − V_{REF}

SERIAL DIGITAL INTERFACE

The ADC121S625 communicates via a synchronous 3-wire serial interface as shown in the timing diagram. Each output bit is sent on the falling edge of SCLK. While most receiving systems will capture the digital output bits on the rising edge of SCLK, the falling edge of SCLK may be used to capture each bit if the minimum hold time for D_{OUT} is acceptable.

Digital Inputs

The Digital inputs consist of the SCLK and $\overline{CS}$. A falling $\overline{CS}$ initiates the conversion and data transfer. The time between the fall of $\overline{CS}$ and the second falling edge of SCLK is used to sample the input signal. The data output is enabled at the second falling edge of SCLK that follows the fall of $\overline{CS}$. Since the first bit clocked out is a null bit, the MSB is clocked out on the third falling edge of SCLK after the fall of $\overline{CS}$. For the next 12 SCLK periods D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, the output data is repeated if CS remains low after the LSB is output, but in a least significant bit first format, with the LSB being output only once, as indicated in the Figure 3. D_{OUT} will go into its high impedance state after the B9 - B10 - B11 sequence. If $\overline{CS}$ is raised between prior to or at the 15th clock fall, D_{OUT} will go into its high impedance state after the LSB (B0) is output and the data is not repeated. Additional clock cycles will not effect the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

SCLK Input

The SCLK (serial clock) is used to time the conversion process and to clock out the conversion results. This input is TTL/CMOS compatible. Internal settling time limits the maximum clock frequency and internal capacitor leakage, or droop, limits the minimum clock frequency. The ADC121S625 offers ensured performance with clock rates in the range indicated in the ADC121S625 Converter Electrical Characteristics section.

Data Output

The output data format of the ADC121S625 is Two's Complement, as shown in Table 2. This table indicates the ideal output code for the given input voltage and does not include the effects of offset, gain error, linearity errors, or noise.

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Table 2. Ideal Output Code vs. Input Voltage

Description	Analog Input (+IN) − (−IN)	2's Complement Binary Output	2's Comp. Hex Code
+ Full Scale	V_{REF} − 1 LSB	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
Midscale − 1 LSB	0V − 1 LSB	1111 1111 1111	FFF
− Full Scale	$-V_{REF}$	1000 0000 0000	800

Applications Information

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC121S625:

$-40°C \le T_A \le +85°C$

$+4.5V\ V_A \le +5.5V$

$0.1V \le V_{REF} \le 2.5V$

$0.8\ MHz \le f_{CLK} \le 4.8\ MHz$

V_{CM}: See Input Common Mode Voltage

POWER CONSUMPTION

The architecture, design and fabrication process allows the ADC121S625 to operate at conversion rates up to 200ksps while requiring very little power. In order to minimize power consumption in applications requiring sample rates below 50ksps, the ADC121S625 should be run at a f_{SCLK} of 3.2 MHz and with the CS rate as slow as the system requires. The ADC will go into the power down mode at the end of each conversion, minimizing power consumption. See Burst Mode Operation for more information.

However, some things should be kept in mind to absolutely minimize power consumption.

The consumption scales directly with conversion rate, so minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

The ADC121S625 goes into its power down mode on the rising edge of $\overline{CS}$ or the 14th or 16th falling edge of SCLK after the fall of $\overline{CS}$, as described in the Functional Description, whichever occurs first (see Timing Diagrams). Ideally, each conversion should occur as quickly as possible, preferably at the maximum rated clock rate and the $\overline{CS}$ rate used to determine the sample rate. This causes the converter to spend the longest possible time in the power down mode. This is very important for minimizing power consumption as the converter uses current for the analog circuitry, which continuously consumes power when converting. So, if less than 12 bits are needed, power may be saved by bringing $\overline{CS}$ high after clocking out the number of bits needed.

Of course, the converter also uses power on each SCLK transition, as is typical for digital CMOS components, so stopping the clock when in the power down mode will further reduce power consumption. As mentioned in REFERENCE INPUT, power consumption is also slightly lower with lower reference voltages.

There is an important difference between entering the power down mode after a conversion is complete and $\overline{CS}$ if left LOW and the full power down mode when $\overline{CS}$ is HIGH. Both of these power down the analog portion of the ADC121S625, but the digital portion is powered down only when $\overline{CS}$ is HIGH. So, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH.

Short Cycling

Another way of saving power is to short cycle the conversion process. This is done by pulling the $\overline{CS}$ line high after the last required bit is received from the ADC121S625 output. This is possible because the ADC121S625 places the latest data bit on the D_{OUT} line as it is generated. If only 8-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ HIGH after the 8th bit has been clocked out. Halting conversion after the last needed bit is received is called short cycling.

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Short cycling can be used to lower the power consumption in those applications that do not need a full 12-bit resolution, or where an analog signal is being monitored until some condition occurs. For example, it may not be necessary to use the full 12-bit resolution of the ADC121S625 as long as the signal being monitored is within certain limits. The conversion, then, can be terminated after the first few bits (as low as 3 or 4 bits, in some cases). This can lower power consumption in both the converter and the rest of the system, because they spend more time in the power down mode and less time in the active mode.

Short cycling can also be used to reduce the required number of SCLK cycles from 16 to 14, allowing for a little faster throughput. That is, SCLK can be raised after the rise of the 14th SCLK, reducing the overall cycle time (t_{CYC}) by about 12%.

Burst Mode Operation

Normal operation requires the SCLK frequency to be 16 times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, because starting a new conversion requires a new fall of $\overline{CS}$, it is possible to have the SCLK rate much higher than 16 times the $\overline{CS}$ rate. When this is done, the device is said to be operating in the Burst Mode.

Burst Mode operation has the advantage of lowering overall power consumption because the device goes into power down when conversion is complete and only the output register and output drivers remain powered up to clock out the data. This circuit also powers down and the output drivers go into their high impedance state once the last bit is clocked out.

Note that the output register and output drivers will remain powered up longer if $\overline{CS}$ is not brought high before the 15th fall of SCLK after the fall of $\overline{CS}$. See Figure 3.

TIMING CONSIDERATIONS

Proper operation requires that the fall of $\overline{CS}$ occur between the fall and rise of SCLK. If the fall of $\overline{CS}$ occurs while SCLK is high, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and characteristics of the individual device. To ensure that the data is always clocked out at a time, it is essential that the fall of $\overline{CS}$ always occurs while SCLK is low.

PCB LAYOUT AND CIRCUIT CONSIDERATIONS

Care should be taken with the physical layout of the printed circuit board so that best performance may be realized. This is especially true with a low reference voltage or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out much faster if accuracy is to be maintained.

Any SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Spikes might originate, for example, from switching power supplies, digital logic, and high power devices, and other sources. This type of problem can be very difficult to track down if the glitch is almost synchronous to the converter's SCLK, but the phase difference between SCLK and the noise source may change with time and temperature, causing sporadic problems. Power to the ADC121S625 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor and a 1µF to 10µF capacitor should be used to bypass the ADC121S625 supply, with the 0.1µF capacitor placed as close to the ADC121S625 package as possible. Adding a 10Ω resistor in series with the power supply line will help to low pass filter a noisy supply.

The reference input should be bypassed with a minimum 0.1µF capacitor. A series resistor and large capacitor can be used to low pass filter the reference voltage. If the reference voltage originates from an op-amp, be careful that the op-amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the AD121S625 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference input that must settle out while SCLK is HIGH. Because these transient spikes can be almost as high as 20mA, it is important that the reference circuit be capable of providing this much current and settle out during the minimum 1.5 clock sampling period. Be sure to observe the minimum SCLK HIGH and LOW times.

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The reference input of the ADC121S625, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if the reference voltage is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. While high frequency noise can be filtered out as described above, voltage variation due to supply ripple (50Hz to 120Hz) can be difficult to remove. The use of an active reference source can ease this problem. The LM4040 and LM4050 shunt reference families and the LM4120, LM4121 and LM4140 low dropout series reference families offer a range of choices for a reference source.

The GND pin on the ADC121S625 should be connected to the ground plane at a quiet point. While there are many opinions as to the best way to use power and ground planes, we have looked into this in great detail and have concluded that all methods can work well up to speeds of about 30MHz to 40MHz if there is strict adherence to the individual method. However, many of these methods lead to excessive EMI/RFI, which is not acceptable from a system standpoint. Generally, good layout and interconnect techniques can provide the provide excellent performance required while minimizing EMI/RFI, often without the need for shielding.

We recommend a single ground plane and the use of two or more power planes. The power planes should all be in the same board layer and will define, for example, the analog board area, general digital board area and high power digital board area. Lines associated with these areas should always be routed within their respective areas. There are rules for those cases where a line must cross to another area, but that is beyond the scope of this document.

Avoid connecting the GND pin too close to the ground point for a microprocessor, microcontroller, digital signal processor, or other high power digital device.

APPLICATION CIRCUITS

The following figures are examples of ADC121S625 typical application circuits. These circuits are basic ones and will generally require modification for specific circumstances.

Data Acquisition

Figure 53 shows a basic low cost, low power data acquisition circuit. Maximum clock rate with a minimum sample rate can reduce the power consumption further.

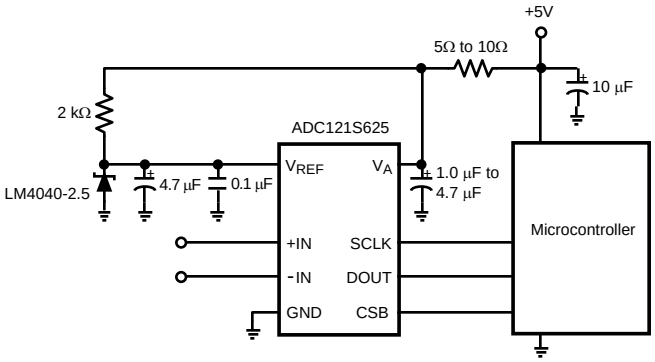


Figure 53. Low cost, low power Data Acquisition System

Motor Control

Figure 54 is a motor control application that isolates the digital outputs of the AD121S625 instead of isolating the analog signal from the motor. As shown here, the reference voltage for the AD121S625 is 150mV, and the analog input of the AD121S625 is connected directly to the current sense resistor. Keeping isolation amplifiers out of the signal path enables a greater system signal-to-noise ratio. However, three optical isolators are needed to isolate the A/D converters rather than an isolation amplifier. For three-phase motors, three of these circuits are needed.

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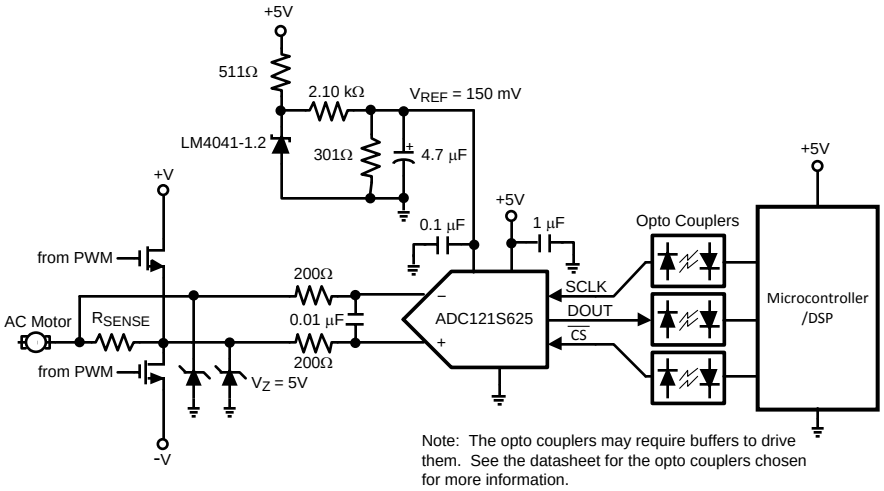


Figure 54. Motor Control using isolated ADC121S625

Strain Gauge Interface

Figure 55 shows an example of interfacing a strain gauge or load cell to the AD121S625. The same voltage used to bias the strain gauge is used as a source for the reference voltage, providing ratiometric operation and making the system immune to variations in the source voltage. Of course, there is no immunity to noise on the reference source or on the strain gauge source. The value of the divider resistors to provide the reference voltage for the ADC121S625 may need to be changed to provide the desired reference voltage for the specific application.

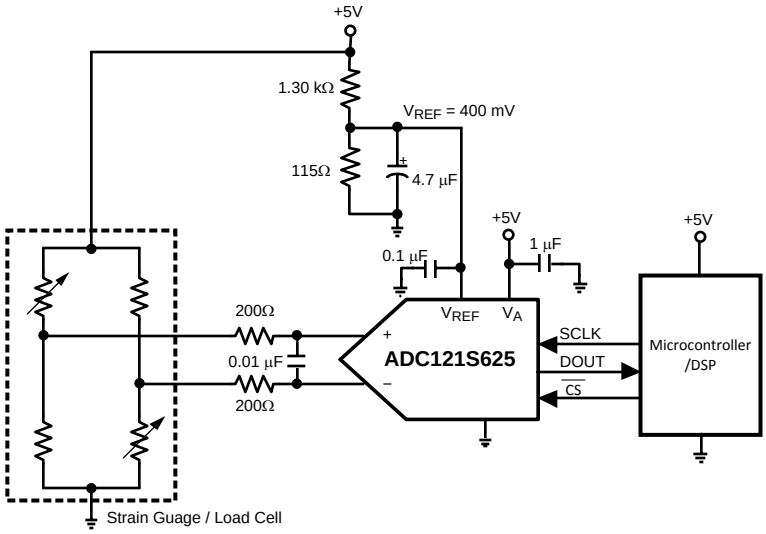


Figure 55. Interfacing the ADC121S625 to a strain gauge

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC121S625CIMM	NRND	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 85	X0AC	
ADC121S625CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X0AC	Samples
ADC121S625CIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X0AC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

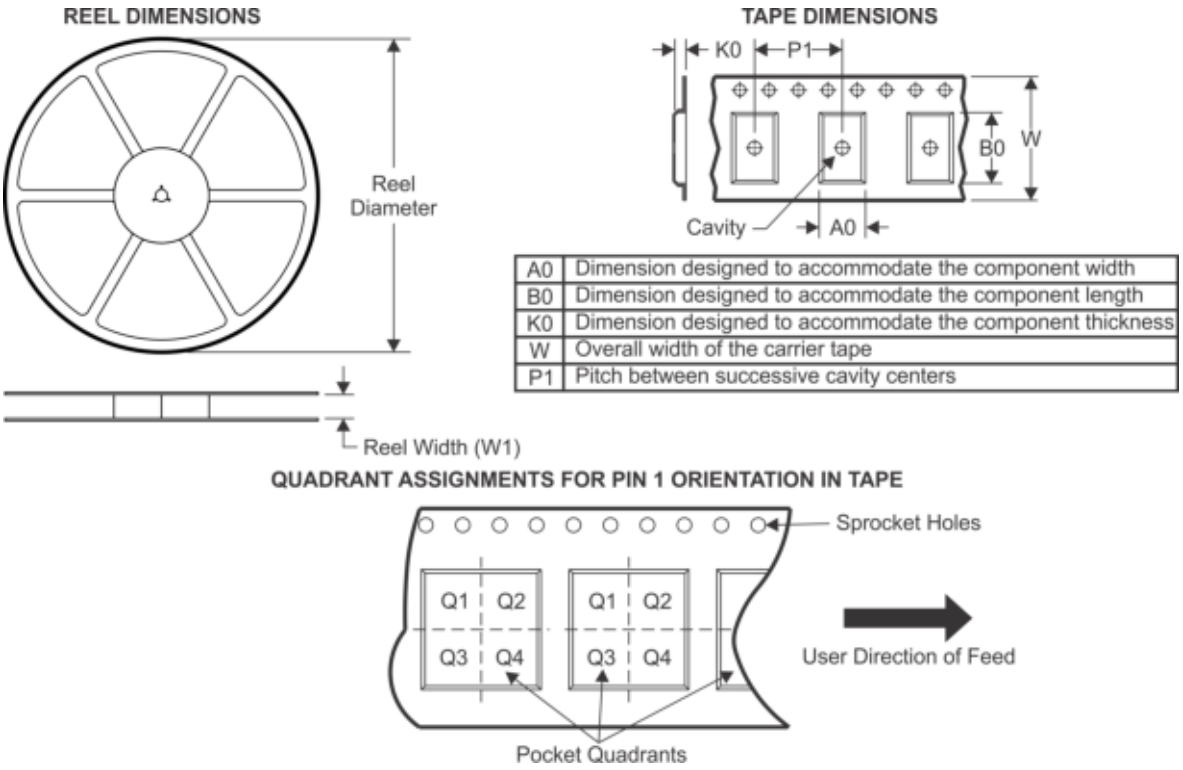
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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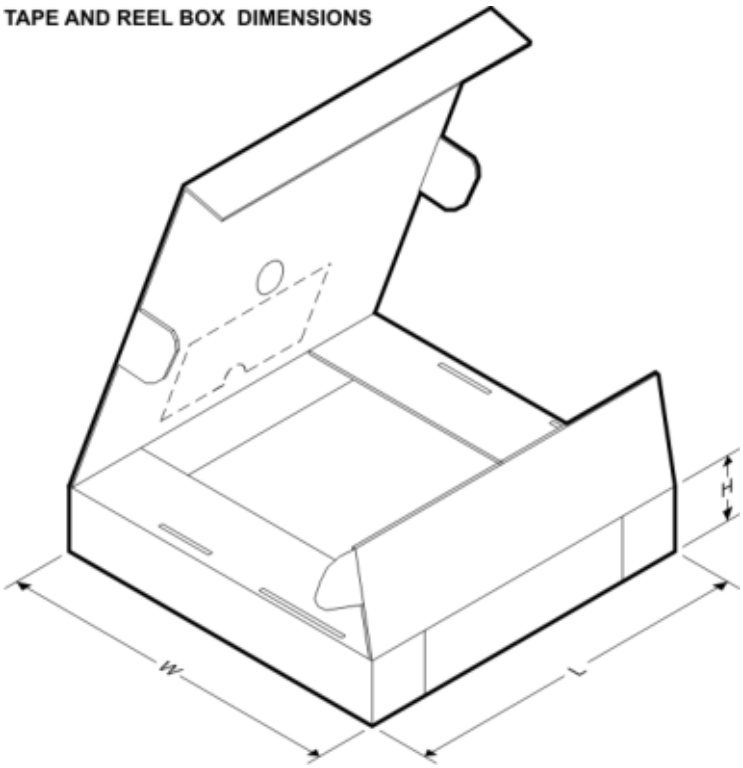


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC121S625CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC121S625CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

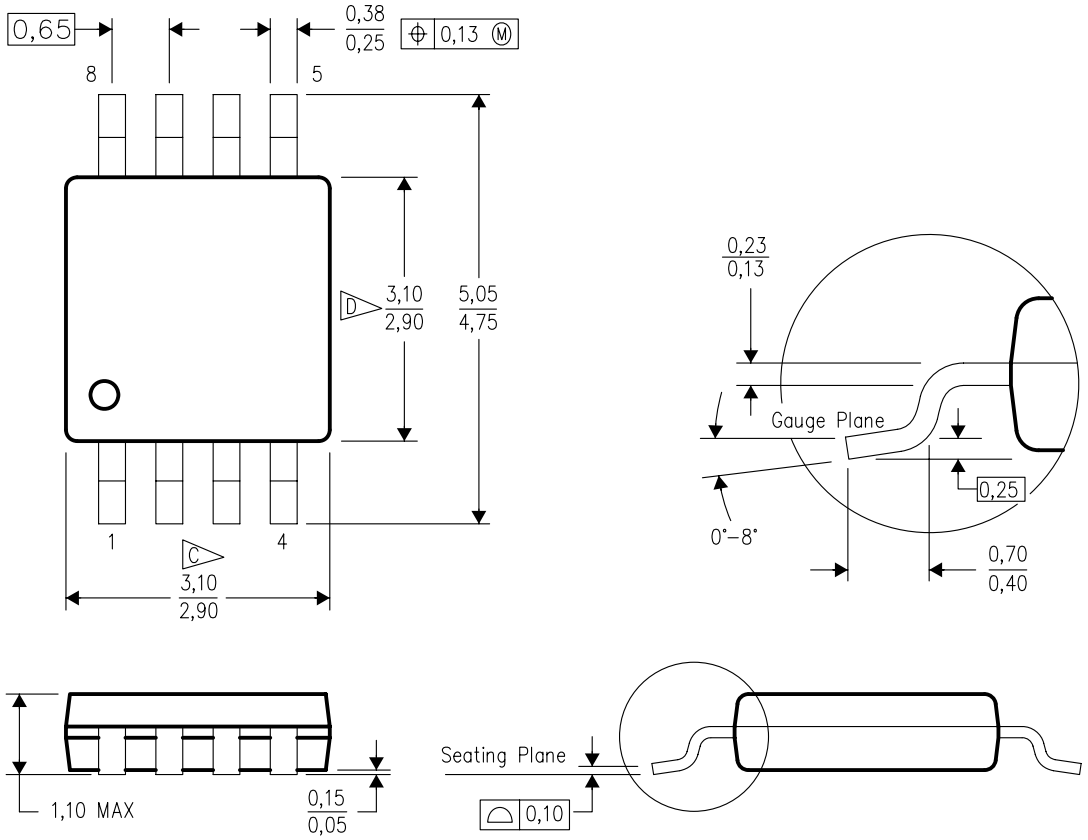
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC121S625CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
ADC121S625CIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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