Energy Metering IC with On-Chip Fault Detection

ADE7760

FEATURES

High accuracy active energy measurement IC, supports IEC 687/61036

Less than 0.1% error over a dynamic range of 500 to 1

Supplies active power on the frequency outputs F1 and F2

High frequency output CF is intended for calibration and supplies instantaneous active power

Continuous monitoring of the phase and neutral current allows fault detection in 2-wire distribution systems

Current channels input level best suited for current transformer sensors

Uses the larger of the two currents (phase or neutral) to bill—even during a fault condition

Two logic outputs (FAULT and REVP) can be used to indicate a potential miswiring or fault condition

Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)

Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time

Reference 2.5 V ± 8% (drift 30 ppm/°C typical) with external overdrive capability

Single 5 V supply, low power

GENERAL DESCRIPTION

The ADE7760 is a high accuracy, fault tolerant, electrical energy measurement IC intended for use with 2-wire distribution systems. The part specifications surpass the accuracy requirements as quoted in the IEC61036 standard.

The only analog circuitry used on the ADE7760 is in the ADCs and reference circuit. All other signal processing (such as multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The ADE7760 incorporates a fault detection scheme similar to the ADE7751 by continuously monitoring both the phase and neutral currents. A fault is indicated when these currents differ by more than 6.25%.

The ADE7760 supplies average active power information on the low frequency outputs F1 and F2. The CF logic output gives instantaneous active power information.

The ADE7760 includes a power supply monitoring circuit on the V_{DD} supply pin. Internal phase-matching circuitry ensures that the voltage and current channels are matched. An internal no-load threshold ensures that the ADE7760 does not exhibit any creep when there is no load.

FUNCTIONAL BLOCK DIAGRAM

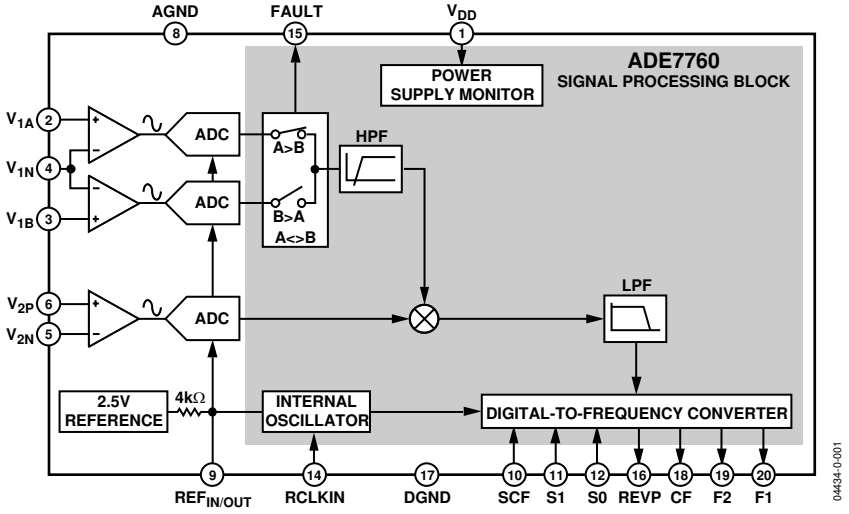


Figure 1.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, on-chip oscillator, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY[1]			
Measurement Error[2]	0.1	% of reading, typ	Over a dynamic range of 500 to 1
Phase Error between Channels			
(PF = 0.8 Capacitive)	±0.05	Degrees, max	Phase lead 37°
(PF = 0.5 Inductive)	±0.05	Degrees, max	Phase lag 60°
AC Power Supply Rejection[2]			
Output Frequency Variation	0.01	%, typ	$V_{1A} = V_{1B} = V_{2P}$ = ±100 mV rms
DC Power Supply Rejection[2]			
Output Frequency Variation	0.01	%, typ	$V_{1A} = V_{1B} = V_{2P}$ = ±100 mV rms
FAULT DETECTION[2, 3]			See the Fault Detection section
Fault Detection Threshold			
Inactive Input <> Active Input	6.25	%, typ	(V_{1A} or V_{1B} active)
Input Swap Threshold			
Inactive Input <> Active Input	6.25	% of larger, typ	(V_{1A} or V_{1B} active)
Accuracy Fault Mode Operation			
V_{1A} Active, V_{1B} = AGND	0.1	% of reading, typ	Over a dynamic range of 500 to 1
V_{1B} Active, V_{1A} = AGND	0.1	% of reading, typ	Over a dynamic range of 500 to 1
Fault Detection Delay	3	Seconds, typ	
Swap Delay	3	Seconds, typ	
ANALOG INPUTS			$V_{1A} – V_{1N}$, $V_{1B} – V_{1N}$, $V_{2P} – V_{2N}$
Maximum Signal Levels	±660	mV peak, max	Differential input
Input Impedance (DC)	400	kΩ, min	
Bandwidth (–3 dB)	7	kHz, typ	
ADC Offset Error[2]	10	mV, max	Uncalibrated error, see the Terminology section for details
Gain Error	±4	%, typ	External 2.5 V reference
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V, max	2.5 V + 8%
	2.3	V, min	2.5 V – 8%
Input Impedance	4	kΩ, min	
Input Capacitance	10	pF, max	
ON-CHIP REFERENCE			
Reference Error	±200	mV, max	
Temperature Coefficient	30	ppm/°C, typ	
Current Source	20	µA, min	
ON-CHIP OSCILLATOR			
Oscillator Frequency	450	kHz	
Oscillator Frequency Tolerance	±12	% of reading, typ	
Temperature Coefficient	30	ppm/°C, typ	
LOGIC INPUTS[4]			
SCF, S1, and S0			
Input High Voltage, V_{INH}	2.4	V, min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V, max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	µA, max	Typical 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF, max	

Parameter	Value	Unit	Test Conditions/Comments
LOGIC OUTPUTS[4]			
CF, REVP, and FAULT			
Output High Voltage, V_{OH}	4	V, min	V_{DD} = 5 V ± 5%
Output Low Voltage, V_{OH}	1	V, max	V_{DD} = 5 V ± 5%
F1 and F2			
Output High Voltage, V_{OH}	4	V, min	V_{DD} = 5 V ± 5%, I_{source} = 10 mA
Output Low Voltage, V_{OH}	1	V, max	V_{DD} = 5 V ± 5%, I_{sink} = 10 mA
POWER SUPPLY			For specified performance
V_{DD}	4.75	V, min	5 V – 5%
	5.25	V, max	5 V + 5%
V_{DD}	4	mA, max	

[1] See plots in the Typical Performance Characteristics section.
[2] See the Terminology section for explanation of specifications.
[3] See the Fault Detection section for explanation of fault detection functionality.
[4] Sample tested during initial release and after any redesign or process change that may affect this parameter.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, on-chip oscillator, T_{MIN} to T_{MAX} = −40°C to +85°C.
Sample tested during initial release and after any redesign or process change that may affect this parameter.
See Figure 2.

Table 2.

Parameter	Value	Unit	Test Conditions/Comments
t_1[1]	120	ms	F1 and F2 Pulse Width (Logic High).
t_2	See Table 6	s	Output Pulse Period. See the Transfer Function section.
t_3	1/2 t_2	s	Time between F1 Falling Edge and F2 Falling Edge.
t_4[1]	90	ms	CF Pulse Width (Logic High).
t_5	See Table 7	s	CF Pulse Period. See the Transfer Function section.
t_6	CLKIN/4	s	Minimum Time between F1 and F2 Pulse.

[1] The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See the Transfer Function section.

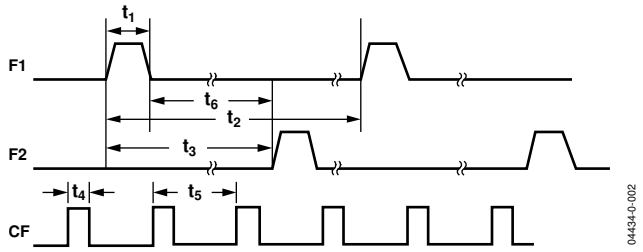


Figure 2. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
Analog Input Voltage to AGND V_{1AP}, V_{1BP}, V_{1N}, V_{2N}, V_{2P}	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
20-Lead SSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7760 is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ registered\ by\ ADE7760 - True\ Energy}{True\ Energy} \times 100\% \right)$$

Phase Error between Channels
The high-pass filter (HPF) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range 40 Hz to 1 kHz.

Power Supply Rejection
This quantifies the ADE7760 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac (175 mV rms/100 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition above).

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see a dc analog input signal. The magnitude of the offset depends on the input range selection (see the Typical Performance Characteristics section). However, when HPFs are switched on, the offset is removed from the current channels and the power calculation is not affected by this offset.

Gain Error
The gain error in the ADE7760 ADCs is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the transfer function (see the Transfer Function section).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

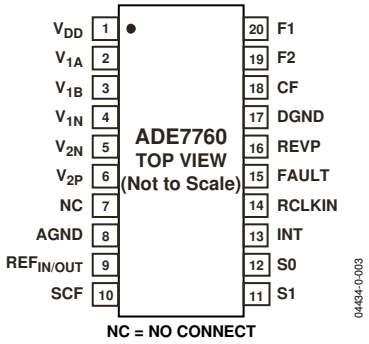


Figure 3. Pin Configuration (SSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7760. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2, 3	V_{1A}, V_{1B}	Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with maximum differential input signal levels of ±660 mV with respect to V_{1N} for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage.
4	V_{1N}	Negative Input Pin for Differential Voltage Inputs V_{1A} and V_{1B}. The maximum signal level at this pin is ±1 V with respect to AGND. The input has internal ESD protection circuitry, and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage. The input should be directly connected to the burden resistor and held at a fixed potential, that is, AGND. See the Analog Inputs section.
5	V_{2N}	Negative Input Pin for Differential Voltage Input V_{2P}. The maximum signal level at this pin is ±1 V with respect to AGND. The input has internal ESD protection circuitry, and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage. The input should be held at a fixed potential, that is, AGND. See the Analog Inputs section.
6	V_{2P}	Analog Inputs for Channel 2 (Voltage Channel). This input is fully differential voltage input with maximum differential input signal levels of ±660 mV with respect to V_{2N} for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. This input has internal ESD protection circuitry, and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage.
7	NC	Not Connected. Nothing should be connected to this pin.
8	AGND	This pin provides the ground reference for the analog circuitry in the ADE7760, that is, ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry such as antialiasing filters, and current and voltage transducers. For good noise suppression, the analog ground plane should be connected only to the digital ground plane at the DGND pin.
9	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor and 100 nF ceramic capacitor.
10	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table 6 shows how the calibration frequencies are selected.
11, 12	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See the Selecting a Frequency for an Energy Meter Application section.
13	INT	This pin is internally used and should be connected to DGND.
14	RCLKIN	To enable the internal oscillator as a clock source on the chip, a precise low temperature drift resistor at nominal value of 6.2 kΩ must be connected from this pin to DGND.

Pin No.	Mnemonic	Description
15	FAULT	This logic output goes active high when a fault condition occurs. A fault is defined as a condition under which the signals on V_{1A} and V_{1B} differ by more than 6.25%. The logic output is reset to zero when a fault condition is no longer detected. See the Fault Detection section.
16	REVP	This logic output goes logic high when negative power is detected, that is, when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and is reset when positive power is once again detected. The output goes high or low at the same time as a pulse is issued on CF.
17	DGND	This pin provides the ground reference for the digital circuitry in the ADE7760, that is, multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry such as counters (mechanical and digital), MCUs, and indicator LEDs. For good noise suppression, the analog ground plane should be connected only to the digital ground plane at the DGND pin.
18	CF	Calibration Frequency Logic Output. The CF logic output, active high, gives instantaneous active power information. This output is intended to be used for operational and calibration purposes. See the Digital-to-Frequency Conversion section.
19, 20	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average active power information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors.

TYPICAL PERFORMANCE CHARACTERISTICS

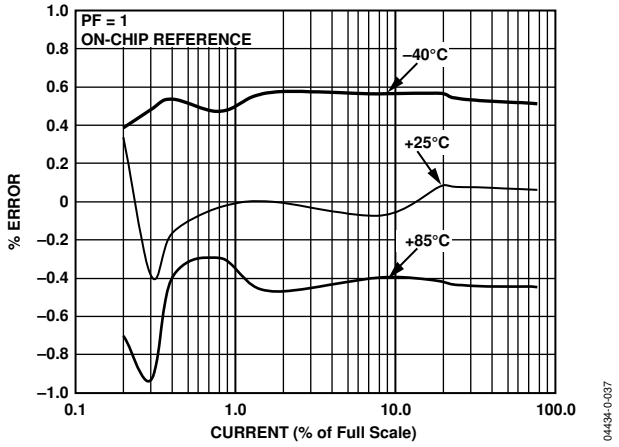


Figure 4. Active Power Error as a Percentage of Reading with Internal Reference

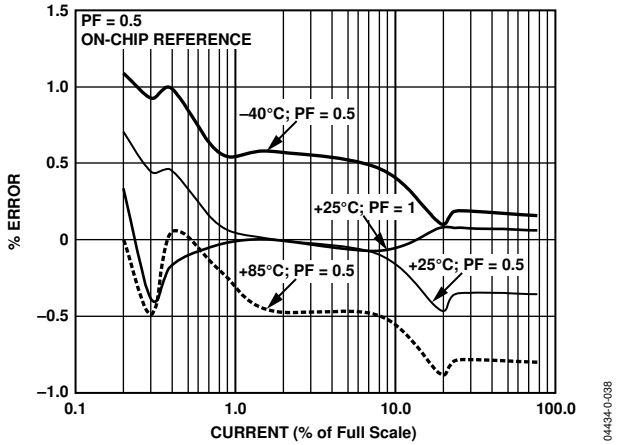


Figure 5. Active Power Error as a Percentage of Reading over Power Factor with Internal Reference

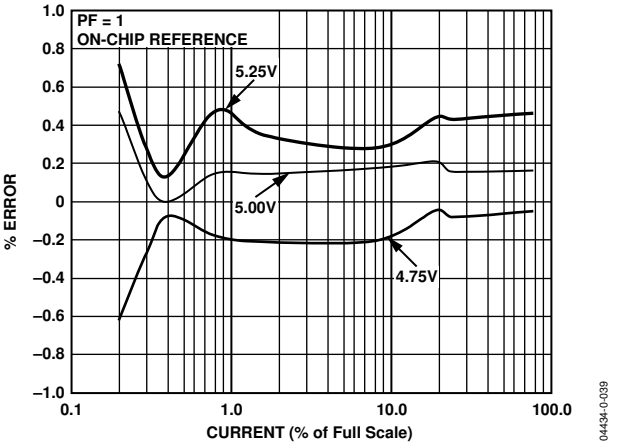


Figure 6. Active Power Error as a Percentage of Reading over Power Supply with Internal Reference

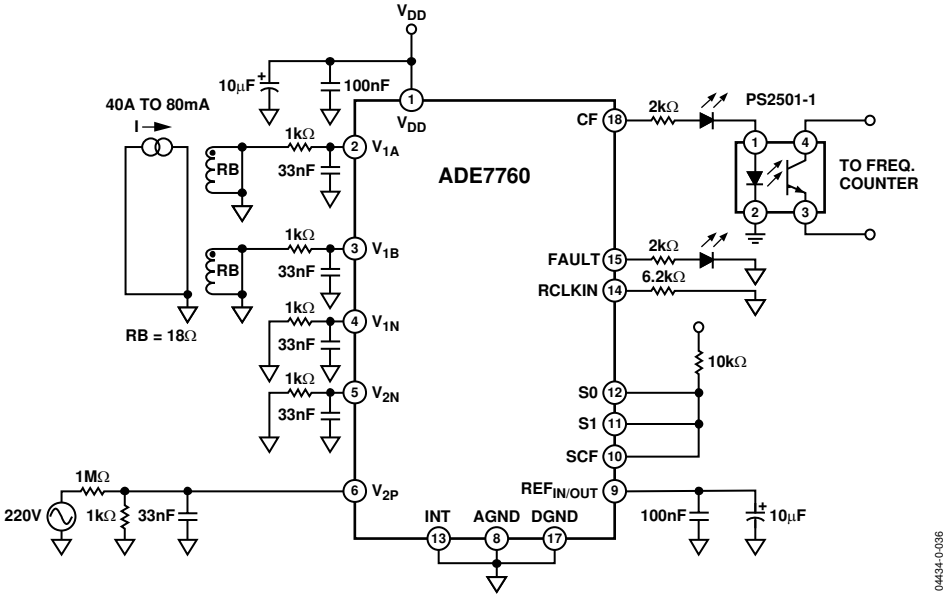


Figure 7. Test Circuit for Performances Curves

OPERATION

POWER SUPPLY MONITOR

The ADE7760 contains an on-chip power supply monitor. The power supply (V_{DD}) is continuously monitored by the ADE7760. If the supply is less than 4 V ± 5%, the ADE7760 goes into an inactive state, that is, no energy is accumulated and the CF, F1, and F2 outputs is disabled. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed 5 V ± 5% as specified for normal operation.

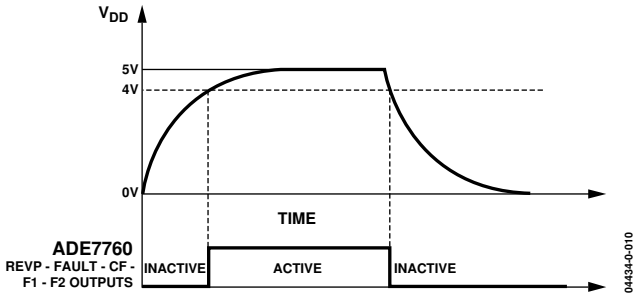


Figure 8. On-Chip Power Supply Monitoring

ANALOG INPUTS

Channel V1 (Current Channel)

The voltage outputs from the current transducers are connected to the ADE7760 here. Channel V1 has two voltage inputs, V_{1A} and V_{1B}. These inputs are fully differential with respect to V_{1N}. However, at any one time, only one is selected to perform the power calculation (see the Fault Detection section).

The maximum peak differential signal on V_{1A}–V_{1N} and V_{1B}–V_{1N} is ±660 mV. Figure 9 shows the maximum signal levels on V_{1A}, V_{1B}, and V_{1N}. The differential voltage signal on the inputs must be referenced to a common mode such as AGND.

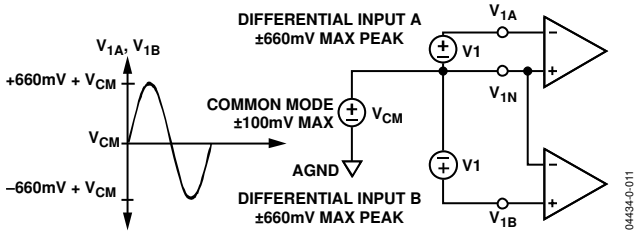


Figure 9. Maximum Signal Levels, Channel 1

Channel V2 (Voltage Channel)

The output of the line voltage transducer is connected to the ADE7760 at this analog input. Channel V2 is a single-ended voltage input. The maximum peak differential signal on Channel 2 is ±660 mV with respect to V_{2N}. Figure 10 shows the maximum signal levels that can be connected to Channel 2.

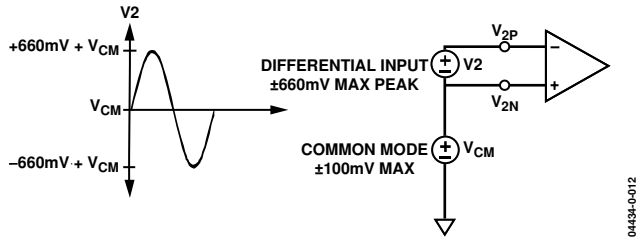


Figure 10. Maximum Signal Levels, Channel 2

The differential voltage V_{2P}–V_{2N} must be referenced to a common mode (usually AGND). The analog inputs of the ADE7760 can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, the best results are achieved using a common mode equal to AGND.

Typical Connection Diagrams

Figure 11 shows a typical connection diagram for Channel V1. The analog inputs are being used to monitor both the phase and neutral currents. Because of the large potential difference between the phase and neutral, two current transformers (CTs) must be used to provide the isolation. Note that both CTs are referenced to AGND (analog ground); the common-mode voltage is, therefore, 0 V. The CT turns ratio and burden resistor (RB) are selected to give a peak differential voltage of ±660 mV.

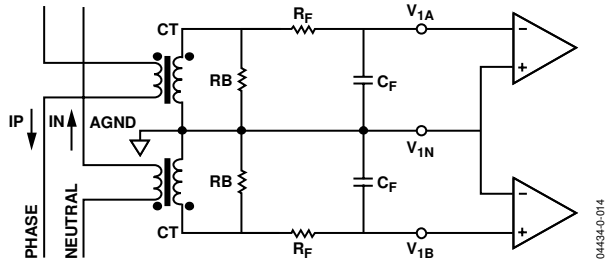


Figure 11. Typical Connection for Channel 1

Figure 12 shows two typical connections for Channel V2. The first option uses a potential transformer (PT) to provide complete isolation from the main voltage. In the second option, the ADE7760 is biased around the neutral wire, and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of RA and RB + VR is a convenient way of carrying out a gain calibration on the meter.

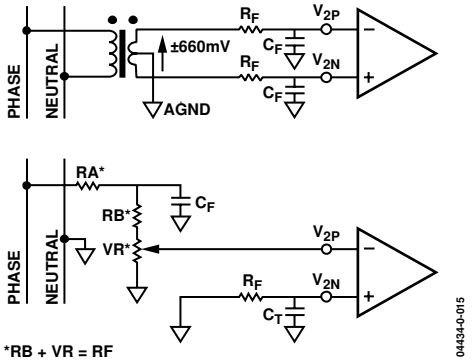


Figure 12. Typical Connection for Channel 2

INTERNAL OSCILLATOR

The nominal internal oscillator frequency is 450 kHz when used with the recommended R_{OSC} resistor value of 6.2 kΩ between RCLKIN and DGND (see Figure 13).

The internal oscillator frequency is inversely proportional to the value of this resistor. Although the internal oscillator operates when used with a R_{OSC} resistor value between 5 kΩ and 12 kΩ, it is recommended to choose a value within the range of the nominal value.

The output frequencies on CF, F1, and F2 are directly proportional to the internal oscillator frequency; thus, the resistor R_{OSC} must have a low tolerance and low temperature drift. A low tolerance resistor limits the variation of the internal oscillator frequency. Small variation of the clock frequency and consequently of the output frequencies from meter to meter contributes to a smaller calibration range of the meter. A low temperature drift resistor directly limits the variation of the internal clock frequency over temperature. The stability of the meter to external variation is then better ensured by design.

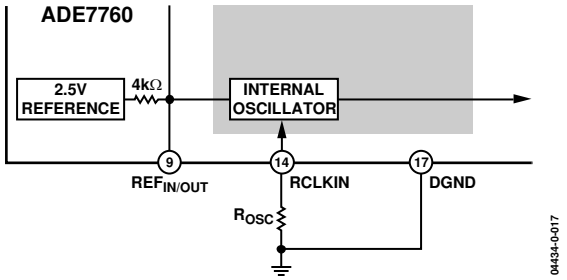


Figure 13. ADE7760 Internal Oscillator Connection

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7760 is carried out using second-order Σ-Δ ADCs. Figure 14 shows a first-order (for simplicity) Σ-Δ ADC. The converter is made up of two parts, the Σ-Δ modulator and the digital low-pass filter.

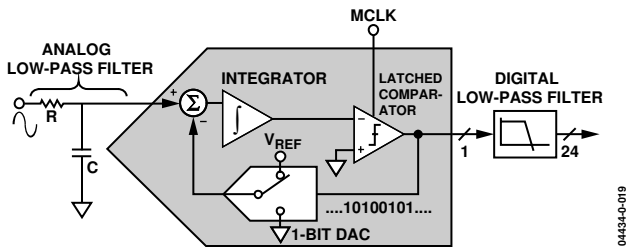


Figure 14. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7760, the sampling clock is equal to CLKIN. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) approaches that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling, which means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7760 is CLKIN (450 kHz) and the band of interest is 40 Hz to 1 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered (see Figure 15).

However, oversampling alone is not an efficient enough method to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. This is what happens in the Σ-Δ modulator; the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is also shown in Figure 15.

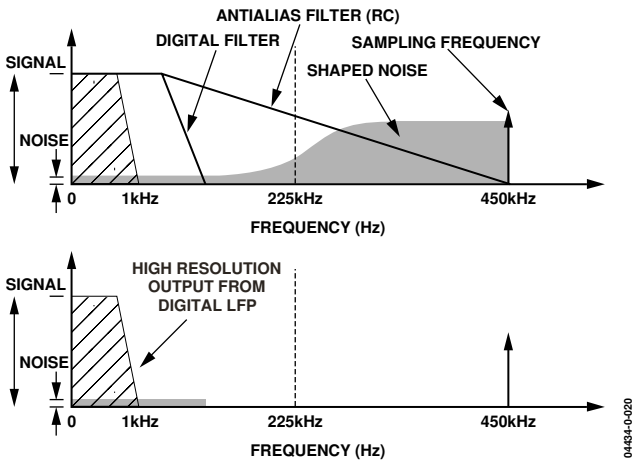


Figure 15. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialias Filter

Figure 15 also shows an analog low-pass filter (RC) on input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems, which means that frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC appear in the sampled signal frequency below half the sampling rate. Figure 16 illustrates the effect.

In Figure 16, frequency components (arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency), that is, 225 kHz get imaged or folded back down below 225 kHz (arrows shown in gray). This happens with all ADCs no matter what the architecture. In the example shown, it can be seen that only frequencies near the sampling frequency (450 kHz) move into the band of interest for metering (40 Hz to 1 kHz). This fact allows the use of a very simple low-pass filter to attenuate these frequencies (near 250 kHz) and thereby prevent distortion in the band of interest. A simple RC filter (single pole) with a corner frequency of 10 kHz produces an attenuation of approximately 33 dB at 450 kHz (see Figure 16). This is sufficient to eliminate the effects of aliasing.

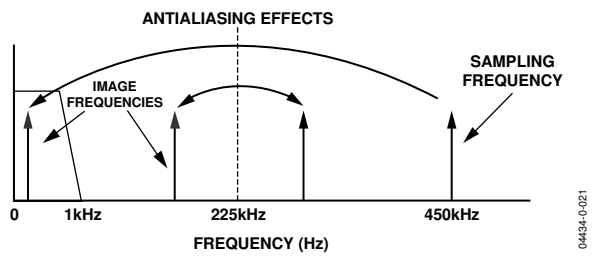


Figure 16. ADC and Signal Processing in Current Channel or Voltage Channel

ACTIVE POWER CALCULATION

The ADCs digitize the voltage signals from the current and voltage transducers. A high-pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the active power calculation due to offsets in the voltage or current signals (see the HPF and Offset Effects section).

The active power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. To extract the active power component (dc component), the instantaneous power signal is low-pass filtered. Figure 17 illustrates the instantaneous active power signal and shows how the active power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates active power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

The low frequency output of the ADE7760 is generated by accumulating this active power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is, therefore, proportional to the average active power. This average active power information can in turn be accumulated (for example, by a counter) to generate active energy information. Because of its high output frequency and therefore shorter integration time, the CF output is proportional to the instantaneous active power. This is useful for system calibration purposes that would take place under steady load conditions.

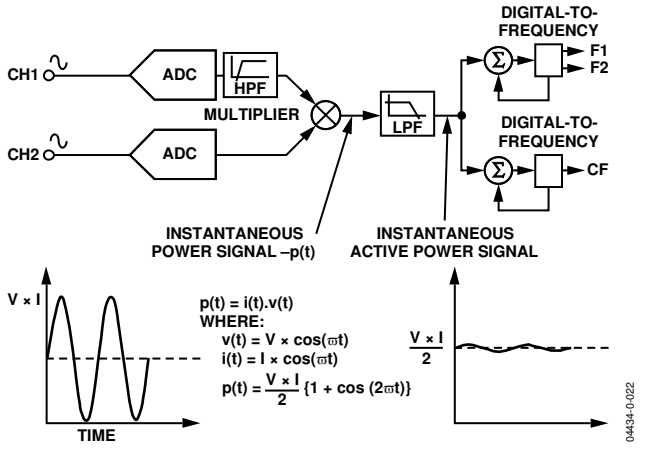


Figure 17. Signal Processing Block Diagram

Power Factor Considerations

The method used to extract the active power information from the instantaneous power signal (by low-pass filtering) is still valid even when the voltage and current signals are not in phase. Figure 18 displays the unity power factor condition and a displacement power factor (DPF = 0.5), that is, current signal lagging the voltage by 60°. If one assumes the voltage and current waveforms are sinusoidal, the active power component of the instantaneous power signal (dc term) is given by (V × I/2) × cos(60°). This is the correct active power calculation.

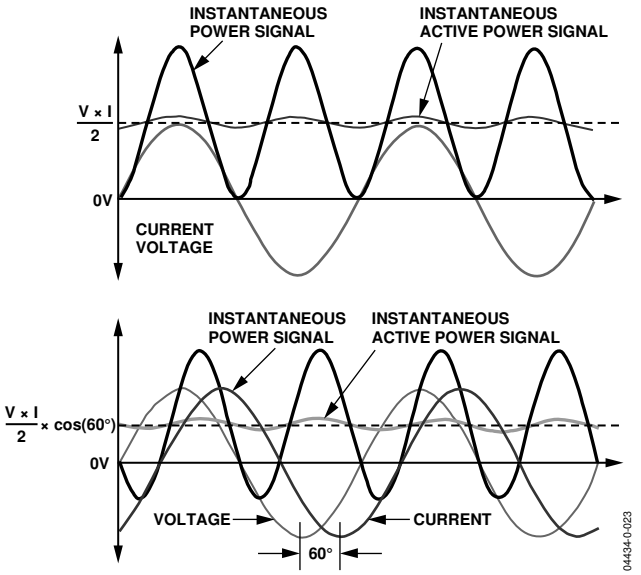


Figure 18. Active Power Calculation over PF

Nonsinusoidal Voltage and Current

The active power calculation method also holds true for nonsinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications have some harmonic content. Using the Fourier transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content:

$$V(t) = V_o + \sqrt{2} \times \sum_{h \neq 0}^{\infty} V_h \times \sin(h\omega t + \alpha_h) \quad (1)$$

where:

$v(t)$ is the instantaneous voltage.
V_h is the rms value of voltage harmonic h.
α_h is the phase angle of the voltage harmonic.

$$i(t) = I_o + \sqrt{2} \times \sum_{h \neq 0}^{\infty} I_h \times \sin(h\omega t + \beta_h) \quad (2)$$

where:

$i(t)$ is the instantaneous current.
I_O is the dc component.
I_h is the rms value of current harmonic h.
β_h is the phase angle of the current harmonic.

Using Equations 1 and 2, the active power P can be expressed in terms of its fundamental active power (P_1) and harmonic active power (P_H):

$$P = P_1 + P_H$$

where:

$$P_1 = V_1 \times I_1 \cos(\Phi_1)$$
$$\Phi_1 = \alpha_1 - \beta_1 \quad (3)$$

and

$$P_H = \sum_{h=2}^{\infty} V_h \times I_h \times \cos(\Phi_h)$$
$$\Phi_h = \alpha_h - \beta_h \quad (4)$$

As can be seen from Equation 4, a harmonic active power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has previously been shown to be accurate in the case of a pure sinusoid; therefore, the harmonic active power must also correctly account for power factor, because it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 7 kHz with the internal oscillator frequency of 450 kHz.

HPF and Offset Effects

Equation 5 shows the effect of offset on the active power calculation. Figure 19 shows the effect of offsets on the active power calculation in the frequency domain.

$$V(t) \times I(t) =$$
$$(V_0 + V_1 \times \cos(\omega t)) \times (I_0 + I_1 \times \cos(\omega t)) = \quad (5)$$
$$V_0 \times I_1 + \frac{V_1 \times I_1}{2} + V_0 \times I_1 \times \cos(\omega t) + V_1 \times I_0 \times \cos(\omega t)$$

As can be seen from Equation 5 and Figure 19, an offset on Channel 1 and Channel 2 contributes a dc component after multiplication. Because this dc component is extracted by the LPF and used to generate the active power information, the offsets contribute a constant error to the active power calculation. This problem is easily avoided in the ADE7760 with the HPF in Channel 1. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion (see the Digital-to-Frequency Conversion section).

The HPF in Channel 1 has an associated phase response that is compensated for on-chip. Figure 20 and Figure 21 show the phase error between channels with the compensation network activated. The ADE7760 is phase compensated up to 1 kHz as shown, which ensures correct active harmonic power calculation even at low power factors.

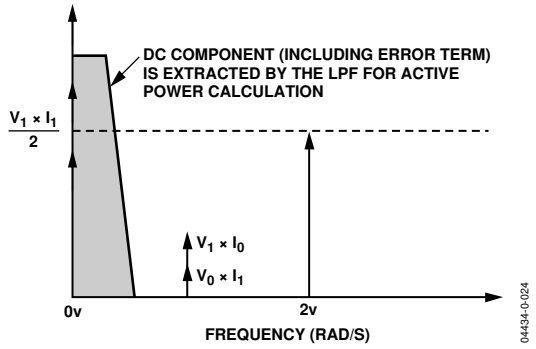


Figure 19. Effect of Channel Offsets on the Active Power Calculation

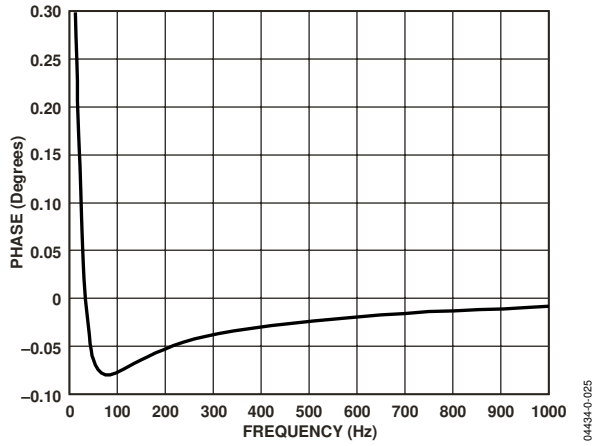


Figure 20. Phase Error between Channels (0 Hz to 1 kHz)

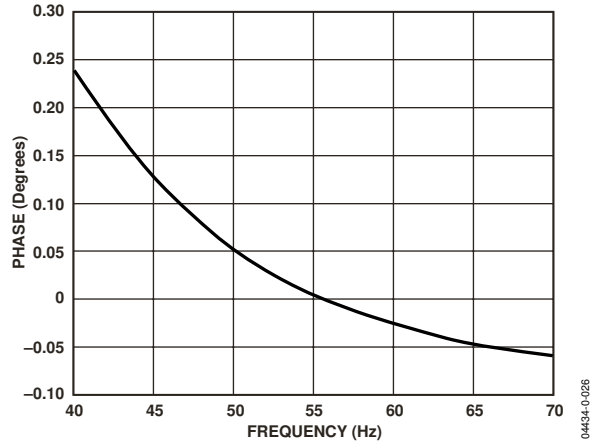


Figure 21. Phase Error between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

As previously described, the digital output of the low-pass filter after multiplication contains the active power information. However, because this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, that is, cos(*hωt*), where *h* = 1, 2, 3, ..., and so on. The magnitude response of the filter is given by

$$\left|H(f)\right| = \frac{1}{\sqrt{1 = (f / 4.5\,\text{Hz})^2}} \qquad (6)$$

For a line frequency of 50 Hz, this gives an attenuation of the 2ω (100 Hz) component of approximately –26.9 dB. The dominating harmonic is at twice the line frequency, that is, cos(2ω*t*), due to the instantaneous power signal.

Figure 22 shows the instantaneous active power signal output of the LPF, which still contains a significant amount of instantaneous power information, cos(2ω*t*). This signal is then passed to the digital-to-frequency converter, where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal suppresses or averages out any non-dc components in the instantaneous active power signal. The average value of a sinusoidal signal is zero. Therefore, the frequency generated by the ADE7760 is proportional to the average active power.

Figure 22 also shows the digital-to-frequency conversion for steady load conditions: constant voltage and current. As can be seen in Figure 22, the frequency output CF varies over time, even under steady load conditions. This frequency variation is primarily due to the cos(2ω*t*) component in the instantaneous active power signal.

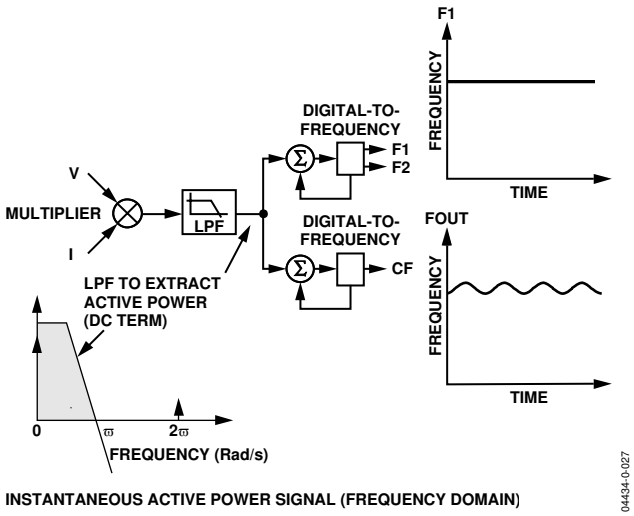


Figure 22. Active Power to Frequency Conversion

The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous active power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. As a consequence, some of this instantaneous power signal passes through the digital-to-frequency conversion. This is not a problem in the application. Where CF is used for calibration purposes, the frequency should be averaged by the frequency counter, which removes any ripple. If CF is being used to measure energy, such as in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs F1 and F2 operate at a much lower frequency, a lot more averaging of the instantaneous active power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7760 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract active power information. This active power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active high pulses. The pulse rate at these outputs is relatively low, for example, 0.34 Hz maximum for ac signals with S0 = S1 = 0 (see Table 7). This means that the frequency at these outputs is generated from active power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average active power. The averaging of the active power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$F_1 - F_2\ Frequency = \frac{5.70 \times V1_{rms} \times V2_{rms} \times F_{1-4}}{V_{REF}{}^2} \quad (7)$$

where:

$F_1 - F_2\ Frequency$ is the output frequency on F1 and F2 (Hz).
$V1_{rms}$ is the differential rms voltage signal on Channel 1 (V).
$V2_{rms}$ is the differential rms voltage signal on Channel 2 (V).
V_{REF} is the reference voltage (2.5 V ± 8%) (V).
F_{1-4} is one of four possible frequencies selected by using the logic inputs S0 and S1 (see Table 5).

Table 5. F_{1-4} Frequency Solution

S1	S0	F_{1-4} (Hz)[1]	OSC/CLKIN[2]
0	0	1.72	OSC/2^{18}
0	1	3.44	OSC/2^{17}
1	0	6.86	OSC/2^{16}
1	1	13.7	OSC/2^{15}

[1] Values are generated using the nominal frequency of 450 kHz.
[2] F_{1-4} are a binary fraction of the master clock and, therefore, varies, if the internal oscillator frequency (OSC).

Frequency Output CF

The pulse output calibration frequency (CF) is intended for use during calibration. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the F_{1-4} frequency selected, the higher the CF scaling. Table 6 shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous active power. As with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this active power information is accumulated over a much shorter time. Therefore, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the active power signal, the CF output is much more responsive to power fluctuations (see Figure 17).

Table 6. Relationship between CF and F1, F2 Frequency Outputs

SCF	S1	S0	F_{1-4} (Hz)	CF Frequency Output
1	0	0	1.72	128 × F1, F2
0	0	0	1.72	64 × F1, F2
1	0	1	3.44	64 × F1, F2
0	0	1	3.44	32 × F1, F2
1	1	0	6.86	32 × F1, F2
0	1	0	6.86	16 × F1, F2
1	1	1	13.7	16 × F1, F2
0	1	1	13.7	2048 × F1, F2

Example

In this example, if ac voltages of ±660 mV peak are applied to V1 and V2, then the expected output frequency on CF, F1, and F2 is calculated as follows:

F_{1-4} = 1.7 Hz, $SCF = S1 = S0 = 0$

$V1_{rms}$ = rms of 660 mV peak ac = 0.66/$\sqrt{2}$ V

$V2_{rms}$ = rms of 660 mV peak ac = 0.66/$\sqrt{2}$ V

V_{REF} = 2.5 V (nominal reference value)

Note that if the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$F_1 - F_2\ Frequency = \frac{5.70 \times 0.66 \times 0.66 \times 1.72\,\text{Hz}}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.34\,\text{Hz}$$

$$CF\ Frequency = F_1 - F_2 \times 64 = 22.0\ \text{Hz}$$

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half of that for dc input signals. Table 7 shows a complete listing of all maximum output frequencies for ac signals.

Table 7. Maximum Output Frequency on CF, F1, and F2 for AC Inputs

SCF	S1	S0	F1, F2 Maximum Frequency (Hz)	CF Maximum Frequency (Hz)	CF to F1 Ratio
1	0	0	0.34	43.52	128
0	0	0	0.34	21.76	64
1	0	1	0.68	43.52	64
0	0	1	0.68	21.76	32
1	1	0	1.36	43.52	32
0	1	0	1.36	21.76	16
1	1	1	2.72	43.52	16
0	1	1	2.72	5570	2048

FAULT DETECTION

The ADE7760 incorporates a novel fault detection scheme that warns of fault conditions and allows the ADE7760 to continue accurate billing during a fault event. The ADE7760 does this by continuously monitoring both the phase and neutral (return) currents. A fault is indicated when these currents differ by more than 6.25%. However, even during a fault, the output pulse rate on F1 and F2 is generated using the larger of the two currents. Because the ADE7760 looks for a difference between the voltage signals on V_{1A} and V_{1B}, it is important that both current transducers be closely matched.

On power-up, the output pulse rate of the ADE7760 is proportional to the product of the voltage signals on V_{1A} and Channel 2. If there is a difference of greater than 6.25% between V_{1A} and V_{1B} on power-up, the fault indicator (FAULT) becomes active after about 1 s. In addition, if V_{1B} is greater than V_{1A}, the ADE7760 selects V_{1B} as the input. The fault detection is automatically disabled when the voltage signal on Channel 1 is less than 0.3% of the full-scale input range. This eliminates false detection of a fault due to noise at light loads.

Fault with Active Input Greater than Inactive Input

If V_{1A} is the active current input (that is, is being used for billing), and the voltage signal on V_{1B} (inactive input) falls below 93.75% of V_{1A}, the fault indicator becomes active. Both analog inputs are filtered and averaged to prevent false triggering of this logic output.

As a consequence of the filtering, there is a time delay of approximately 3 s on the logic output FAULT after the fault event. The FAULT logic output is independent of any activity on outputs F1 or F2. Figure 23 shows one condition under which FAULT becomes active. Because V_{1A} is the active input and it is still greater than V_{1B}, billing is maintained on V_{1A}, that is, no swap to the V_{1B} input occurs. V_{1A} remains the active input.

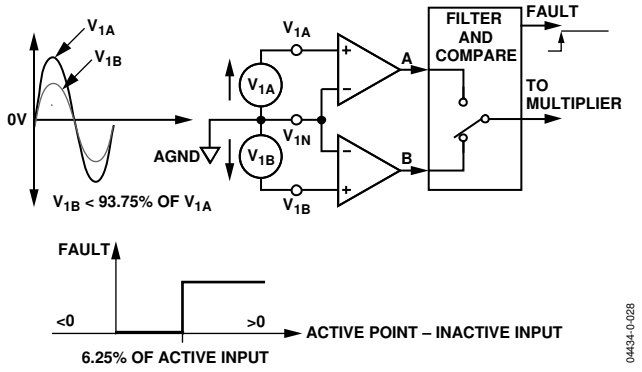


Figure 23. Fault Conditions for Active Input Greater than Inactive Input

Fault with Inactive Input Greater than Active Input

Figure 24 illustrates another fault condition. If the difference between V_{1B}, the inactive input, and V_{1A}, the active input (used for billing), becomes greater than 6.25% of V_{1B}, the FAULT indicator goes active, and there is also a swap over to the V_{1B} input. The analog input V_{1B} becomes the active input. Again, there is a time constant of about 3 s associated with this swap. V_{1A} does not swap back to being the active channel until V_{1A} is greater than V_{1B} and the difference between V_{1A} and V_{1B}—in this order—becomes greater than 6.25% of V_{1A}. The FAULT indicator, however, becomes inactive as soon as V_{1A} is within 6.25% of V_{1B}. This threshold eliminates potential chatter between V_{1A} and V_{1B}.

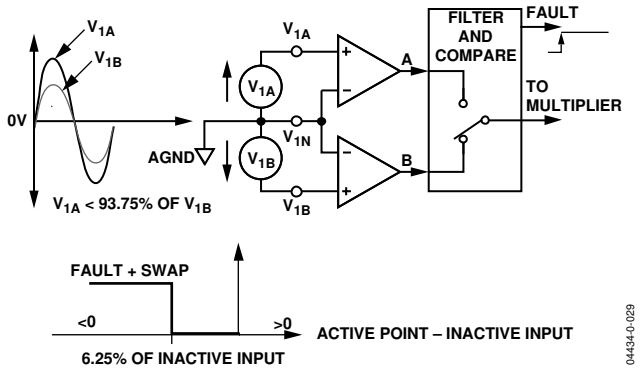


Figure 24. Fault Conditions for Inactive Input Greater than Active Input

Calibration Concerns

Typically, when a meter is being calibrated, the voltage and current circuits are separated as shown in Figure 25. This means that current passes through only the phase or neutral circuit. Figure 25 shows current being passed through the phase circuit. This is the preferred option, because the ADE7760 starts billing on the input V_{1A} on power-up. The phase circuit CT is connected to V_{1A} in the diagram. Because there is no current in the neutral circuit, the FAULT indicator comes on under these conditions. However, this does not affect the accuracy of the calibration and can be used as a means to test the functionality of the fault detection.

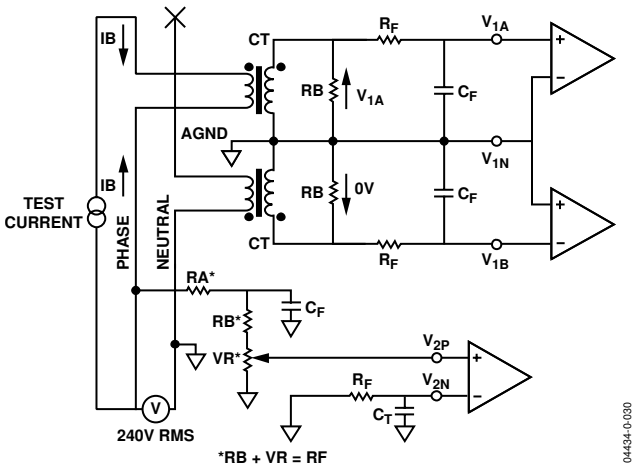


Figure 25. Fault Conditions for Inactive Input Greater than Active Input

If the neutral circuit is chosen for the current circuit in the arrangement shown in Figure 25, this may have implications for the calibration accuracy. The ADE7760 powers up with the V_{1A} input active as normal. However, because there is no current in the phase circuit, the signal on V_{1A} is zero. This causes a fault to be flagged and the active input to be swapped to V_{1B} (neutral). The meter can be calibrated in this mode, but the phase and neutral CTs might differ slightly. Because under no-fault conditions all billing is carried out using the phase CT, the meter should be calibrated using the phase circuit. Of course, both phase and neutral circuits can be calibrated.

APPLICATIONS

INTERFACING TO A MICROCONTROLLER FOR ENERGY MEASUREMENT

The easiest way to interface the ADE7760 to a microcontroller is to use the CF high frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table 7). With full-scale ac signals on the analog inputs, the output frequency on CF is approximately 5.5 kHz. Figure 26 illustrates one scheme that could be used to digitize the output frequency and carry out the necessary averaging mentioned in the previous section.

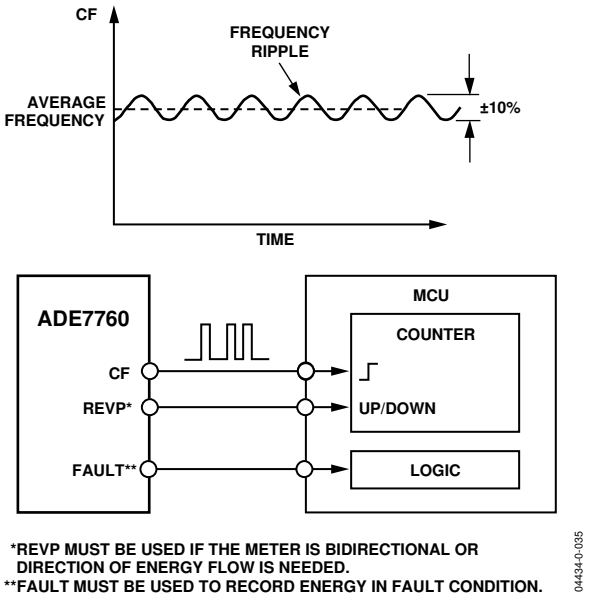


Figure 26. Interfacing the ADE7760 to an MCU

As shown, the frequency output CF is connected to an MCU counter or port, which counts the number of pulses in a given integration time, determined by an MCU internal timer. The average power, proportional to the average frequency, is given by

$$Average\ Frequency = Average\ Active\ Power = \frac{Counter}{Timer}$$

The energy consumed during an integration period is given by

$$Energy = Average\ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time could be 10 s to 20 s in order to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time could be reduced to 1 s or 2 s depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update might still have a small amount of ripple, even under steady load conditions. However, over a minute or more, the measured energy has no ripple.

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table 5, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Because only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 impulses/kWh with a maximum current of between 10 A and 120 A. Table 8 shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 240 V. In all cases, the meter constant is 100 impulses/kWh.

Table 8. F1 and F2 Frequency at 100 Impulses/kWh

I_{MAX}	F1 and F2 (Hz)
12.5 A	0.083
25 A	0.166
40 A	0.266
60 A	0.4
80 A	0.533
120 A	0.8

The F_{1-4} frequencies allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter the nominal design voltage on Channel 2 (voltage) should be set to half-scale to allow for calibration of the meter constant. The current channel should also be no more than half-scale when the meter sees maximum load. This accommodates overcurrent signals and signals with high crest factors. Table 9 shows the output frequency on F1 and F2 when both analog inputs are half-scale. The frequencies listed in Table 9 align well with those listed in Table 8 for maximum load.

Table 9. F1 and F2 Frequency with Half-Scale AC Inputs

S0	S1	F_{1-4}	Frequency on F1 and F2, CH1 and CH2, Half-Scale AC Inputs
0	0	1.72	0.085 Hz
0	1	3.44	0.17 Hz
1	0	6.86	0.34 Hz
1	1	13.5	0.68 Hz

When selecting a suitable F_{1-4} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 impulses /kWh should be compared with Column 4 of Table 9. The frequency that is closest in Table 9 determines the best choice of frequency (F_{1-4}). For example, if a meter with a maximum current of 40 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 impulses /kWh is 0.266 Hz at 40 A and 240 V (from Table 8). Looking at Table 9, the closest frequency to 0.266 Hz in Column 4 is 0.17 Hz. Therefore, F2 (3.4 Hz; see Table 5) is selected for this design.

Frequency Outputs

Figure 2 shows a timing diagram for the various frequency outputs. The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms wide, active high pulse (t_4) at a frequency that is proportional to active power. The CF output frequencies are given in Table 7. As in the case of F1 and F2, if the period of CF (t_5) falls below 180 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms.

No-Load Threshold

The ADE7760 also includes a no-load threshold and startup current feature that eliminates any creep effects in the meter. The ADE7760 is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum frequency does not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0045% of the full-scale output frequency. (See Table 7 for maximum output frequencies for ac signals.)

For example, an energy meter with a meter constant of 100 impulses /kWh on F1, F2 using SCF = 1, S1 = 0, and S0 = 1, the maximum output frequency at F1 or F2 would be 0.68 Hz and 43.52 Hz on CF. The minimum output frequency at F1 or F2 would be 0.0045% of 0.68 Hz or 3.06×10^{-5} Hz. This would be 1.96×10^{-3} Hz at CF (64 × F1 Hz). In this example, the no-load threshold would be equivalent to 1.1 W of load or a startup current of 4.6 mA at 240 V. Compare this value to the IEC61036 specification, which states that the meter must start up with a load equal to or less than 0.4% I_B. For a 5 A (I_B) meter, 0.4% of I_B is equivalent to 20 mA.

Note that the no-load threshold is not enabled when using the high CF frequency mode: SCF = 0, S1 = S0 = 1.

NEGATIVE POWER INFORMATION

The ADE7760 detects when the current and voltage channels have a phase shift greater than 90°. This mechanism can detect wrong connection of the meter or generation of negative power. The REVP pin output goes active high when negative power is detected and active low, when positive power is detected. The REVP pin output changes state as a pulse is issued on CF.

OUTLINE DIMENSIONS

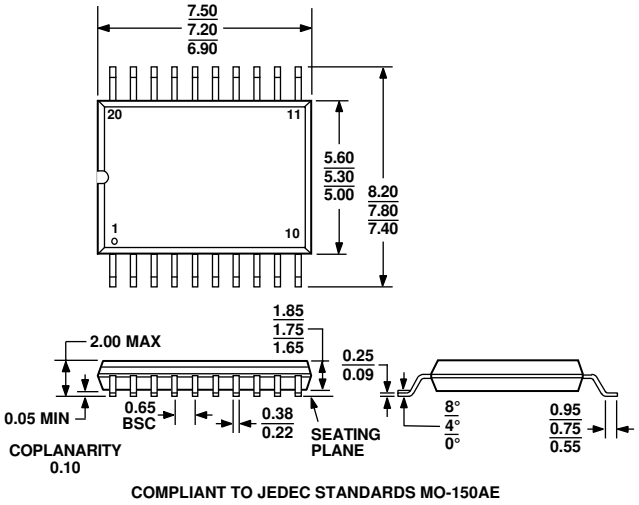


Figure 27. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7760ARS	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADE7760ARSRL	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20

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