Dual RF PLL Frequency Synthesizers

ADF4216/ADF4217/ADF4218

OBSOLETE

FEATURES

ADF4216: 550 MHz/1.2 GHz
ADF4217: 550 MHz/2.0 GHz
ADF4218: 550 MHz/2.5 GHz
2.7 V to 5.5 V Power Supply
Selectable Charge Pump Currents
Selectable Dual Modulus Prescaler
IF: 8/9 or 16/17
RF: 32/33 or 64/65
3-Wire Serial Interface
Power-Down Mode

APPLICATIONS

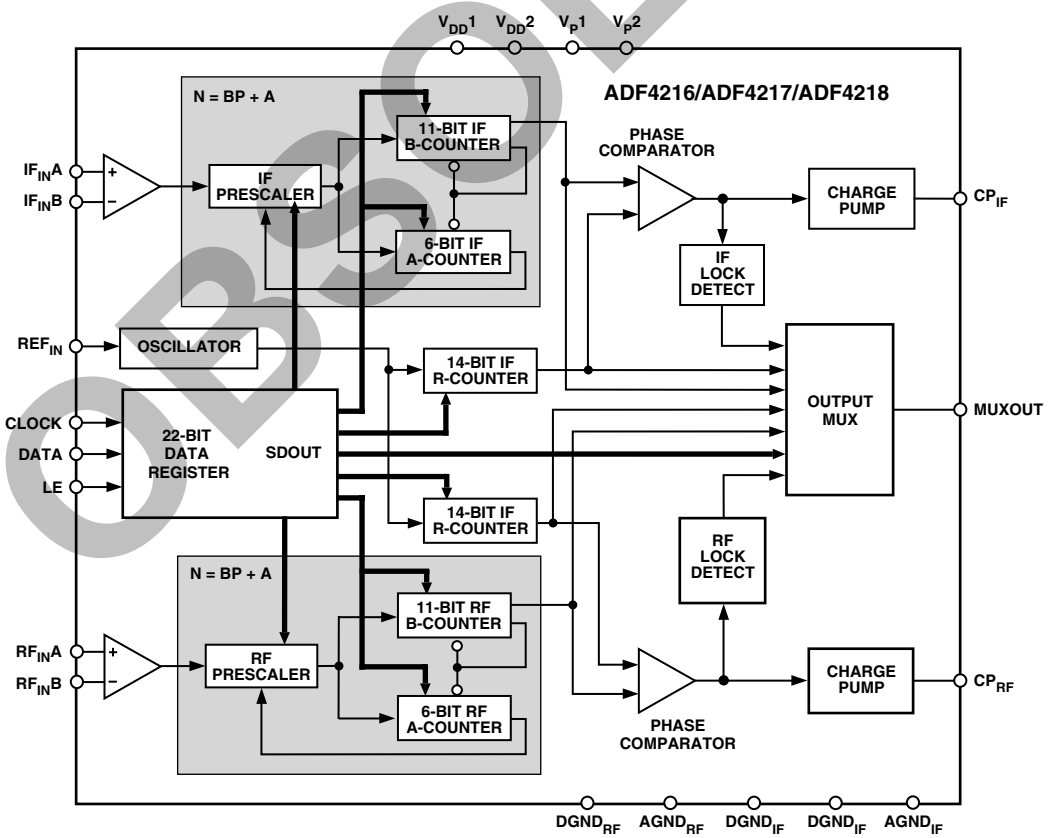
Wireless Handsets (GSM, PCS, DCS, CDMA, WCDMA)
Base Stations for Wireless Radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANS
Communications Test Equipment
CATV Equipment

GENERAL DESCRIPTION

The ADF4216/ADF4217/ADF4218 are dual frequency synthesizers that can be used to implement local oscillators (LOs) in the upconversion and downconversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCOs (Voltage Controlled Oscillators).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADF4216/ADF4217/ADF4218–SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1, V_{DD}2 \leq V_P1, V_P2 \leq 6.0$ V; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0$ V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
RF/IF CHARACTERISTICS (3 V)				
RF Input Frequency (RF_{IN})				See Figure 3 for Input Circuit.
ADF4216	0.2/1.2	0.2/1.2	GHz min/max	For lower frequency operation (below the
ADF4217	0.2/2.0	0.2/2.0	GHz min/max	minimum stated) use a square wave source.
ADF4218	0.5/2.5	0.5/2.5	GHz min/max	
IF Input Frequency (IF_{IN})	45/550	45/550	MHz min/max	
RF Input Sensitivity	–15/+4	–15/+4	dBm min/max	
IF Input Sensitivity	–10/+4	–10/+4	dBm min/max	
Maximum Allowable				
Prescaler Output Frequency[3]	165	165	MHz max	
RF/IF CHARACTERISTICS (5 V)				
RF Input Frequency (RF_{IN})				See Figure 3 for Input Circuit.
ADF4216	0.2/1.2	0.2/1.2	GHz min/max	For lower frequency operation (below the
ADF4217	0.2/2.0	0.2/2.0	GHz min/max	minimum stated) use a square wave source.
ADF4218	0.5/2.5	0.5/2.5	GHz min/max	
IF Input Frequency (IF_{IN})	25/550	25/550	MHz min/max	
RF Input Sensitivity	–15/+4	–15/+4	dBm min/max	
IF Input Sensitivity	–10/+4	–10/+4	dBm min/max	
Maximum Allowable				
Prescaler Output Frequency[3]	200	200	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	5/40	5/40	MHz min/max	For f < 5 MHz, use dc-coupled square wave (0 to V_{DD}).
REFIN Input Sensitivity[4]	0.5	0.5	V p-p min	AC-Coupled. When DC-Coupled: 0 to V_{DD} max (CMOS-Compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[5]	40	40	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				
High Value	4.5	4.5	mA typ	
Low Value	1.125	1.125	mA typ	
Absolute Accuracy	1	1	% typ	
I_{CP} Three-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	1	1	% typ	
I_{CP} vs. V_{CP}	10	10	% max	$0.5 \text{ V} \leq V_{CP} \leq V_P - 0.5 \text{ V}$
I_{CP} vs. Temperature	10	10	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8 \times V_{DD}$	$0.8 \times V_{DD}$	V min	
V_{INL}, Input Low Voltage	$0.2 \times V_{DD}$	$0.2 \times V_{DD}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	$V_{DD} - 0.4$	$V_{DD} - 0.4$	V min	$I_{OH} = 500$ µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$I_{OL} = 500$ µA
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P	$V_{DD}1$/6.0	$V_{DD}1$/6.0	V min/V max	$AV_{DD} \leq V_P \leq 6.0$ V

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Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
POWER SUPPLIES (Continued)				
I_{DD} (RF + IF)[6]				See TPC 22 and TPC 23
ADF4216	18	9	mA max	9.0 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4217	21	12	mA max	12 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4218	25	14	mA max	14 mA typical at V_{DD} = 3 V and T_A = 25°C
I_{DD} (RF Only)				
ADF4216	10	5	mA max	5.0 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4217	14	7	mA max	7.0 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4218	18	9	mA max	9.0 mA typical at V_{DD} = 3 V and T_A = 25°C
I_{DD} (IF Only)				
ADF4216	9	4.5	mA max	4.5 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4217	9	4.5	mA max	4.5 mA typical at V_{DD} = 3 V and T_A = 25°C
ADF4218	9	4.5	mA max	4.5 mA typical at V_{DD} = 3 V and T_A = 25°C
I_P (I_P1 + I_P2)	0.6	0.6	mA max	T_A = 25°C
Low-Power Sleep Mode	5	5	µA max	0.5 µA typical
NOISE CHARACTERISTICS				
Phase Noise Floor[7]	–171	–171	dBc/Hz typ	@ 25 kHz PFD Frequency
	–164	–164	dBc/Hz typ	@ 200 kHz PFD Frequency
Phase Noise Performance[8]				@ VCO Output
ADF4216, ADF4217, ADF4218 (IF)[9]	–91	–91	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4216 (RF): 900 MHz Output[10]	–87	–87	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4217 (RF): 900 MHz Output[10]	–88	–88	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4218 (RF): 900 MHz Output[10]	–90	–90	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4216 (RF): 836 MHz Output[11]	–78	–78	dBc/Hz typ	@ 300 Hz Offset and 30 kHz PFD Frequency
ADF4217 (RF): 1750 MHz Output[12]	–85	–85	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4217 (RF): 1750 MHz Output[13]	–66	–66	dBc/Hz typ	@ 200 Hz Offset and 10 kHz PFD Frequency
ADF4218 (RF): 1960 MHz Output[14]	–84	–84	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
Spurious Signals				
ADF4216 ADF4217, ADF4218 (IF)[9]	–97/–106	–97/–106	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4216 (RF): 900 MHz Output[10]	–98/–106	–98/–106	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4217 (RF): 900 MHz Output[10]	–91/–100	–91/–100	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4218 (RF): 900 MHz Output[10]	–80/–84	–80/–84	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4216 (RF): 836 MHz Output[11]	–80/–84	–80/–84	dB typ	@ 30 kHz/60 kHz and 30 kHz PFD Frequency
ADF4217 (RF): 1750 MHz Output[12]	–88/–90	–88/–90	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4217 (RF): 1750 MHz Output[13]	–65/–73	–65/–73	dB typ	@ 10 kHz/20 kHz and 10 kHz PFD Frequency
ADF4218 (RF): 1960 MHz Output[14]	–80/–84	–80/–84	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency

OBSOLETE

NOTES

[1]Operating temperature range is as follows: B Version: –40°C to +85°C.

[2]The B Chip specifications are given as typical values.

[3]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the IF/RF input is divided down to a frequency that is less than this value.

[4]$V_{DD}1 = V_{DD}2$ = 3 V; For $V_{DD}1 = V_{DD}2$ = 5 V, use CMOS-compatible levels.

[5]Guaranteed by design. Sample tested to ensure compliance.

[6]P = 16; RF_{IN} = 900 MHz; IF_{IN} = 540 MHz.

[7]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N divider value).

[8]The phase noise is measured with the EVAL-ADF421XEB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).

[9]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{IF} = 540 MHz; N = 2700; Loop B/W = 20 kHz.

[10]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; Loop B/W = 20 kHz.

[11]f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; Offset frequency = 300 Hz; f_{RF} = 836 MHz; N = 27867; Loop B/W = 3 kHz.

[12]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; Loop B/W = 20 kHz.

[13]f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; Offset frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; Loop B/W = 1 kHz.

[14]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 1960 MHz; N = 9800; Loop B/W = 20 kHz.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

($V_{DD}1 = V_{DD}2 = 3\ V \pm 10\%, 5\ V \pm 10\%$; $V_P1, V_P2 = V_{DD}, 5\ V \pm 10\%$; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulsewidth

NOTES
Guaranteed by design but not production tested.
Specification subject to change without notice.

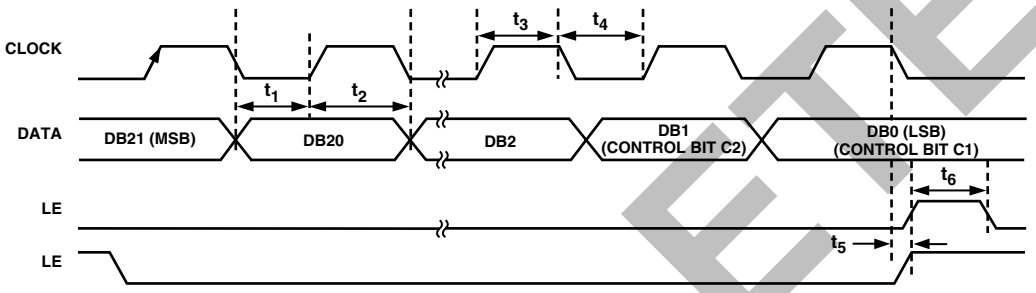


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted)

$V_{DD}1$ to GND[3] . . . . . –0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$ . . . . . –0.3 V to +0.3 V
V_P1, V_P2 to GND . . . . . –0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$ . . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$,
$IF_{IN}A$, $IF_{IN}B$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]This device is a high-performance RF integrated circuit with an ESD rating of < 2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[3]GND = AGND = DGND = 0 V.

TRANSISTOR COUNT

11749 (CMOS) and 522 (Bipolar).

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADF4216BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4217BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4218BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20

*Contact the factory for chip availability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4216/ADF4217/ADF4218 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

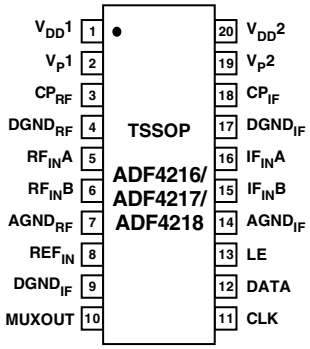


PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{DD}1$	Positive Power Supply for the RF Section. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. $V_{DD}1$ should have a value of between 2.7 V and 5.5 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
2	V_P1	Power Supply for the RF Charge Pump. This should be greater than or equal to V_{DD}.
3	CP_{RF}	Output from the RF Charge Pump. When enabled this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
4	$DGND_{RF}$	Ground Pin for the RF Digital Circuitry.
5	$RF_{IN}A$	Input to the RF Prescaler. This low-level input signal is normally ac-coupled to the external VCO.
6	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
7	$AGND_{RF}$	Ground Pin for the RF Analog Circuitry.
8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	$DGND_{IF}$	Ground Pin for the IF Digital (Interface and Control Circuitry).
10	MUXOUT	This multiplexer output allows either the IF/RF lock detect, the scaled RF, or the scaled Reference Frequency to be accessed externally. See Table V.
11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	$AGND_{IF}$	Ground Pin for the IF Analog Circuitry.
15	$IF_{IN}B$	Complementary Input to the IF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
16	$IF_{IN}A$	Input to the IF Prescaler. This low-level input signal is normally ac-coupled to the external VCO.
17	$DGND_{IF}$	Ground Pin for the IF Digital, Interface, and Control Circuitry.
18	CP_{IF}	Output from the IF Charge Pump. When enabled this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
19	V_P2	Power Supply for the IF Charge Pump. This should be greater than or equal to V_{DD}.
20	$V_{DD}2$	Positive Power Supply for the IF, Interface, and Oscillator Sections. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. $V_{DD}2$ should have a value of between 2.7 V and 5.5 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.

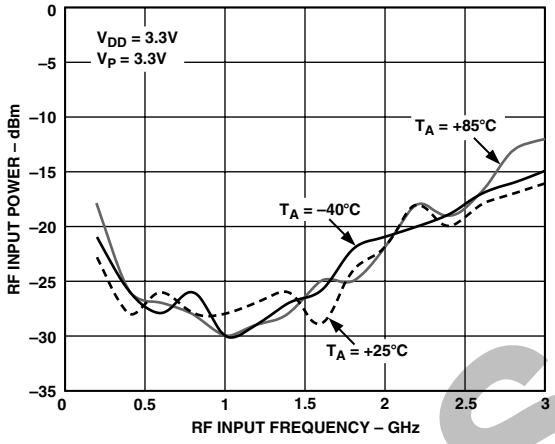
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PIN CONFIGURATION

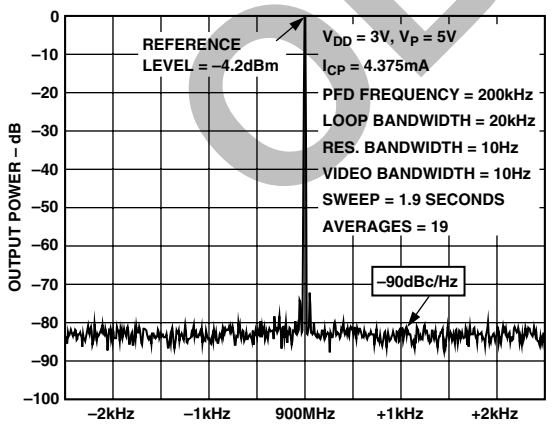


FREQ-UNIT GHz	PARAM-TYPE S	DATA-FORMAT MA	KEYWORD R	IMPEDANCE – OHMS 50	
FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.0	0.957111193	–3.130429321	1.35	0.816886959	–51.80711782
0.15	0.963546793	–6.686426265	1.45	0.825983016	–56.20373378
0.25	0.953621785	–11.19913586	1.55	0.791737125	–61.21554647
0.35	0.953757706	–15.35637483	1.65	0.770543186	–61.88187496
0.45	0.929831379	–20.3793432	1.75	0.793897072	–65.39516615
0.55	0.908459709	–22.69144845	1.85	0.745765233	–69.24884474
0.65	0.897303634	–27.07001443	1.95	0.7517547	–71.21608147
0.75	0.876862863	–31.32240763	2.05	0.745594889	–75.93169947
0.85	0.849338092	–33.68058163	2.15	0.713387801	–78.8391674
0.95	0.858403269	–38.57674885	2.25	0.711578577	–81.71934806
1.05	0.841888714	–41.48606772	2.35	0.698487131	–85.49067481
1.15	0.840354983	–45.97597958	2.45	0.669871818	–88.41958754
1.25	0.822165839	–49.19163116	2.55	0.668353367	–91.70921678

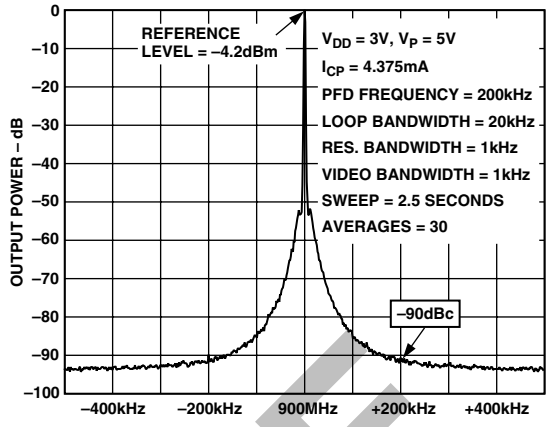
TPC 1. S-Parameter Data for the AD4218 RF Input (Up to 2.5 GHz)



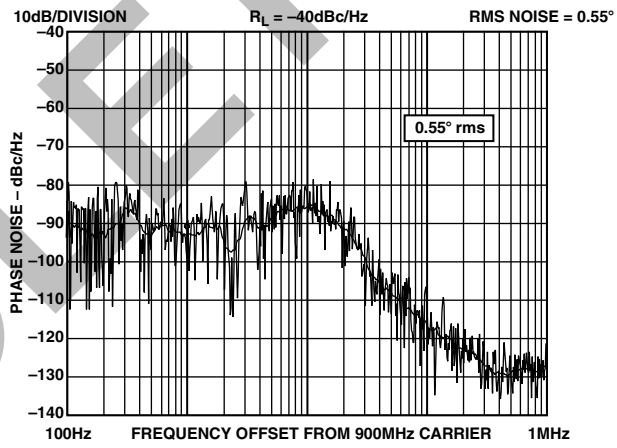
TPC 2. Input Sensitivity for the ADF4218 (RF)



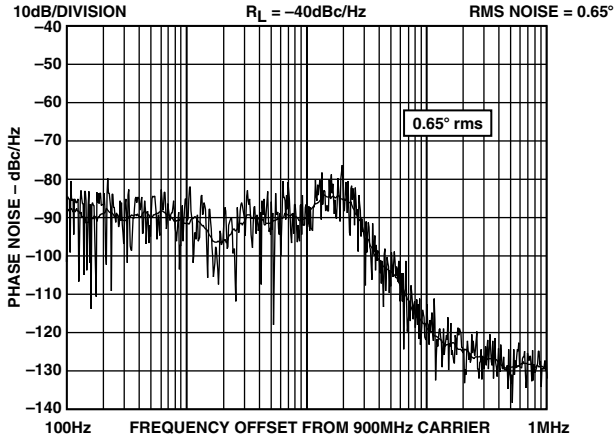
TPC 3. ADF4218 RF Phase Noise (900 MHz, 200 kHz, 20 kHz)



TPC 4. ADF4218 RF Reference Spurs (900 MHz, 200 kHz, 20 kHz)

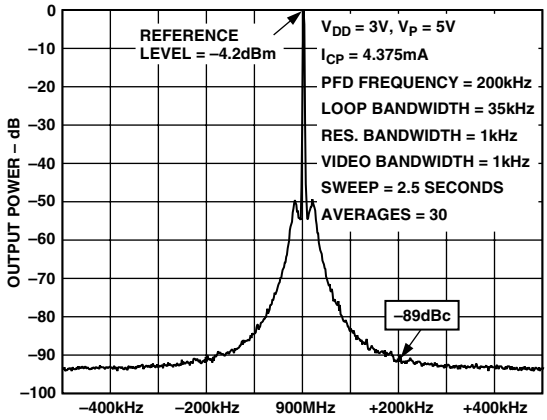


TPC 5. ADF4218 RF Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz)

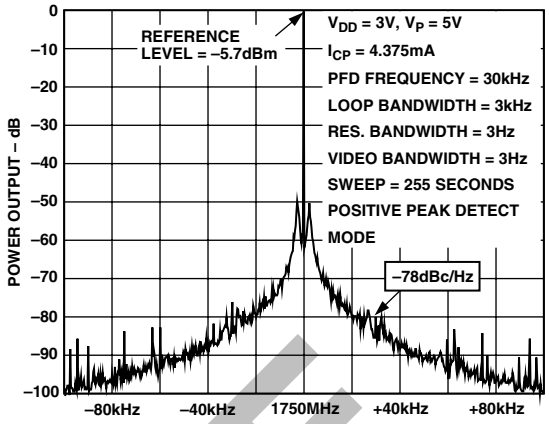


TPC 6. ADF4218 RF Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz)

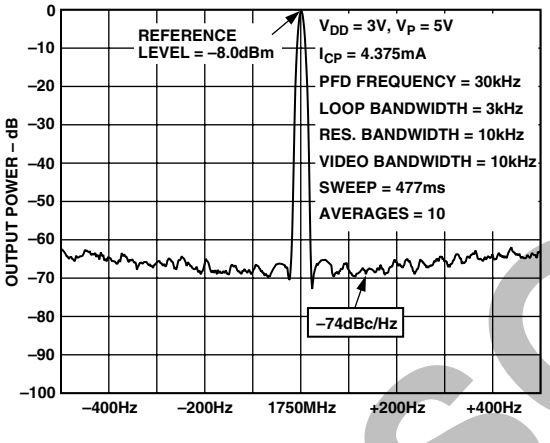
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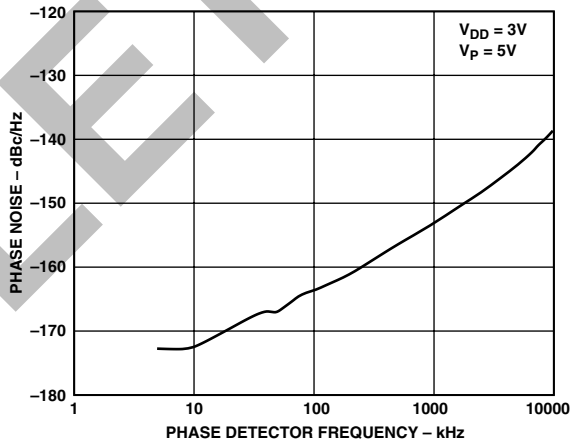
TPC 7. ADF4218 RF Reference Spurs (900 MHz, 200 kHz, 35 kHz)



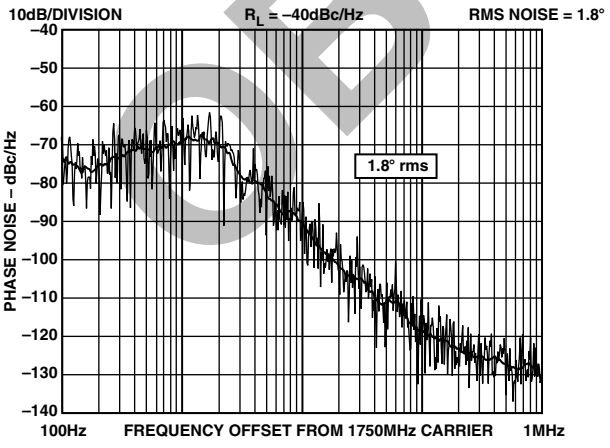
TPC 10. ADF4218 RF Reference Spurs (1750 MHz, 30 kHz, 3 kHz)



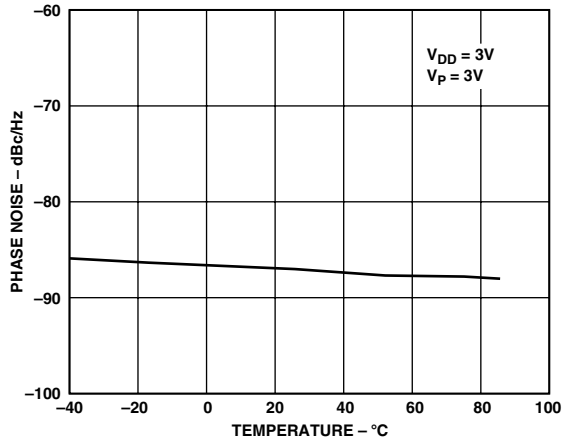
TPC 8. ADF4218 RF Phase Noise (1750 MHz, 30 kHz, 3 kHz)



TPC 11. ADF4218 RF Phase Noise vs. PFD Frequency

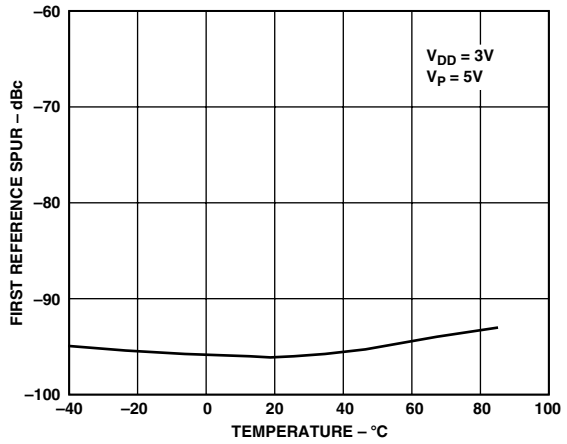


TPC 9. ADF4218 RF Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)

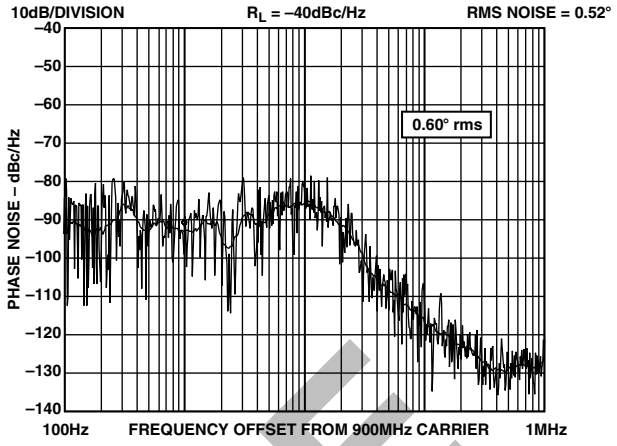


TPC 12. ADF4218 RF Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)

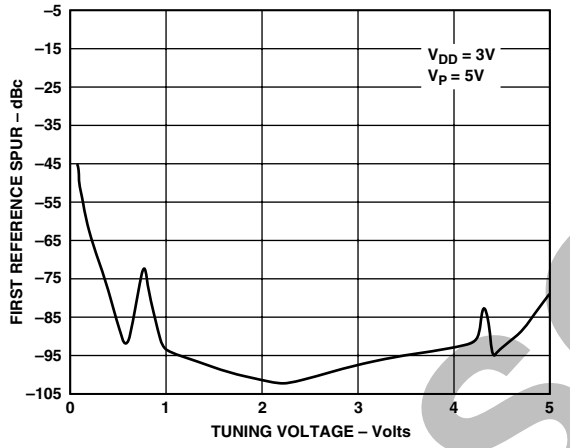
OBSOLETE



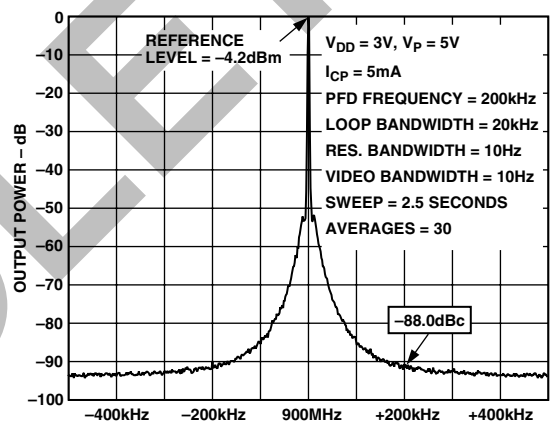
TPC 13. ADF4218 RF Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)



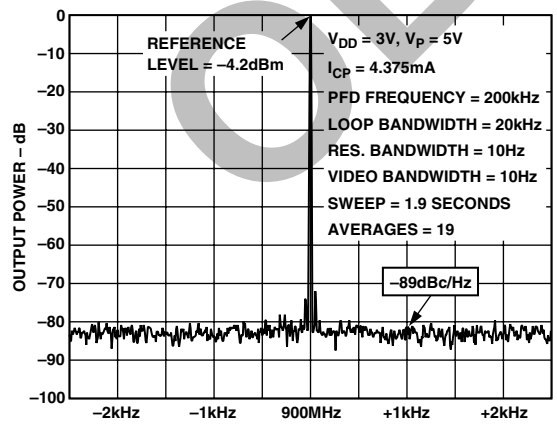
TPC 16. ADF4218 IF Integrated Phase Noise (540 MHz, 200 kHz, 20 kHz)



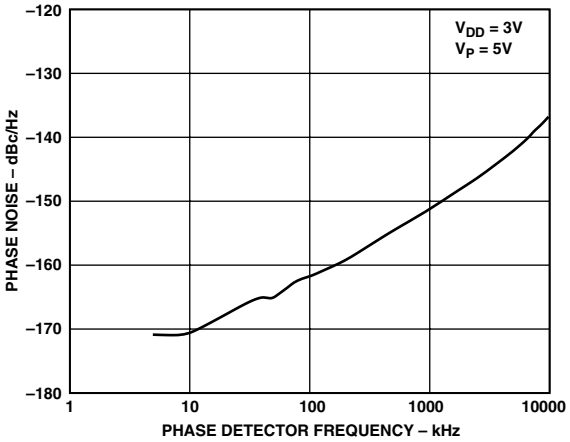
TPC 14. ADF4218 RF Reference Spurs vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)



TPC 17. ADF4218 IF Reference Spurs (540 MHz, 200 kHz, 20 kHz)

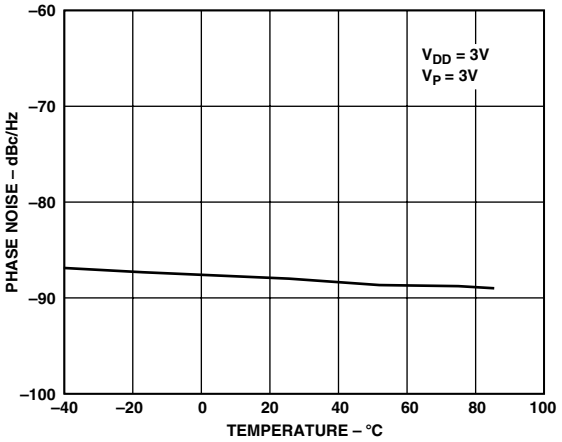


TPC 15. ADF4218 IF Phase Noise (540 MHz, 200 kHz, 20 kHz)

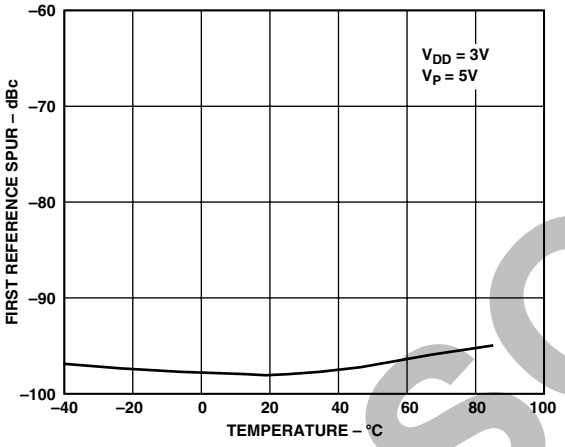


TPC 18. ADF4218 IF Phase Noise vs. PFD Frequency

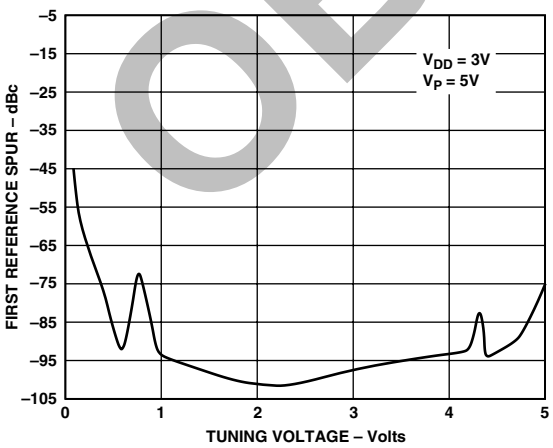
OBSOLETE



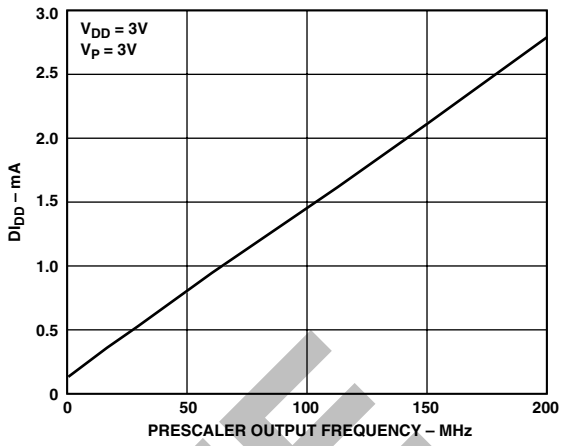
TPC 19. ADF4218 IF Phase Noise vs. Temperature (540 MHz, 200 kHz, 20 kHz)



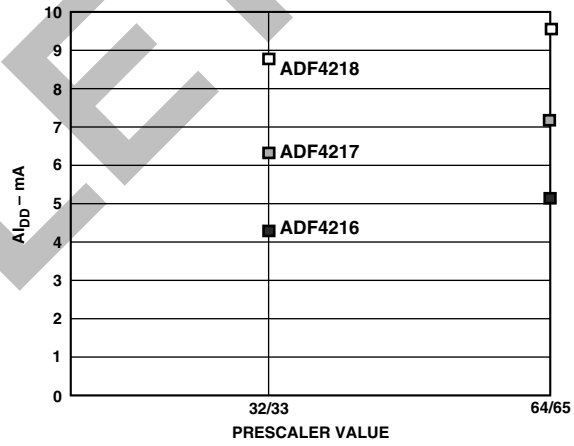
TPC 20. ADF4218 IF Reference Spurs vs. Temperature (540 MHz, 200 kHz, 20 kHz)



TPC 21. ADF4218 IF Reference Spurs vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)



TPC 22. DI_{DD} vs. Prescaler Output Frequency (ADF4218, RF Only)



TPC 23. ADF4218 AI_{DD} vs. Prescaler Value (RF)

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown below in Figure 2. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

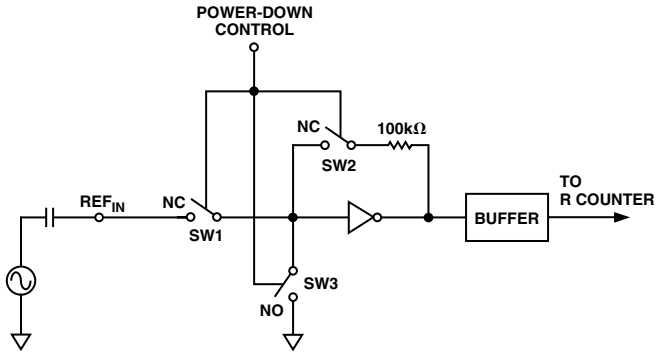


Figure 2. Reference Input Stage

IF/RF INPUT STAGE

The IF/RF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

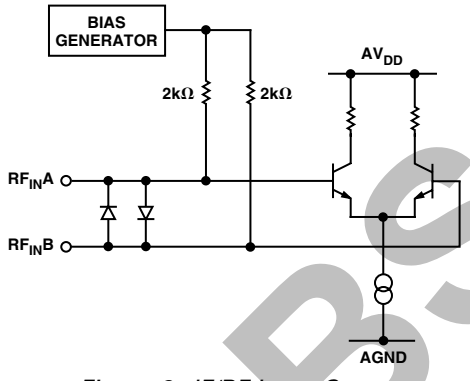


Figure 3. IF/RF Input Stage

PRESCALER

The dual modulus prescaler (P/P+1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). This prescaler, operating at CML levels, takes the clock from the IF/RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. It is based on a synchronous 4/5 core.

The prescaler is selectable. On the IF side it can be set to either 8/9 (DB20 of the IF AB Counter Latch set to 0) or 16/17 (DB20 set to 1). On the RF side it can be set to 64/65 (DB20 of the RF AB Counter Latch set to 0) or 32/33 (DB20 set to 1). See Tables IV and VI.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guaranteed to work when the prescaler output is 165 MHz or less. Typically they will work with 200 MHz output from the prescaler.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO} = Output frequency of external voltage controlled oscillator (VCO).

P = Preset modulus of dual modulus prescaler (8/9, 16/17, etc.).

B = Preset Divide Ratio of binary 11-bit counter (1 to 2047).

A = Preset Divide Ratio of binary 6-bit A counter (0 to 63).

f_{REFIN} = Output frequency of the external reference frequency oscillator.

R = Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383).

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

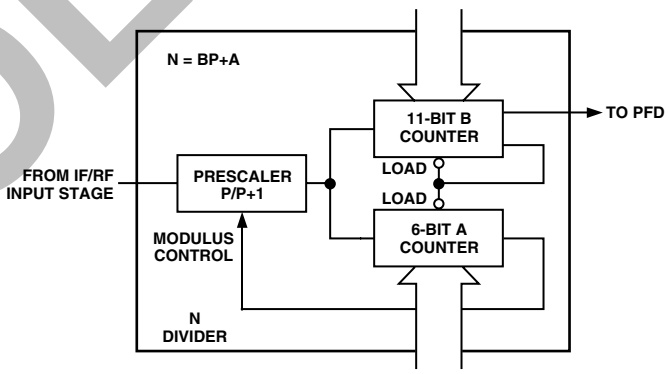


Figure 4. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic.

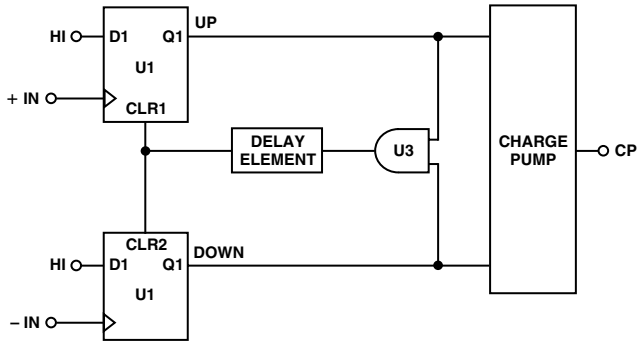


Figure 5. PFD Simplified Schematic

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MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4216 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11 and P12. See Tables III and V. Figure 6 shows the MUXOUT section in block diagram form.

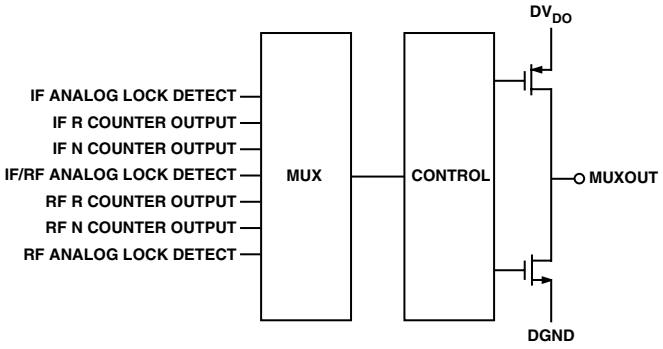


Figure 6. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for analog lock detect. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected it is high with narrow low-going pulses.

INPUT SHIFT REGISTER

The functional block diagram for the ADF4216 family is shown on Page 1. The main blocks include a 22-bit input shift register, a 14-bit R counter and an 17-bit N counter, comprising a 6-bit A counter and an 11-bit B counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table I.

Table I. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	IF R Counter
0	1	IF AB Counter (and Prescaler Select)
1	0	RF R Counter
1	1	RF AB Counter (and Prescaler Select)

PROGRAM MODES

Table III and Table V show how to set up the Program Modes in the ADF4216 family. The following should be noted:

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either IF or RF Analog Lock Detect is selected, the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen, the locked condition is indicated only when both IF and RF loops are locked.
2. The IF Counter Reset mode resets the R and N counters in the IF section and also puts the IF charge pump into three-state. The RF Counter Reset mode resets the R and N counters in the RF section and also puts the RF charge pump into three-state. The IF and RF Counter Reset mode does both of the above.

   Upon removal of the reset bits, the N counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to one.

POWER-DOWN

It is possible to program the ADF4216 family for either synchronous or asynchronous power-down on either the IF or RF side.

Synchronous IF Power-Down

Programming a "1" to P7 of the ADF4216 family will initiate a power-down. If P2 of the ADF4216 family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-State and then complete the power-down.

Asynchronous IF Power-Down

If P2 of the ADF4216 family has been set to "1" (three-state the IF charge pump), and P7 is subsequently set to "1," then an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the IF power-down bit (P7).

Synchronous RF Power-Down

Programming a "1" to P16 of the ADF4216 family will initiate a power-down. If P10 of the ADF4216 family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous RF Power-Down

If P10 of the ADF4216 families has been set to "1" (three-state the RF charge pump), and P16 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the RF power-down bit (P16).

Activation of either synchronous or asynchronous power-down forces the IF/RF loop's R and N dividers to their load state conditions and the IF/RF input section is debiased to a high impedance state.

The REF_{IN} oscillator circuit is only disabled if both the IF and RF power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power-down modes.

The IF/RF section of the devices will return to normal powered up operation immediately upon LE latching a "0" to the appropriate power-down bit.

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Table II. ADF4216 Family Latch Summary

IF REFERENCE COUNTER LATCH

IF F_O	IF LOCK DETECT	THREE-STATE CP_{IF}	IF CP GAIN	IF PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF AB COUNTER LATCH

IF POWER-DOWN	IF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF REFERENCE COUNTER LATCH

RE F_O	RF LOCK DETECT	THREE-STATE CP_{RF}	RF CP GAIN	RF PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF AB COUNTER LATCH

RF POWER-DOWN	RF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

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Table III. IF Reference Counter Latch Map

IF F_O	IF LOCK DETECT	THREE-STATE CP_{IF}	IF CP GAIN	IF PD POLARITY	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P1	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

P5	I_{CP}
0	1.25mA
1	4.375mA

P2	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

FROM RFR LATCH P12	P11	P4	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	X	1	0	IF REFERENCE DIVIDER OUTPUT
0	X	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
1	X	0	0	RF REFERENCE DIVIDER
1	X	0	1	RF N DIVIDER
1	0	1	0	FASTLOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	IF COUNTER RESET
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

OBSOLETE

Table IV. IF AB Counter Latch Map

IF POWER-DOWN	IF PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
X	X	0	0	0	0	0
X	X	0	0	0	1	1
X	X	0	0	1	0	2
X	X	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
X	X	1	1	1	0	14
X	X	1	1	1	1	15

B11	B10	B9		B3	B2	B1	B COUNTER DIVIDER RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P6	IF PRESCALER
0	8/9
1	16/17

P7	IF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. TO ENSURE CONTINUOUSLY ADJACENT VALUES OF N, N_{MIN} IS (P^2 – P).

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Table V. RF Reference Counter Latch Map

RF F_O	RF LOCK DETECT	THREE-STATE CP_{RF}	RF CP GAIN	RF PD POLARITY		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P9	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

P13	I_{CP}
0	1.25mA
1	4.375mA

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	FROM IFR LATCH P4	FROM IFR LATCH P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	X	1	0	IF REFERENCE DIVIDER OUTPUT
0	X	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
1	X	0	0	RF REFERENCE DIVIDER
1	X	0	1	RF N DIVIDER
1	0	1	0	FASTLOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	IF COUNTER RESET
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

OBSOLETE

Table VI. RF AB Counter Latch Map

RF POWER-DOWN	RF PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
X	X	0	0	0	0	0
X	X	0	0	0	1	1
X	X	0	0	1	0	2
X	X	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
X	X	1	1	1	0	14
X	X	1	1	1	1	15

B11	B10	B9	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P14	RF PRESCALER
0	64/65
1	32/33

P16	RF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. FOR ENSURE CONTINUOUSLY ADJACENT VALUES OF N, N_{MIN} IS (P^2 – P).

OBSOLETE

IF SECTION

Programmable IF Reference (R) Counter

If control bits C2, C1 are 0, 0 then the data is transferred from the input shift register to the 14 Bit IF R counter. Table III shows the input shift register data format for the IF R counter and the divide ratios possible.

IF Phase Detector Polarity

P1 sets the IF Phase Detector Polarity. When the IF VCO characteristics are positive, this should be set to "1." When they are negative, it should be set to "0." See Table III.

IF Charge Pump Three-State

P2 puts the IF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table III.

IF Charge Pump Currents

P5 sets the IF Charge Pump current. With P5 set to "0," I_{CP} is 1.25 mA. With P5 set to "1," I_{CP} is 4.375 mA. See Table III.

Programmable IF AB Counter

If control bits C2, C1 are 0, 1, the data in the input register is used to program the IF AB counter. The AB counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table IV shows the input register data format for programming the IF AB counter and the divide ratios possible.

IF Prescaler Value

P6 in the IF AB Counter Latch sets the IF prescaler value. Either 8/9 or 16/17 is available. See Table IV.

IF Power-Down

Table III and Table V show the power-down bits in the ADF4216 family. See Power-Down section for functional description.

RF SECTION

Programmable RF Reference (R) Counter

If control bits C2, C1 are 1, 0, the data is transferred from the input shift register to the 14-bit RFR counter. Table V shows the input shift register data format for the RFR counter and the divide ratios possible.

RF Phase Detector Polarity

P9 sets the IF Phase Detector Polarity. When the RF VCO characteristics are positive this should be set to "1." When they are negative it should be set to "0." See Table V.

RF Charge Pump Three-State

P10 puts the RF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table V.

RF Program Modes

Table III and Table V show how to set up the Program Modes in the ADF4216 family.

RF Charge Pump Currents

P13 sets the RF Charge Pump current. With P13 set to "0," I_{CP} is 1.25 mA. With P5 set to "1," I_{CP} is 4.375 mA. See Table V.

Programmable RF AB Counter

If control bits C2, C1 are 1, 1, the data in the input register is used to program the RF N (AB) counter. The AB counter consists of a 6-bit swallow counter (A Counter) and an 11-bit programmable counter (B Counter). Table VI shows the input register data format for programming the RF N counter and the divide ratios possible.

RF Prescaler Value

P14 in the RF AB Counter Latch sets the RF prescaler value. Either 32/33 or 64/65 is available. See Table VI.

RF Power-Down

Table IV and Table VI show the power-down bits in the ADF4216 family. See Power-Down section for functional description.

RF Fastlock

The RF CP Gain bit (P17) of the RF N register in the ADF4210 family is the Fastlock Enable Bit. Only when this is "1" is IF Fastlock enabled. When Fastlock is enabled, the RF CP current is set to its maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin, thus compensating for the change in loop characteristics while in Fastlock. Since the RF CP Gain bit is contained in the RF N Counter, only one write is needed both to program a new output frequency and to initiate Fastlock. To come out of Fastlock, the RF CP Gain bit on the RF N register must be set to "0." See Table VI.

APPLICATIONS SECTION

Local Oscillator for GSM Handset Receiver

Figure 7 shows the ADF4216 being used in a classic superheterodyne receiver to provide the required LOs (Local Oscillators).

In this circuit, the reference input signal is applied to the circuit at REF_{IN} and is being generated by a 13 MHz TCXO (Temperature Controlled Crystal Oscillator).

In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference counter.

The RF output frequency range is 1050 MHz to 1085 MHz. Loop filter component values are chosen so that the loop bandwidth is 20 kHz. The synthesizer is set up for a charge pump current of 4.375 mA and the VCO sensitivity is 15.6 MHz/V.

The IF output is fixed at 125 MHz. The IF loop bandwidth is chosen to be 20 kHz with a channel spacing of 200 kHz. Loop filter component values are chosen accordingly.

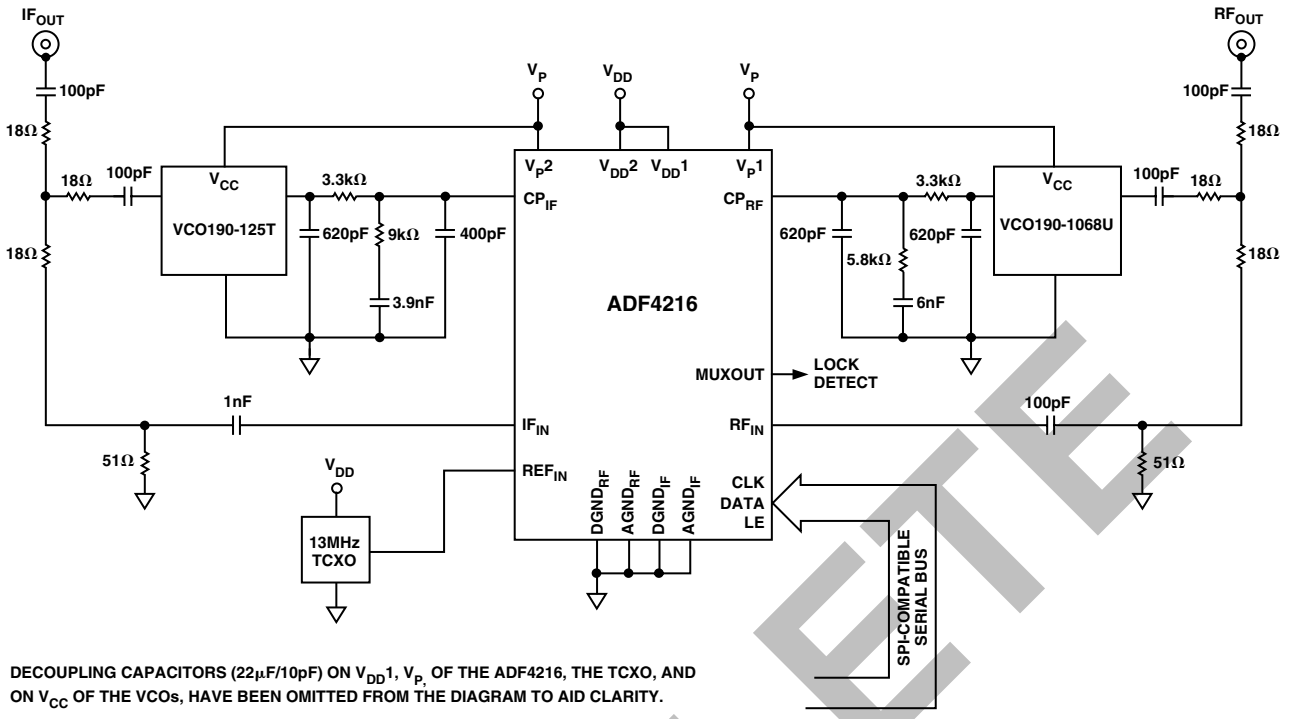
Local Oscillator for WCDMA Receiver

Figure 8 shows the ADF4217 being used to generate the local oscillator frequencies for a Wideband CDMA (WCDMA) system.

The RF output range needed is 1720 MHz to 1780 MHz. The VCO190–1750T will accomplish this. Channel spacing is 200 kHz with a 20 kHz loop bandwidth. VCO sensitivity is 32 MHz/V. Charge pump current of 4.375 mA is used and the desired phase margin for the loop is 45°.

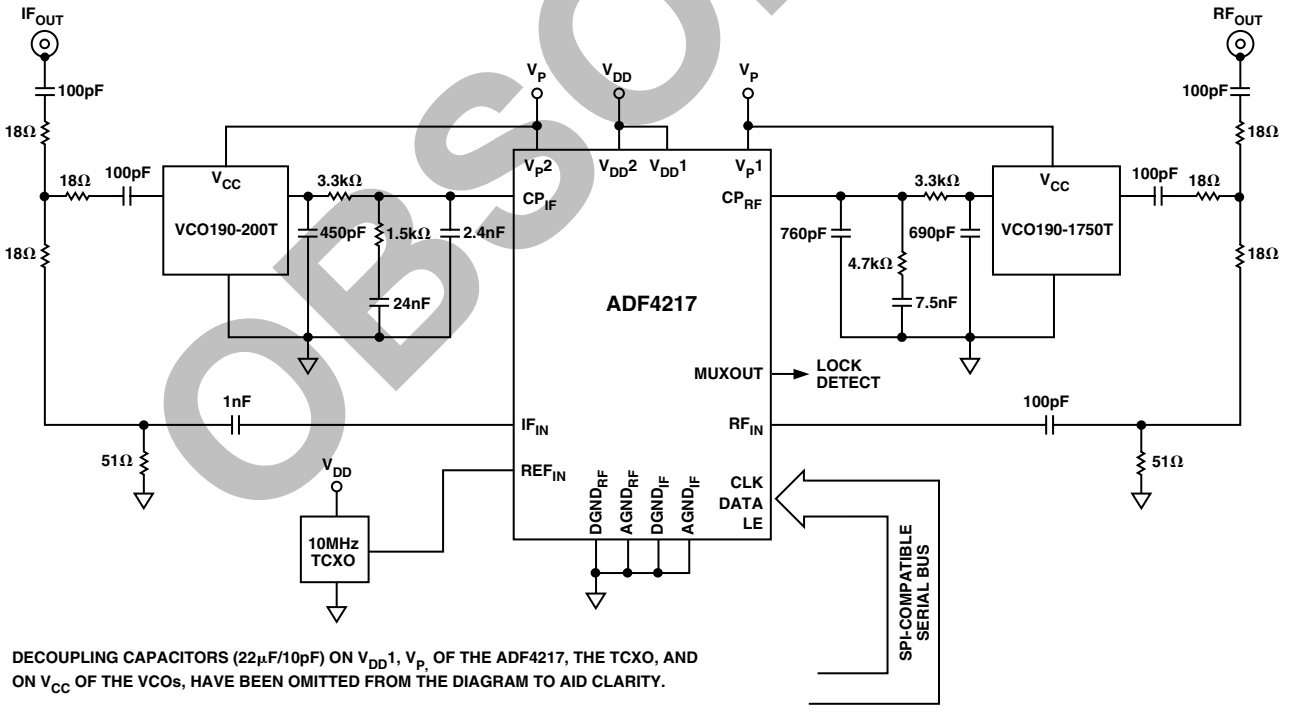
The IF output is fixed at 200 MHz. The VCO190–200T is used. It has a sensitivity of 11.5 MHz/V. Channel spacing and loop bandwidth is chosen to be the same as the RF side.

OBSOLETE



DECOUPLING CAPACITORS (22μF/10pF) ON $V_{DD}1$, V_P, OF THE ADF4216, THE TCXO, AND ON V_{CC} OF THE VCOs, HAVE BEEN OMITTED FROM THE DIAGRAM TO AID CLARITY.

Figure 7. GSM Handset Receiver Local Oscillator Using the ADF4216



DECOUPLING CAPACITORS (22μF/10pF) ON $V_{DD}1$, V_P, OF THE ADF4217, THE TCXO, AND ON V_{CC} OF THE VCOs, HAVE BEEN OMITTED FROM THE DIAGRAM TO AID CLARITY.

Figure 8. Local Oscillator for WCDMA Receiver Using the ADF4217

OBSOLETE

INTERFACING

The ADF4216/ADF4217/ADF4218 family has a simple SPI-compatible serial interface for writing to the device. SCLK, SDATA, and LE (Latch Enable) control the data transfer. When LE goes high, the 22 bits that have been clocked into the input register on each rising edge of SCLK will be transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Latch Truth Table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 ms. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 9 shows the interface between the ADF421x family and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI Master Mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF421x family needs a 22-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF421x family, it requires four writes (one each to the R counter latch and the AB counter latch for both RF1 and RF2 side) for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be about 180 kHz.

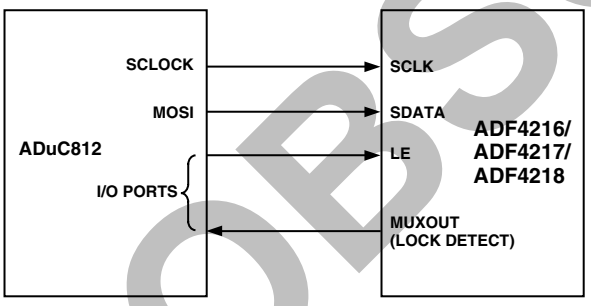


Figure 9. ADuC812 to ADF421x Family Interface

ADSP-2181 Interface

Figure 10 shows the interface between the ADF421x family and the ADSP-21xx Digital Signal Processor. As previously noted, the ADF421x family needs a 22-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the Autobuffered Transmit Mode of operation with Alternate Framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 22-bit word. To program each 22-bit latch, store the three 8-bit bytes, enable the Autobuffered mode and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

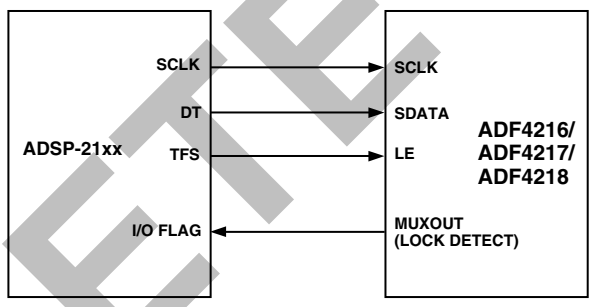


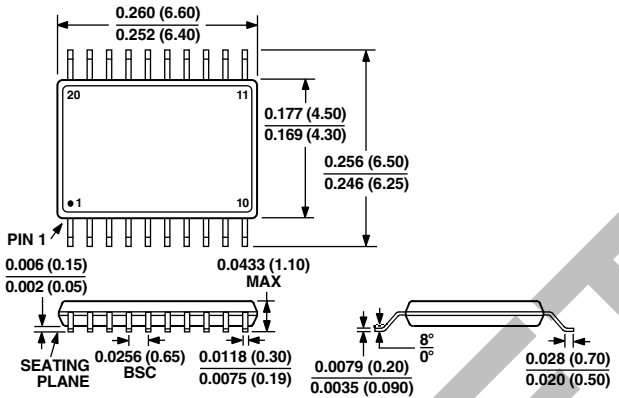
Figure 10. ADSP-21xx to ADF421x Family Interface

OBSOLETE

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Thin Shrink Small Outline Package (TSSOP)
(RU-20)



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C01028–2.5–10/00 (rev. 0)

PRINTED IN U.S.A.