Bidirectional Fault Protection and Detection, 10 Ω R_{ON}, Quad SPST Switches

Data Sheet

ADG5412BF/ADG5413BF

FEATURES

- Overvoltage protection up to −55 V and +55 V
- Power-off protection up to −55 V and +55 V
- Overvoltage detection on source and drain pins
- Low on resistance: 10 Ω
  - On-resistance flatness of 0.5 Ω
- 3 kV human body model (HBM) ESD rating
- Latch-up immune under any circumstance
- Known state without digital inputs present
- V_{SS} to V_{DD} analog signal range
  - ±5 V to ±22 V dual-supply operation
  - 8 V to 44 V single-supply operation
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAMS

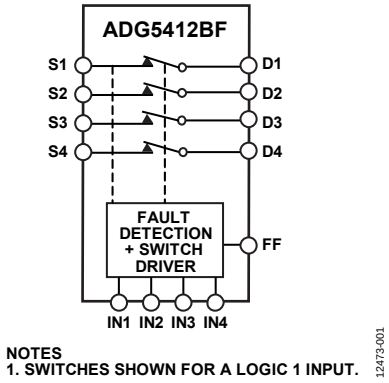


Figure 1. ADG5412BF

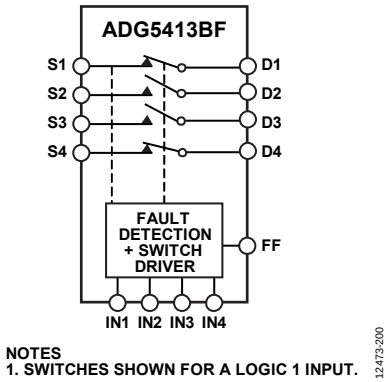


Figure 2. ADG5413BF

GENERAL DESCRIPTION

The ADG5412BF and ADG5413BF contain four independently controlled single-pole/single-throw (SPST) switches. The ADG5412BF has four switches that turn on with Logic 1 inputs. The ADG5413BF has two switches that turn on and two switches that turn off with Logic 1 inputs. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any switch pin exceed V_{DD} or V_{SS} by a threshold voltage, V_T, the switch turns off. Input signal levels up to +55 V and −55 V relative to ground are blocked, in both the powered and unpowered condition.

The low on resistance of these switches, combined with on-resistance flatness over a significant portion of the signal range make them an ideal solution for data acquisition and gain switching applications where excellent linearity and low distortion are critical.

PRODUCT HIGHLIGHTS

1. Switch pins are protected against voltages greater than the supply rails, up to −55 V and +55 V.
2. Switch pins are protected against voltages between −55 V and +55 V, in an unpowered state.
3. Overvoltage detection with digital output indicates operating state of switches.
4. Trench isolation guards against latch-up.
5. Optimized for low on resistance and on-resistance flatness.
6. The ADG5412BF/ADG5413BF can be operated from a dual-supply of ±5 V up to ±22 V or a single power supply of 8 V up to 44 V.

Rev. B
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REVISION HISTORY

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7/14—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL-SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 13.5 V, V_{SS} = −13.5 V, see Figure 32
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	V_S = ±10 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
	9.5			Ω typ	V_S = ±9 V, I_S = −10 mA
	10.7	13.5	16	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.6			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.9	1.1	1.1	Ω max	
	0.1			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 28
LEAKAGE CURRENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 33
	±1.5	±5.5	±24	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 33
	±1.5	±5.5	±20	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±10 V, see Figure 34
	±2.0	±2.5	±5.5	nA max	
FAULT					
Input Leakage Current, I_S or I_D					
With Overvoltage			±78	µA typ	V_{DD} = 16.5 V, V_{SS} = 16.5 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S or V_D = ±55 V, see Figure 38
Output Leakage Current, I_S or I_D					
With Overvoltage	±20			nA typ	V_{DD} = 16.5 V, V_{SS} = 16.5 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
	±200	±250	±250	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Output Voltage				V min	
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	495	525	550	ns max	V_S = 10 V, see Figure 47
t_{OFF}	410			ns typ	R_L = 300 Ω, C_L = 35 pF
	510	545	555	ns max	V_S = 10 V, see Figure 47
Break-Before-Make Time Delay, t_D (ADG5413BF Only)	285			ns typ	R_L = 300 Ω, C_L = 35 pF
			185	ns min	V_{S1} = V_{S2} = 10 V, see Figure 46
Overvoltage Response Time, $t_{RESPONSE}$	460			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 41
	585	615	630	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	720			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	930	1050	1100	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 10 pF, see Figure 43
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 10 pF, see Figure 44
	600			ns typ	C_L = 10 pF, R_{PULLUP} = 1 kΩ, see Figure 45
Charge Injection, Q_{INJ}	−680			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 35
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion Plus Noise, THD + N	0.0015			% typ	R_L = 10 kΩ, V_S = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 40
−3 dB Bandwidth	270			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 39
Insertion Loss	−0.72			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
C_S (Off)	13			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	12			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	24			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	µA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
	1.0		1.8	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL-SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 18 V, V_{SS} = −18 V, see Figure 32
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	V_S = ±15 V, I_S = −10 mA
	11.5	14.5	16.5	Ω max	
	9.5			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
	0.05			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.0			Ω typ	V_S = ±15 V, I_S = −10 mA
	1.4	1.5	1.5	Ω max	
	0.1			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 28
LEAKAGE CURRENTS					V_{DD} = 22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 33
	±1.5	±5.5	±24	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 33
	±1.5	±5.5	±20	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±15 V, see Figure 34
	±2.0	±2.5	±5.5	nA max	
FAULT					
Input Leakage Current, I_S or I_D					
With Overvoltage			±78	µA typ	V_{DD} = 22 V, V_{SS} = −22 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S or V_D = ±55 V, see Figure 38
Output Leakage Current, I_S or I_D					
With Overvoltage	±0.4			µA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
	±1.0	±1.0	±1.0	µA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	500	530	555	ns max	V_S = 10 V, see Figure 47
t_{OFF}	415			ns typ	R_L = 300 Ω, C_L = 35 pF
	515	550	565	ns max	V_S = 10 V, see Figure 47
Break-Before-Make Time Delay, t_D (ADG5413BF Only)	295			ns typ	R_L = 300 Ω, C_L = 35 pF
			200	ns min	V_{S1} = V_{S2} = 10 V, see Figure 46
Overvoltage Response Time, $t_{RESPONSE}$	370			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 41
	480	500	515	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	840			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	1200	1400	1700	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 10 pF, see Figure 43
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 10 pF, see Figure 44
	600			ns typ	C_L = 10 pF, R_{PULLUP} = 1 kΩ, see Figure 45
Charge Injection, Q_{INJ}	−640			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 35
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 40
−3 dB Bandwidth	270			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 39
Insertion Loss	−0.73			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
C_S (Off)	12			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	23			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 22 V, V_{SS} = −22 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
	1.0		1.8	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE-SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V, see Figure 32
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.6			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −10 mA
	0.9	1.1	1.3	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 28
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 33
	±1.5	±5.5	±24	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 33
	±1.5	±5.5	±20	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/10 V, see Figure 34
	±2.0	±2.5	±5.5	nA max	
FAULT					
Input Leakage Current, I_S or I_D					
With Overvoltage			±78	µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S or V_D = ±55 V, see Figure 38
Output Leakage Current, I_S or I_D					
With Overvoltage	±20			nA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, see Figure 37
	±200	±250	±250	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	485	515	540	ns max	V_S = 8 V, see Figure 47
t_{OFF}	375			ns typ	R_L = 300 Ω, C_L = 35 pF
	460	495	520	ns max	V_S = 8 V, see Figure 47
Break-Before-Make Time Delay, t_D (ADG5413BF Only)	260			ns typ	R_L = 300 Ω, C_L = 35 pF
			170	ns min	V_{S1} = V_{S2} = 8 V, see Figure 46
Overvoltage Response Time, $t_{RESPONSE}$	560			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 41
	660	700	720	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	640			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	800	865	960	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 10 pF, see Figure 43
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 10 pF, see Figure 44
	600			ns typ	C_L = 10 pF, R_{PULLUP} = 1 kΩ, see Figure 45
Charge Injection, Q_{INJ}	−340			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 35
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 40
−3 dB Bandwidth	270			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 39
Insertion Loss	−0.74			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
C_S (Off)	16			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	15			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	25			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
	1.0		1.8	mA max	
V_{DD}			8	V min	V_{SS} = GND = 0 V
			44	V max	V_{SS} = GND = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE-SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V, see Figure 32
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.1			Ω typ	V_S = 4.5 V to 28 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 28
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 33
	±1.5	±5.5	±24	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 33
	±1.5	±5.5	±20	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/30 V, see Figure 34
	±2.0	±2.5	±5.5	nA max	
FAULT					
Input Leakage Current, I_S or I_D					
With Overvoltage			±78	µA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = +55 V, −40 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S or V_D = ±55 V, see Figure 38
Output Leakage Current, I_S or I_D					
With Overvoltage	±20			nA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = +55 V, −40 V, see Figure 37
	±200	±250	±250	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S or V_D = ±55 V, INx = 0 V, see Figure 38
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	400			ns typ	R_L = 300 Ω, C_L = 35 pF
	490	520	545	ns max	V_S = 18 V, see Figure 47
t_{OFF}	375			ns typ	R_L = 300 Ω, C_L = 35 pF
	460	485	510	ns max	V_S = 18 V, see Figure 47
Break-Before-Make Time Delay, t_D (ADG5413BF Only)	285			ns typ	R_L = 300 Ω, C_L = 35 pF
			195	ns min	V_{S1} = V_{S2} = 18 V, see Figure 46
Overvoltage Response Time, $t_{RESPONSE}$	250			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 41
	350	360	375	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	1500			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	2000	2300	2700	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 10 pF, see Figure 43
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 10 pF, see Figure 44
	600			ns typ	C_L = 10 pF, R_{PULLUP} = 1 kΩ, see Figure 45
Charge Injection, Q_{INJ}	−610			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 35
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 40
−3 dB Bandwidth	270			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 39
Insertion Loss	−0.75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
C_S (Off)	12			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	11			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	23			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
	0.65		0.7	mA max	
Isolation Mode					V_S = +55 V, −40 V
I_{DD}	1.2			mA typ	
	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
	1.0		1.8	mA max	
V_{DD}			8	V min	V_{SS} = GND = 0 V
			44	V max	V_{SS} = GND = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
16-LEAD TSSOP					
θ_{JA} = 112.6°C/W	83	59	39	mA max	$V_S = V_{SS} + 4.5$ V to $V_{DD} - 4.5$ V
	64	48	29	mA max	$V_S = V_{SS}$ to V_{DD}
16-LEAD LFCSP					
θ_{JA} = 30.4°C/W	152	99	61	mA max	$V_S = V_{SS} + 4.5$ V to $V_{DD} - 4.5$ V
	118	80	52	mA max	$V_S = V_{SS}$ to V_{DD}

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−48 V to +0.3 V
Sx and Dx	−55 V to +55 V
Sx to V_{DD} or V_{SS}	80 V
V_S to V_D	80 V
Digital Inputs	GND − 0.7 V to +48 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	288 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pins	Data[1] + 15%
Digital Output	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA} (4-Layer Board)	
16-Lead TTSOP	112.6°C/W
16-Lead LFSCP	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
ESD (HBM: ANSI/ESD STM5.1-2007)	
I/O Port to Supplies	5.5 kV
I/O Port to I/O Port	5.5 kV
All Other Pins	3 kV

[1] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

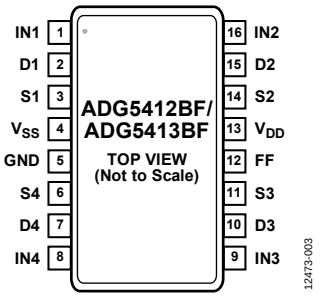
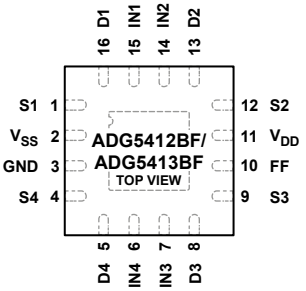


Figure 3. TSSOP Pin Configuration



NOTES
1. THE EXPOSED PAD IS INTERNALLY CONNECTED. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE CONNECTED TO THE LOWEST SUPPLY VOLTAGE, V_{SS}.

12473-104

Figure 4. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1	Logic Control Input.
2	16	D1	Overvoltage Protected Drain Terminal. This pin can be an input or an output.
3	1	S1	Overvoltage Protected Source Terminal. This pin can be an input or an output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Overvoltage Protected Source Terminal. This pin can be an input or an output.
7	5	D4	Overvoltage Protected Drain Terminal. This pin can be an input or an output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Overvoltage Protected Drain Terminal. This pin can be an input or an output.
11	9	S3	Overvoltage Protected Source Terminal. This pin can be an input or an output.
12	10	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation or a low when a fault condition occurs on any of the Sx inputs.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Overvoltage Protected Source Terminal. This pin can be an input or an output.
15	13	D2	Overvoltage Protected Drain Terminal. This pin can be an input or an output.
16	14	IN2	Logic Control Input.
	EP	Exposed Pad	The exposed pad is internally connected. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be connected to the lowest supply voltage, V_{SS}.

Table 8. ADG5412BF Truth Table

INx	**Switch Condition (S1 to S4)**
1	On
0	Off

Table 9. ADG5413BF Truth Table

	Switch Condition	
INx	**S1, S4**	**S2, S3**
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

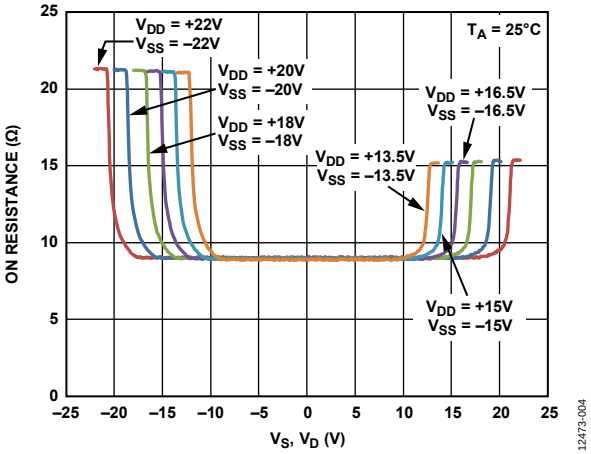


Figure 5. R_{ON} as a Function of V_S,V_D (Dual-Supply)

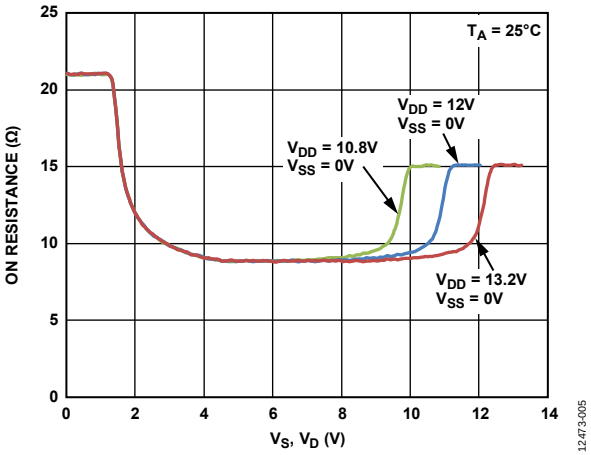


Figure 6. R_{ON} as a Function of V_S,V_D (12 V Single-Supply)

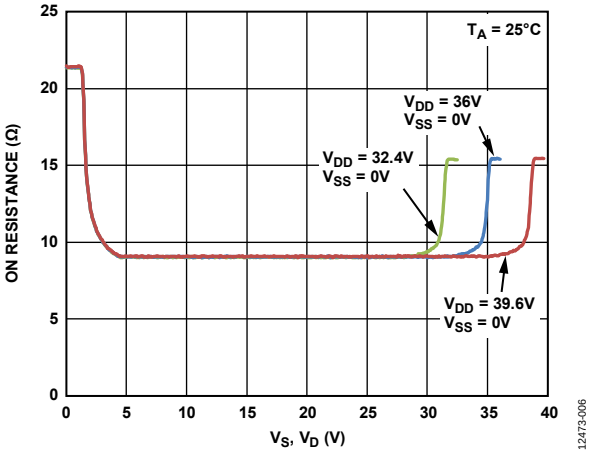


Figure 7. R_{ON} as a Function of V_S,V_D (36 V Single-Supply)

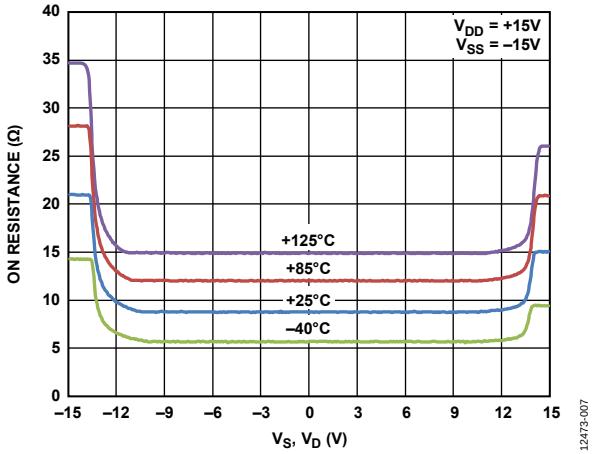


Figure 8. R_{ON} as a Function of V_S,V_D for Different Temperatures, ±15 V Dual-Supply

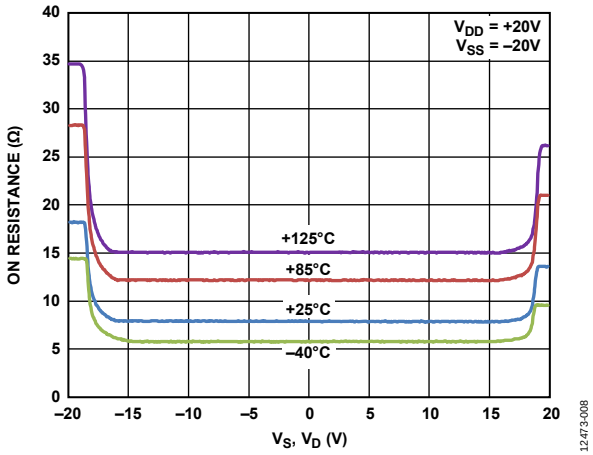


Figure 9. R_{ON} as a Function of V_S,V_D for Different Temperatures, ±20 V Dual-Supply

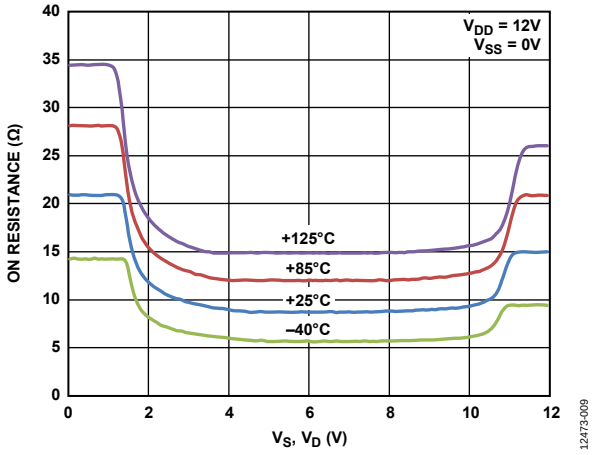


Figure 10. R_{ON} as a Function of V_S,V_D for Different Temperatures, 12 V Single-Supply

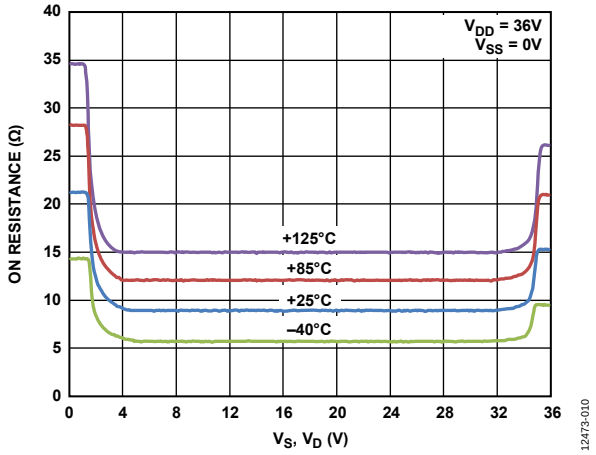


Figure 11. R_{ON} as a Function of V_S,V_D for Different Temperatures, 36 V Single-Supply

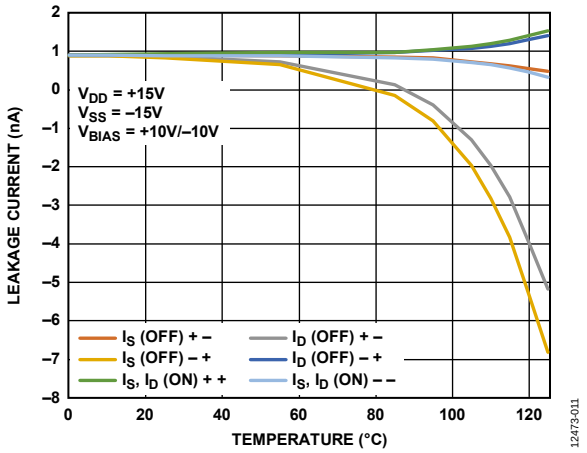


Figure 12. Leakage Current vs. Temperature, ±15 V Dual-Supply

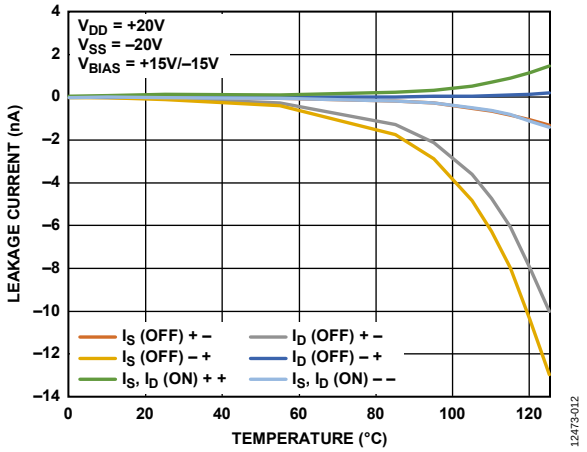


Figure 13. Leakage Current vs. Temperature, ±20 V Dual-Supply

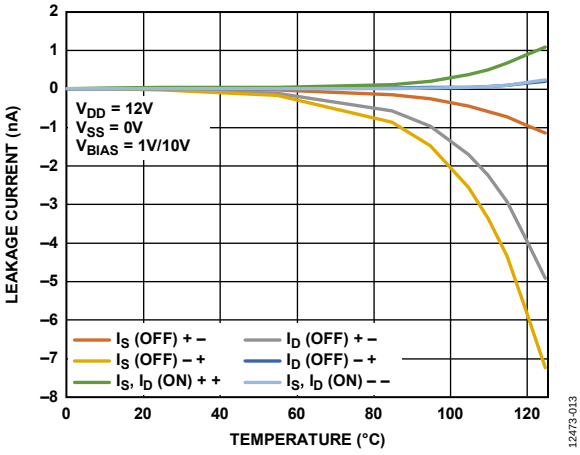


Figure 14. Leakage Current vs. Temperature, 12 V Single-Supply

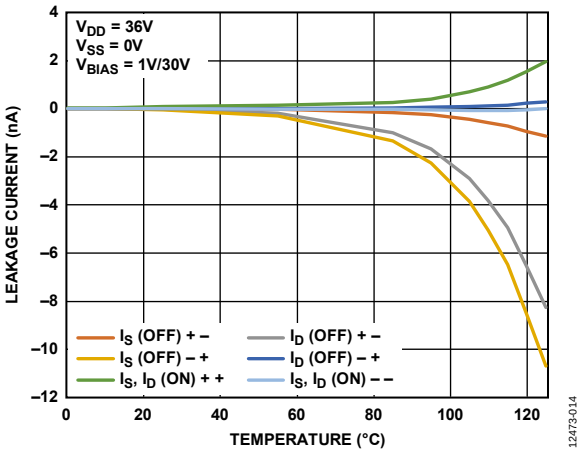


Figure 15. Leakage Current vs. Temperature, 36 V Single-Supply

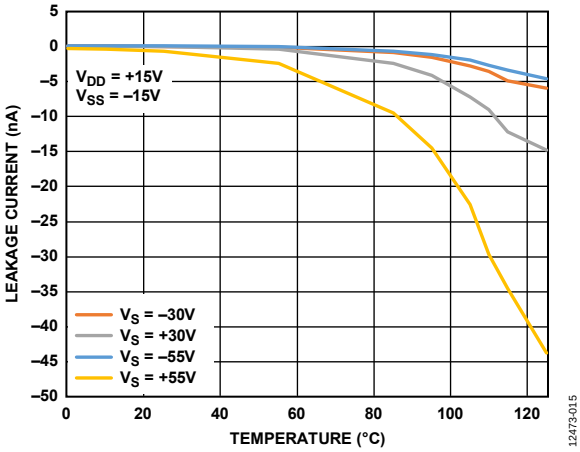


Figure 16. Overvoltage Drain Leakage Current vs. Temperature, ±15 V Dual-Supply

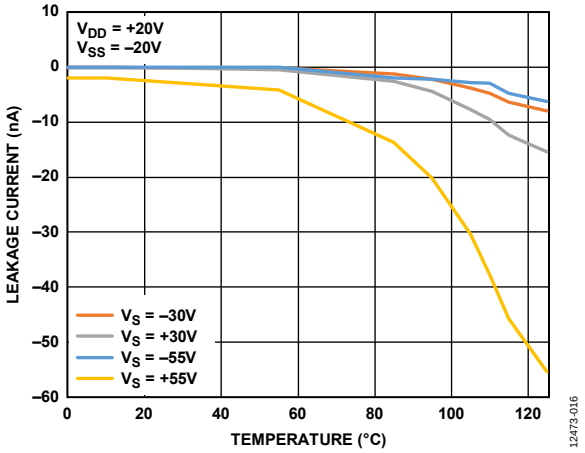


Figure 17. Overvoltage Drain Leakage Current vs. Temperature, ±20 V Dual-Supply

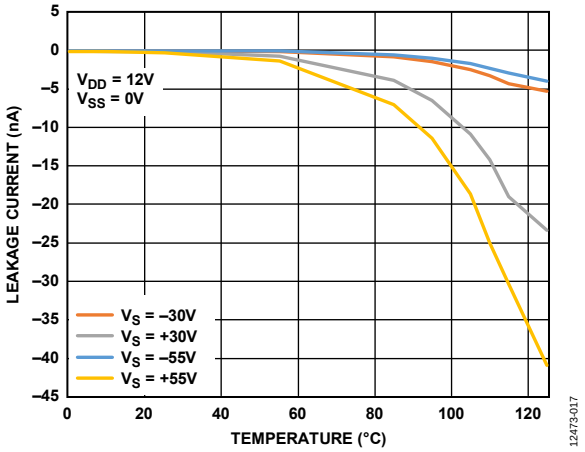


Figure 18. Overvoltage Drain Leakage Current vs. Temperature, 12 V Single-Supply

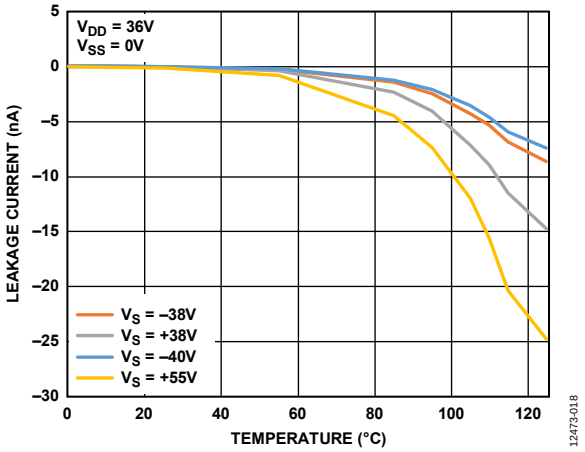


Figure 19. Overvoltage Drain Leakage Current vs. Temperature, 36 V Single-Supply

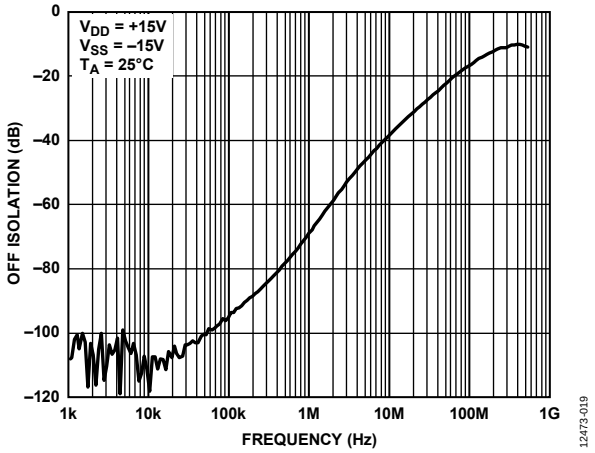


Figure 20. Off Isolation vs. Frequency, ±15 V Dual-Supply

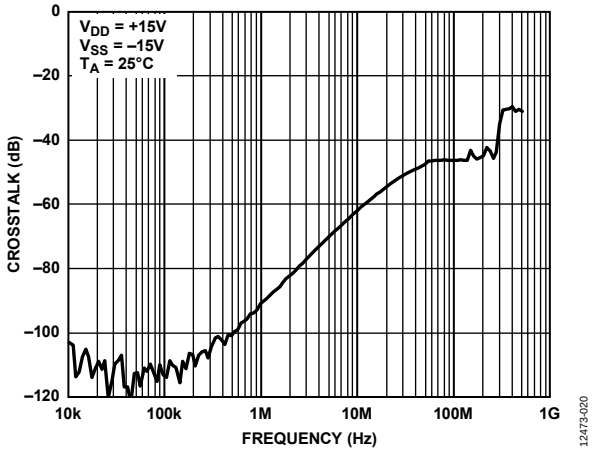


Figure 21. Crosstalk vs. Frequency, ±15 V Dual-Supply

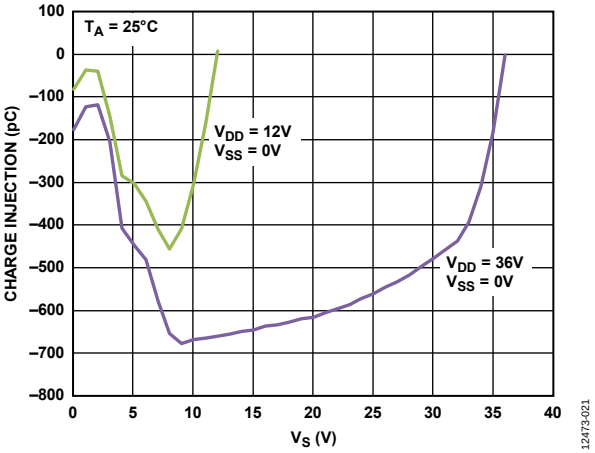


Figure 22. Charge Injection vs. Source Voltage (V_S), Single-Supply

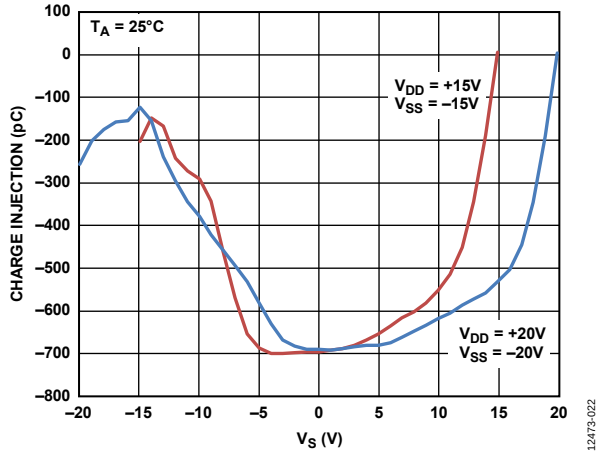


Figure 23. Charge Injection vs. Source Voltage (V_S), Dual-Supply

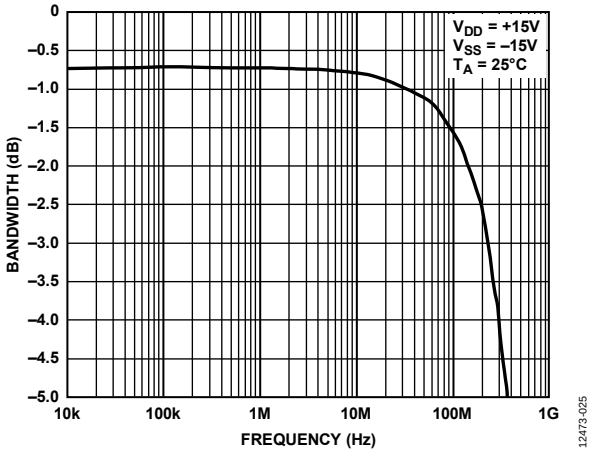


Figure 26. Bandwidth vs. Frequency

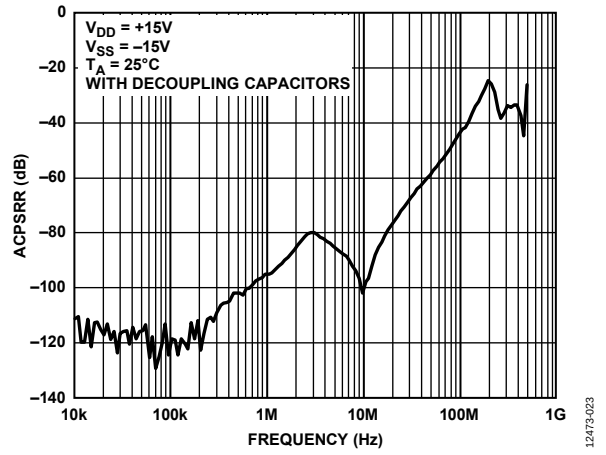


Figure 24. ACPSRR vs. Frequency, ±15 V Dual-Supply

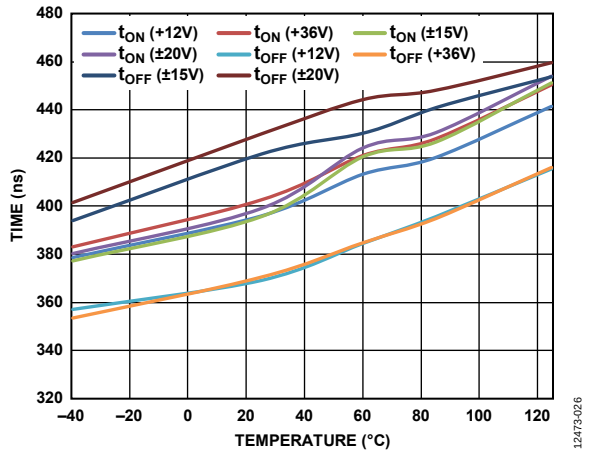


Figure 27. t_{ON}, t_{OFF} Times vs. Temperature

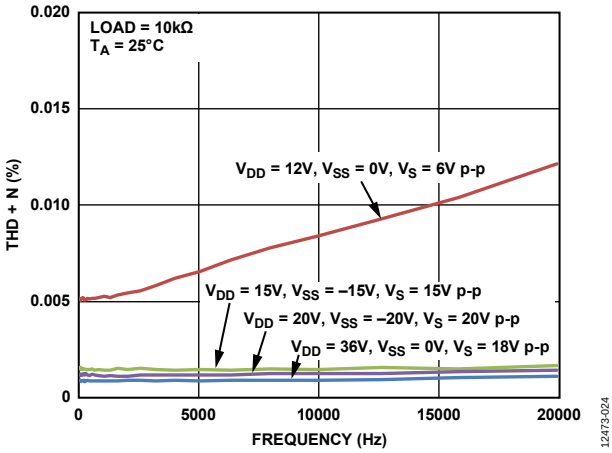


Figure 25. THD + N vs. Frequency, ±15 V Dual-Supply

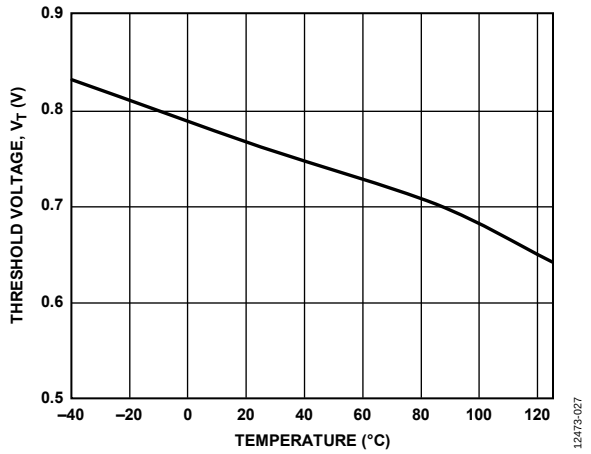


Figure 28. Threshold Voltage (V_T) vs. Temperature

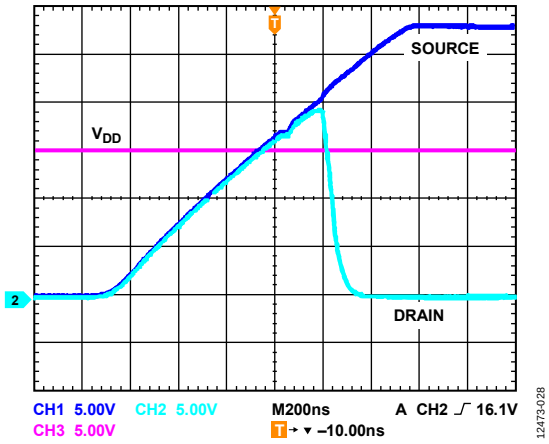


Figure 29. Drain Output Response to Positive Overvoltage

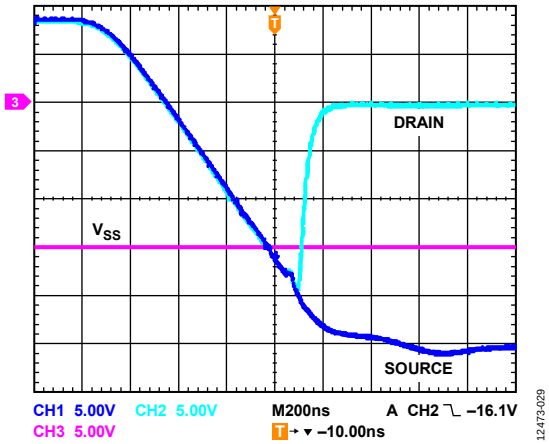


Figure 30. Drain Output Response to Negative Overvoltage

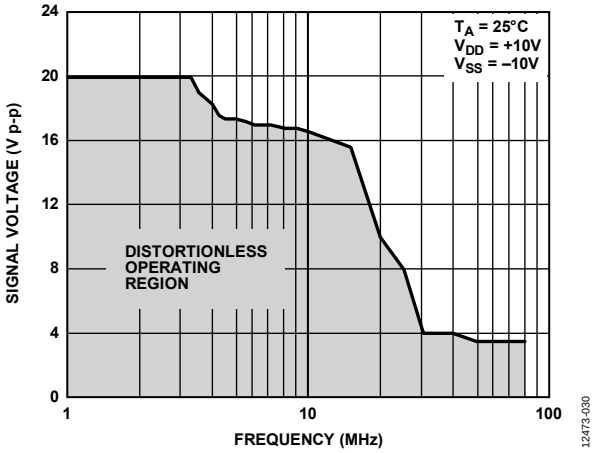


Figure 31. Large Voltage Signal Tracking vs. Frequency

TEST CIRCUITS

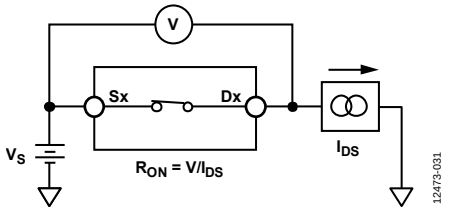


Figure 32. On Resistance

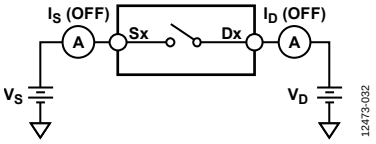


Figure 33. Off Leakage

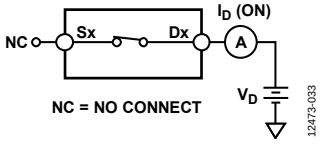


Figure 34. On Leakage

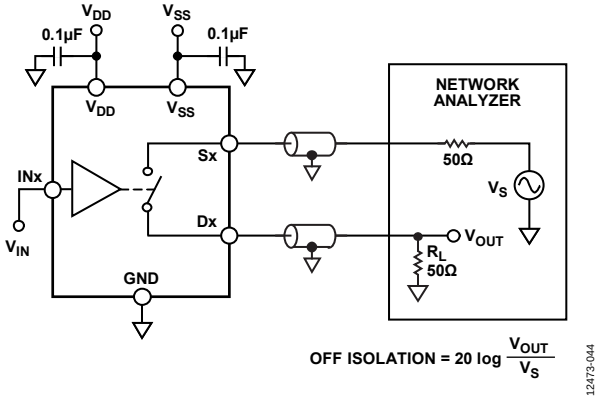


Figure 35. Off Isolation

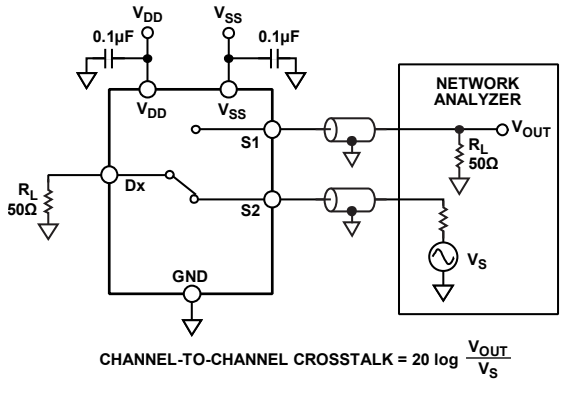


Figure 36. Channel-to-Channel Crosstalk

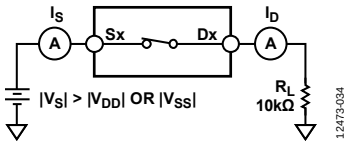


Figure 37. Switch Overvoltage Leakage

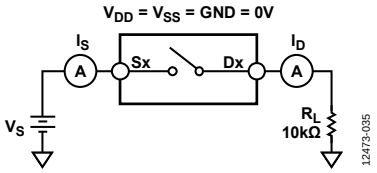


Figure 38. Switch Unpowered Leakage

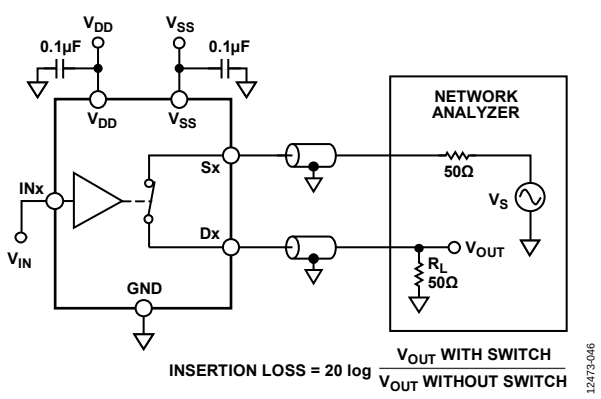


Figure 39. Bandwidth

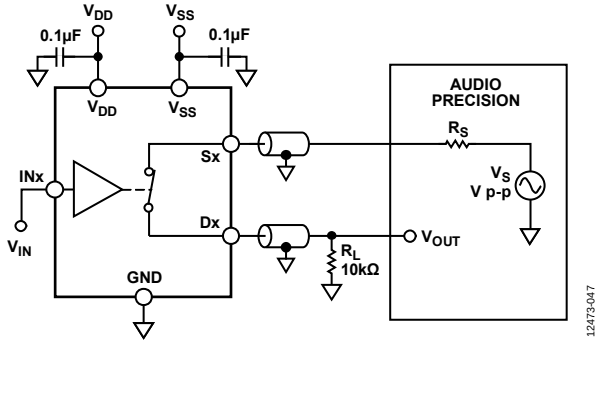


Figure 40. THD + N

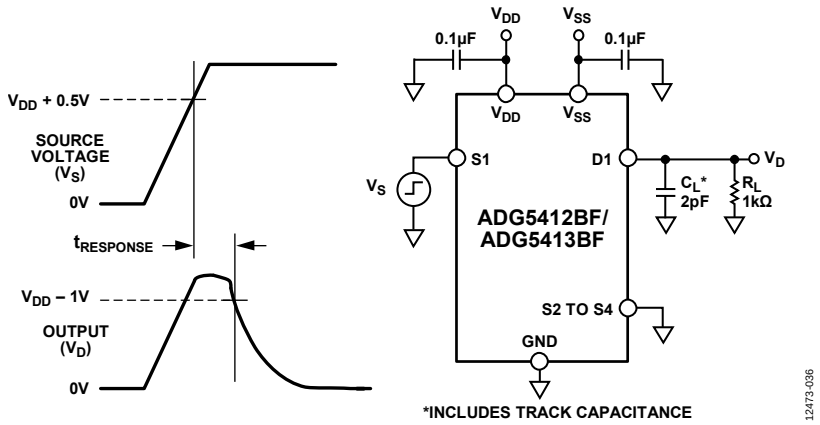


Figure 41. Overvoltage Response Time, $t_{RESPONSE}$

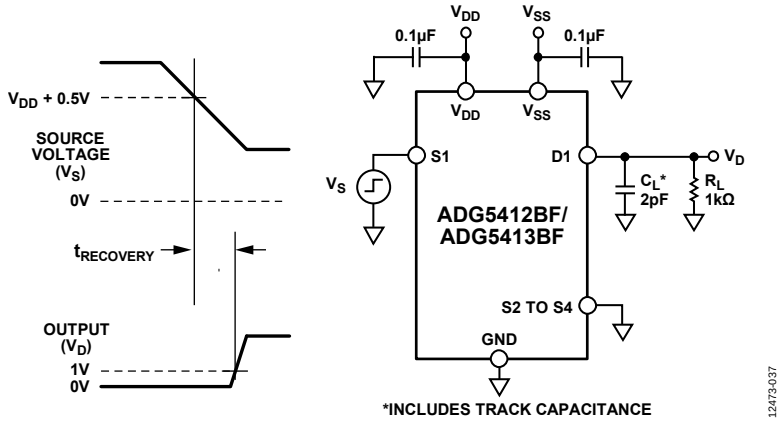


Figure 42. Overvoltage Recovery Time, $t_{RECOVERY}$

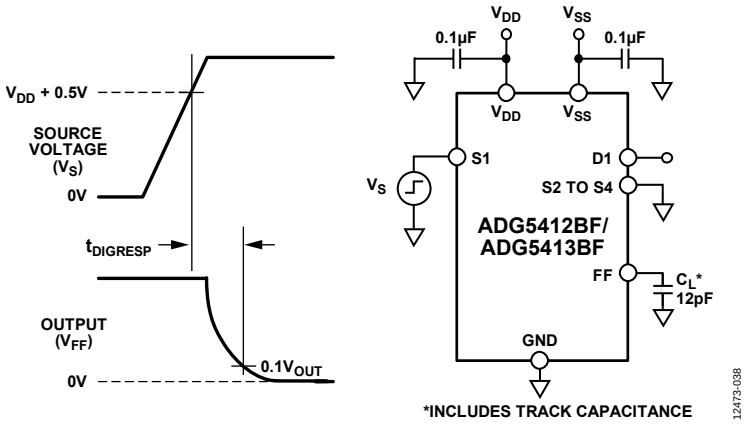


Figure 43. Interrupt Flag Response Time, $t_{DIGRESP}$

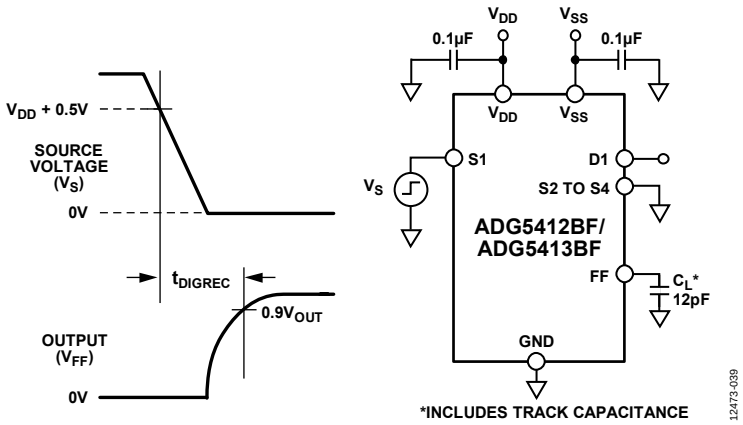


Figure 44. Interrupt Flag Recovery Time, t_{DIGREC}

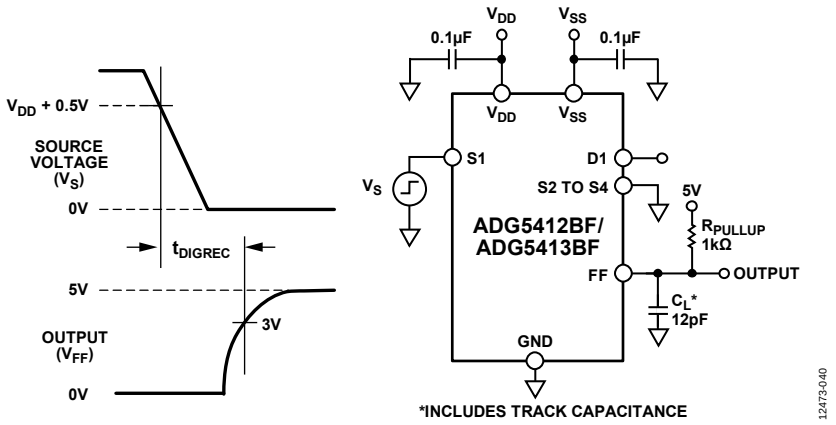


Figure 45. Interrupt Flag Recovery Time, t_{DIGREC}, with a 1 kΩ Pull-Up Resistor

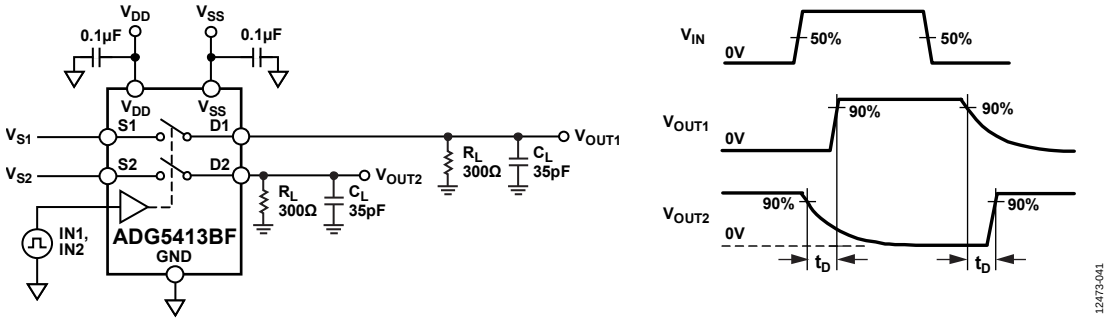


Figure 46. Break-Before-Make Time Delay, t_D

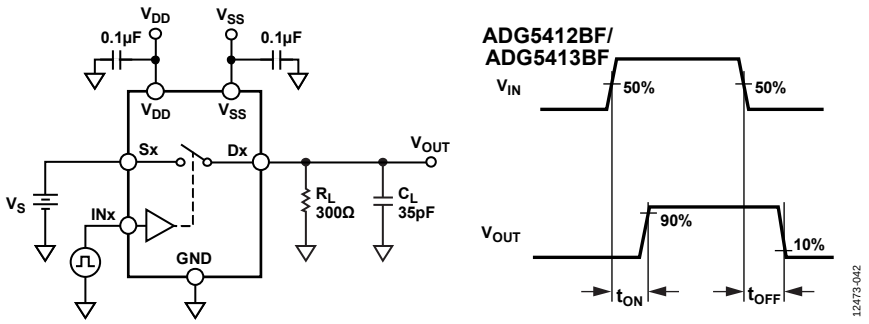


Figure 47. Switching Times, t_{ON} and t_{OFF}

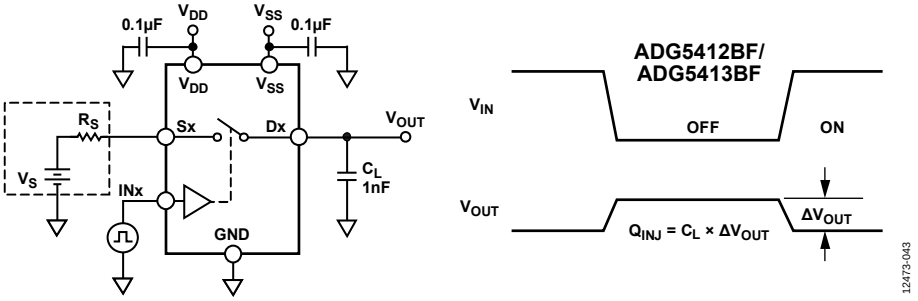


Figure 48. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on the Dx pins and the Sx pins, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on (see Figure 47).

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off (see Figure 47).

t_D
t_D represents the off time measured between the 90% point of both switches when switching from one address state to another.

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high (3 V), measured with respect to voltage on the Sx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion Plus Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages. See Figure 28.

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the ADG5412BF/ADG5413BF consists of a parallel pair of N-channel diffused metal-oxide semiconductor (NDMOS) and P-channel DMOS (PDMOS) transistors. This construction provides excellent performance across the signal range. The ADG5412BF/ADG5413BF channels operate as standard switches when input signals with a voltage between V_{SS} and V_{DD} are applied. For example, the on resistance is 10 Ω typically and the appropriate control pin, INx, controls the opening or closing of the switch.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on the source or drain pin with V_{DD} and V_{SS}. A signal is considered overvoltage if it exceeds the supply voltages by the voltage threshold, V_T. The threshold voltage is typically 0.7 V, but can range from 0.8 V (when operating at −40°C) down to 0.6 V at +125°C. See Figure 28 to see the change in V_T with operating temperature.

The maximum voltage that can be applied to any switch input is +55 V or −55 V. When the device is powered using the single-supply of 25 V or greater, the maximum signal level reduces from −55 V to −40 V at V_{DD} = 40 V to remain within the 80 V maximum rating. Construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

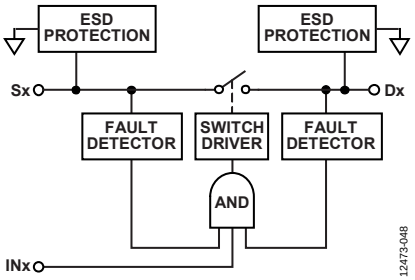


Figure 49. Switch Channel and Control Function

When an overvoltage condition is detected on either the source pin or drain pin, the switch is automatically opened regardless of the digital logic state, INx. The source and drain pins both become high impedance and ensure that no current flows through the switch. In Figure 29, the voltage on the drain pin can be seen to follow the voltage on the source pin until the switch has turned off completely and the drain voltage discharges through the load. The maximum voltage and the rate at which the output voltage discharges is dependent on the load at the pin. The ADG5412F/ADG5413F are pin-compatible devices that are overvoltage protected on the source pin only, with ESD diodes on the drain pin that limit the maximum voltage while the switch is opening.

During overvoltage conditions, the leakage current into and out of the switch pins is limited to tens of microamperes. This limit protects the switch and connected circuitry from over stresses as well as restricting the current drawn from the signal source. When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The ADG5412BF/ADG5413BF has an ESD rating of 3 kV for the human body model (HBM). ESD protection cells allow the voltage at the pins to exceed the supply voltage. See Figure 49 for a switch channel overview.

Trench Isolation

In the ADG5412BF and ADG5413BF, an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances. These devices pass a JESD78D latch-up test of ±500 mA for 1 sec, which is the harshest test in the specification.

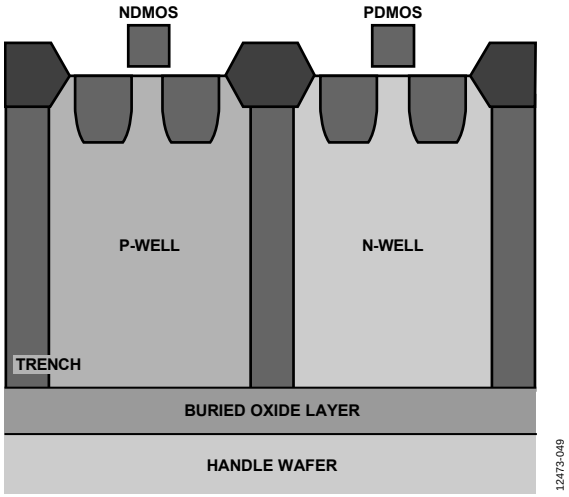


Figure 50. Trench Isolation

FAULT PROTECTION

When the voltages at the switch inputs exceed V_{DD} or V_{SS} by V_T, the switch turns off or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +55 V and −55 V are blocked in both the powered and unpowered condition as long as the 80 V limitation between the switch and supply pins is met.

Power-On Protection

The following three conditions must be satisfied for the switch to be in the on condition:

- V_{DD} to $V_{SS} \geq 8$ V
- Input signal is between $V_{SS} - V_T$ and $V_{DD} + V_T$
- Digital logic control input, INx, is turned on

When the switch is turned on, signal levels up to the supply rails are passed.

The switch responds to an analog input that exceeds V_{DD} or V_{SS} by a threshold voltage, V_T, by turning off. The absolute input voltage limits are −55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the switch pin returns to between V_{DD} and V_{SS}.

The fault response time ($t_{RESPONSE}$) when powered by ±15 V dual-supply is typically 460 ns, and the fault recovery time ($t_{RECOVERY}$) is 720 ns. These vary with supply voltages and output load conditions.

Exceeding ±55 V on any switch input may damage the ESD protection circuitry on the device.

The maximum stress across the switch channel is 80 V; therefore, the user must pay close attention to this limit if using the device in a multiplexed configuration and one channel is on while another channel is in a fault condition.

For example, consider the case where the device is set up in a multiplexer configuration as shown in Figure 51.

- V_{DD}/V_{SS} = ±22 V, S1 = 22 V, all switches are on
- D1 is externally multiplexed with D2; therefore, D1 and D2 = 22 V
- S2 has a −55 V fault and S3 has a +55 V fault
- The voltage between S2 and D1 or between S2 and D2 = +22 V − (−55 V) = +77 V
- The voltage between S3 and D3 = 55 V− 0 V = 55 V

These calculations are all within device specifications: 55 V maximum fault on switch inputs and a maximum of 80 V across the off switch channel.

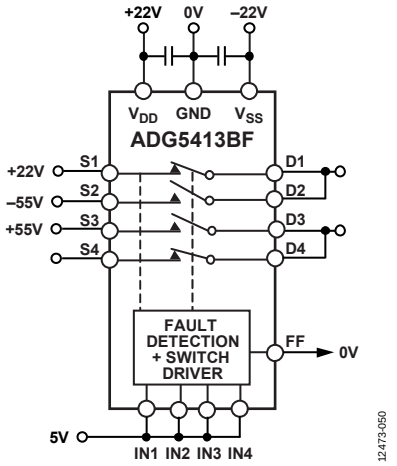


Figure 51. ADG5413BF in Multiplexer Configuration under Overvoltage Conditions

Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5412BF and the ADG5413BF can tolerate digital input signals being present on the device without power. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

Overvoltage Interrupt Flag

The voltages on the switch inputs of the ADG5412BF and the ADG5413BF are continuously monitored and the state of the switch is indicated by an active low digital output pin, FF.

The voltage on the FF pin indicates if any of the switch input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all switch pins are within normal operating range. If any switch pin voltage exceeds the supply voltage by V_T, the FF output reduces to below 0.8 V.

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required.

The ADG5412BF and the ADG5413BF can operate with bipolar supplies between ±5 V and ±22 V. The supplies on VDD and VSS need not be symmetrical but the VDD to VSS range must not exceed 44 V. The ADG5412BF and the ADG5413BF can also operate with single supplies between 8 V and 44 V with VSS connected to GND.

These devices are fully specified at ±15 V, ±20 V, +12 V, and +36 V supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the device is unpowered and signals from −55 V to +55 V can be applied without damaging the device. Only when the supplies are connected and a suitable digital control signal is placed on the INx pin does the switch channel close and then allow a signal to pass. Placing the ADG5412BF/ADG5413BF between external connectors and sensitive components offers protection in systems where a signal is presented to the switch pins before the supply voltages are available.

SIGNAL RANGE

The ADG5412BF/ADG5413BF switches have fault detection circuitry on their inputs that compares the voltage levels at the switch terminals with V_{DD} and V_{SS}, relative to ground. To protect downstream circuitry from overvoltages, supply the ADG5412BF/ADG5413BF by voltages that match the intended signal range. The low on-resistance switch allows signals up to the supply rails to be passed with very little distortion. A signal that exceeds the supply rail by the threshold voltage is then blocked. This offers protection to both the device and any downstream circuitry.

LOW IMPEDANCE CHANNEL PROTECTION

The ADG5412BF/ADG5413BF can be used as protective elements in signal chains that are sensitive to both channel impedance and overvoltage signals. Traditionally, series resistors are used to limit the current during an overvoltage condition to protect susceptible components. These series resistors affect the performance of the signal chain and reduce the precision that can be reached. A compromise must be reached on the value of the series resistance that is high enough to sufficiently protect sensitive components but low enough that the precision performance of the signal chain is not sacrificed.

The ADG5412BF/ADG5413BF enable the designer to remove these resistors and retain the precision performance without compromising the protection of the circuit.

HIGH VOLTAGE SURGE SUPPRESSION

The ADG5412BF/ADG5413BF is not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltages exceeding the breakdown voltage, use transient voltage suppressors (TVSs), or similar.

INTELLIGENT FAULT DETECTION

The ADG5412BF/ADG5413BF digital output pin, FF, can interface with a microprocessor or control system and be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt to start a variety of actions, such as

- Initiating investigation into the source of the overvoltage fault
- Shutting down critical systems in response to the overvoltage
- Data recorders marking data during these events as unreliable or out of specification

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5412BF/ADG5413BF are powered on and that all input voltages are within normal operating range before initiating operation.

The FF pin is a weak pull-up, which allows the signals to be combined into a single interrupt for larger modules that contain multiple devices.

The recovery time, t_{DIGREC}, can be decreased from a typical 60 µs to 600 ns by using a 1 kΩ pull-up resistor.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

Figure 31 illustrates the voltage range and frequencies that the ADG5412BF/ADG5413BF can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD}, keep the frequency below 3 MHz. If the required frequency is greater than 3 MHz, decrease the signal voltage appropriately to ensure signal integrity.

OUTLINE DIMENSIONS

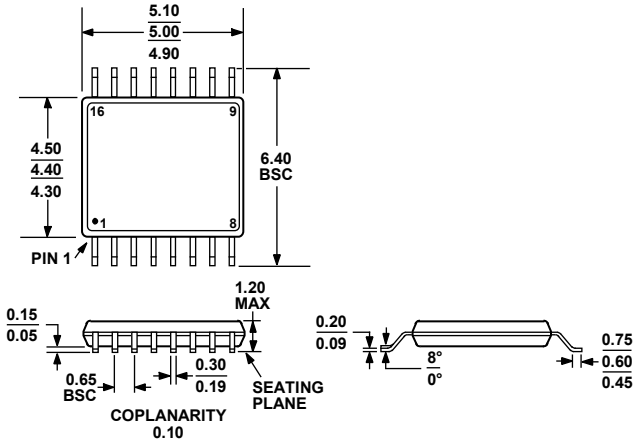


Figure 52. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

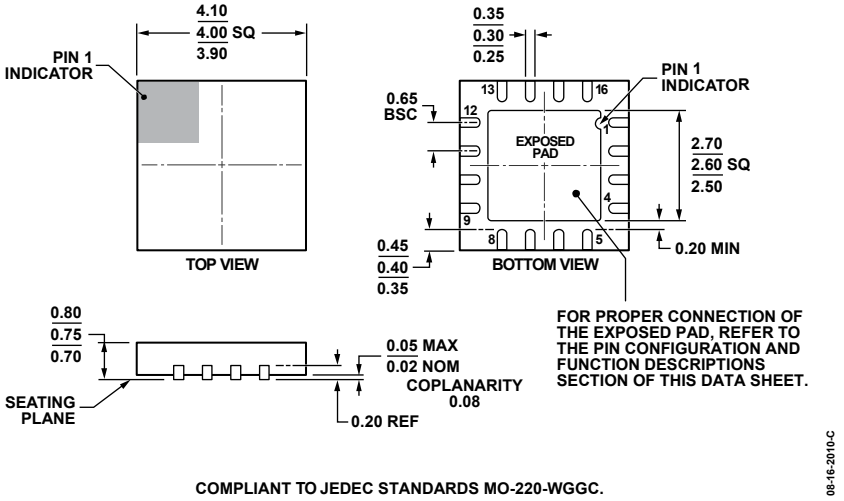


Figure 53. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5412BFBRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5412BFBRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5412BFBCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
EVAL-ADG5412BFEBZ		Evaluation Board	
ADG5413BFBRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5413BFBRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5413BFBCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17

[1] Z = RoHS Compliant Part.

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