CMOS 1.8 V to 5.5 V, 2.5 Ω 2:1 Mux/SPDT Switch in SOT-23

ADG719

FEATURES

1.8 V to 5.5 V single supply
4 Ω (max) on resistance
0.75 Ω (typ) on resistance flatness
−3 dB bandwidth > 200 MHz
Rail-to-rail operation
6-Lead SOT-23 package and 8-Lead MSOP package
Fast switching times:
t_{ON} = 12 ns
t_{OFF} = 6 ns
Typical power consumption: (< 0.01 µW)
TTL/CMOS compatible

APPLICATIONS

Battery-powered systems
Communication systems
Sample-and-hold systems
Audio signal routing
Video switching
Mechanical reed relay replacement

FUNCTIONAL BLOCK DIAGRAM

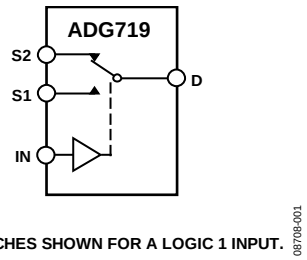


Figure 1.

GENERAL DESCRIPTION

The ADG719 is a monolithic CMOS SPDT switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

The ADG719 can operate from a single-supply range of 1.8 V to 5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc.

Each switch of the ADG719 conducts equally well in both directions when on. The ADG719 exhibits break-before-make switching action.

Because of the advanced submicron process, −3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG719 is available in a 6-lead SOT-23 package and an 8-lead MSOP package.

PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation. The ADG719 offers high performance, including low on resistance and fast switching times, and is fully specified and guaranteed with 3 V and 5 V supply rails.
2. Very Low R_{ON} (4 Ω Max at 5 V and 10 Ω Max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
3. Automotive Temperature Range: −40°C to +125°C.
4. On Resistance Flatness ($R_{FLAT(ON)}$) (0.75 Ω typ).
5. −3 dB Bandwidth > 200 MHz.
6. Low Power Dissipation. CMOS construction ensures low power dissipation.
7. Fast t_{ON}/t_{OFF}.
8. Tiny, 6-lead SOT-23 and 8-lead MSOP packages.

Rev. D
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REVISION HISTORY

3/10—Rev. C to Rev. D

Removed B Version Text ..... Throughout
Changes to Figure 1 1
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12/09—Rev. B to Rev. C

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7/02—Rev. A to Rev. B.

Changes to Product Name 1
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Additions to Product Highlights 1
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Edits to Absolute Maximum Ratings 4
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Edits to Ordering Guide 4
Added New TPCs 4 and 5 5
Replaced TPC 10 6
Test Circuits 6, 7, and 8 Replaced 7
Updated RM-8 and RT-6 Package Outlines 9

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})					V_S = 0 V to V_{DD}, I_S = −10 mA;
	2.5			Ω typ	See Figure 14
	4	5	7	Ω max	
On Resistance Match Between					
Channels (ΔR_{ON})		0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.4	0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.75			Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.2	1.5	Ω max	
LEAKAGE CURRENTS I_S (Off)					V_{DD} = 5.5 V
Source Off Leakage	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±0.35	1	nA max	See Figure 15
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V or V_S = V_D = 4.5 V;
	±0.25	±0.35	5	nA max	See Figure 16
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	7			ns typ	R_L = 300 Ω, C_L = 35 pF
			12	ns max	V_S = 3 V; See Figure 17
t_{OFF}	3			ns typ	R_L = 300 Ω, C_L = 35 pF
			6	ns max	V_S = 3 V; See Figure 17
Break-Before-Make Time Delay, t_D	8			ns typ	RL = 300 Ω, C_L = 35 pF,
			1	ns min	V_{S1} = V_{S2} = 3 V; See Figure 18
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See Figure 19
Channel-to-Channel Crosstalk	−62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See Figure 20
Bandwidth −3 dB	200			MHz typ	R_L = 50 Ω, C_L = 5 pF; See Figure 21
C_S (Off)	7			pF typ	
C_D, C_S (On)	27			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
					Digital inputs = 0 V or 5.5 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

[1] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH			0 V to V_{DD}	V	
Analog Signal Range					
On Resistance (R_{ON})	6	7		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA;
		10	12	Ω max	See Figure 14
On Resistance Match Between Channels (ΔR_{ON})		0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.4	0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source Off Leakage I_S (Off)	±0.01			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±0.35	1	nA max	See Figure 15
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V or V_S = V_D = 3 V;
	±0.25	±0.35	5	nA max	See Figure 16
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	10			ns typ	R_L = 300 Ω, C_L = 35 pF
			15	ns max	V_S = 2 V; See Figure 17
t_{OFF}	4			ns typ	R_L = 300 Ω, C_L = 35 pF
			8	ns max	V_S = 2 V; See Figure 17
Break-Before-Make Time Delay, t_D	8			ns typ	R_L = 300 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 2 V; See Figure 18
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See Figure 19
Channel-to-Channel Crosstalk	−62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See Figure 20
Bandwidth −3 dB	200			MHz typ	R_L = 50 Ω, C_L = 5 pF; See Figure 21
C_S (Off)	7			pF typ	
C_D, C_S (On)	27			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.3 V
					Digital inputs = 0 V or 3.3 V
I_{DD}	0.001			μA typ	
	1.0			μA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package, Power Dissipation	315 mW
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
SOT-23 Package, Power Dissipation	282 mW
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	220°C
Soldering (Pb-Free)	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec
ESD	1 kV

[1] Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

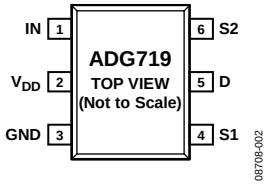


Figure 2. 6-Lead SOT-23

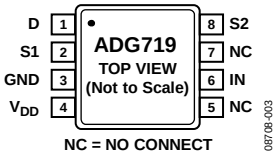


Figure 3. 8-Lead MSOP

Table 4. Pin description

Pin Number			
MSOP	**SOT-23**	**Mnemonic**	**Description**
1	5	D	Drain Terminal. Can be used as an input or output.
2	4	S1	Source Terminal. Can be used as an input or output.
3	3	GND	Ground (0 V) Reference Pin.
4	2	VDD	Most Positive Power Supply Pin.
5	–	NC	Not Internally Connected.
6	1	IN	Digital Switch Control Pin.
7	–	NC	Not Internally Connected.
8	6	S2	Source Terminal. Can be used as an input or output.

Table 5. Truth Table

ADG719 IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

TYPICAL PERFORMANCE CHARACTERISTICS

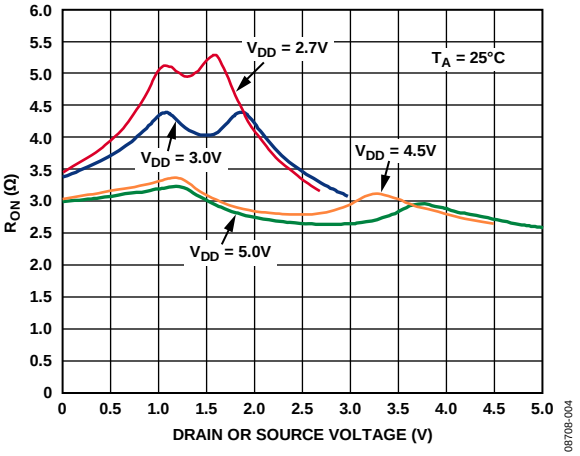


Figure 4. On Resistance vs. V_D (V_S), Single Supplies

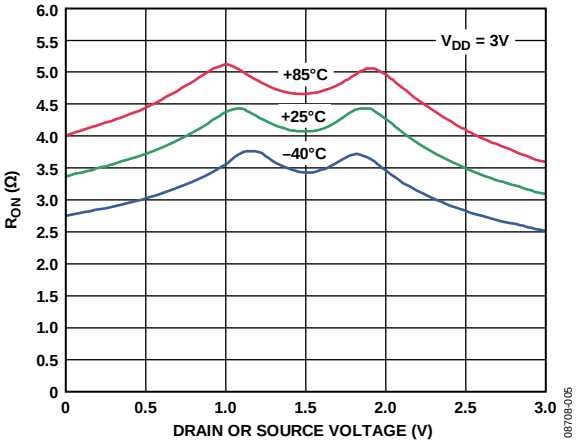


Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 3 V

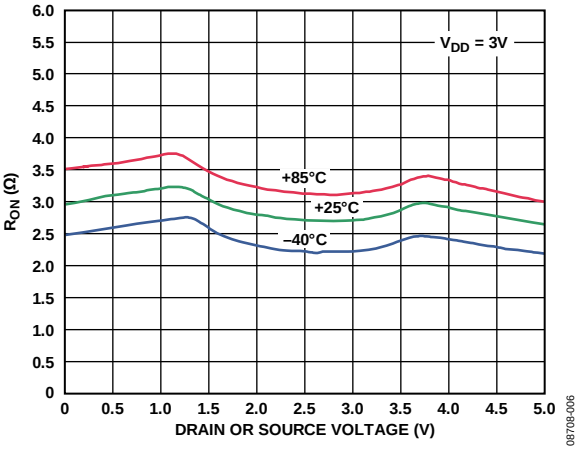


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 5 V

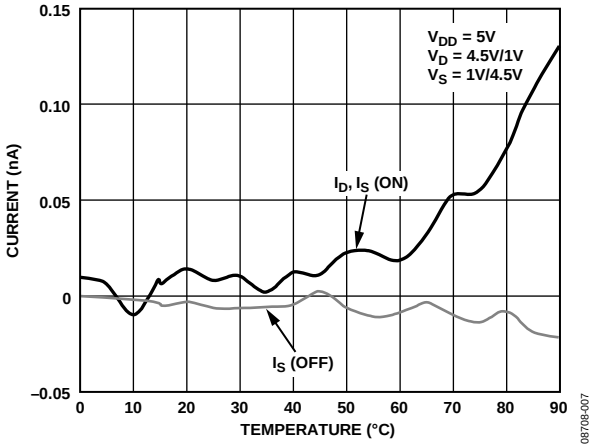


Figure 7. Leakage Currents vs. Temperature

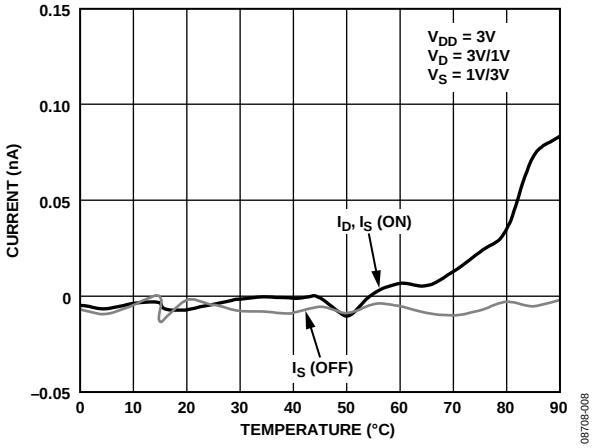


Figure 8. Leakage Currents vs. Temperature

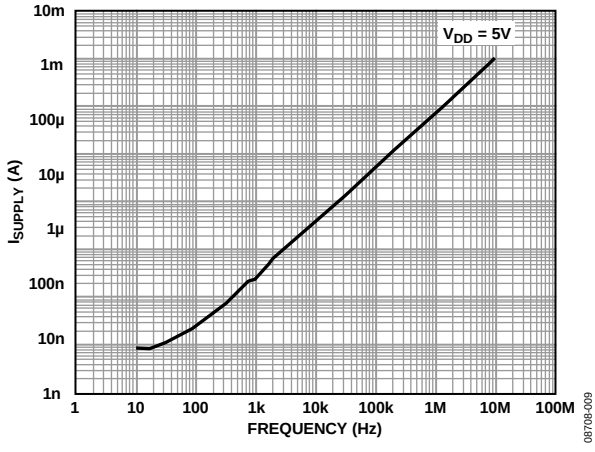


Figure 9. Supply Current vs. Input Switching Frequency

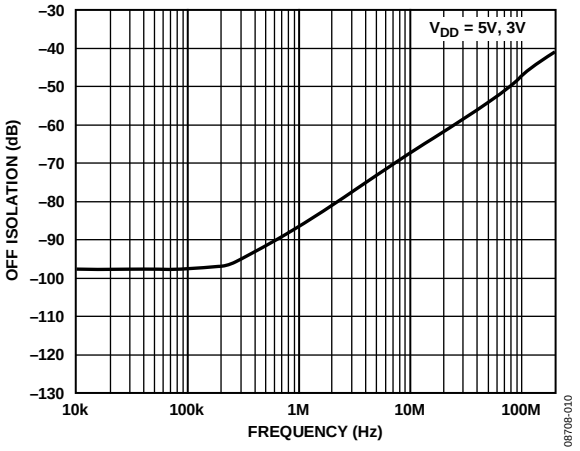


Figure 10. Off Isolation vs. Frequency

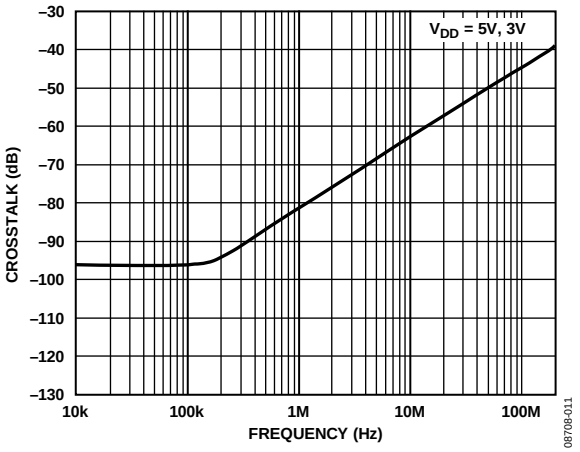


Figure 11. Crosstalk vs. Frequency

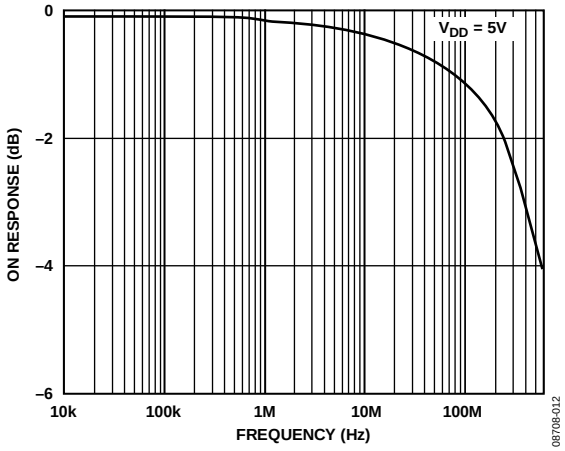


Figure 12. On Response vs. Frequency

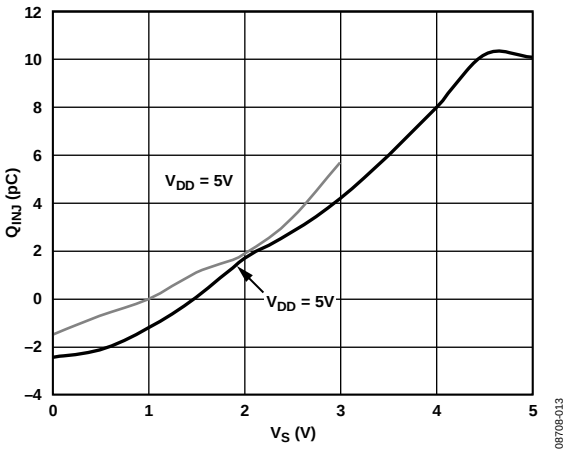


Figure 13. Charge Injection vs. Source Voltage

TEST CIRCUITS

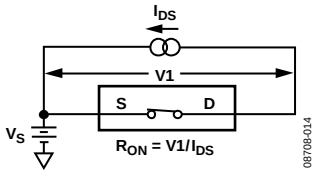


Figure 14. On Resistance

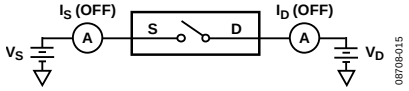


Figure 15. Off Leakage

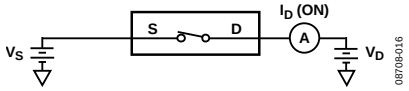


Figure 16. On Leakage

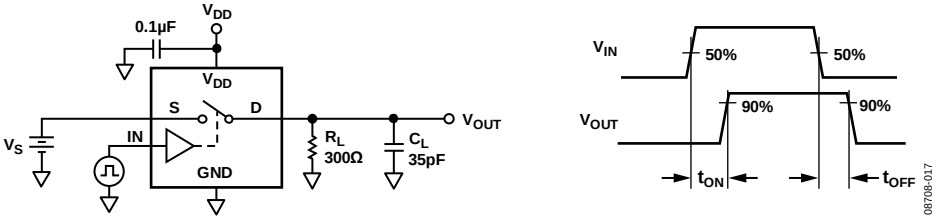


Figure 17. Switching Times

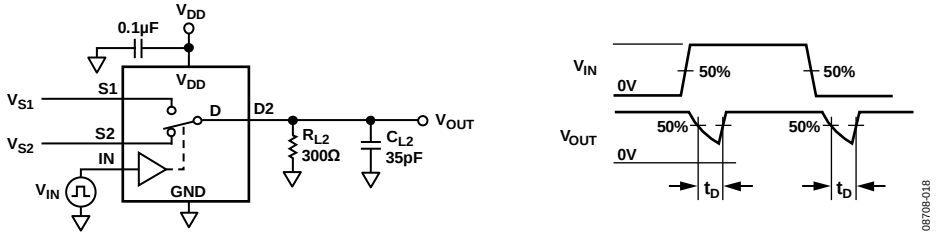


Figure 18. Break-Before-Make Time Delay, t_D

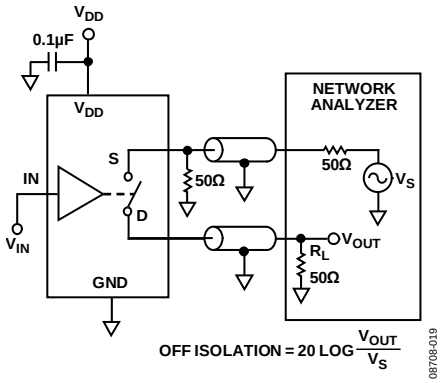


Figure 19. Off Isolation

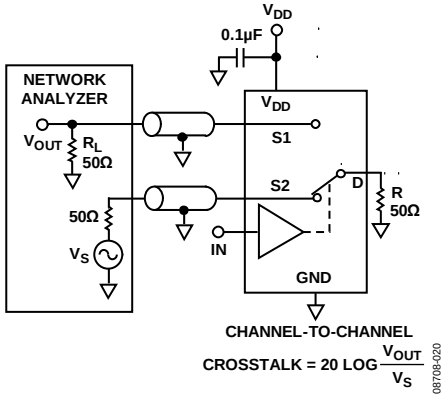


Figure 20. Channel-to-Channel Crosstalk

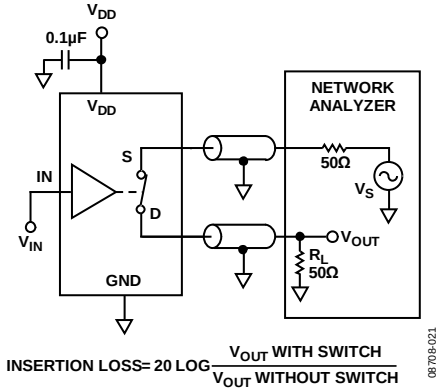


Figure 21. Bandwidth

TERMINOLOGY

R_{ON}
Ohmic Resistance between D and S.

ΔR_{ON}
On Resistance Match between Any Two Channels
that is, R_{ON} max − R_{ON} min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
Source Leakage Current with the Switch Off.

I_D, I_S (On)
Channel Leakage Current with the Switch On.

V_D (V_S)
Analog Voltage on Terminals D and S.

C_S (Off)
Off Switch Source Capacitance.

C_D, C_S (On)
On Switch Capacitance.

t_{ON}
Delay between Applying the Digital Control Input and the Output Switching On.

t_{OFF}
Delay between Applying the Digital Control Input and the Output Switching Off.

t_D
Off Time or On Time Measured between the 90% Points of Both Switches, when Switching From One Address State to Another.

Crosstalk
A Measure of Unwanted Signal That Is Coupled through from One Channel to Another as a Result of Parasitic Capacitance.

Off Isolation
A Measure of Unwanted Signal Coupling through an Off Switch.

Bandwidth
The Frequency at Which the Output is Attenuated by −3 dBs.

On Response
The Frequency Response of the On Switch.

Insertion Loss
Loss due to On Resistance of Switch.

APPLICATIONS INFORMATION

The ADG719 belongs to Analog Devices' new family of CMOS switches. This series of general-purpose switches has improved switching times, lower on resistance, higher bandwidths, low power consumption, and low leakage currents.

ADG719 SUPPLY VOLTAGES

Functionality of the ADG719 extends from 1.8 V to 5.5 V single supply, which makes it ideal for battery-powered instruments where power efficiency and performance are important design parameters.

It is important to note that the supply voltage effects the input signal range, the on resistance, and the switching times of the part. By taking a look at the Typical Performance Characteristics and the Specifications, the effects of the power supplies can be clearly seen.

For V_{DD} = 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.

ON RESPONSE VS. FREQUENCY

Figure 22 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances will further degrade some performance. These capacitances affect feedthrough, crosstalk, and system bandwidth.

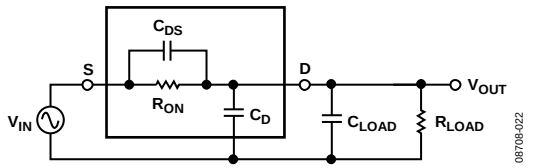


Figure 22. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 22) is of the form A(s) shown below:

$$A(s) = R_T\left[\frac{s(R_{ON}\ C_{DS}) + 1}{s(R_T\ R_{ON}\ C_T) + 1}\right]$$

where:

$R_T = R_{LOAD}/(R_{LOAD} + R_{ON})$

$C_T = C_{LOAD} + C_D + C_{DS}$

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function *A(s)*. Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with C_{DS} and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of *A(s)*.

The dominant effect of the output capacitance, C_D, causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth, a switch must have a low input and output capacitance and low on resistance. The On Response vs. Frequency plot for the ADG719 can be seen in Figure 12.

OFF ISOLATION

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, C_{DS}, couples the input signal to the output load when the switch is off, as shown in Figure 23.

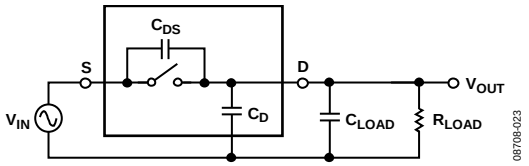
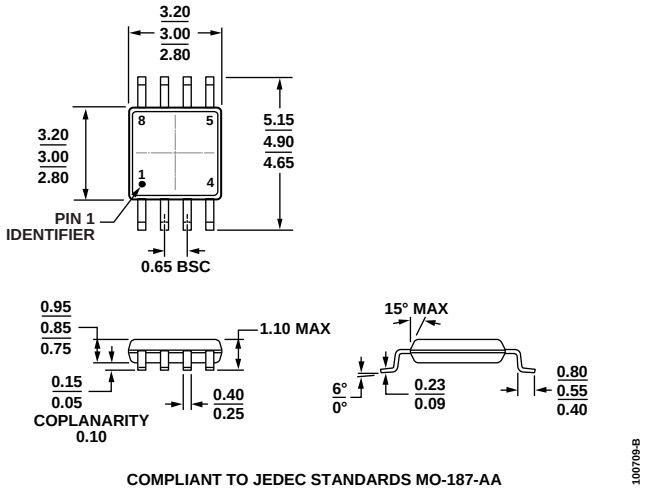


Figure 23. Off Isolation Is Affected by External Load Resistance and Capacitance

The larger the value of C_{DS}, the larger the values of feedthrough that will be produced. Figure 10 illustrates the drop in off isolation as a function of frequency. From dc to roughly 200 kHz, the switch shows better than −95 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than −67 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest C_{DS} possible. The values of load resistance and capacitance also affect off isolation, since they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

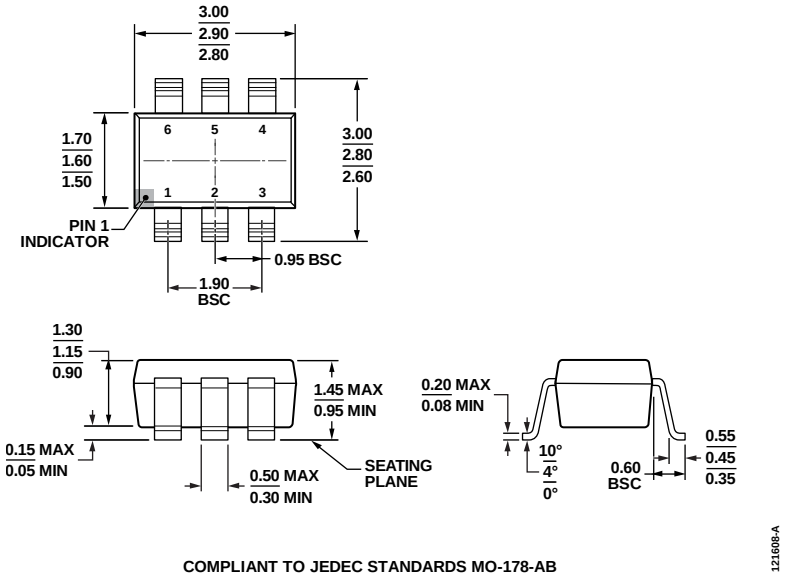
$$A(s) = \left[\frac{s(R_{LOAD}\ C_{DS})}{s(R_{LOAD})\,(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 24. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 25. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG719BRM	−40°C to +125°C	8-Lead MSOP	RM-8	S5B
ADG719BRM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	S5B
ADG719BRM-REEL7	−40°C to +125°C	8-Lead MSOP	RM-8	S5B
ADG719BRMZ	−40°C to +125°C	8-Lead MSOP	RM-8	S5B#
ADG719BRMZ-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	S5B#
ADG719BRMZ-REEL7	−40°C to +125°C	8-Lead MSOP	RM-8	S5B#
ADG719BRT-REEL	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B
ADG719BRT-REEL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B
ADG719BRT -500RL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B
ADG719BRTZ -500RL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B#
ADG719BRTZ-R2	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B#
ADG719BRTZ-REEL	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B#
ADG719BRTZ-REEL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	S5B#

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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