EMI-/EMC-Compliant ±15 kV ESD Protected, Dual RS-232 Port with Standby

ADM2209E

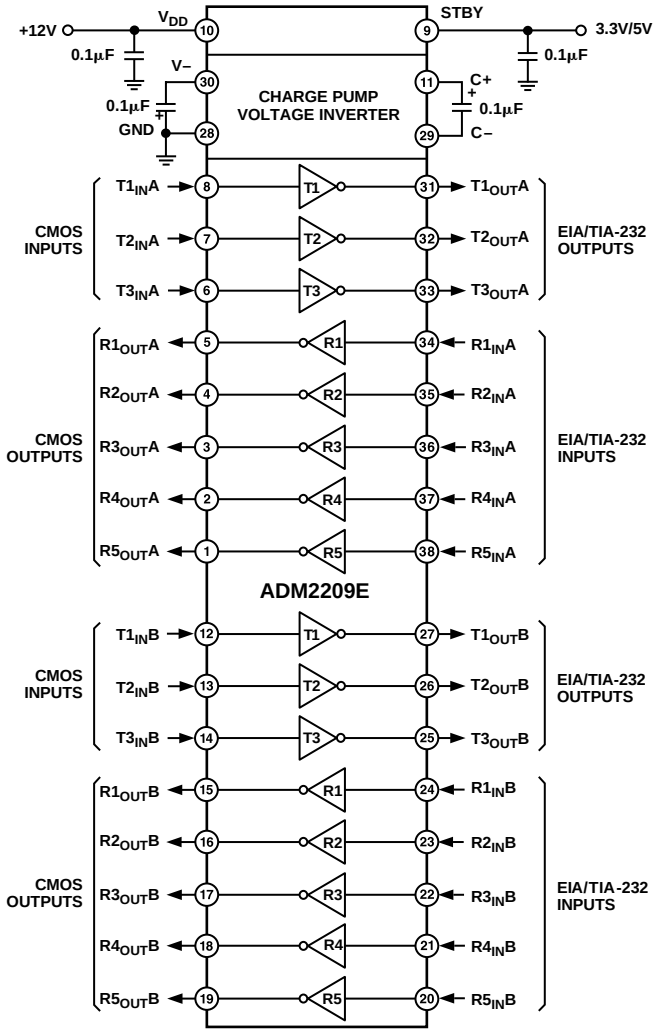
FEATURES

Two Complete Serial Ports, Six Drivers and Ten Receivers
Operates with 3 V or 5 V Logic
Low Power CMOS: <5 mA Operation
Low Standby Current: 100 μA
460 kbit/s Data Rate Guaranteed Laplink®-Compatible
0.1 μF Charge Pump Capacitors
Single +12 V Power Supply
+3.3 V/+5 V Standby Supply
One Receiver on Each Port Active in Standby
Complies with 89/336/EEC EMC Directive
ESD Protection to IEC1000-4-2 (801.2)
±8 kV: Contact Discharge
±15 kV: Air-Gap Discharge
±15 kV: Human Body Model
Electrical Fast Transient (EFT) Immunity (IEC1000-4-4)
Low EMI Emissions (EN55022)
Eliminates Costly TransZorbs®
Conforms to EIA/TIA-232-E Specifications
Fail-Safe Receiver Outputs

APPLICATIONS

Personal Computers
Printers
Peripherals
Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM2209E is a complete, dual RS-232 port on a single chip, containing six drivers and ten receivers and fully meeting EIA-232 and V.28 specifications. The device features an on-board dc-to-dc converter to generate a –12 V power rail, eliminating the need for a negative power supply.

The ADM2209E is suitable for operation in harsh electrical environments and is compliant with the EU directive on EMC (89/336/EEC). Both the level of emissions and immunity are in compliance. EM immunity includes ESD protection in excess of ±15 kV on all I-O lines (1000-4-2), Electrical Fast Transient protection (1000-4-4) and Radiated Immunity (1000-4-3). EM emissions include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

The ADM2209E conforms to the EIA-232E and CCITT V.28 specifications and operates at data rates up to 460 kbps.

In standby mode, one receiver on each port (R5) remains active to allow monitoring of peripheral devices while the rest of the system is in power-saving mode. This feature allows the ADM2209E to wake up the system when a peripheral device begins communication.

The ADM2209E is available in a 38-lead TSSOP package.

Laplink is a registered trademark of Traveling Software, Inc.
TransZorb is a registered trademark of General Semiconductor Industries, Inc.

REV. 0

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ADM2209E–SPECIFICATIONS (V_{DD} = 10.8 V to 13.2 V, V_{STBY} = 3.3 V ± 5% or 5 V ± 10%, C1 = C2 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ[1]	Max	Units	Test Conditions/Comments
OPERATING CONDITIONS					
Operating Voltage Range, V_{DD}	+10.8	+12	+13.2	V	
Standby Voltage Range, V_{STBY}	+3.15		+5.5	V	
V_{DD} Power Supply Current[2]			5	mA	No Load, All Driver Inputs at 0.8 V or 2 V, All Receiver Inputs at +15 V or –15 V
V_{STBY} Supply Current		100	200	µA	No Load, All Tx IN at V_{STBY} or Open
TRANSMITTER (DRIVER) CMOS INPUTS					
Input Pull-Up Current		10	25	µA	Transmitter Input at GND
High Level Input Voltage, V_{INH}	2.1			V	
Low Level Input Voltage, V_{INL}			0.4	V	
TRANSMITTER (DRIVER) EIA-232 OUTPUTS					
Output Voltage Swing	±5.0	±9.0		V	All Transmitter Outputs Loaded with 3 kΩ to GND
Output Short-Circuit Current, I_{OS}	±5	±15	±30	mA	V_O = 0 V, V_{IN} = 0.8 V[3]
Output Resistance	300			Ω	V_{DD} = 0 V, V_{STBY} = 0 V, V_{IN} = ±2 V
RECEIVER EIA-232 INPUTS					
Input Voltage Range	–15		+15	V	
Input Low Threshold, V_{TL}	0.4	1.45		V	
Input High Threshold, V_{TH}		1.7	2.4	V	
Input Hysteresis		0.25		V	
Input Resistance, R_{IN}	3	5	7	kΩ	V_{IN} = ±15 V
RECEIVER OUTPUTS[4]					
High Level Output Voltage, V_{OH}	2.4			V	I_{OH} = –40 µA
Low Level Output Voltage, V_{OL}		0.2	0.4	V	I_{OL} = +1.6 mA
Output Leakage Current (Except R5A, R5B)		0.05	±5	µA	V_{DD} = 0 V
DRIVER SWITCHING CHARACTERISTICS[5]					
Maximum Data Rate	460			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 470 pF
	460			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF, T_A = 0°C to +85°C, 5 V ± 10% Only
	920			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 470 pF, V_{STBY} = 5 V ± 5%, V_{DD} = 12 V ± 5%
Propagation Delay, High to Low, T_{PHL}		1		µs	R_L = 3 kΩ, C_L = 1000 pF (Figures 1 and 2)
Propagation Delay, Low to High, T_{PLH}		1		µs	R_L = 3 kΩ, C_L = 1000 pF (Figures 1 and 2)
Transition Region Slew Rate	6	16		V/µs	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 470 pF
Transition Region Slew Rate (5 V)	4	16		V/µs	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF, V_{STBY} = 5 V ± 10% Only. Measured from +3 V to –3 V or Vice Versa
RECEIVER SWITCHING CHARACTERISTICS					
Maximum Data Rate	920			kbps	C_L = 150 pF, V_{STBY} = 5 V ± 5% Only
	460			kbps	C_L = 150 pF
Propagation Delay, R1–R4		0.4	0.75	µs	C_L = 150 pF
Propagation Delay, R5		1	2	µs	C_L = 150 pF
Output Rise Time, t_r		30		ns	Figures 3 and 4
Output Fall Time, t_f		30		ns	
ESD AND EMC					
ESD Protection (I-O Pins)		±15		kV	Human Body Model
		±15		kV	IEC1000-4-2 Air Discharge
		±8		kV	IEC1000-4-2 Contact Discharge
(All Other Pins)		±2.5		kV	Human Body Model, MIL-STD-883B
EFT Protection (I-O Pins)		±2		kV	IEC1000-4-4
EMI Immunity		10		V/m	IEC1000-4-3

NOTES

[1]All typicals are given for V_{DD} = +12 V, V_{STBY} = 5 V, T_A = +25°C.

[2]Current into device pins is defined as positive. Current out-of-device pins is defined as negative. All voltages are referred to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if –6 V is a maximum, the typical value (–6.8 V) is more negative.

[3]Only one driver output shorted at a time.

[4]If receiver inputs are unconnected, receiver output is a logic high.

[5]Refer to typical curves. Driver output slew rate is measured from the +3.0 V to the –3.0 V level on the output waveform. Slew rate is determined by load capacitance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

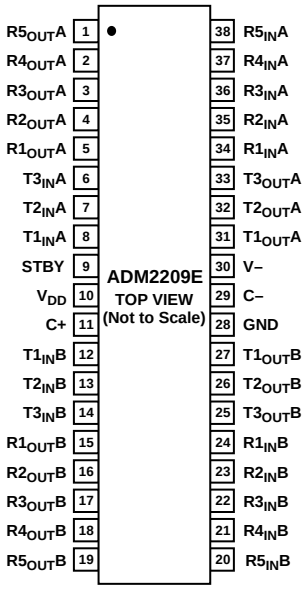
V_{STBY} . . . . . –0.3 V to +7 V
V_{DD} . . . . . +14 V
Input Voltages
  Driver Inputs Tn_{IN}A/B . . . . . –0.3 V to (V_{STBY}, +0.3 V)
  Receiver Inputs Rn_{IN}A/B . . . . . ±25 V
Output Voltages
  Driver Outputs Tn_{OUT}A/B . . . . . ±15 V
  Receiver Outputs Rn_{OUT}A/B . . . . –0.3 V to (V_{STBY}, +0.3 V)
Short Circuit Duration
  Tn_{OUT}A/B . . . . . Continuous
Power Dissipation
  RU-38 TSSOP (Derate 12 mW/°C Above +70°C) . . . 1488 mW
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
ESD Rating (MIL-STD-883B) (I-O Pins) . . . . . ±15 kV
(Except I-O) . . . . . ±2.5 kV
(IEC1000-4-2 Air) (I-O Pins) . . . . . ±15 kV
(IEC1000-4-2 Contact) (I-O Pins) . . . . . ±8 kV
EFT Rating (IEC1000-4-4) (I-O Pins) . . . . . ±2 kV

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM2209EARU	–40°C to +85°C	RU-38

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	$R5_{OUT}A$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
2	$R4_{OUT}A$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
3	$R3_{OUT}A$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
4	$R2_{OUT}A$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
5	$R1_{OUT}A$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
6	$T3_{IN}A$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
7	$T2_{IN}A$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
8	$T1_{IN}A$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
9	STBY	3.3 V/5 V Standby Power Supply for Receiver R5 in Ports A and B
10	V_{DD}	Positive Power Supply, Nominally +12 V
11	C+	Positive Terminal of C1 (If C1 is polarized capacitor.)
12	$T1_{IN}B$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
13	$T2_{IN}B$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
14	$T3_{IN}B$	Driver Input (3.3 V/5 V TTL/CMOS Logic Levels)
15	$R1_{OUT}B$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
16	$R2_{OUT}B$	Receiver Output (3 V/5 V TTL/CMOS Logic Levels)
17	$R3_{OUT}B$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
18	$R4_{OUT}B$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
19	$R5_{OUT}B$	Receiver Output (3.3 V/5 V TTL/CMOS Logic Levels)
20	$R5_{IN}B$	Receiver Input (EIA-232 Signal Levels)
21	$R4_{IN}B$	Receiver Input (EIA-232 Signal Levels)
22	$R3_{IN}B$	Receiver Input (EIA-232 Signal Levels)
23	$R2_{IN}B$	Receiver Input (EIA-232 Signal Levels)
24	$R1_{IN}B$	Receiver Input (EIA-232 Signal Levels)
25	$T3_{OUT}B$	Driver Output (EIA-232 Signal Levels)
26	$T2_{OUT}B$	Driver Output (EIA-232 Signal Levels)
27	$T1_{OUT}B$	Driver Output (EIA-232 Signal Levels)
28	GND	Ground Pin. Must Be Connected to 0 V
29	C–	Negative Terminal of C1 (If C1 is polarized capacitor.)
30	V–	Inverter Output (–12 V Nominal)–Terminal of C2 (If C2 is polarized capacitor.)
31	$T1_{OUT}A$	Driver Output (EIA-232 Signal Levels)
32	$T2_{OUT}A$	Driver Output (EIA-232 Signal Levels)
33	$T3_{OUT}A$	Driver Output (EIA-232 Signal Levels)
34	$R1_{IN}A$	Receiver Input (EIA-232 Signal Levels)
35	$R2_{IN}A$	Receiver Input (EIA-232 Signal Levels)
36	$R3_{IN}A$	Receiver Input (EIA-232 Signal Levels)
37	$R4_{IN}A$	Receiver Input (EIA-232 Signal Levels)
38	$R5_{IN}A$	Receiver Input (EIA-232 Signal Levels)

Test Circuits

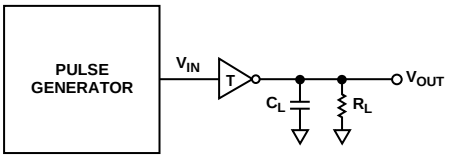


Figure 1. Test Circuit for Driver Propagation Delay and Transition Time

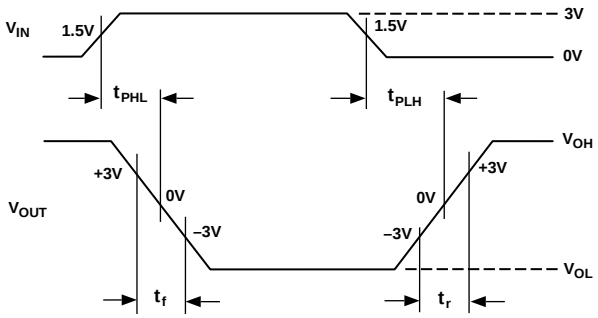


Figure 2. Driver Propagation Delay and Transition Time Waveforms

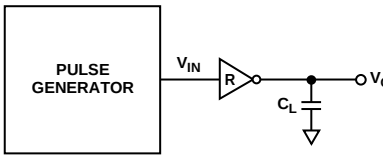


Figure 3. Test Circuit for Receiver Propagation Delay and Transition Time

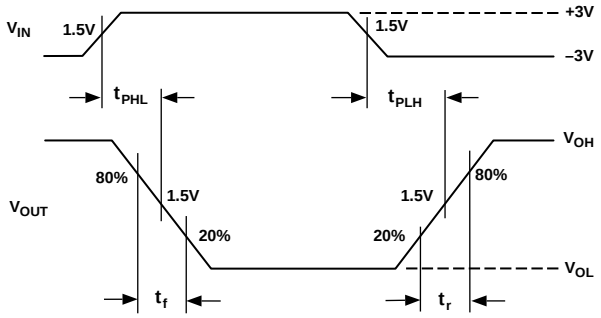


Figure 4. Receiver Propagation Delay and Transition Time Waveforms

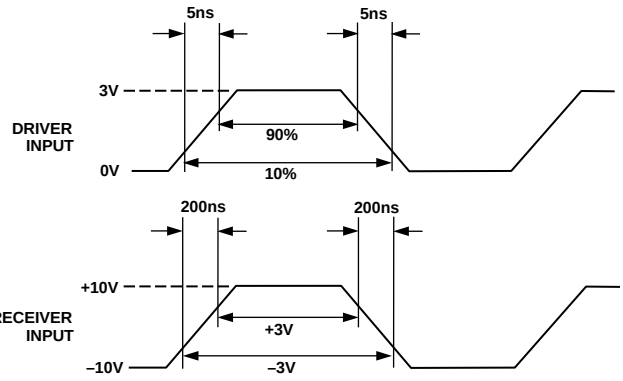


Figure 5. Input Waveforms Used in AC Performance Tests

Typical Performance Curves (V_{STBY} = +5 V)

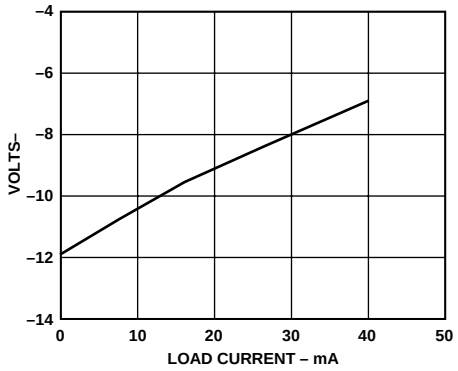


Figure 6. V– vs. Load Current

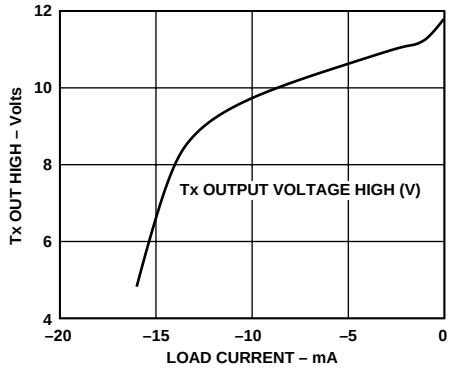


Figure 7. Transmitter Output Voltage High vs. Load Current

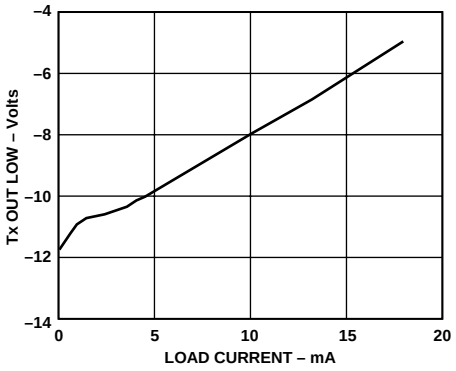


Figure 8. Transmitter Output Voltage Low vs. Load Current

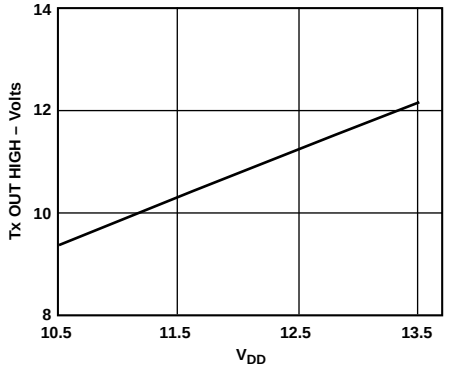


Figure 9. Transmitter Output Voltage High vs. V_{DD}

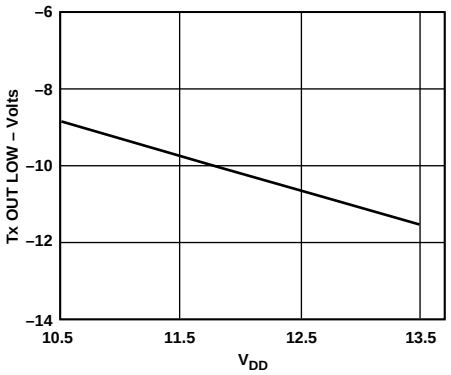


Figure 10. Transmitter Output Voltage Low vs. V_{DD}

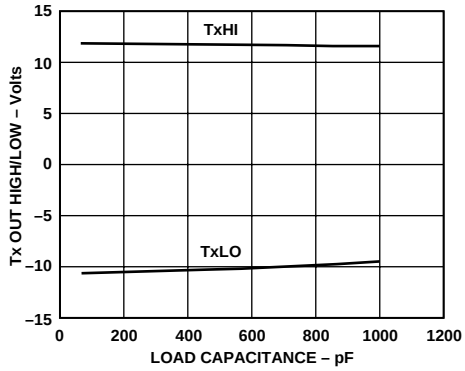


Figure 11. Transmitter Output Voltage High/Low vs. Load Capacitance

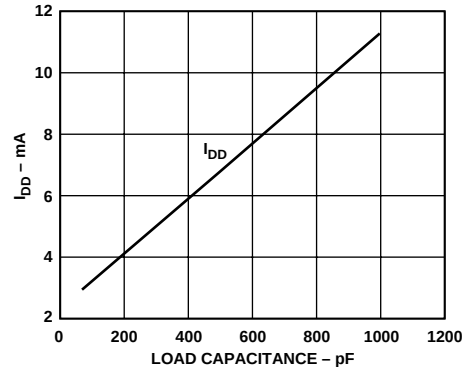


Figure 12. I_{DD} vs. Load Capacitance V_{STBY} = 5 V

Typical Performance Curves (V_{STBY} = +3.3 V)

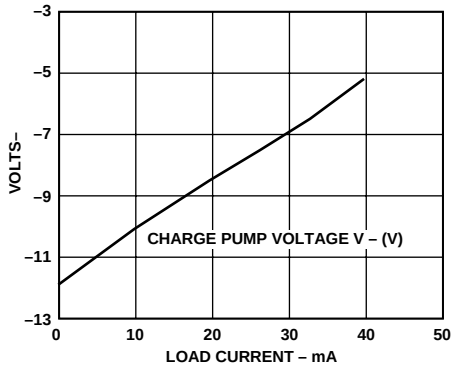


Figure 13. V– vs. Load Current

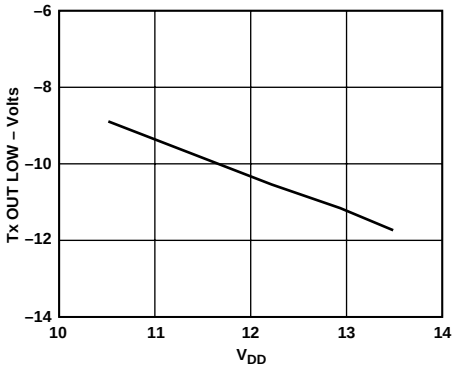


Figure 17. Transmitter Output Voltage Low vs. V_{DD}

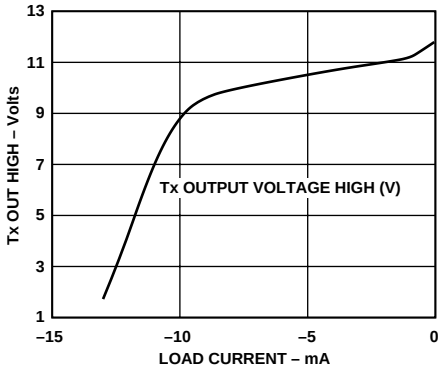


Figure 14. Transmitter Output Voltage High vs. Load Current

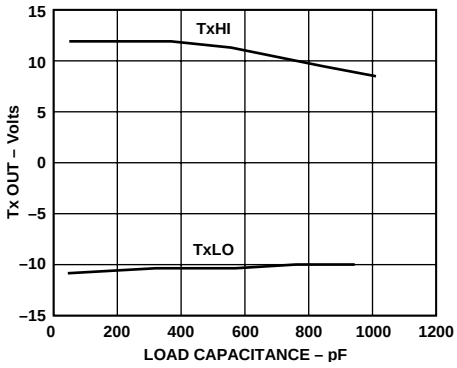


Figure 18. Transmitter Output Voltage vs. Load Capacitance @ 460 kBPS

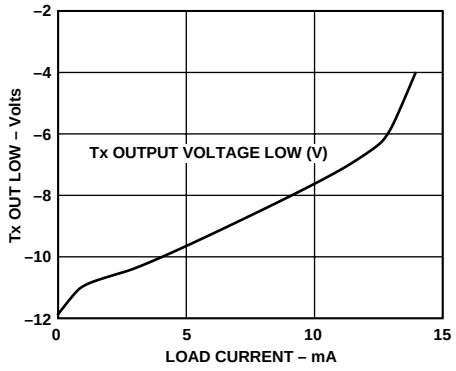


Figure 15. Transmitter Output Voltage Low vs. Load Current

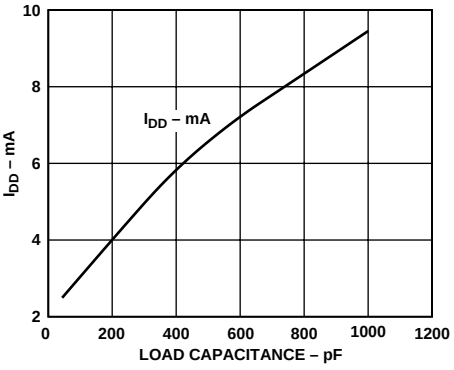


Figure 19. I_{DD} vs. Load Capacitance

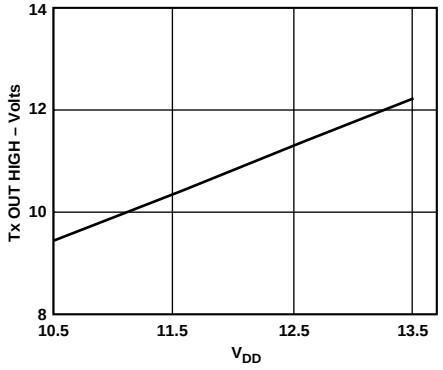


Figure 16. Transmitter Output Voltage High vs. V_{DD}

GENERAL DESCRIPTION

The ADM2209E is a rugged dual-port RS-232 line driver/receiver that operates from a single, +12 V supply, thus removing the need for a –12 V power supply. It contains ten receivers and six drivers, and provides a one-chip solution for both serial ports in desktop or portable personal computers.

Features include low power consumption, high transmission rates and compatibility with the EU directive on electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference including high levels of electrostatic discharge.

All RS-232 inputs and outputs contain protection against electrostatic discharges up to ±15 kV and electrical fast transients up to ±2 kV. This ensures compliance to IE1000-4-2 and IEC1000-4-4 requirements.

This device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions. Emissions are also controlled to within very strict limits.

A novel feature of this device is that one receiver (R5) in each port can be kept active by a low-current, +3 V/+5 V power supply, while the rest of the system is powered down. This allows the system to be awakened when peripheral devices begin to communicate with it.

CIRCUIT DESCRIPTION

The internal circuitry consists of four main sections. These are:

1. A charge pump dc-to-dc converter
2. Logic (3 V/5 V)-to-EIA-232 transmitters
3. EIA-232-to-logic receivers
4. Transient protection circuit on all I-O lines

Charge Pump DC-DC Converter

The dc-dc converter generates a negative supply voltage from the +12 V supply, thus removing the need for a separate –12 V rail. It consists of an on-chip 200 kHz oscillator, switching matrix and two external capacitors, as shown in Figure 20.

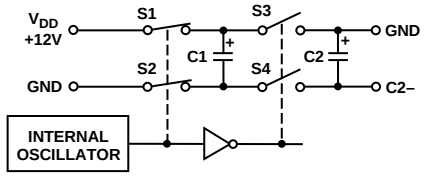


Figure 20. Charge Pump DC-DC Converter

When S1 and S2 are closed, S3 and S4 are open, and C1 charges to +12 V. S1 and S2 are then opened, while S3 and S4 are closed to connect C1 across C2, dumping charge into C2. Since the positive terminal of C2 is at ground, a negative voltage will be built up on its negative terminal with each cycle of the oscillator. This voltage depends on the current drawn from C2. If the current is small, the voltage will be close to –12 V, but will fall as the current drawn increases.

Standby Operation

The ADM2209E automatically enters a standby or shutdown mode when the V_{DD} power supply is removed. An on-chip comparator circuit generates an internal shutdown signal. This signal disables the internal oscillator and hence the charge pump. The inverted output V– goes to GND. All transmitter outputs are disabled and receivers R1 through R4 on each port are three-stated. The remaining receiver on each port (R5) remains fully active.

The standby current I_{STBY} remains less than 200 μA in this mode.

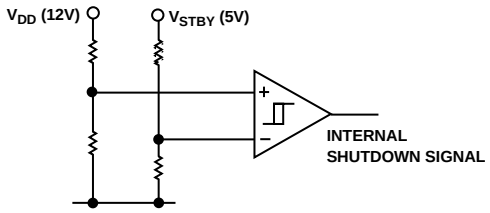


Figure 21. Standby Detection Circuit

Charge Pump Capacitors And Supply Decoupling

For proper operation of the charge pump, the capacitors should have an equivalent series resistance (ESR) less than 1 Ω. As the charge pump draws current pulses from V_{DD}, the V_{DD} decoupling capacitor should also have low ESR. The V– decoupling capacitor and reservoir capacitor should also have low ESR because they determine how effectively ESD pulses are clamped to V_{DD} or V– by the on-chip clamp diodes. Tantalum or monolithic ceramic capacitors are suitable for these components. If using tantalum capacitors, do not forget to observe polarity.

Transmitter (Driver) Section

The drivers convert 5 V logic input levels into EIA-232 output levels. With V_{DD} = +12 V and driving an EIA-232 load, the output voltage swing is typically ±9 V.

Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high, forcing the outputs into a low state. The input pull-up resistors typically source 10 μA when grounded, so unused inputs should either be connected to V_{STBY} or left unconnected in order to minimize power consumption.

Receiver Section

The receivers are inverting level shifters that accept EIA-232 input levels and translate them into 5 V logic output levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.4 V minimum and 2.4 V maximum. Unconnected inputs are pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for unconnected inputs or for inputs connected to GND.

The receivers have Schmitt trigger input with a hysteresis level of 0.25 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

HIGH BAUD RATE

The ADM2209E features high slew rates permitting data transmission at rates well in excess of the EIA-232-E specifications. RS-232 levels are maintained at data rates up to 920 kb/s. This allows for high speed data links between two terminals and, indeed, is suitable for the new generation modem standards.

ESD/EFT TRANSIENT PROTECTION SCHEME

The ADM2209E uses protective clamping structures on all inputs and outputs, which clamps the voltage to a safe level and dissipates the energy present in ESD (Electrostatic) and EFT

(Electrical Fast Transient) discharges. A simplified schematic of the protection structure is shown in Figures 22a and 22b. Each input and output contains two back-to-back high speed clamping diodes. During normal operation with maximum RS-232 signal levels, the diodes have no effect as one or the other is reverse-biased, depending on the polarity of the signal. If, however, the voltage exceeds about ±50 V, reverse breakdown occurs and the voltage is clamped at this level. The diodes are large p-n junctions designed to handle the instantaneous current surge which can exceed several amperes.

The transmitter outputs and receiver inputs have a similar protection structure. The receiver inputs can also dissipate some of the energy through the internal 5 kΩ resistor to GND as well as through the protection diodes.

The protection structure achieves ESD protection up to ±15 kV and EFT protection up to ±2 kV on all RS-232 I-O lines. The methods used to test the protection scheme are discussed later.

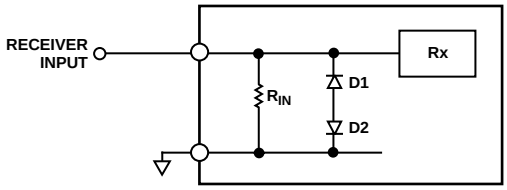


Figure 22a. Receiver Input Protection Scheme

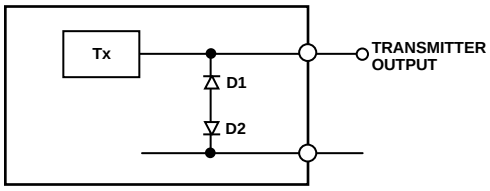


Figure 22b. Transmitter Output Protection Scheme

ESD TESTING (IEC1000-4-2)

IEC1000-4-2 (previously 801-2) specifies compliance testing using two coupling methods, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved towards the unit under test developing an arc across the air gap, hence the term air-discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

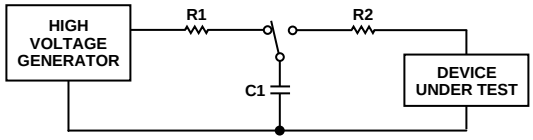
I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port. Traditional ESD test methods such as the MIL-STD-883B method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the traditional test and the IEC test:

(a) The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.

(b) The current rise time is significantly faster in the IEC test.

(c) The IEC test is carried out while power is applied to the device.

It is possible that the ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum peace of mind, however, both tests should be performed, to ensure maximum protection both during handling and later, during field service.



ESD TEST METHOD	R2	C1
H. BODY MIL-STD-883B	1.5kΩ	100pF
IEC1000-4-2	330Ω	150pF

Figure 23. ESD Test Standards

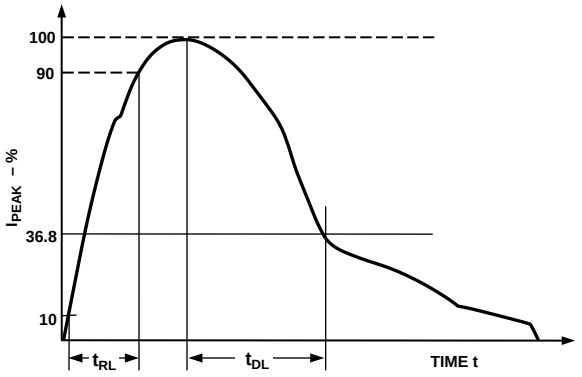


Figure 24. Human Body Model ESD Current Waveform

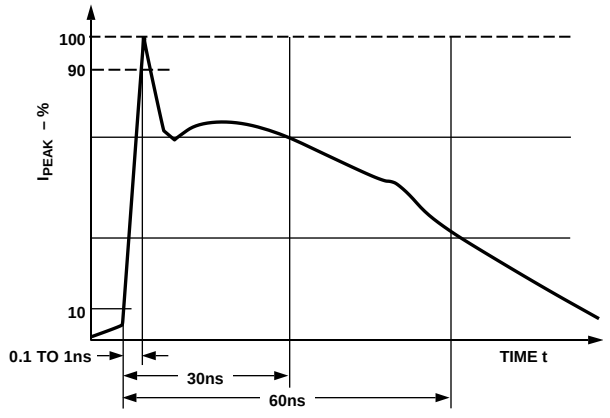


Figure 25. IEC1000-4-2 ESD Current Waveform

The ADM2209E is tested using both of the above-mentioned test methods. All pins are tested with respect to all other pins as per the MIL-STD-883B specification. In addition, all I-O pins are tested as per the IEC test specification. The products were tested under the following conditions:

(a) Power-On—Normal Operation
(b) Power-Off

There are four levels of compliance defined by IEC1000-4-2. The ADM2209E meets the most stringent compliance level for both contact and air-gap discharge. This means that the products are able to withstand contact discharges in excess of 8 kV and air-gap discharges in excess of 15 kV.

Table IV. IEC1000-4-2 Compliance Levels

Level	Contact Discharge kV	Air Discharge kV
1	2	2
2	4	4
3	6	8
4	8	15

Table V. ADM2209E ESD Test Results

ESD Test Method	I-O Pins	Other Pins
MIL-STD-883B	±15 kV	±2.5 kV
IEC1000-4-2		
Contact	±8 kV	
Air	±15 kV	

FAST TRANSIENT BURST TESTING (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast-transient/burst (EFT) immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when, for example, a power relay disconnects an inductive load. A spark is generated due to the well-known back EMF effect. In fact the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line, therefore, consists of a burst of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient burst test defined in IEC1000-4-4 simulates this arcing and its waveform is illustrated in Figure 26. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

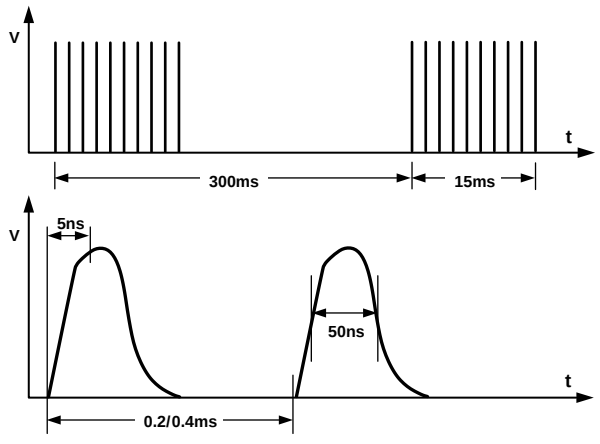


Figure 26. IEC1000-4-4 Fast Transient Waveform

Table VI.

Level	V Peak (kV) PSU	V Peak (kV) I-O
1	0.5	0.25
2	1	0.5
3	2	1
4	4	2

A simplified circuit diagram of the actual EFT generator is illustrated in Figure 27.

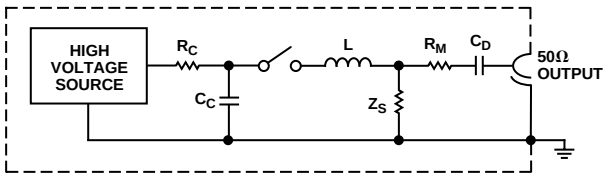


Figure 27. IEC1000-4-4 Fast Transient Generator

The transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 meter long and it completely surrounds the cable, providing maximum coupling capacitance (50 pF to 200 pF typ) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns) as specified by the standard result in very effective coupling. This test is very severe since high voltages are coupled onto the signal lines. The repetitive transients can often cause problems where single pulses do not. Destructive latch-up may be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst case transient current on an I-O line can be as high as 40 A.

Test results are classified according to the following:

1. Normal performance within specification limits.
2. Temporary degradation or loss of performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable due to damage.

The ADM2209E has been tested under worst case conditions using unshielded cables and meets Classification 2. Data transmission during the transient condition is corrupted, but it may be resumed immediately following the EFT event without user intervention.

IEC1000-4-3 RADIATED IMMUNITY

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers or any other device that generates continuous wave radiated electromagnetic energy. Its scope has since been broadened to include spurious EM energy which can be radiated from fluorescent lights, thyristor drives, inductive loads, etc.

Testing for immunity involves irradiating the device with an EM field. There are various methods of achieving this, including use of an echoic chamber, stripline cell, TEM cell, GTEM cell. A stripline cell consists of two parallel plates with an electric field developed between them. The device under test is placed within the cell and exposed to the electric field. There are three severity levels having field strengths ranging from 1 V to 10 V/m. Results are classified in a fashion similar to those for IEC1000-4-4.

1. Normal operation.
2. Temporary degradation or loss of function that is self-recoverable when the interfering signal is removed.
3. Temporary degradation or loss of function that requires operator intervention or system reset when the interfering signal is removed.
4. Degradation or loss of function that is not recoverable due to damage.

The ADM2209E easily meets Classification 1 at the most stringent (Level 3) requirement. In fact, field strengths up to 30 V/m showed no performance degradation and error-free data transmission continued even during irradiation.

Table VII. Test Severity Levels (IEC1000-4-3)

Level	Field Strength V/m
1	1
2	3
3	10

EMISSIONS/INTERFERENCE

EN55 022, CISPR22 defines the permitted limits of radiated and conducted interference from Information Technology (IT) equipment. The objective of the standard is to minimize the level of emissions, both conducted and radiated.

APPLICATIONS INFORMATION

In a typical Data Terminal Equipment (DTE) to Data Circuit Terminating Equipment (DCE) 9-lead de facto interface implementation, two data lines (TxD and RxD) and six control lines (RTS, DTR, DSR, CTS and RI) are required. With its six drivers and ten receivers, the ADM2209E offers a single-chip solution for the two RS-232 ports normally supplied as standard in a desktop or notebook personal computer, as shown in Figure 28. The flow-through pinout of the device allows for a very simple PCB layout, and allows a ground plane to be placed beneath the IC, and ground lines to be inserted between the signal lines to minimize crosstalk, without the complication of multilayer PCBs.

Note that the two receivers kept active by the standby supply ($R5_{IN}A$ and $R5_{IN}B$) should be connected to the Ring In (RI) line, so that the system can be awakened when a peripheral device begins to communicate.

FAIL-SAFE RECEIVER OUTPUTS

The ADM2209E has fail-safe receiver outputs that assume a high output level if the receiver input is zero or open-circuit.

LAPLINK COMPATIBILITY

The ADM2209E can operate up to 460 kbps data rate under maximum driver load conditions of C_L = 1000 pF and R_L = 3 kΩ at minimum power supply voltages.

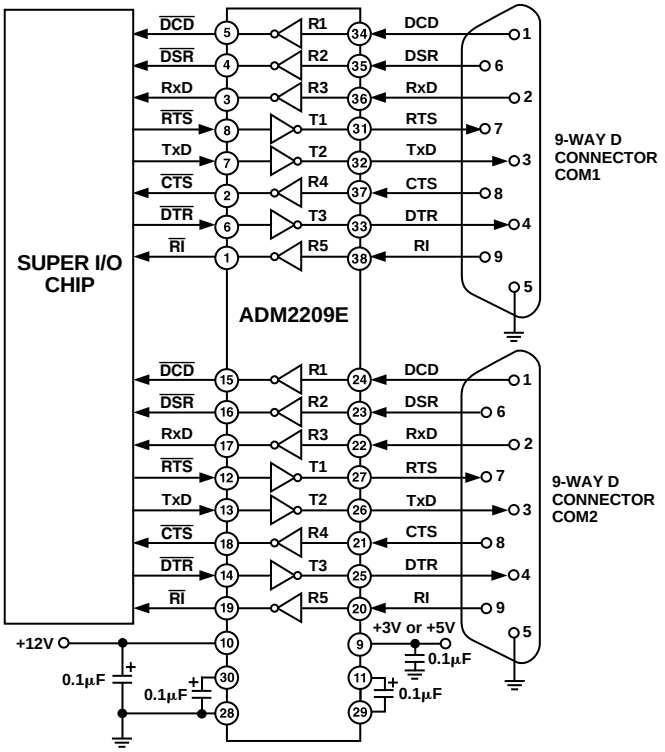
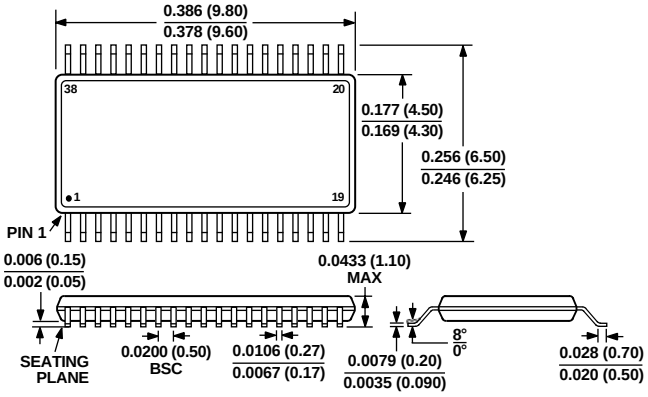


Figure 28. Typical Application for a Dual Serial Port

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

38-Lead TSSOP Package (RU-38)



C3642–8–7/99

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