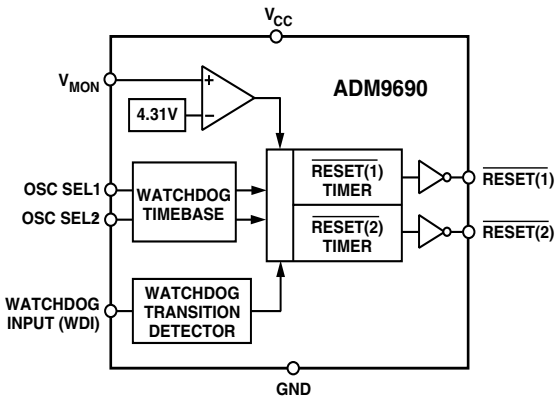
Power Supply and Watchdog Timer Monitoring Circuit

ADM9690

Precision Voltage Monitor (4.31 V)
Watchdog Timeout Monitor
Selectable Watchdog Timeout—0.75 ms, 1.5 ms, 12.5 ms, 25 ms
Two RESET Outputs

APPLICATIONS
Microprocessor Systems
Computers
Printers
Controllers
Intelligent Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM9690 contains a voltage monitoring comparator and a watchdog timer monitor. It is designed to monitor the 5 V power supply to a microprocessor and the microprocessor operation via a watchdog function.

The voltage monitoring comparator monitors the voltage on V_{MON}. If it drops outside tolerance, as will happen during a power-fail, two reset signals are generated. Both reset signals go active (low) simultaneously. They will remain active while V_{MON} is below the threshold, and for 50 ms (RESET(1)) or 60 ms ($\overline{\text{RESET(2)}}$) after V_{MON} climbs above the reset threshold. RESET(1) is intended to provide a power-on reset signal for the µP while RESET(2) is used to hold additional circuitry in a reset state until the µP has regained control following a power-up. The voltage monitoring circuitry remains operational with V_{CC} as low as 2 V.

The watchdog timer monitoring circuit is designed to monitor the activity on the WDI input. This input is normally connected to an output line on the µP. Its function is to check that the microprocessor has not stalled in an infinite loop. If there is a period of inactivity for the watchdog timeout period, both reset outputs are activated. As above, RESET(1) remains low for 50 ms while $\overline{\text{RESET(2)}}$ remains low for an additional 10 ms. The watchdog timer is restarted when RESET(1) goes inactive. The actual watchdog timeout period is adjustable using two select inputs SEL1 and SEL2.

The ADM9690 is available in an 8-lead SOIC package. It is specified over the industrial temperature range.

REV. A

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ADM9690–SPECIFICATIONS (V_{CC} = Full Operating Range. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} OPERATING VOLTAGE RANGE	4.3		5.5	V	
SUPPLY CURRENT		55	100	µA	
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	4.2	4.31	4.42	V	V_{MON} Falling T_A = 0°C to +70°C
Reset Threshold Hysteresis		30		mV	
Reset Timeout Delay (t_1)		50	75	ms	Figure 7, 8
RESET(2) Timeout Delay (t_2)		10	15	ms	Figure 7, 8
WATCHDOG TIMEOUT PERIOD (TWD)	0.4	0.75	1.28	ms	SEL2 = 0, SEL1 = 0
	1.0	1.5	2.4	ms	SEL2 = 0, SEL1 = 1
	9.0	12.5	19	ms	SEL2 = 1, SEL1 = 0
	18	25	38	ms	SEL2 = 1, SEL1 = 1
WDI INPUT PULSEWIDTH	100			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
RESET(1)/(2) Output Voltage		0.1	0.4	V	I_{SINK} = 3.2 mA
		0.3	0.4	V	I_{SINK} = 10 mA,
		0.45	0.7	V	I_{SINK} = 15 mA,
	3.5			V	I_{SOURCE} = 1 µA
WDI INPUT THRESHOLD					
Logic Low			0.8	V	150 ns Pulse
Logic High	3.5			V	150 ns Pulse
WDI Input Current		1.2	5	µA	WDI = V_{CC}
	–5	–1.2		µA	WDI = 0 V
SEL1/2 Input Current	–1		+1	µA	SEL = V_{CC}
	–10	–5	10	µA	SEL = 0 V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

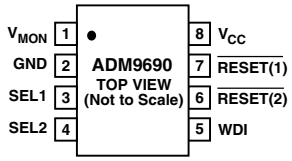
V_{CC} . . . . . –0.3 V to +6 V
V_{MON} . . . . . –0.3 V to V_{CC} + 0.3 V
Input Current
  V_{CC} . . . . . 200 mA
  GND . . . . . 200 mA
Digital Output Current . . . . . 200 mA
Power Dissipation, R-8 SOIC . . . . . 400 mW
θ_{JA} Thermal Impedance . . . . . 120°C/W
Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
  Vapor Phase (60 secs) . . . . . +215°C
  Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C
ESD Rating . . . . . 4 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM9690AR	–40°C to +85°C	8-Lead Narrow Body SOIC	SO-8

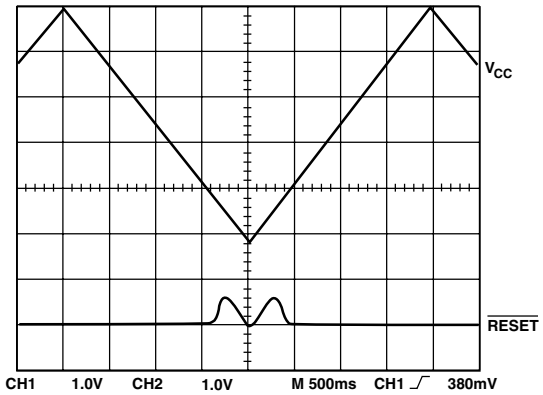
PIN CONFIGURATION

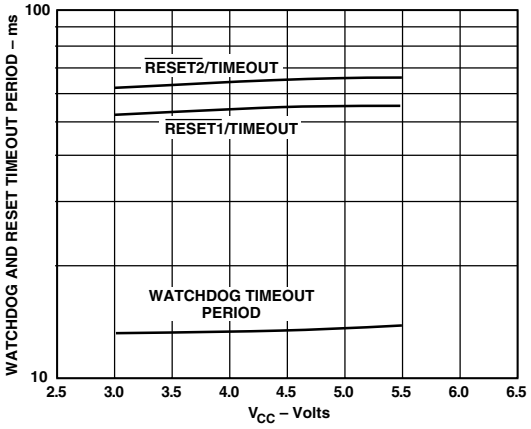


PIN FUNCTION DESCRIPTIONS

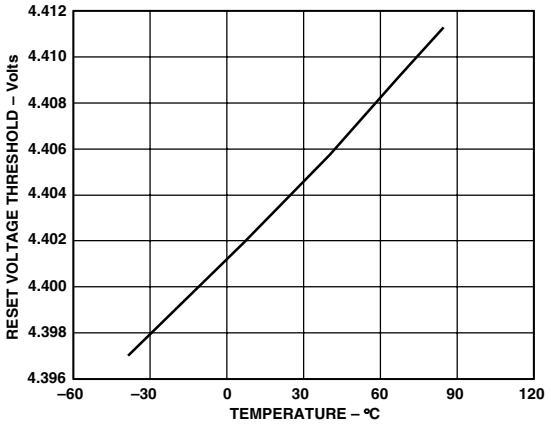
Mnemonic	Function
V_{CC}	Power Supply Input; +5 V.
V_{MON}	Voltage Monitoring Input.
GND	0 V. Ground reference for all signals.
RESET(1)	Logic Output. RESET(1) goes low if V_{MON} falls below the Reset Threshold or the Watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.4 V for the ADM9690. RESET(1) remains low for 50 ms after V_{CC} returns above the threshold. RESET(1) also goes low for 50 ms if the Watchdog Timer is not serviced within its timeout period.
RESET(2)	Logic Output. RESET(2) goes low simultaneously with RESET(1) but remains low for an additional 10 ms.
WDI	Watchdog Input. If an edge is not detected on WDI within the selectable watchdog timeout period, RESET(1) and RESET(2) are forced low for their respective timeout periods. The watchdog timer restarts with each positive or negative going transition on the WDI line. Following a reset it is restarted when RESET(1) goes inactive (high). The Watchdog Timer may be disabled if WDI is left floating or is driven to midsupply.
SEL1, 2	Watchdog Timeout selection inputs. Refer to Table I.

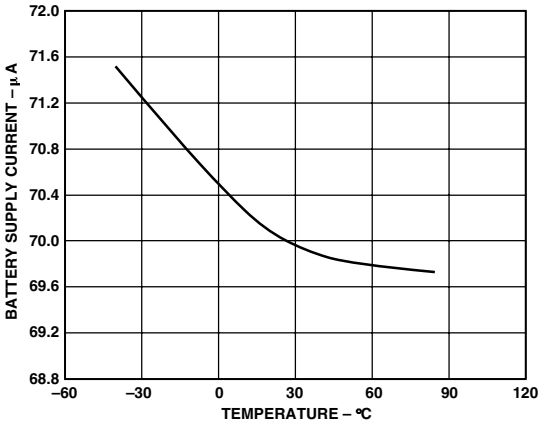
–Typical Performance Curves

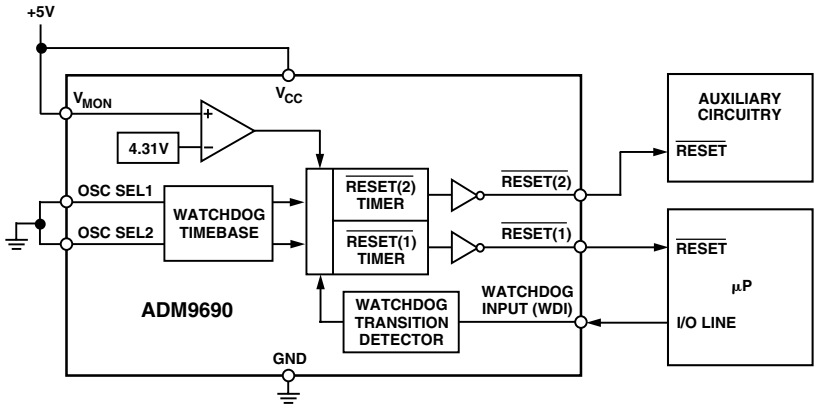




@ –40°C







POWER SUPPLY AND WATCHDOG MONITORING CIRCUIT

The ADM9690 contains a power supply voltage monitoring comparator and a watchdog timer monitor. Either V_{MON} dropping outside tolerance or the watchdog timer timing out results in a reset sequence as discussed below. Two reset outputs are provided. $\overline{RESET(1)}$ and $\overline{RESET(2)}$.

POWER FAIL/POWER-ON $\overline{RESET}$

When V_{MON} falls below the reset threshold (4.4 V) both RESET outputs are forced low immediately.

On power-up, $\overline{RESET(1)}$ will remain low for 50 milliseconds after V_{MON} rises above the reset threshold. This provides a power-on reset for the microprocessor. $\overline{RESET(2)}$ remains active low for an additional 10 ms. $\overline{RESET(1)}$ is intended to provide a power-on reset signal for the µP while $\overline{RESET(2)}$ is used to hold additional circuitry in a reset state until the µP has regained control following a power-up.

The guaranteed minimum and maximum thresholds for the ADM9690 are 4.3 V and 4.5 V.

Watchdog Timer $\overline{RESET}$

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an infinite loop. An output line on the processor may be used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, both $\overline{RESET}$ outputs are taken active (low). $\overline{RESET(1)}$ remains low for 50 ms and $\overline{RESET(2)}$ remains low for an additional 10 ms . Each transition (either positive-going or negative-going) of WDI after $\overline{RESET(1)}$ has gone inactive restarts the watchdog timer. The actual watchdog timeout period is adjustable using SEL1 and SEL2. Four timeout periods are selectable. Please refer to Table I.

The watchdog timer is restarted at the end of $\overline{RESET(1)}$ ($\overline{RESET(1)}$ going high), whether the reset was caused by lack of activity on WDI or by V_{MON} falling below the reset threshold.

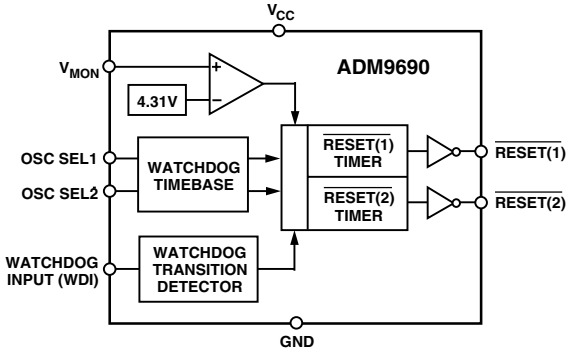
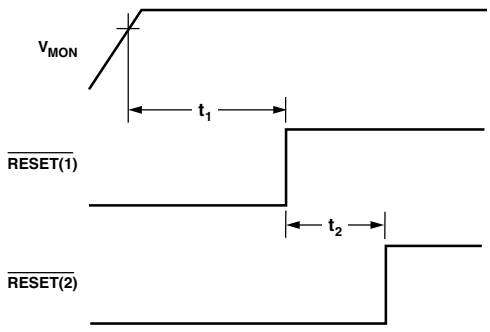
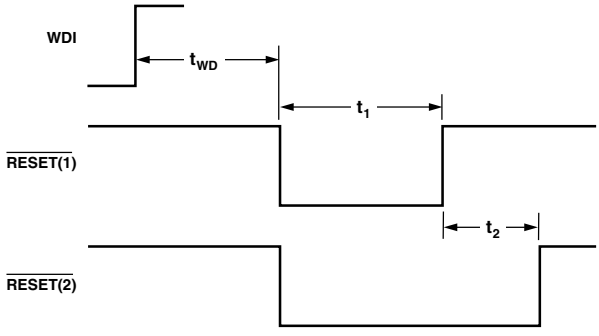


Table I.

SEL2	SEL1	Watchdog Timeout Period t_{WD} (ms)
0	0	0.75
0	1	1.5
1	0	12.5
1	1	25



$\overline{RESET}$ Timing

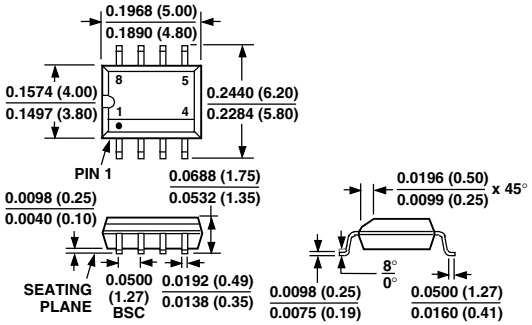


$\overline{RESET}$ Timing

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Narrow Body SOIC
(SO-8)



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