5 kV RMS and 3.75 kV RMS, Dual-Channel LVDS Gigabit Isolators

Data Sheet

ADN4654/ADN4655/ADN4656

FEATURES

- 5 kV rms and 3.75 kV rms LVDS isolators
- Complies with TIA/EIA-644-A LVDS standard
- Multiple dual-channel configurations
- Any data rate up to 1.1 Gbps switching with low jitter
  - 4 ns typical propagation delay
  - 2.6 ps rms typical random jitter, rms
  - 90 ps typical peak-to-peak total jitter at 1.1 Gbps
- 2.5 V or 3.3 V supplies
- −75 dBc power supply ripple rejection, phase spur level
- Glitch immunity
- ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- High common-mode transient immunity: >25 kV/µs
- Passes EN 55022 Class B radiated emissions limits with 1.1 Gbps PRBS
- Safety and regulatory approvals (20-lead SOIC_W package)
  - UL (pending): 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 424 V_{PEAK}
- Fail-safe output high for open, short, and terminated input conditions (ADN4655/ADN4656)
- Operating temperature range: −40°C to +125°C
- 7.8 mm minimum creepage and clearance

APPLICATIONS

- Isolated video and imaging data
- Analog front-end isolation
- Data plane isolation
- Isolated high speed clock and data links

FUNCTIONAL BLOCK DIAGRAMS

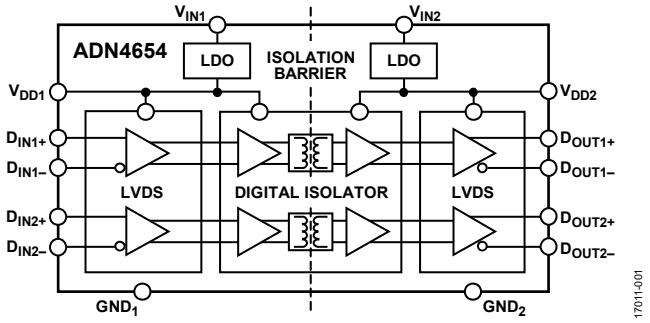


Figure 1.

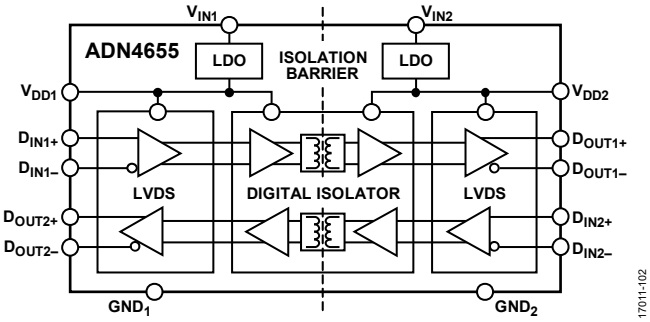


Figure 2.

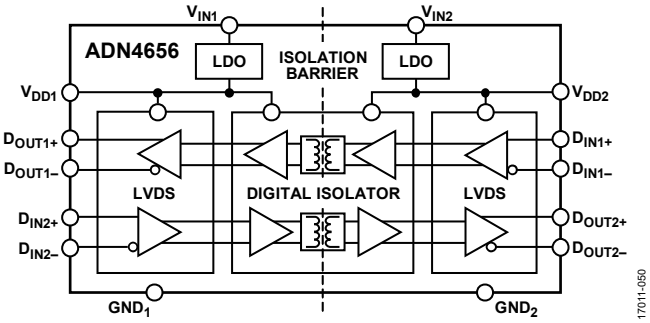


Figure 3.

GENERAL DESCRIPTION

The ADN4654/ADN4655/ADN4656[1] are signal isolated, low voltage differential signaling (LVDS) buffers that operate at up to 1.1 Gbps with low jitter. The devices integrate Analog Devices, Inc., *i*Coupler® technology, enhanced for high speed operation to provide galvanic isolation of the TIA/EIA-644-A compliant LVDS drivers and receivers. This integration allows drop-in isolation of an LVDS signal chain.

The ADN4654/ADN4655/ADN4656 comprise multiple channel configurations, and the LVDS receivers on the ADN4655 and ADN4656 include a fail-safe mechanism to ensure a Logic 1 on the corresponding LVDS driver output when the inputs are floating, shorted, or terminated but not driven.

For high speed operation with low jitter, the LVDS and isolator circuits rely on a 2.5 V supply. An integrated on-chip low dropout (LDO) regulator can provide the required 2.5 V from an external 3.3 V power supply. The devices are fully specified over a wide industrial temperature range and come in a 20-lead, wide body SOIC_W package with 5 kV rms isolation or in a 20-lead SSOP package with 3.75 kV rms isolation.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. D Document Feedback

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REVISION HISTORY

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SPECIFICATIONS

For all minimum and maximum specifications, V_{DD1} = V_{DD2} = 2.375 V to 2.625 V, T_A = −40°C to +125°C, unless otherwise noted. For all typical specifications, V_{DD1} = V_{DD2} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUTS (RECEIVERS)						
Input Threshold						See Figure 38 and Table 2
High	V_{TH}			100	mV	
Low	V_{TL}	−100			mV	
Differential Input Voltage	$\|V_{ID}\|$	100			mV	See Figure 38 and Table 2
Input Common-Mode Voltage	V_{IC}	$0.5\|V_{ID}\|$		$2.4 - 0.5\|V_{ID}\|$	V	See Figure 38 and Table 2
Input Current, High and Low	I_{IH}, I_{IL}	−5		+5	µA	$D_{INx\pm}$ = V_{DDx} or 0 V, other input = 1.2 V, V_{DDx} = 2.5 V or 0 V
Differential Input Capacitance[1]	$C_{INx\pm}$		2		pF	$D_{INx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V, other input = 1.2 V[2]
OUTPUTS (DRIVERS)						
Differential Output Voltage	$\|V_{OD}\|$	250	310	450	mV	See Figure 36 and Figure 37, load resistance (R_L) = 100 Ω
V_{OD} Magnitude Change	$\|\Delta V_{OD}\|$			50	mV	See Figure 36 and Figure 37, R_L = 100 Ω
Offset Voltage	V_{OS}	1.125	1.17	1.375	V	See Figure 36, R_L = 100 Ω
V_{OS} Magnitude Change	ΔV_{OS}			50	mV	See Figure 36, R_L = 100 Ω
V_{OS}, Peak to Peak[1]	$V_{OS(PP)}$			150	mV	See Figure 36, R_L = 100 Ω
Output Short-Circuit Current	I_{OS}			−20	mA	$D_{OUTx\pm}$ = 0 V
				12	mA	$\|V_{OD}\|$ = 0 V
Differential Output Capacitance[1]	$C_{OUTx\pm}$		5		pF	$D_{OUTx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V, other input = 1.2 V, V_{DD1} or V_{DD2} = 0 V
POWER SUPPLY						
Supply Current	I_{DD1}, I_{IN1}, I_{DD2}, or I_{IN2}					
ADN4655/ADN4656 only				55	mA	No output load, inputs with 100 Ω, no applied $\|V_{ID}\|$
			58	82	mA	All outputs loaded, R_L = 100 Ω, frequency = 0.55 GHz
ADN4654 only			50	65	mA	No output load, inputs with 100 Ω, $\|V_{ID}\|$ = 200 mV
			60	80	mA	All outputs loaded, R_L = 100 Ω, frequency = 0.55 GHz
LDO Input Range	V_{IN1} or V_{IN2}	3.0	3.3	3.6	V	No external supply on V_{DD1} or V_{DD2}
LDO Output Range	V_{DD1} or V_{DD2}	2.375	2.5	2.625	V	
Power Supply Ripple Rejection, Phase Spur Level	PSRR		−75		dBc	Phase spur level on $D_{OUTx\pm}$ with 0.55 GHz clock on $D_{INx\pm}$ and applied ripple of 100 kHz, 100 mV p-p on a 2.5 V supply to V_{DD1} or V_{DD2}
COMMON-MODE TRANSIENT IMMUNITY[3]	|CM|	25	50		kV/µs	Common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V

[1] These specifications are guaranteed by design and characterization.
[2] t denotes time.
[3] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining any D_{OUTx+}/D_{OUTx-} pin in the same state as the corresponding D_{INx+}/D_{INx-} pin (no change in output), or producing the expected transition on any D_{OUTx+}/D_{OUTx-} pin if the applied common-mode transient edge is coincident with a data transition on the corresponding D_{INx+}/D_{INx-} pin. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

RECEIVER INPUT THRESHOLD TEST VOLTAGES

Table 2. Test Voltages for Receiver Operation

Applied Voltages				
D_{INx+} (V)	D_{INx-} (V)	Input Voltage, Differential, V_{ID} (V)	Input Voltage, Common-Mode, V_{IC} (V)	Driver Output, Differential V_{OD} (mV)
1.25	1.15	0.1	1.2	>250
1.15	1.25	−0.1	+1.2	<−250
2.4	2.3	0.1	2.35	>250
2.3	2.4	−0.1	+2.35	<−250
0.1	0	0.1	0.05	>250
0	0.1	−0.1	+0.05	<−250
1.5	0.9	0.6	1.2	>250
0.9	1.5	−0.6	+1.2	<−250
2.4	1.8	0.6	2.1	>250
1.8	2.4	−0.6	+2.1	<−250
0.6	0	0.6	0.3	>250
0	0.6	−0.6	+0.3	<−250

TIMING SPECIFICATIONS

For all minimum and maximum specifications, $V_{DD1} = V_{DD2} = 2.375$ V to 2.625 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. All typical specifications, $V_{DD1} = V_{DD2} = 2.5$ V, $T_A = 25°C$, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
PROPAGATION DELAY	t_{PLH}, t_{PHL}		4	4.5	ns	See Figure 39, from any D_{INx+}/D_{INx-} to D_{OUTx+}/D_{OUTx-}
SKEW						See Figure 39, across all D_{OUTx+}/D_{OUTx-}
Duty Cycle[2]	$t_{SK(D)}$			100	ps	
Channel to Channel[3]	$t_{SK(CH)}$		150	300	ps	ADN4654 only
			200	500	ps	ADN4655 and ADN4656 only
Part to Part[4]	$t_{SK(PP)}$			500	ps	ADN4654 to ADN4654 only
				600	ps	ADN4654, ADN4655, ADN4656, or combinations
JITTER[5]						See Figure 39, for any D_{OUTx+}/D_{OUTx-}
Random Jitter, RMS[6] (1σ)	$t_{RJ(RMS)}$		2.6	4.8	ps rms	0.55 GHz clock input
Deterministic Jitter, Peak to Peak[7, 8]	$t_{DJ(PP)}$		50	116	ps	1.1 Gbps, $2^{23} - 1$ pseudorandom bit stream (PRBS)
With Crosstalk	$t_{DJC(PP)}$		50		ps	1.1 Gbps, $2^{23} - 1$ PRBS
Total Jitter at Bit Error Rate (BER) 1×10^{-12}	$t_{TJ(PP)}$		90	171	ps	0.55 GHz, 1.1 Gbps, $2^{23} - 1$ PRBS[9]
Additive Phase Jitter	t_{ADDJ}		387		fs rms	100 Hz to 100 kHz, output frequency (f_{OUT}) = 10 MHz[10]
			288		fs rms	12 kHz to 20 MHz, f_{OUT} = 0.55 GHz[11]
RISE AND FALL TIME	t_R, t_F			350	ps	See Figure 39, any D_{OUTx+}/D_{OUTx-}, 20% to 80%, R_L = 100 Ω, load capacitance (C_L) = 5 pF
FAIL-SAFE DELAY[12]	t_{FSH}, t_{FSL}		1	1.2	µs	ADN4655 and ADN4656 only; see Figure 39 and Figure 4, any D_{OUTx+}/D_{OUTx-}, R_L = 100 Ω
MAXIMUM DATA RATE		1.1	1.25		Gbps	

[1] These specifications are guaranteed by design and characterization.
[2] Duty cycle or pulse skew is the magnitude of the maximum difference between t_{PLH} and t_{PHL} for any channel of a device, that is, $|t_{PLHx} - t_{PHLx}|$, where x denotes either Channel 1 or Channel 2 propagation delay.
[3] Channel to channel or output skew is the difference between the largest and smallest values of t_{PLHx} within a device or the difference between the largest and smallest values of t_{PHLx} within a device, whichever of the two is greater.
[4] Part to part output skew is the difference between the largest and smallest values of t_{PLHx} across multiple devices or the difference between the largest and smallest values of t_{PHLx} across multiple devices, whichever of the two is greater.
[5] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter. V_{ID} = 400 mV p-p, $t_R = t_F$ = 0.3 ns (20% to 80%).
[6] This specification is measured over a population of ~7,000,000 edges.
[7] Peak-to-peak jitter specifications include jitter due to pulse skew ($t_{SK(D)}$).
[8] This specification is measured over a population of ~3,000,000 edges.
[9] Using the formula: $t_{TJ(PP)} = 14 \times t_{RJ(RMS)} + t_{DJ(PP)}$.
[10] With input phase jitter of 250 fs rms subtracted.
[11] With input phase jitter of 100 fs rms subtracted.
[12] The fail-safe delay is the delay before $D_{OUTx\pm}$ is switched high to reflect an idle input to $D_{INx\pm}$ ($|V_{ID}| < 100$ mV, with open, short, or terminated input condition).

Timing Diagram

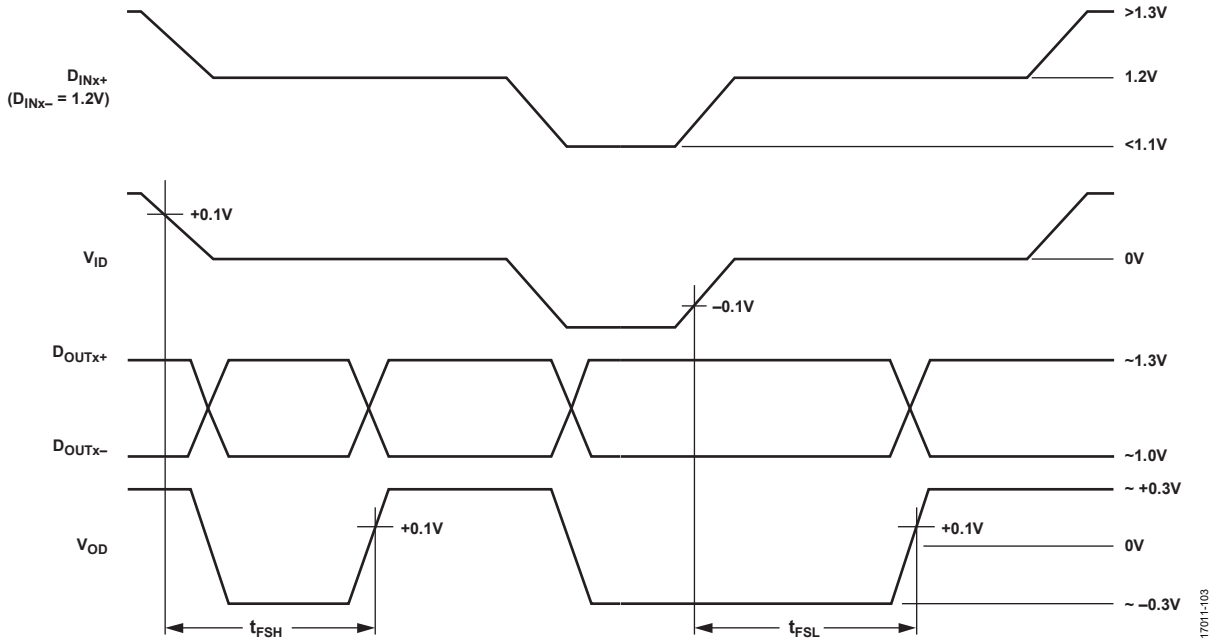


Figure 4. Fail-Safe Timing Diagram

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 4. 20-Lead SOIC_W Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		22	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 5. 20-Lead SSOP Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3.75	kV rms	1 minute duration
Minimum Clearance	L (I01)	5.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum Creepage	L (I02)	5.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum PCB Clearance	L (PCB)	5.6	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Clearance		22	µm min	Insulation distance through insulation
Comparative Tracking Index	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Frequency = 1 MHz
Input Capacitance[2]	C_I		3.7		pF	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 12 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 7.

UL (Pending)	CSA (Pending)	VDE (Pending)
To Be Recognized Under UL 1577 Component Recognition Program[1]	To be approved under CSA Component Acceptance Notice 5A	To be certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection, Isolation Voltage		Reinforced insulation, V_{IORM} = 424 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}
20-Lead SOIC, 5000 V rms		
20-Lead SSOP, 3750 V rms		
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADN4654/ADN4655/ADN4656 is proof tested by applying an insulation test voltage ≥ 6000 V rms (20-lead SOIC_W) or ≥ 4500 V rms (20-lead SSOP) for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADN4654/ADN4655/ADN4656 is proof tested by applying an insulation test voltage ≥ 795 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 8.

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	424	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PD(M)}$, 100% production test, $t_{INI} = t_M = 1$ sec, partial discharge < 5 pC	$V_{PD(M)}$	795	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD(M)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{PD(M)}$, $t_{INI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC		636	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PD(M)}$, $t_{INI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC		509	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	7000	V_{PEAK}
Surge Isolation Voltage				
Basic	$V_{PEAK} = 12.8$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10,000	V_{PEAK}
Reinforced	$V_{PEAK} = 12.8$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S		
20-Lead SOIC			2.78	W
20-Lead SSOP			1.8	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-10.

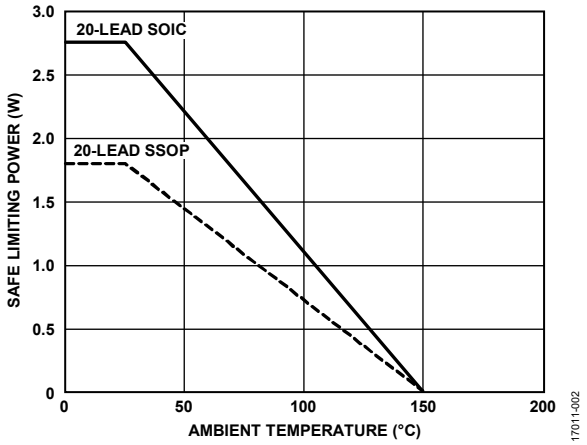


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 9.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages		
Supply to LDO Regulator	V_{IN1}, V_{IN2}	3.0 V to 3.6 V
LDO Bypass, V_{INx} Shorted to V_{DDx}	V_{DD1}, V_{DD2}	2.375 V to 2.625 V

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
V_{IN1} to GND_1/V_{IN2} to GND_2	−0.3 V to +6.5 V
V_{DD1} to GND_1/V_{DD2} to GND_2	−0.3 V to +2.8 V
Input Voltage (D_{INx+}, D_{INx-}) to GND_x on the Same Side	−0.3 V to V_{DD} + 0.3 V
Output Voltage (D_{OUTx+}, D_{OUTx-}) to GND_x on the Same Side	−0.3 V to V_{DD} + 0.3 V
Short-Circuit Duration (D_{OUTx+}, D_{OUTx-}) to GND_x on the Same Side	Continuous
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Electrostatic Discharge (ESD)	
Human Body Model (All Pins to Respective GND_x, 1.5 kΩ, 100 pF)	±4 kV
IEC 61000-4-2 (LVDS Pins to Isolated GND_x Across Isolation Barrier)	
20-Lead SOIC	±8 kV
20-Lead SSOP	±7 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one-cubic foot sealed enclosure.

Table 11. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
RW-20	45.7	°C/W
RS-20	69.6	°C/W

[1] Test Condition 1: thermal impedance simulated with 4-layer standard JEDEC PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 12. Maximum Continuous Working Voltage[1]

Parameter	Rating		Constraint
	RW-20	RS-20	
AC Voltage			
Bipolar Waveform			
Basic Insulation	424 V_{PEAK}	424 V_{PEAK}	50-year minimum insulation lifetime for 1% failure
Reinforced Insulation	424 V_{PEAK}	424 V_{PEAK}	50-year minimum insulation lifetime for 1% failure
Unipolar Waveform			
Basic Insulation	848 V_{PEAK}	848 V_{PEAK}	50-year minimum insulation lifetime for 1% failure
Reinforced Insulation	875 V_{PEAK}	620 V_{PEAK}	Lifetime limited by package creepage, maximum approved working voltage
DC Voltage			
Basic Insulation	1079 V_{PEAK}	754 V_{PEAK}	Lifetime limited by package creepage, maximum approved working voltage
Reinforced Insulation	536 V_{PEAK}	380 V_{PEAK}	Lifetime limited by package creepage, maximum approved working voltage

[1] The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

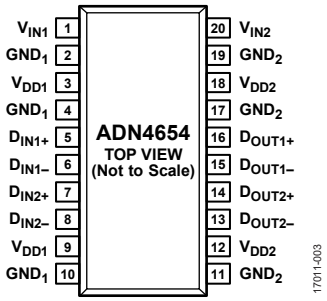


Figure 6. ADN4654 Pin Configuration

Table 13. ADN4654 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IN1}	Optional 3.3 V Power Supply and LDO Input for Side 1. Bypass V_{IN1} to GND_1 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN1} directly to V_{DD1}.
2, 4, 10	GND_1	Ground, Side 1.
3, 9	V_{DD1}	2.5 V Power Supply for Side 1. Connect both pins externally and bypass to GND_1 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN1}, connect a 1 µF capacitor between Pin 3 and GND_1 for proper regulation of the 2.5 V output of the internal LDO regulator.
5	D_{IN1+}	Noninverted Differential Input 1.
6	D_{IN1-}	Inverted Differential Input 1.
7	D_{IN2+}	Noninverted Differential Input 2.
8	D_{IN2-}	Inverted Differential Input 2.
11, 17, 19	GND_2	Ground, Side 2.
12, 18	V_{DD2}	2.5 V Power Supply for Side 2. Connect both pins externally and bypass to GND_2 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN2}, connect a 1 µF capacitor between Pin 18 and GND_2 for proper regulation of the 2.5 V output of the internal LDO regulator.
13	D_{OUT2-}	Inverted Differential Output 2.
14	D_{OUT2+}	Noninverted Differential Output 2.
15	D_{OUT1-}	Inverted Differential Output 1.
16	D_{OUT1+}	Noninverted Differential Output 1.
20	V_{IN2}	Optional 3.3 V Power Supply and LDO Input for Side 2. Bypass V_{IN2} to GND_2 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN2} directly to V_{DD2}.

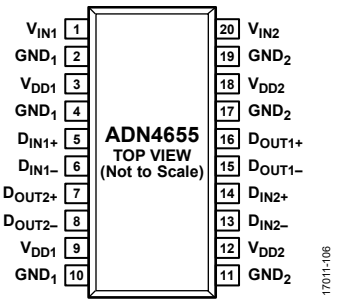


Figure 7. ADN4655 Pin Configuration

Table 14. ADN4655 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IN1}	Optional 3.3 V Power Supply and LDO Input for Side 1. Bypass V_{IN1} to GND_1 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN1} directly to V_{DD1}.
2, 4, 10	GND_1	Ground, Side 1.
3, 9	V_{DD1}	2.5 V Power Supply for Side 1. Connect both pins externally and bypass to GND_1 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN1}, connect a 1 µF capacitor between Pin 3 and GND_1 for proper regulation of the 2.5 V output of the internal LDO regulator.
5	D_{IN1+}	Noninverted Differential Input 1.
6	D_{IN1-}	Inverted Differential Input 1.
7	D_{OUT2+}	Noninverted Differential Output 2.
8	D_{OUT2-}	Inverted Differential Output 2.
11, 17, 19	GND_2	Ground, Side 2.
12, 18	V_{DD2}	2.5 V Power Supply for Side 2. Connect both pins externally and bypass to GND_2 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN2}, connect a 1 µF capacitor between Pin 18 and GND_2 for proper regulation of the 2.5 V output of the internal LDO regulator.
13	D_{IN2-}	Inverted Differential Input 2.
14	D_{IN2+}	Noninverted Differential Input 2.
15	D_{OUT1-}	Inverted Differential Output 1.
16	D_{OUT1+}	Noninverted Differential Output 1.
20	V_{IN2}	Optional 3.3 V Power Supply and LDO Input for Side 2. Bypass V_{IN2} to GND_2 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN2} directly to V_{DD2}.

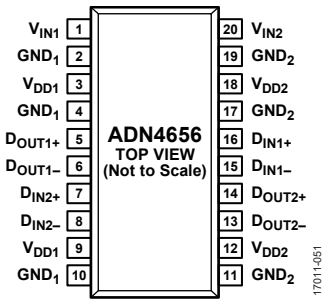


Figure 8. ADN4656 Pin Configuration

Table 15. ADN4656 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IN1}	Optional 3.3 V Power Supply and LDO Input for Side 1. Bypass V_{IN1} to GND_1 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN1} directly to V_{DD1}.
2, 4, 10	GND_1	Ground, Side 1.
3, 9	V_{DD1}	2.5 V Power Supply for Side 1. Connect both pins externally and bypass to GND_1 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN1}, connect a 1 µF capacitor between Pin 3 and GND_1 for proper regulation of the 2.5 V output of the internal LDO regulator.
5	D_{OUT1+}	Noninverted Differential Output 1.
6	D_{OUT1-}	Inverted Differential Output 1.
7	D_{IN2+}	Noninverted Differential Input 2.
8	D_{IN2-}	Inverted Differential Input 2.
11, 17, 19	GND_2	Ground, Side 2.
12, 18	V_{DD2}	2.5 V Power Supply for Side 2. Connect both pins externally and bypass to GND_2 with 0.1 µF capacitors. If supplying 3.3 V to V_{IN2}, connect a 1 µF capacitor between Pin 18 and GND_2 for proper regulation of the 2.5 V output of the internal LDO regulator.
13	D_{OUT2-}	Inverted Differential Output 2.
14	D_{OUT2+}	Noninverted Differential Output 2.
15	D_{IN1-}	Inverted Differential Input 1.
16	D_{IN1+}	Noninverted Differential Input 1.
20	V_{IN2}	Optional 3.3 V Power Supply and LDO Input for Side 2. Bypass V_{IN2} to GND_2 using a 1 µF capacitor. Alternatively, if using a 2.5 V supply, connect V_{IN2} directly to V_{DD2}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD1} = V_{DD2} = 2.5 V, T_A = 25°C, R_L = 100 Ω, 0.55 GHz input with |V_{ID}| = 200 mV, and V_{IC} = 1.1 V for ADN4654, unless otherwise noted.

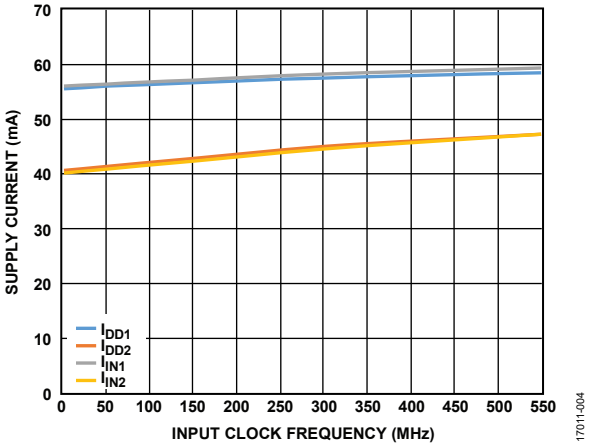


Figure 9. Supply Current vs. Input Clock Frequency ($D_{IN1\pm}$ Switching, $D_{IN2\pm}$ Not Switching)

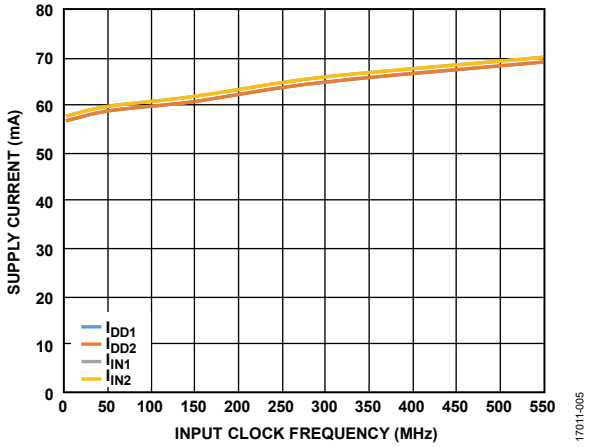


Figure 10. Supply Current vs. Input Clock Frequency ($D_{IN1\pm}$ and $D_{IN2\pm}$ Switching)

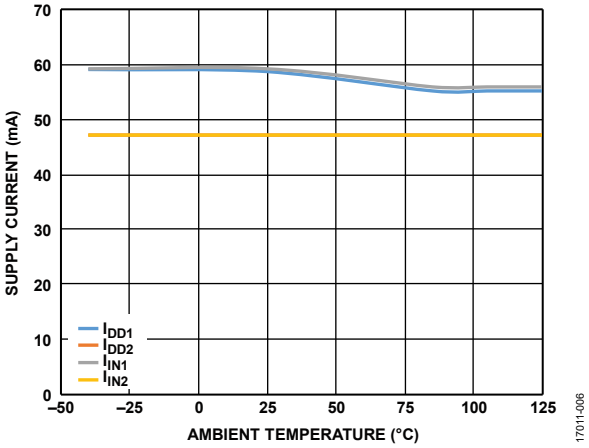


Figure 11. Supply Current vs. Ambient Temperature ($D_{IN1\pm}$ with 550 MHz Clock Input, $D_{IN2\pm}$ Not Switching)

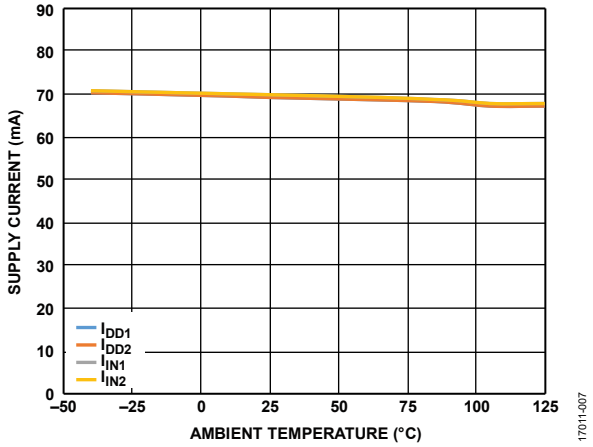


Figure 12. Supply Current vs. Ambient Temperature ($D_{IN1\pm}$ and $D_{IN2\pm}$ with 550 MHz Clock Inputs)

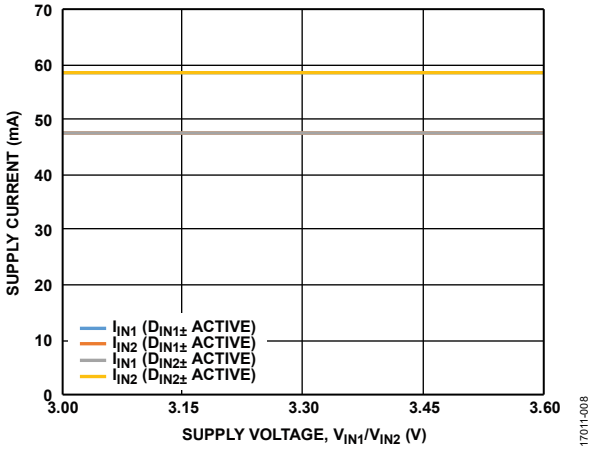


Figure 13. Supply Current vs. Supply Voltage, V_{IN1}/V_{IN2}

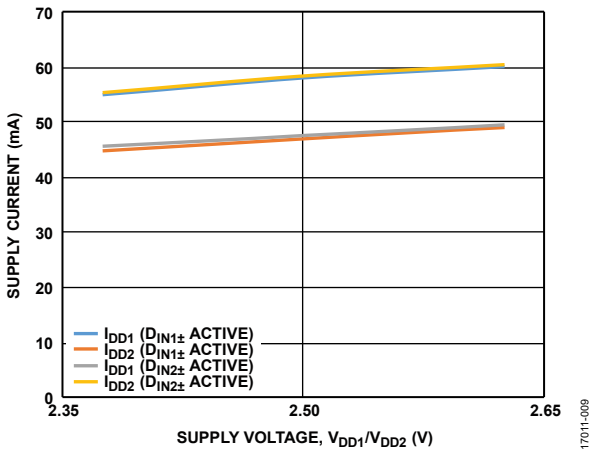


Figure 14. Supply Current vs. Supply Voltage, V_{DD1}/V_{DD2}

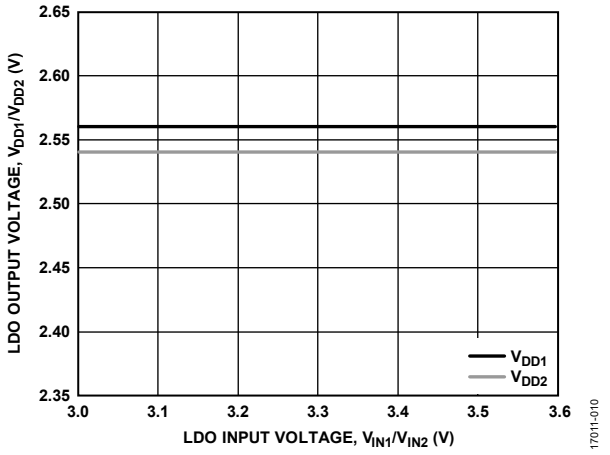


Figure 15. LDO Output Voltage, V_{DD1}/V_{DD2} vs. LDO Input Voltage, V_{IN1}/V_{IN2}

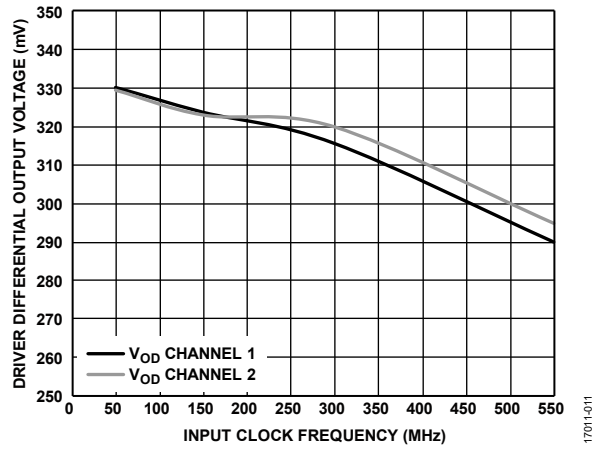


Figure 16. Driver Differential Output Voltage vs. Input Clock Frequency

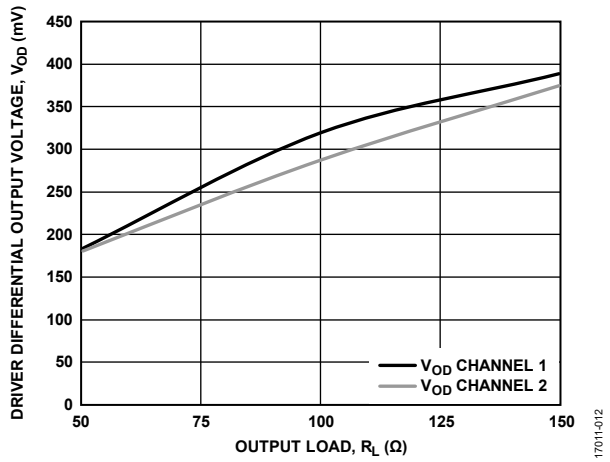


Figure 17. Driver Differential Output Voltage, V_{OD} vs. Output Load, R_L

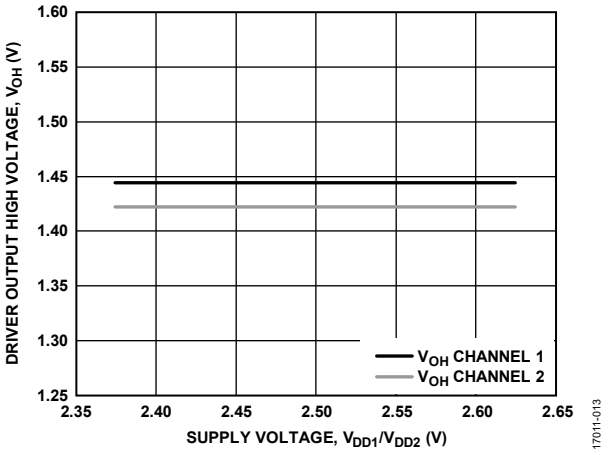


Figure 18. Driver Output High Voltage, V_{OH} vs. Supply Voltage, V_{DD1}/V_{DD2}

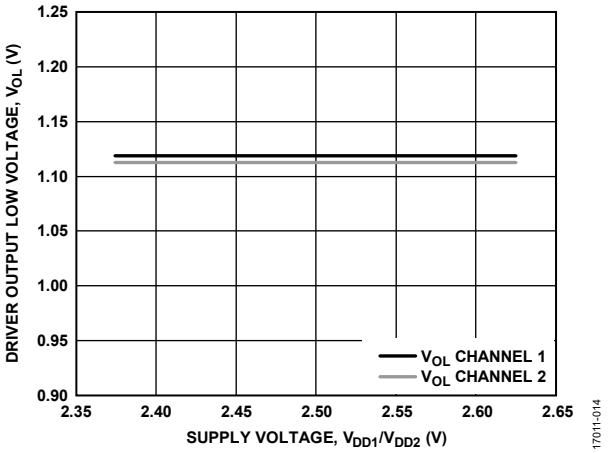


Figure 19. Driver Output Low Voltage, V_{OL} vs. Supply Voltage, V_{DD1}/V_{DD2}

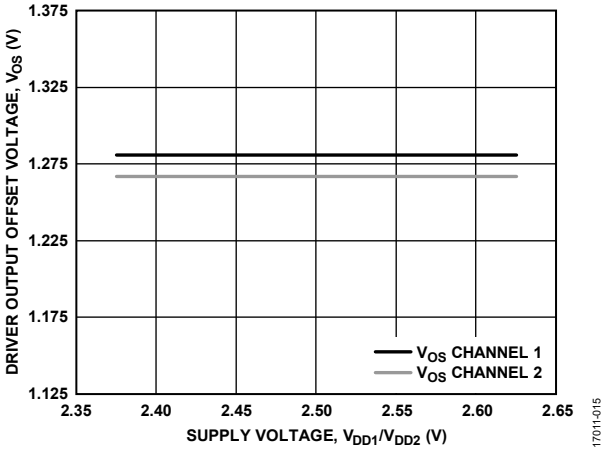


Figure 20. Driver Output Offset Voltage, V_{OS} vs. Supply Voltage, V_{DD1}/V_{DD2}

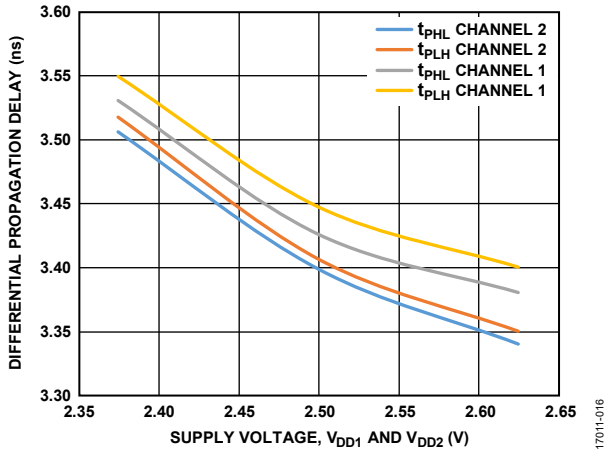


Figure 21. Differential Propagation Delay vs. Supply Voltage, V_{DD1} and V_{DD2}

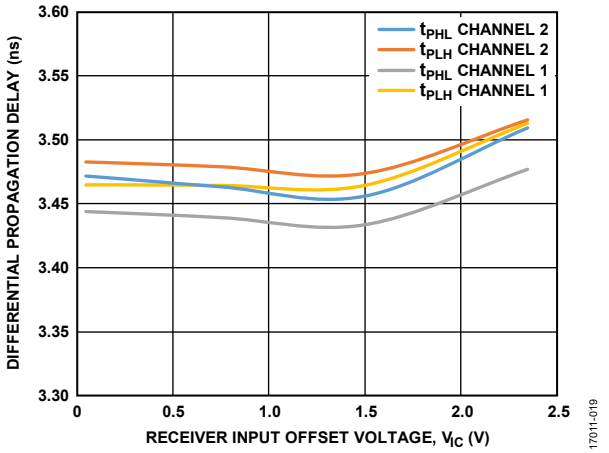


Figure 24. Differential Propagation Delay vs. Receiver Input Offset Voltage, V_{IC}

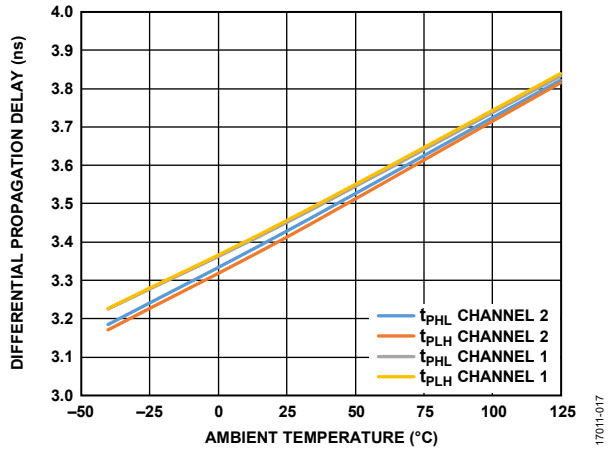


Figure 22. Differential Propagation Delay vs. Ambient Temperature

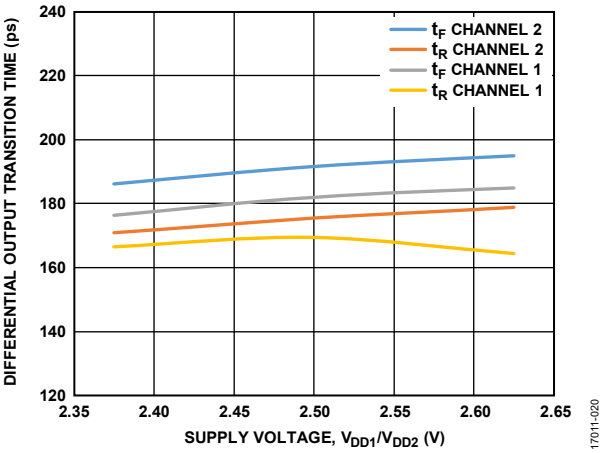


Figure 25. Differential Output Transition Time vs. Supply Voltage, V_{DD1}/V_{DD2}

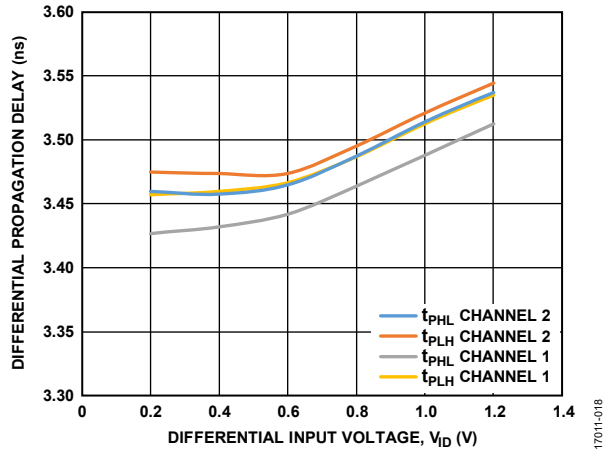


Figure 23. Differential Propagation Delay vs. Differential Input Voltage, V_{ID}

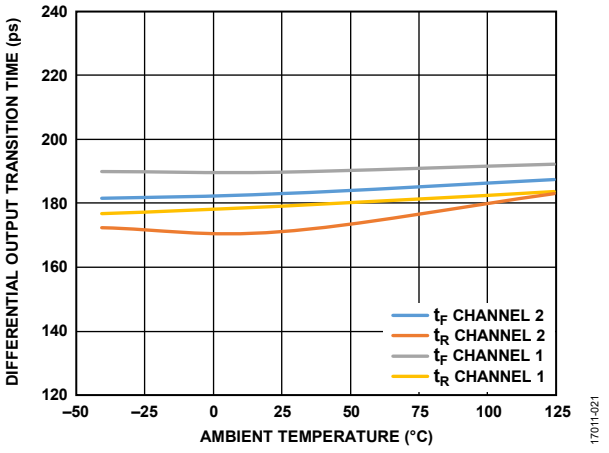


Figure 26. Differential Output Transition Time vs. Ambient Temperature

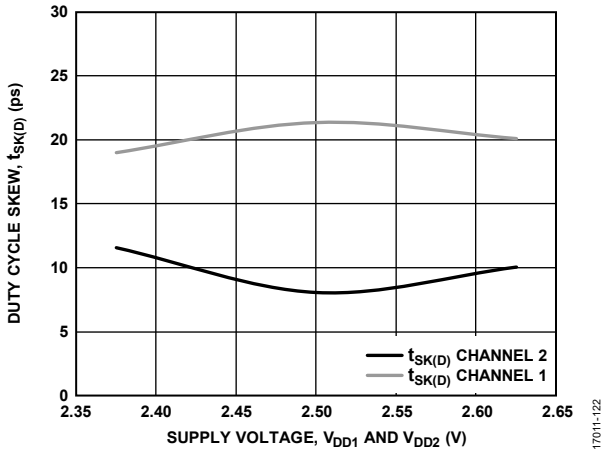


Figure 27. Duty Cycle Skew, $t_{SK(D)}$ vs. Supply Voltage, V_{DD1} and V_{DD2}

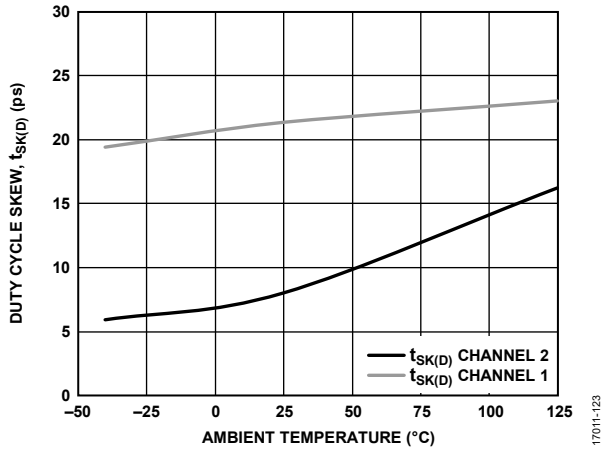


Figure 28. Duty Cycle Skew, $t_{SK(D)}$ vs. Ambient Temperature

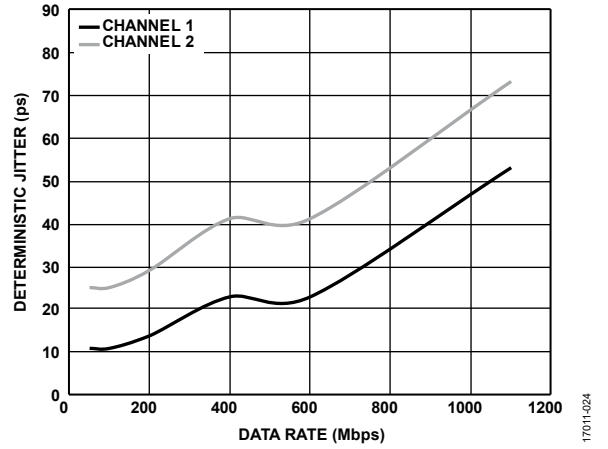


Figure 29. Deterministic Jitter vs. Data Rate

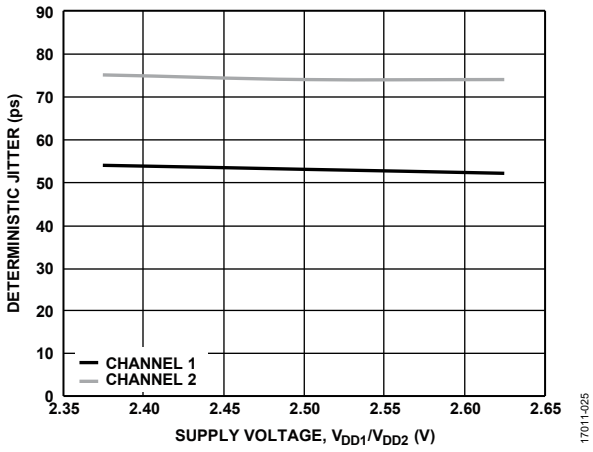


Figure 30. Deterministic Jitter vs. Supply Voltage, V_{DD1}/V_{DD2}

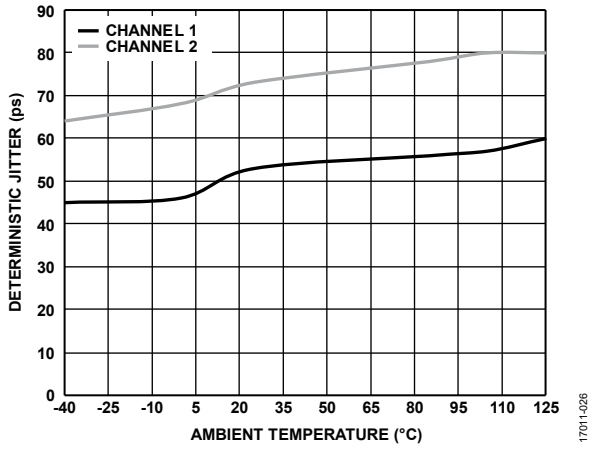


Figure 31. Deterministic Jitter vs. Ambient Temperature

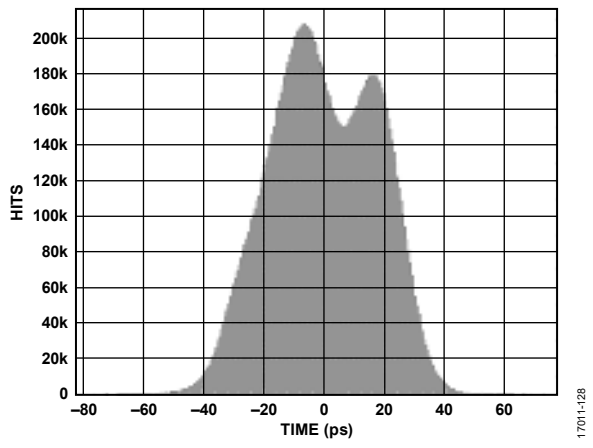


Figure 32. Time Interval Error (TIE) Histogram for $D_{OUT1\pm}$ at 550 MHz

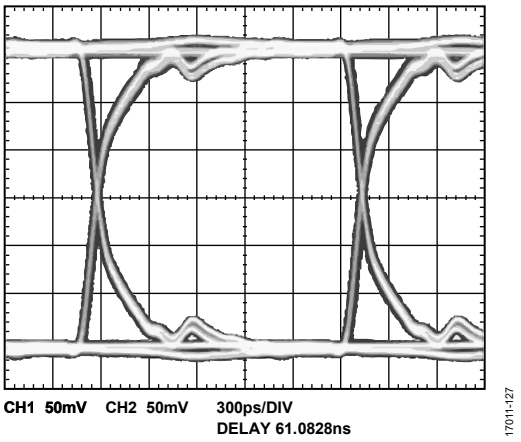


Figure 33. Eye Diagram for $D_{OUT1\pm}$ at 300 MHz

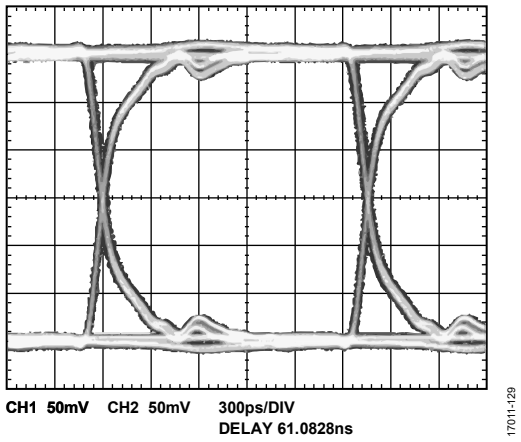


Figure 35. Eye Diagram for $D_{OUT2\pm}$ at 300 MHz

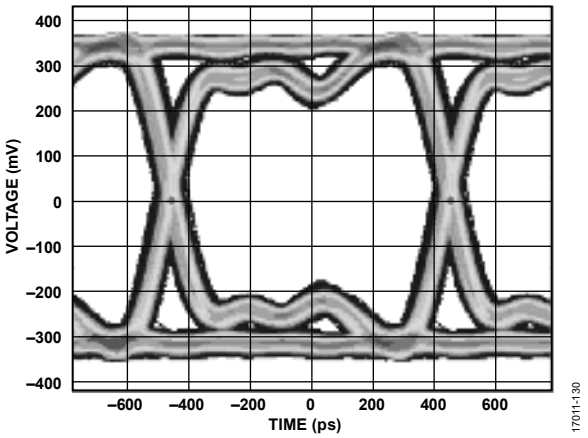


Figure 34. Eye Diagram for $D_{OUT1\pm}$ at 550 MHz

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

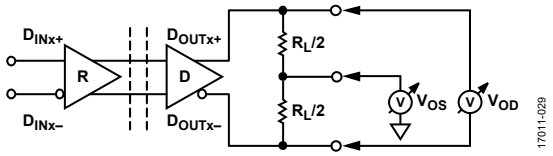


Figure 36. Driver Test Circuit

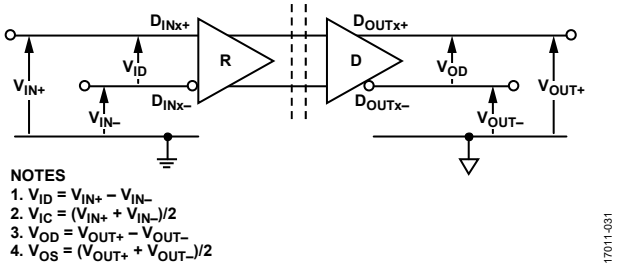


Figure 38. Voltage Definitions

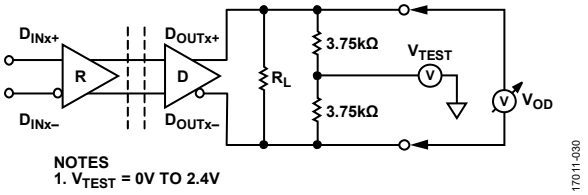


Figure 37. Driver Test Circuit (Full Load Across Common-Mode Range)

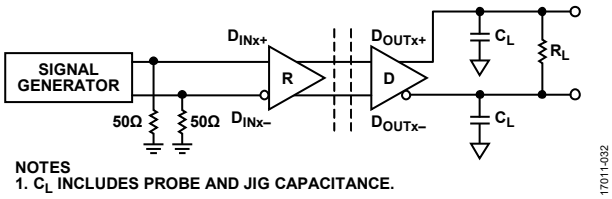


Figure 39. Timing Test Circuit

THEORY OF OPERATION

The ADN4654/ADN4655/ADN4656 are TIA/EIA-644-A LVDS compliant isolated buffers. LVDS signals applied to the inputs are transmitted on the outputs of the buffer, and galvanic isolation is integrated between the two sides of the device. This integration allows drop-in isolation of the LVDS signal chains.

The LVDS receiver detects the differential voltage present across a termination resistor on an LVDS input. An integrated digital isolator transmits the input state across the isolation barrier, and an LVDS driver outputs the same state as the input.

When there is a positive differential voltage of ≥100 mV across any $D_{INx\pm}$ pin, the corresponding D_{OUTx+} pin sources current. This current flows across the connected transmission line and termination at the receiver at the far end of the bus, while DOUTx− sinks the return current. When there is a negative differential voltage of ≤−100 mV across any $D_{INx\pm}$ pin, the corresponding D_{OUTx+} pin sinks current and the D_{OUTx-} pin sources current. Table 16 and Table 17 show these input and output combinations.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.1 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor (R_T). The received voltage is centered around 1.2 V. Because the differential voltage (V_{ID}) reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage magnitude ($|V_{ID}|$).

TRUTH TABLE AND FAIL-SAFE RECEIVER

The LVDS standard, TIA/EIA-644-A, defines normal receiver operation under two conditions: an input differential voltage of ≥+100 mV corresponding to one logic state, and a voltage of ≤−100 mV for the other logic state. Between these thresholds, standard LVDS receiver operation is undefined (the LVDS receiver can detect either state), as shown in Table 16 for the ADN4654. The ADN4655/ADN4656 incorporates a fail-safe circuit to ensure that the LVDS outputs are in a known state (logic high) when the input state is undefined (−100 mV < V_{ID} < +100 mV), as shown in Table 17.

This input state occurs when the inputs are floating (unconnected with no termination resistor), shorted, or when there is no active driver connected to the inputs with a termination resistor present. Open-circuit, short-circuit, and terminated or idle bus fail-safes, respectively, ensure a known output state for these conditions, as implemented by the ADN4655/ADN4656.

After these input states (−100 mV < V_{ID} < +100 mV) trigger the fail-safe circuit, there is a delay of up to 1.2 µs before the output is guaranteed to be high (V_{OD} ≥ 250 mV). During this time, the output may transition to, or stay in, a logic low state (V_{OD} ≤ −250 mV).

The fail-safe circuit triggers as soon as the input differential voltage remains between +100 mV and −100 mV for some nanoseconds. Therefore, very slow rise and fall times on the input signal, outside typical LVDS operation (350 ps maximum t_R/t_F), can potentially trigger the fail-safe circuit on a high to low crossover.

At the minimum $|V_{ID}|$ of 100 mV for normal operation, the rise and fall time must be ≤5 ns to avoid triggering a fail-safe state. Increasing $|V_{ID}|$ to 200 mV allows an input rise and fall time of up to 10 ns without triggering a fail-safe state. For speed applications with restricting data rates less than 30 Mbps, where slow high to low transitions in excess of this limit are expected, use external biasing resistors to introduce a minimum $|V_{ID}|$ of 100 mV if the fail-safe cannot trigger.

Table 16. ADN4654 Input and Output Operation

Input ($D_{INx\pm}$)			Output ($D_{OUTx\pm}$)		
Powered On	**V_{ID} (mV)**	**Logic**	**Powered On**	**V_{OD} (mV)**	**Logic**
Yes	≥100	High	Yes	≥250	High
Yes	≤−100	Low	Yes	≤−250	Low
Yes	−100 < V_{ID} < +100	Indeterminate	Yes	Indeterminate	Indeterminate
No	Don't care	Don't care	Yes	≥250	High

Table 17. ADN4655/ADN4656 Input and Output Operation

Input ($D_{INx\pm}$)			Output ($D_{OUTx\pm}$)		
Powered On	**V_{ID} (mV)**	**Logic**	**Powered On**	**V_{OD} (mV)**	**Logic**
Yes	≥100	High	Yes	≥250	High
Yes	≤−100	Low	Yes	≤−250	Low
Yes	−100 < V_{ID} < +100	Indeterminate	Yes	≥250	High
No	Don't care	Don't care	Yes	≥250	High

ISOLATION

In response to any change in the input state detected by the integrated LVDS receiver, an encoder circuit sends narrow (~1 ns) pulses to a decoder circuit using integrated transformer coils. The decoder is bistable and is, therefore, either set or reset by the pulses that indicate input transitions. The decoder state determines the LVDS driver output state in normal operation, which reflects the isolated LVDS buffer input state.

In the absence of input transitions for more than approximately 1 μs, a periodic set of refresh pulses, indicative of the correct input state, ensures dc correctness at the output (including the fail-safe output state, if applicable).

On power-up, the output state may initially be in the incorrect dc state if there are no input transitions. The output state is corrected within 1 μs by the refresh pulses.

If the decoder receives no internal pulses for more than approximately 1 μs, the device assumes that the input side is unpowered or nonfunctional, in which case, the output is set to a positive differential voltage (logic high).

APPLICATIONS INFORMATION

PCB LAYOUT

The ADN4654/ADN4655/ADN4656 can operate with high speed LVDS signals up to 0.55 GHz clock, or 1.1 Gbps nonreturn to zero (NRZ) data. When operating with such high frequencies, apply best practices for the LVDS trace layout and termination. Place a 100 Ω termination resistor as close as possible to the receiver, across the D_{INx+} and D_{INx-} pins.

Controlled 50 Ω impedance traces are needed on LVDS signal lines for full signal integrity, reduced system jitter, and minimizing electromagnetic interference (EMI) from the PCB. Trace widths, lateral distance within each pair, and distance to the ground plane underneath all must be chosen appropriately. Via fencing to the PCB ground between pairs is also a best practice to minimize crosstalk between adjacent pairs.

The ADN4654/ADN4655/ADN4656 pass EN 55022 Class B emissions limits without extra considerations required for the isolator when operating with up to 1.1 Gbps PRBS data. When isolating high speed clocks (for example, 0.55 GHz), a reduced PCB clearance (isolation gap) may be required with the 20-lead SOIC_W model to reduce dipole antenna effects and provide sufficient margin below Class B emissions limits.

The best practice for high speed PCB design avoids any other emissions from PCBs in applications that use the ADN4654/ADN4655/ADN4656. Take care when configuring off-board connections, where switching transients from high speed LVDS signals (clocks in particular) can conduct onto cabling, resulting in radiated emissions. Use common-mode chokes, ferrites, or other filters as appropriate at the LVDS connectors, as well as cable shield or PCB ground connections to earth or chassis.

The ADN4654/ADN4655/ADN4656 require appropriate decoupling of the V_{DDx} pins with 100 nF capacitors. If the integrated LDO regulator is not used, and a 2.5 V supply is connected directly, connect the appropriate V_{INx} pin to the supply as well, as shown in Figure 40, using the ADN4654 as an example.

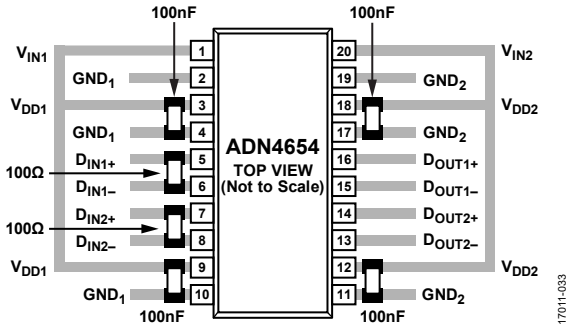


Figure 40. Required PCB Layout When Not Using LDO Regulator (2.5 V Supply)

When the integrated LDO regulator is used, bypass capacitors of 1 µF are required on the V_{INx} pins and on the nearest V_{DDx} pins (LDO output), as shown in Figure 41.

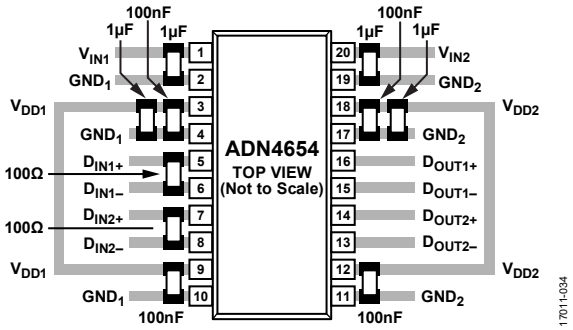


Figure 41. Required PCB Layout When Using LDO Regulator (3.3 V Supply)

APPLICATION EXAMPLES

High speed LVDS interfaces for the analog front-end (AFE), processor to processor communication, or video and imaging data can be isolated using the ADN4654, as an example, between components, between boards, or at a cable interface. The ADN4654 provides the galvanic isolation required for robust external ports, and the low jitter and high drive strength of the device allow communication along short cable runs of a few meters. High common-mode immunity ensures communication integrity even in harsh, noisy environments, and isolation can protect against electromagnetic compatibility (EMC) transients up to ±8 kV peak, such as ESD, electrical fast transient (EFT), and surge. The ADN4654 can isolate a range of video and imaging protocols, including protocols that use current mode logic (CML) rather than LVDS for the physical layer. One example is High-Definition Multimedia Interface (HDMI), where ac coupling and biasing and termination resistor networks are used as shown in Figure 42 to convert between CML (used by the transition minimized differential signaling (TMDS) data and clock lanes) and the LVDS levels required by the ADN4654. Additional Analog Devices isolator components, such as the ADuM1250/ADuM1251 I^2C isolators, can be used to isolate control signals and power (ADuM5020 *iso*Power integrated, isolated dc-to-dc converter). This circuit supports resolutions up to 720p.

Other circuits can use the ADN4654 for isolating MIPI CSI-2, DisplayPort, and LVDS-based protocols such as FPD-Link. Use of a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) serializer/deserializer (SERDES) expands bandwidth through multiple ADN4654 devices to support 1080p or 4K video resolutions, providing an alternative to short reach fiber links.

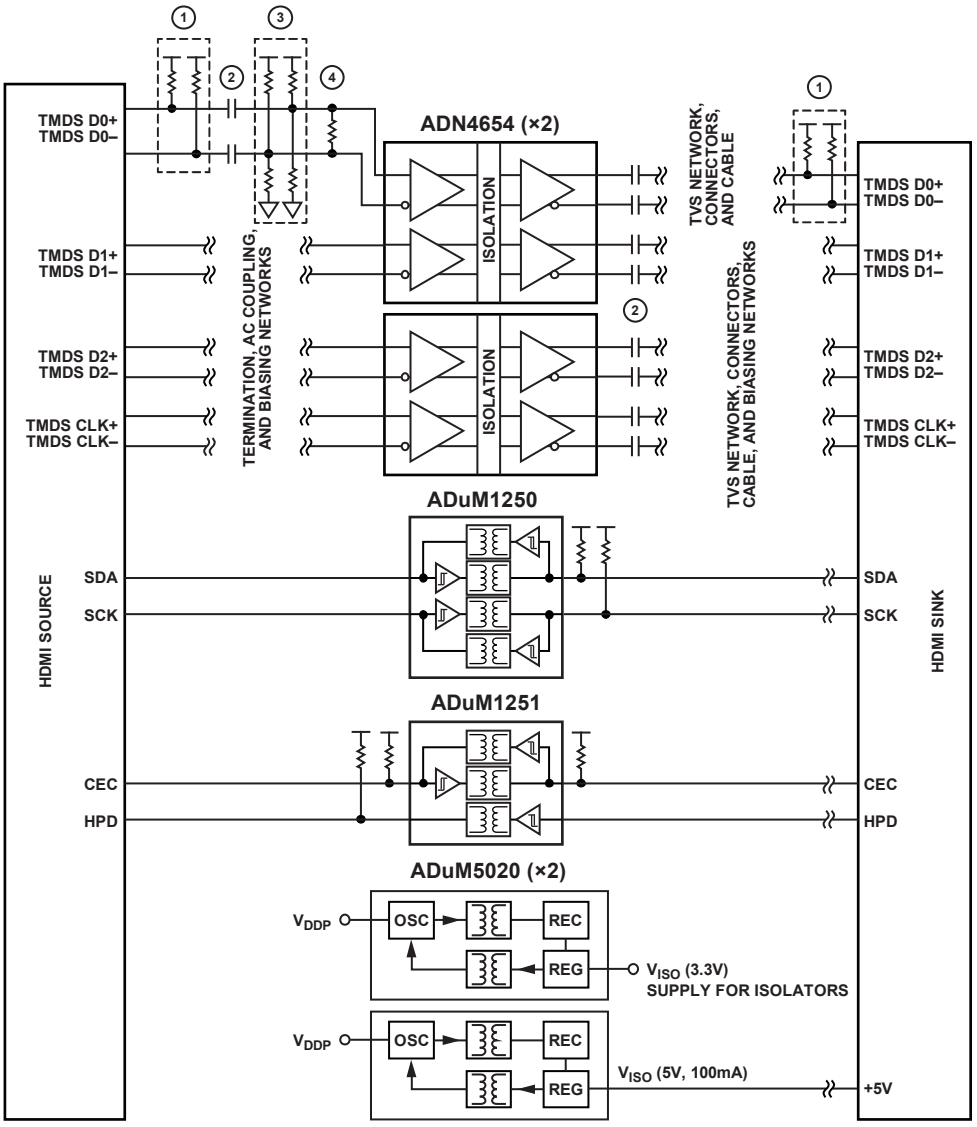


Figure 42. Example Isolated Video Interface (HDMI) Using the ADN4654

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the device is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large, either to falsely set or reset the decoder. The following analysis defines such conditions. The ADN4654/ADN4655/ADN4656 are examined in a 2.375 V operating condition because this operating condition represents the most susceptible mode of operation for these products.

The pulses at the transformer output have an amplitude greater than 0.5 V. The decoder has a sensing threshold of about 0.25 V, therefore establishing a 0.25 V margin in which induced voltages are tolerated. The voltage (V) induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
$d\beta$ is the change in magnetic flux density.
dt is the change in time.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADN4654/ADN4655/ADN4656 and an imposed requirement that the induced voltage be, at most, 50% of the 0.25 V margin at the decoder, a maximum allowable external magnetic flux density is calculated as shown in Figure 43.

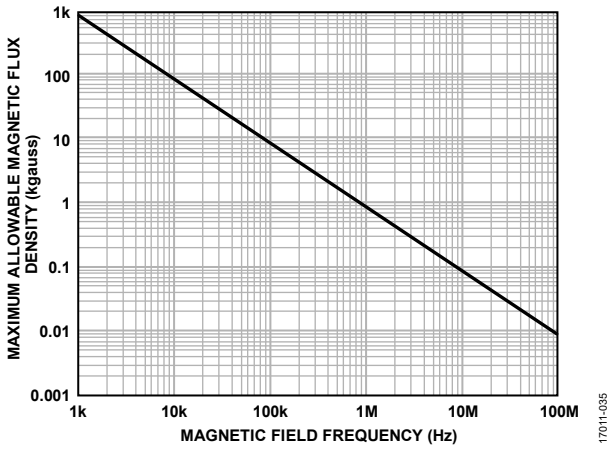


Figure 43. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.92 kgauss induces a voltage of 0.125 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs with the worst case polarity during a transmitted pulse, the applied magnetic field reduces the received pulse from >0.5 V to 0.375 V. This voltage is still higher than the 0.25 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADN4654/ADN4655/ADN4656 transformers. Figure 44 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADN4654/ADN4655/ADN4656 are insensitive to external fields. Only extremely large, high frequency currents that are close to the component can potentially be a concern. For the 1 MHz example noted, a 2.29 kA current must be placed 5 mm from the ADN4654/ADN4655/ADN4656 to affect component operation.

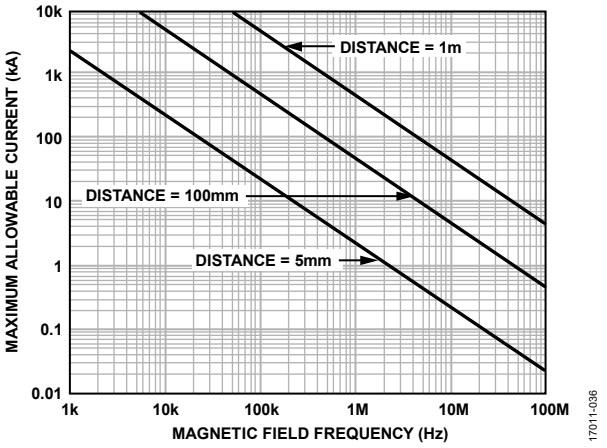


Figure 44. Maximum Allowable Current for Various Current to ADN4654 Spacings

In combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Avoid PCB structures that form loops.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, which allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation barrier, pollution degree, and material group. The material group and creepage for ADN4654/ADN4655/ADN4656 are detailed in Table 4 and Table 5.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness of the insulation, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this type of waveform reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the isolation barrier, as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 45 and the following equations.

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\ \text{V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\,RMS} = 240\ \text{V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. Table 12 compares the value to the limits for the working voltage for the expected lifetime. Note that the dc working voltage limit in Table 12 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

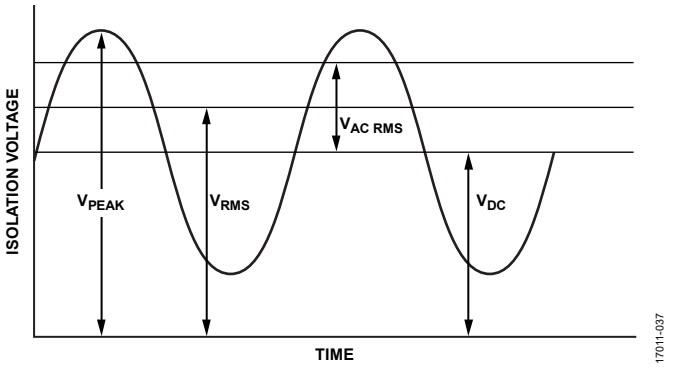
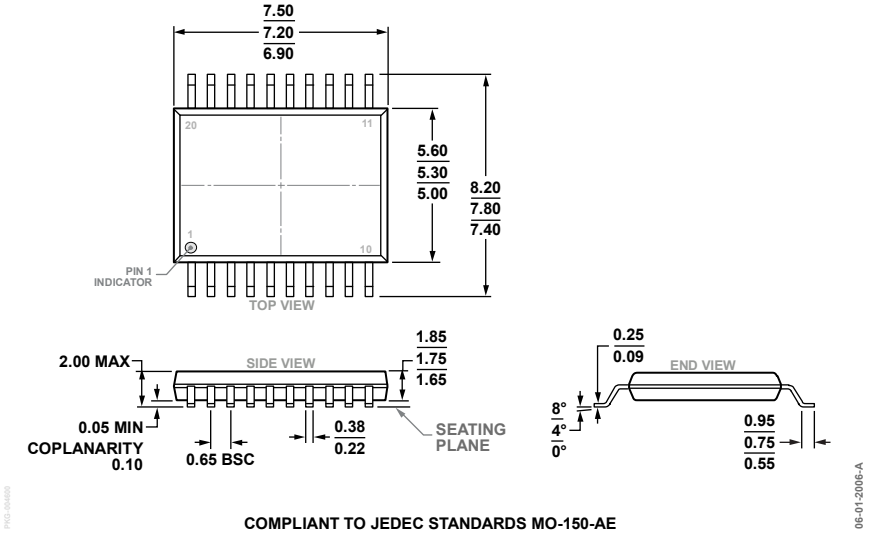


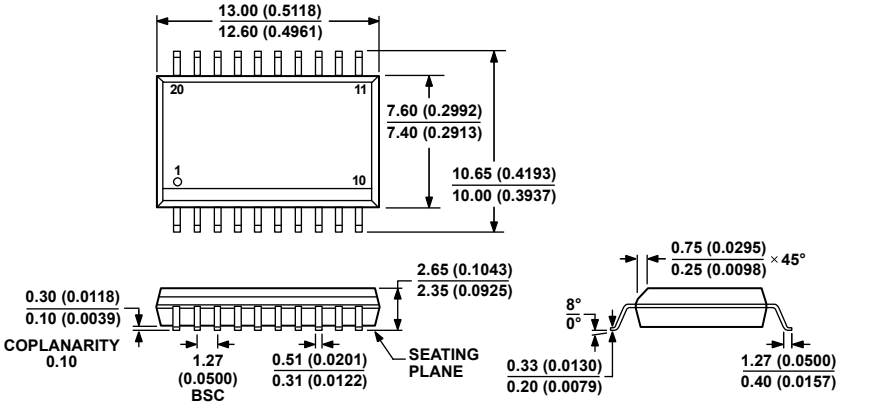
Figure 45. Critical Voltage Example

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AE

Figure 46. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 47. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN4654BRSZ	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4654BRSZ-RL7	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4654BRWZ	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
ADN4654BRWZ-RL7	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
ADN4655BRSZ	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4655BRSZ-RL7	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4655BRWZ	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
ADN4655BRWZ-RL7	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
ADN4656BRSZ	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4656BRSZ-RL7	−40°C to +125°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADN4656BRWZ	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
ADN4656BRWZ-RL7	−40°C to +125°C	20-Lead Wide Body, Standard Small Outline Package [SOIC_W]	RW-20
EVAL-ADN4654EBZ		ADN4654 SSOP Evaluation Board	
EVAL-ADN4654EB1Z		ADN4654 SOIC_W Evaluation Board	
EVAL-ADN4655EBZ		ADN4655 SSOP Evaluation Board	
EVAL-ADN4655EB1Z		ADN4655 SOIC_W Evaluation Board	
EVAL-ADN4656EBZ		ADN4656 SSOP Evaluation Board	
EVAL-ADN4656EB1Z		ADN4656 SOIC_W Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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