1.2 A, Low V_{IN}, Low Dropout Linear Regulator

Data Sheet

ADP1754/ADP1755

FEATURES

- Maximum output current: 1.2 A
- Input voltage range: 1.6 V to 3.6 V
- Low shutdown current: <2 µA
- Very low dropout voltage: 105 mV at 1.2 A load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: ±2%
- 7 fixed output voltage options with soft start
  - 0.75 V to 2.5 V (ADP1754)
- Adjustable output voltage option with soft start
  - 0.75 V to 3.3 V (ADP1755)
- High PSRR
  - 65 dB at 1 kHz
  - 65 dB at 10 kHz
  - 54 dB at 100 kHz
- 23 µV rms at 0.75 V output
- Stable with small 4.7 µF ceramic output capacitor
- Excellent load and line transient response
- Current-limit and thermal overload protection
- Power-good indicator
- Logic-controlled enable
- Reverse current protection

APPLICATIONS

- Server computers
- Memory components
- Telecommunications equipment
- Network equipment
- DSP/FPGA/microprocessor supplies
- Instrumentation equipment/data acquisition systems

TYPICAL APPLICATION CIRCUITS

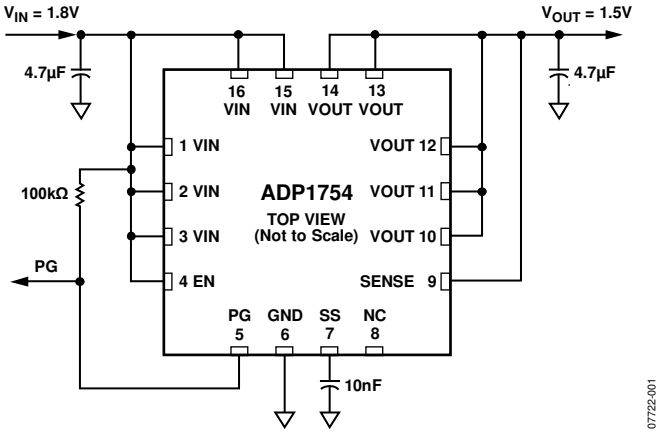


Figure 1. ADP1754 with Fixed Output Voltage, 1.5 V

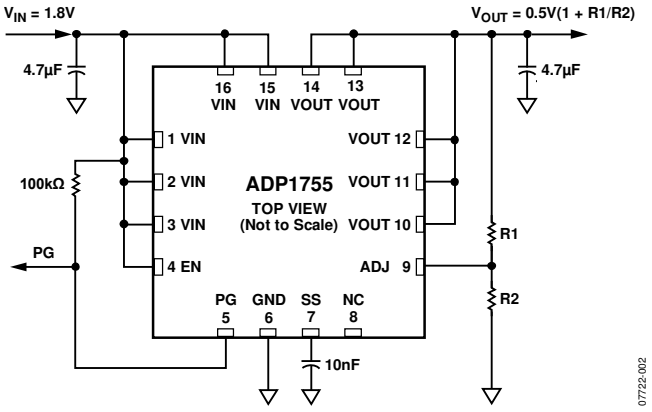


Figure 2. ADP1755 with Adjustable Output Voltage, 0.75 V to 3.3 V

GENERAL DESCRIPTION

The ADP1754/ADP1755 are low dropout (LDO) CMOS linear regulators that operate from 1.6 V to 3.6 V and provide up to 1.2 A of output current. These low V_{IN}/V_{OUT} LDOs are ideal for regulation of nanometer FPGA geometries operating from 2.5 V down to 1.8 V I/O rails, and for powering core voltages down to 0.75 V. Using an advanced proprietary architecture, the ADP1754/ADP1755 provide high power supply rejection ratio (PSRR) and low noise, and achieve excellent line and load transient response with only a small 4.7 µF ceramic output capacitor.

The ADP1754 is available in seven fixed output voltage options. The ADP1755 is the adjustable version, which allows output voltages that range from 0.75 V to 3.3 V via an external divider. The ADP1754/ADP1755 allow an external soft start capacitor to be connected to program the startup. A digital power-good output allows power system monitors to check the health of the output voltage.

The ADP1754/ADP1755 are available in a 16-lead, 4 mm × 4 mm LFCSP, making them not only very compact solutions, but also providing excellent thermal performance for applications that require up to 1.2 A of output current in a small, low profile footprint.

Rev. G
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REVISION HISTORY

4/14—Rev. F to Rev. G

Changes to Figure 1 and Figure 2 ... 1
Change to Table 4 ... 5
Changes to Figure 3 and Figure 4 ... 6
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

8/13—Rev. E to Rev. F

Changes to Ordering Guide ... 19

6/13—Rev. D to Rev. E

Changed Adjustable Output Voltage Option with Soft Start (ADP1755) from 0.75 V to 3.0 V to 0.75 V to 3.3 V (Throughout) ... 1
Updated Outline Dimensions ... 19

12/12—Rev. C to Rev. D

Added Junction Temperature of 150°C, Table 3 ... 5

9/12—Rev. B to Rev. C

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Changes to Ordering Guide ... 19

2/10—Rev. A to Rev. B

Changes to Table 4 ... 5
Changes to Ordering Guide ... 19

4/09—Rev. 0 to Rev. A

Changes to Adjustable Output Voltage Accuracy (ADP1755) Parameter, Table 1 ... 3
Changes to Table 3 ... 5

10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 1.6 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	1.6		3.6	V
OPERATING SUPPLY CURRENT[1]	I_{GND}	I_{OUT} = 500 µA		90		µA
		I_{OUT} = 100 mA		400		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			800	µA
		I_{OUT} = 1.2 A		1.1		mA
		I_{OUT} = 1.2 A, T_J = −40°C to +125°C			1.4	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND, V_{IN} = 1.6 V		2	6	µA
		EN = GND, V_{IN} = 1.6 V, T_J = −40°C to +85°C			30	µA
		EN = GND, V_{IN} = 3.6 V, T_J = −40°C to +85°C			100	µA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy (ADP1754)	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		I_{OUT} = 10 mA to 1.2 A	−1.5		+1.5	%
		10 mA < I_{OUT} < 1.2 A, T_J = −40°C to +125°C	−2		+2	%
Adjustable Output Voltage Accuracy (ADP1755)[2]	V_{ADJ}	I_{OUT} = 10 mA	0.495	0.5	0.505	V
		I_{OUT} = 10 mA to 1.2 A	0.495		0.505	V
		10 mA < I_{OUT} < 1.2 A, T_J = −40°C to +125°C	0.490		0.510	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 3.6 V, T_J = −40°C to +125°C	−0.3		+0.3	%/V
LOAD REGULATION[3]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 1.2 A, T_J = −40°C to +125°C			0.6	%/A
DROPOUT VOLTAGE[4]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 1.8 V		10		mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			16	mV
		I_{OUT} = 1.2 A, V_{OUT} ≥ 1.8 V		105		mV
		I_{OUT} = 1.2 A, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			200	mV
START-UP TIME[5]	$t_{START-UP}$	C_{SS} = 0 nF, I_{OUT} = 10 mA		200		µs
		C_{SS} = 10 nF, I_{OUT} = 10 mA		5.2		ms
CURRENT-LIMIT THRESHOLD[6]	I_{LIMIT}		1.5	2	5	A
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
PG OUTPUT LOGIC LEVEL						
PG Output Logic High	PG_{HIGH}	1.6 V ≤ V_{IN} ≤ 3.6 V, I_{OH} < 1 µA	1.0			V
PG Output Logic Low	PG_{LOW}	1.6 V ≤ V_{IN} ≤ 3.6 V, I_{OL} < 2 mA			0.4	V
PG Output Delay from EN Transition Low to High		1.6 V ≤ V_{IN} ≤ 3.6 V, C_{SS} = 10 nF		5.5		ms
PG OUTPUT THRESHOLD						
Output Voltage Falling	PG_{FALL}	1.6 V ≤ V_{IN} ≤ 3.6 V		−10		%
Output Voltage Rising	PG_{RISE}	1.6 V ≤ V_{IN} ≤ 3.6 V		−6.5		%
EN INPUT						
EN Input Logic High	V_{IH}	1.6 V ≤ V_{IN} ≤ 3.6 V	1.2			V
EN Input Logic Low	V_{IL}	1.6 V ≤ V_{IN} ≤ 3.6 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = VIN or GND		0.1	1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			1.58	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	1.25			V
Hysteresis	$UVLO_{HYS}$	T_J = 25°C		100		mV
SOFT START CURRENT	I_{SS}	1.6 V ≤ V_{IN} ≤ 3.6 V	0.6	0.9	1.2	µA
ADJ INPUT BIAS CURRENT (ADP1755)	ADJ_{I-BIAS}	1.6 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +125°C		10	150	nA
SENSE INPUT BIAS CURRENT	SNS_{I-BIAS}	1.6 V ≤ V_{IN} ≤ 3.6 V		10		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 0.75 V		23		μV rms
		10 Hz to 100 kHz, V_{OUT} = 2.5 V		65		μV rms
POWER SUPPLY REJECTION RATIO	PSRR	V_{IN} = V_{OUT} + 1 V, I_{OUT} = 10 mA				
		1 kHz, V_{OUT} = 0.75 V		65		dB
		1 kHz, V_{OUT} = 2.5 V		56		dB
		10 kHz, V_{OUT} = 0.75 V		65		dB
		10 kHz, V_{OUT} = 2.5 V		56		dB
		100 kHz, V_{OUT} = 0.75 V		54		dB
		100 kHz, V_{OUT} = 2.5 V		51		dB

[1] Minimum output load current is 500 μA.
[2] Accuracy when VOUT is connected directly to ADJ. When VOUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.
[3] Based on an end-point calculation using 10 mA and 1.2 A loads. See Figure 6 for typical load regulation performance.
[4] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.6 V.
[5] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 95% of its nominal value.
[6] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	3.3			μF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.1	Ω

[1] The minimum input and output capacitance should be greater than 3.3 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with this LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +4.0 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to VIN
SS to GND	−0.3 V to VIN
PG to GND	−0.3 V to +4.0 V
SENSE/ADJ to GND	−0.3 V to VIN
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−40°C to +125°C
Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP1754/ADP1755 may be damaged if the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in × 3 in circuit board. Refer to JEDEC JESD51-7 for detailed information about board construction. For more information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JEDEC JESD51-8 and JESD51-12 documents for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

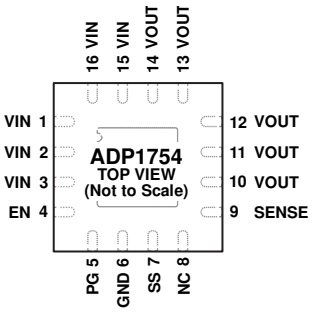
Package Type	θ_{JA}	Ψ_{JB}	Unit
16-Lead LFCSP with Exposed Pad (CP-16-23)	42	25.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

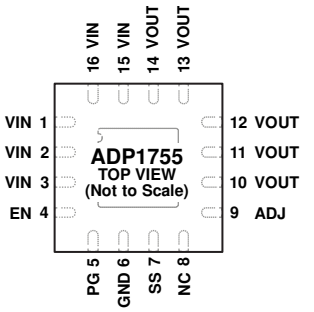
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO THE GROUND PLANE ON THE BOARD.

07722-003

Figure 3. ADP1754 Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO THE GROUND PLANE ON THE BOARD.

07722-004

Figure 4. ADP1755 Pin Configuration

Table 5. Pin Function Descriptions

ADP1754 Pin No.	ADP1755 Pin No.	Mnemonic	Description
1, 2, 3, 15, 16	1, 2, 3, 15, 16	VIN	Regulator Input Supply. Bypass VIN to GND with a 4.7 µF or greater capacitor. Note that all five VIN pins must be connected to the source.
4	4	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to VIN.
5	5	PG	Power Good. This open-drain output requires an external pull-up resistor to VIN. If the part is in shutdown mode, current-limit mode, thermal shutdown, or if it falls below 90% of the nominal output voltage, PG immediately transitions low.
6	6	GND	Ground.
7	7	SS	Soft Start. A capacitor connected to this pin determines the soft start time.
8	8	NC	Not Connected. No internal connection.
9	N/A	SENSE	Sense. This pin measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load.
N/A	9	ADJ	Adjust. A resistor divider from VOUT to ADJ sets the output voltage.
10, 11, 12, 13, 14	10, 11, 12, 13, 14	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 4.7 µF or greater capacitor. Note that all five VOUT pins must be connected to the load.
17 (EPAD)	17 (EPAD)	Exposed paddle (EPAD)	The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to GND inside the package. It is recommended that the exposed pad be connected to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.9 V, V_{OUT} = 1.5 V, I_{OUT} = 10 mA, C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

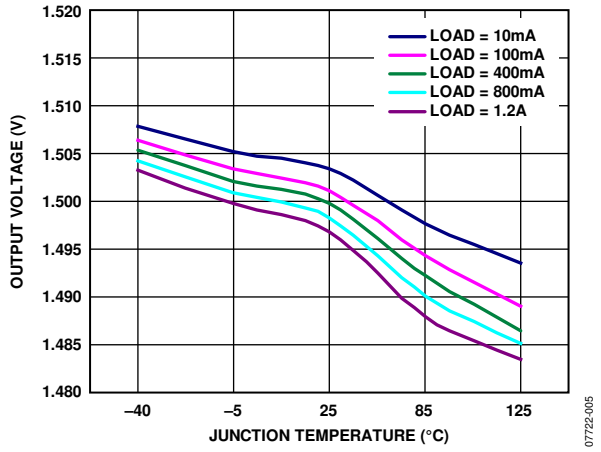


Figure 5. Output Voltage vs. Junction Temperature

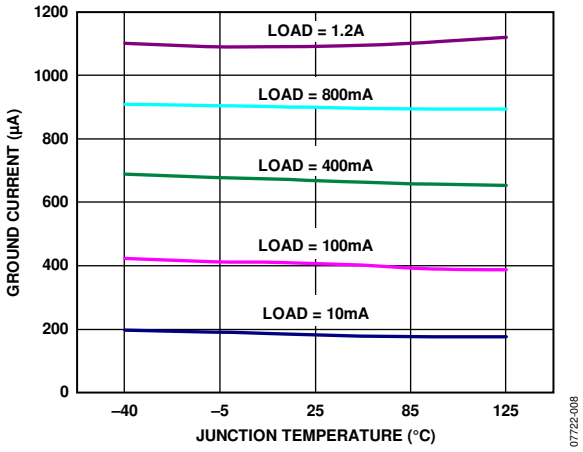


Figure 8. Ground Current vs. Junction Temperature

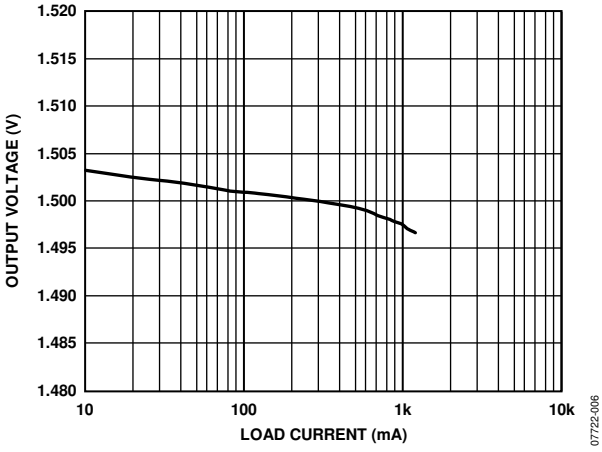


Figure 6. Output Voltage vs. Load Current

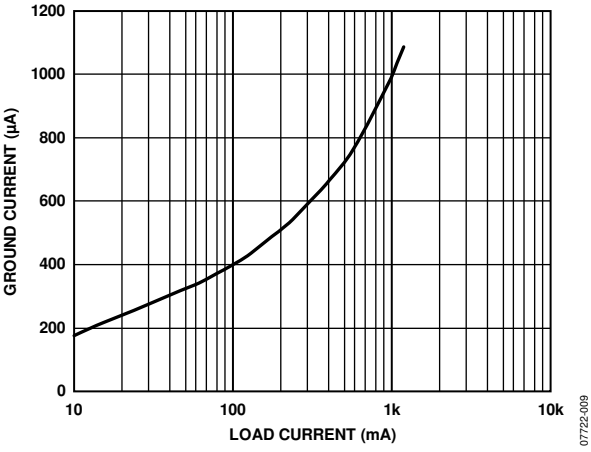


Figure 9. Ground Current vs. Load Current

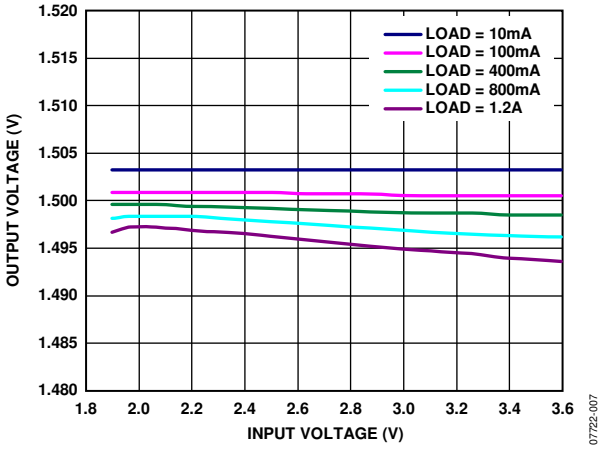


Figure 7. Output Voltage vs. Input Voltage

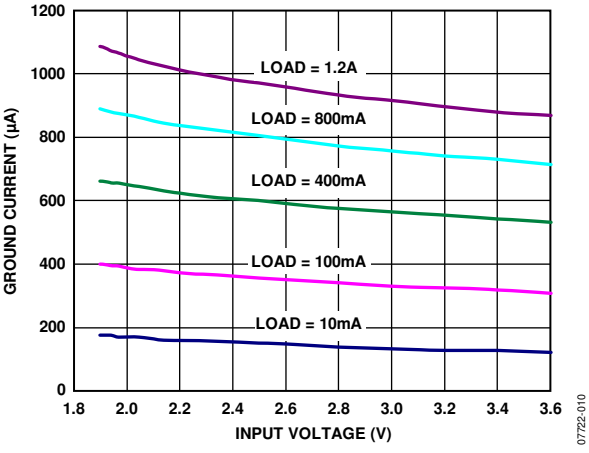


Figure 10. Ground Current vs. Input Voltage

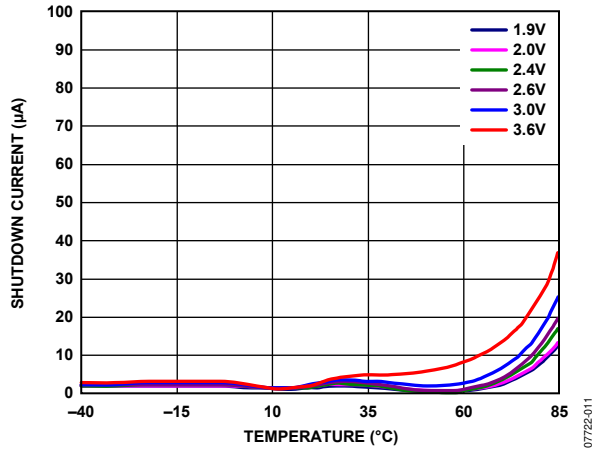


Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

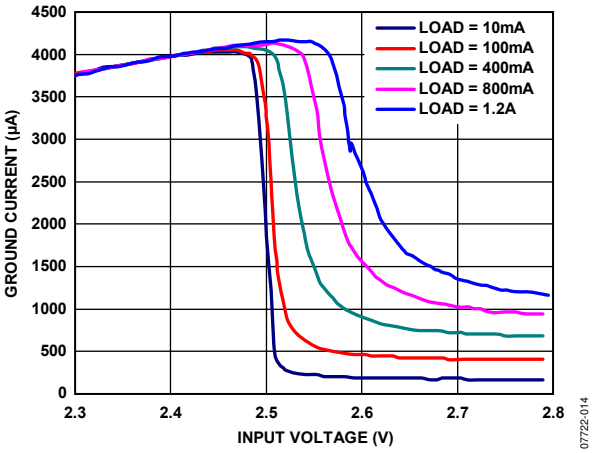


Figure 14. Ground Current vs. Input Voltage (in Dropout), V_{OUT} = 2.5 V

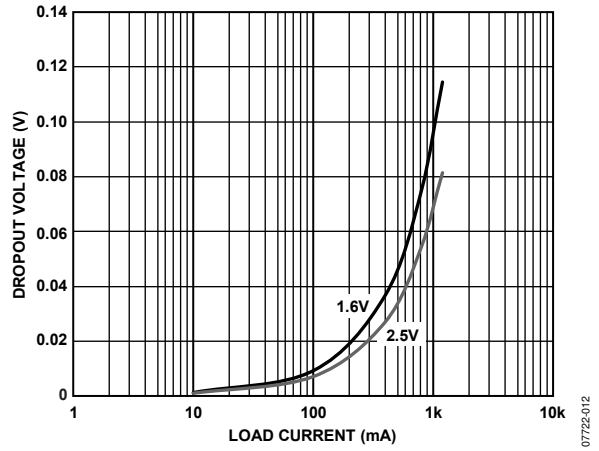


Figure 12. Dropout Voltage vs. Load Current, V_{OUT} = 1.6 V, 2.5 V

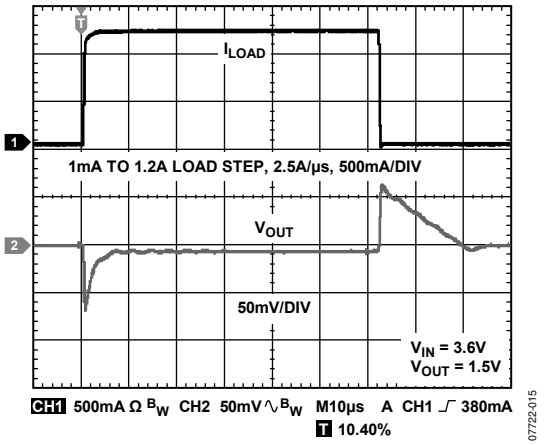


Figure 15. Load Transient Response, C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF

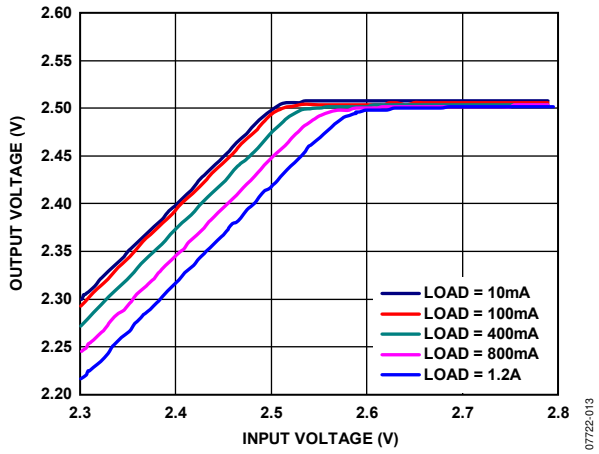


Figure 13. Output Voltage vs. Input Voltage (in Dropout), V_{OUT} = 2.5 V

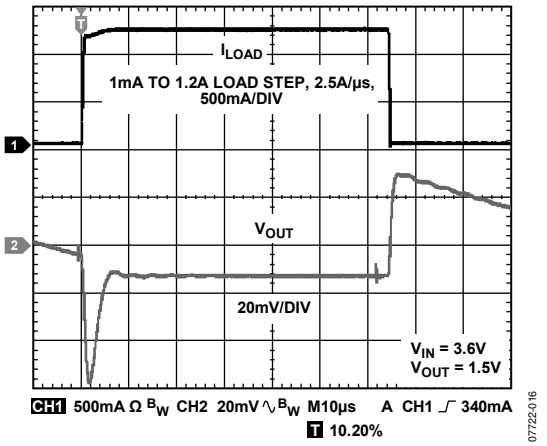


Figure 16. Load Transient Response, C_{IN} = 22 µF, C_{OUT} = 22 µF

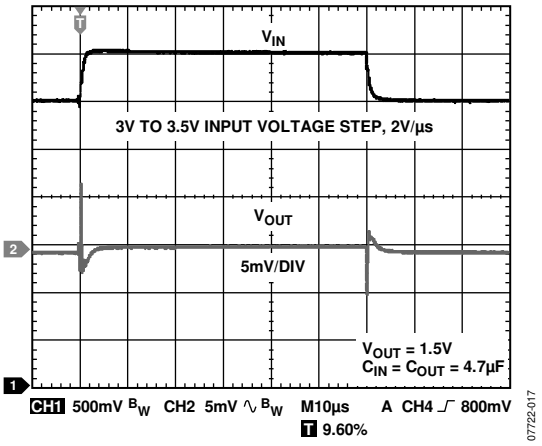


Figure 17. Line Transient Response, Load Current = 1200 mA

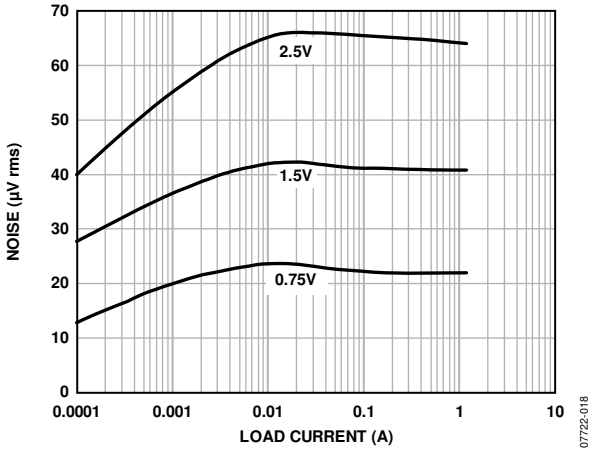


Figure 18. Noise vs. Load Current and Output Voltage

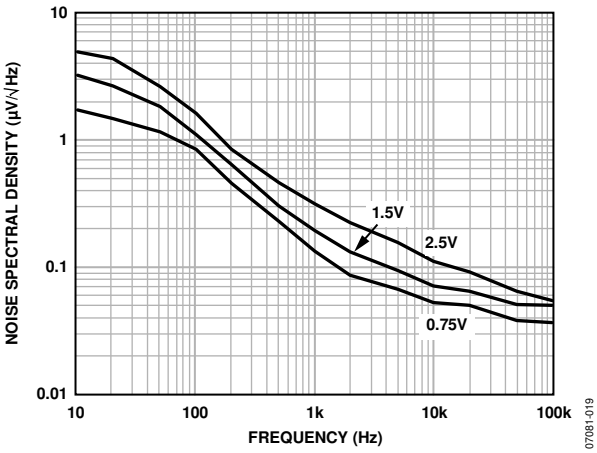


Figure 19. Noise Spectral Density vs. Output Voltage, I_{LOAD} = 10 mA

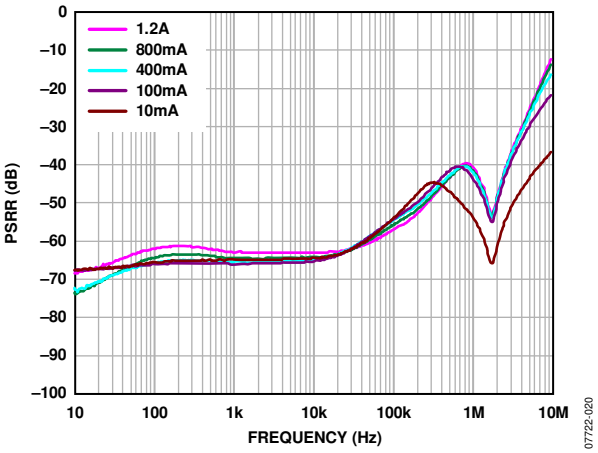


Figure 20. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 0.75 V, V_{IN} = 1.75 V

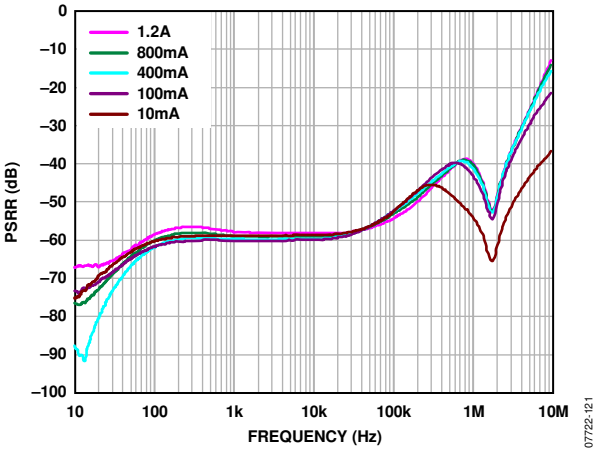


Figure 21. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.5 V, V_{IN} = 2.5 V

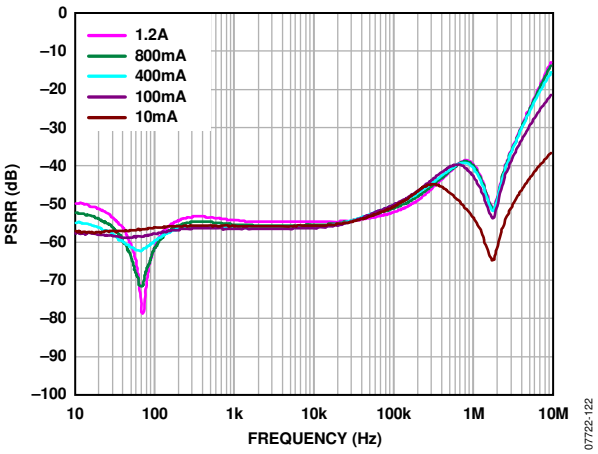


Figure 22. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 2.5 V, V_{IN} = 3.5 V

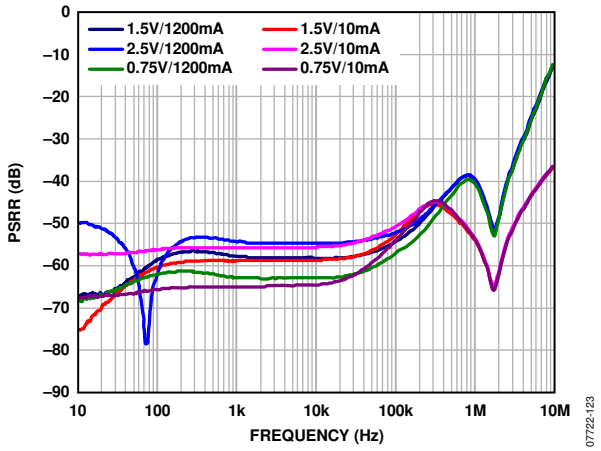


Figure 23. Power Supply Rejection Ratio vs. Frequency and Output Voltage

THEORY OF OPERATION

The ADP1754/ADP1755 are low dropout linear regulators that use an advanced, proprietary architecture to provide high power supply rejection ratio (PSRR) and excellent line and load transient response with only a small 4.7 µF ceramic output capacitor. Both devices operate from a 1.6 V to 3.6 V input rail and provide up to 1.2 A of output current. Supply current in shutdown mode is typically 2 µA.

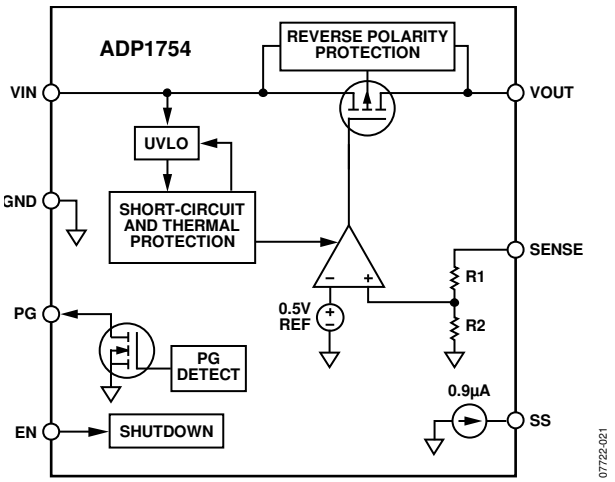


Figure 24. ADP1754 Internal Block Diagram

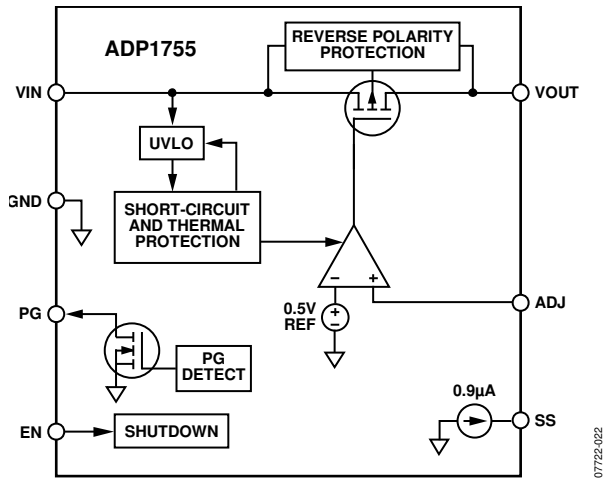


Figure 25. ADP1755 Internal Block Diagram

Internally, the ADP1754/ADP1755 consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass transistor, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP1754 is available in seven fixed output voltage options between 0.75 V and 2.5 V. The ADP1754 allows for connection of an external soft start capacitor that controls the output voltage ramp during startup. The ADP1755 is the adjustable version with an output voltage that can be set to a value between 0.75 V and 3.3 V by an external voltage divider. Both devices are controlled by an enable pin (EN).

SOFT START FUNCTION (ADP1754/ADP1755)

For applications that require a controlled startup, the ADP1754/ADP1755 provide a programmable soft start function. The programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. Upon startup, a 0.9 µA current source charges this capacitor. The ADP1754/ADP1755 start-up output voltage is limited by the voltage at SS, providing a smooth ramp-up to the nominal output voltage. The soft start time is calculated as follows:

$$t_{SS} = V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

where:

t_{SS} is the soft start period.
V_{REF} is the 0.5 V reference voltage.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (0.9 µA).

When the ADP1754/ADP1755 is disabled (using the EN pin), the soft start capacitor is discharged to GND through an internal 100 Ω resistor.

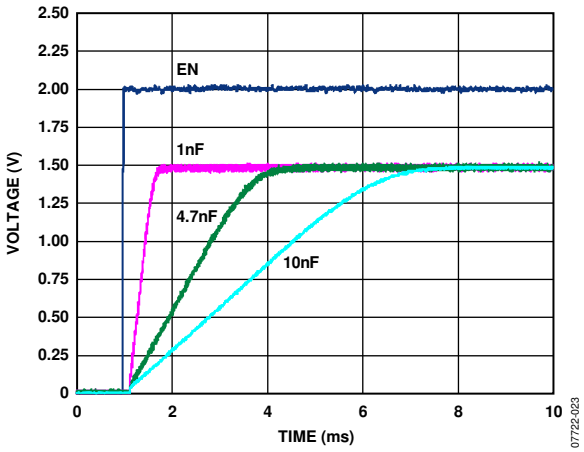


Figure 26. V_{OUT} Ramp-Up with External Soft Start Capacitor

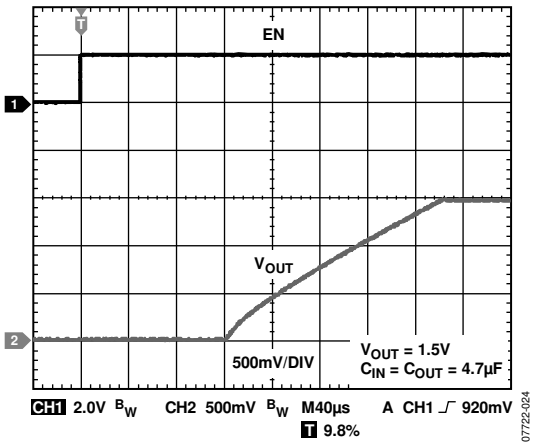


Figure 27. V_{OUT} Ramp-Up with Internal Soft Start

ADJUSTABLE OUTPUT VOLTAGE (ADP1755)

The output voltage of the ADP1755 can be set over a 0.75 V to 3.3 V range. The output voltage is set by connecting a resistive voltage divider from VOUT to ADJ. The output voltage is calculated using the following equation:

$$V_{OUT} = 0.5\ V \times (1 + R1/R2) \quad (2)$$

where:
R1 is the resistor from VOUT to ADJ.
R2 is the resistor from ADJ to GND.

The maximum bias current into ADJ is 150 nA. Therefore, to achieve less than 0.5% error due to the bias current, use values less than 60 kΩ for R2.

ENABLE FEATURE

The ADP1754/ADP1755 use the EN pin to enable and disable the VOUT pins under normal operating conditions. As shown in Figure 28, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

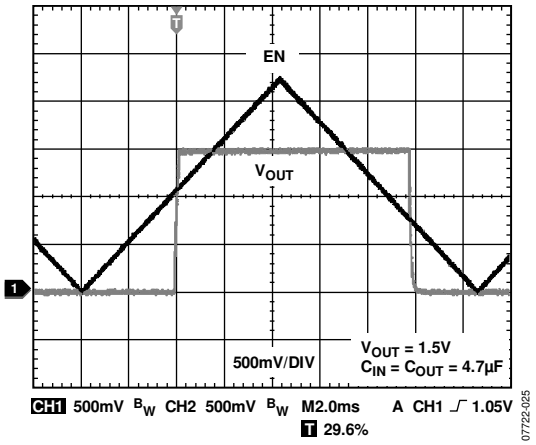


Figure 28. Typical EN Pin Operation

As shown in Figure 28, the EN pin has hysteresis built in. This hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 29 shows typical EN active/inactive thresholds when the input voltage varies from 1.6 V to 3.6 V.

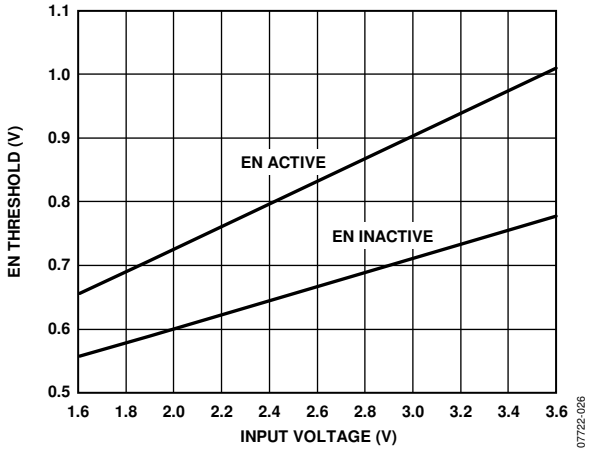


Figure 29. Typical EN Pin Thresholds vs. Input Voltage

POWER-GOOD FEATURE

The ADP1754/ADP1755 provide a power-good pin, PG, to indicate the status of the output. This open-drain output requires an external pull-up resistor to V_{IN}. If the part is in shutdown mode, current-limit mode, thermal shutdown, or if it falls below 90% of the nominal output voltage, PG immediately transitions low. During soft start, the rising threshold of the power-good signal is 93.5% of the nominal output voltage.

The open-drain output is held low when the ADP1754/ADP1755 have sufficient input voltage to turn on the internal PG transistor. An optional soft start delay can be detected. The PG transistor is terminated via a pull-up resistor to V_{OUT} or V_{IN}.

Power-good accuracy is 93.5% of the nominal regulator output voltage when this voltage is rising, with a 90% trip point when this voltage is falling.

Regulator input voltage brownouts or glitches trigger a power no-good if V_{OUT} falls below 90%.

A normal power-down triggers a power no-good when V_{OUT} drops below 90%.

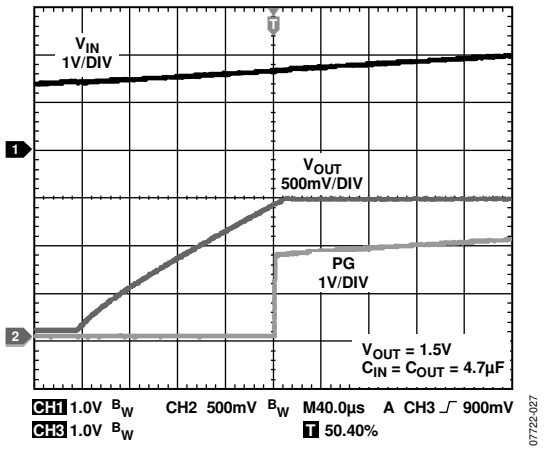


Figure 30. Typical PG Behavior vs. V_{OUT}, V_{IN} Rising (V_{OUT} = 1.5 V)

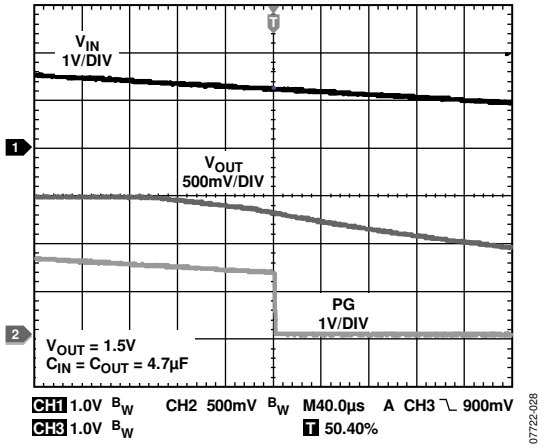


Figure 31. Typical PG Behavior vs. V_{OUT}, V_{IN} Falling (V_{OUT} = 1.5 V)

REVERSE CURRENT PROTECTION FEATURE

The ADP1754/ADP1755 have additional circuitry to protect against reverse current flow from VOUT to VIN. For a typical LDO with a PMOS pass device, there is an intrinsic body diode between VIN and VOUT. When V_{IN} is greater than V_{OUT}, this diode is reverse-biased. If V_{OUT} is greater than V_{IN}, the intrinsic diode becomes forward-biased and conducts current from VOUT to VIN, potentially causing destructive power dissipation. The reverse current protection circuitry detects when V_{OUT} is greater than V_{IN} and reverses the direction of the intrinsic diode connection, reverse-biasing the diode. The gate of the PMOS pass device is also connected to VOUT, keeping the device off.

Figure 32 shows a plot of the reverse current vs. the V_{OUT} to V_{IN} differential.

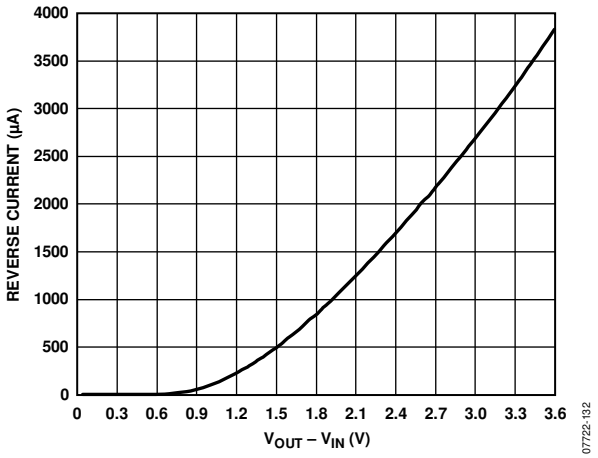


Figure 32. Reverse Current vs. $V_{OUT} - V_{IN}$

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1754/ADP1755 are designed for operation with small, space-saving ceramic capacitors, but they can function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 3.3 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure the stability of the ADP1754/ADP1755. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1754/ADP1755 to large changes in load current. Figure 33 and Figure 34 show the transient responses for output capacitance values of 4.7 µF and 22 µF, respectively.

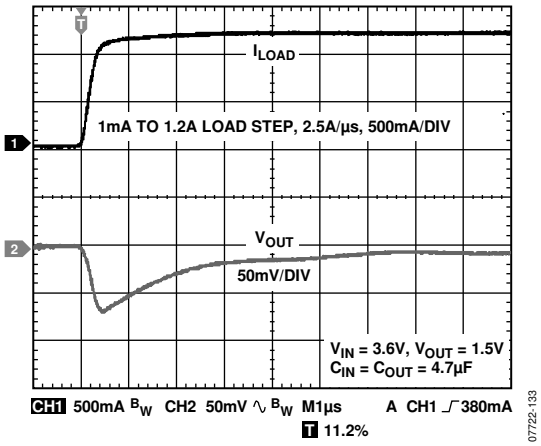


Figure 33. Output Transient Response, C_{OUT} = 4.7 µF

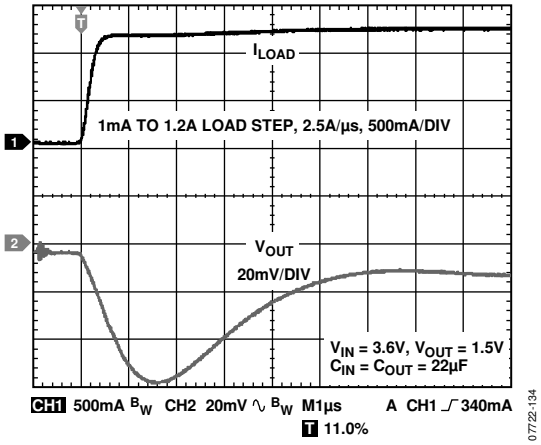


Figure 34. Output Transient Response, C_{OUT} = 22 µF

Input Bypass Capacitor

Connecting a 4.7 µF capacitor from the VIN pin to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 4.7 µF is required, it is recommended that the input capacitor be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1754, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 35 shows the capacitance vs. voltage bias characteristics of an 0805 case, 4.7 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package size or voltage rating.

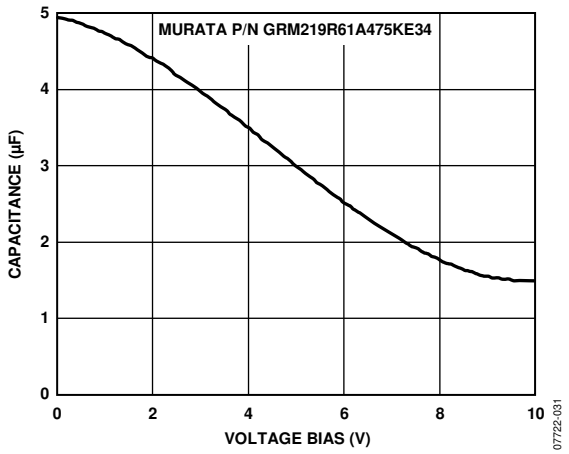


Figure 35. Capacitance vs. Voltage Bias Characteristics

Equation 3 can be used to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (3)$$

where:

C_{EFF} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} = 4.46 µF at 1.8 V, as shown in Figure 35.

Substituting these values in Equation 3 yields

$$C_{EFF} = 4.46\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.41\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP1754/ADP1755, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP1754/ADP1755 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 1.58 V. This ensures that the ADP1754/ADP1755 inputs and the output behave in a predictable manner during power-up.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1754/ADP1755 are protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP1754/ADP1755 are designed to reach current limit when the output load reaches 2 A (typical). When the output load exceeds 2 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP1754/ADP1755 reach current limit so that only 2 A is conducted into the short. If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 2 A into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 2A and 0 A that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation should be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1754/ADP1755 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper to which the GND pin and the exposed pad (EPAD) of the package are soldered on the PCB. Table 6 shows typical θ_{JA} values for the 16-lead LFCSP for various PCB copper sizes. Table 7 shows typical Ψ_{JB} values for the 16-lead LFCSP.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W), LFCSP
0[1]	130
100	80
500	69
1000	54
6400	42

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

Copper Size (mm²)	Ψ_{JB} (°C/W) at 1 W
100	32.7
500	31.5
1000	25.5

The junction temperature of the ADP1754/ADP1755 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (4)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (5)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (6)$$

As shown in Equation 6, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

Figure 36 through Figure 41 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

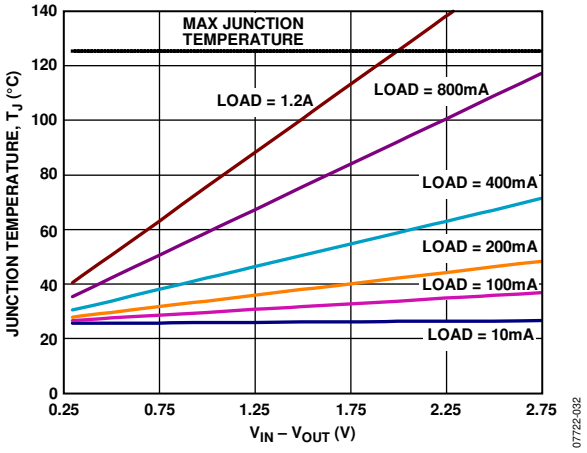


Figure 36. 6400 mm² of PCB Copper, T_A = 25°C, LFCSP

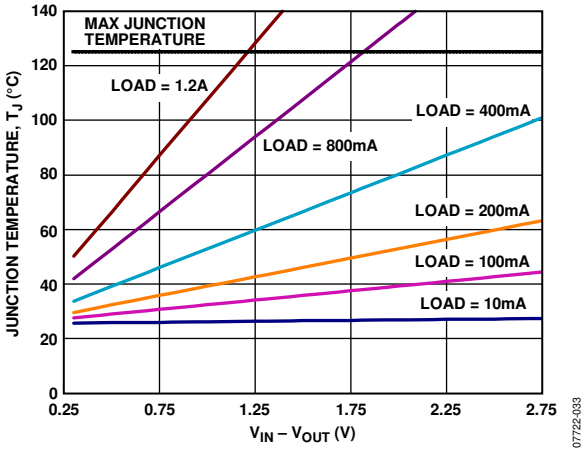


Figure 37. 500 mm² of PCB Copper, T_A = 25°C, LFCSP

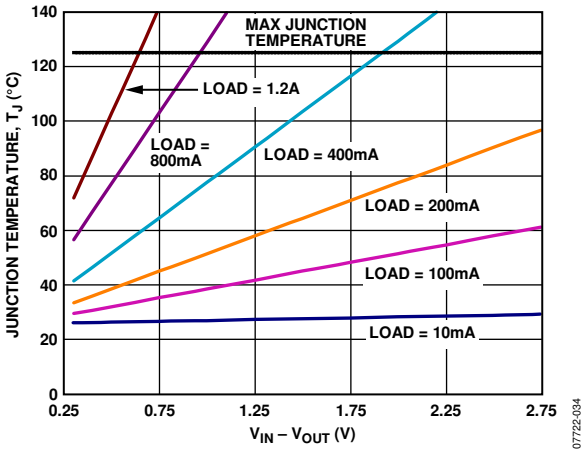


Figure 38. 0 mm² of PCB Copper, T_A = 25°C, LFCSP

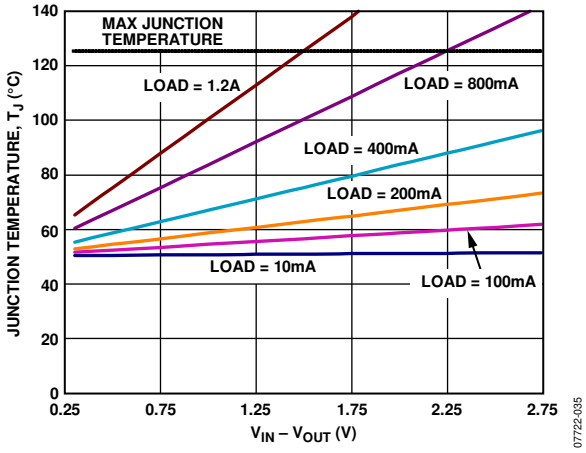


Figure 39. 6400 mm² of PCB Copper, T_A = 50°C, LFCSP

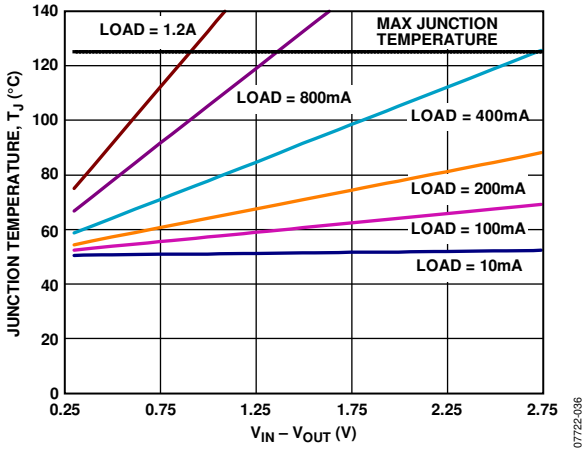


Figure 40. 500 mm² of PCB Copper, T_A = 50°C, LFCSP

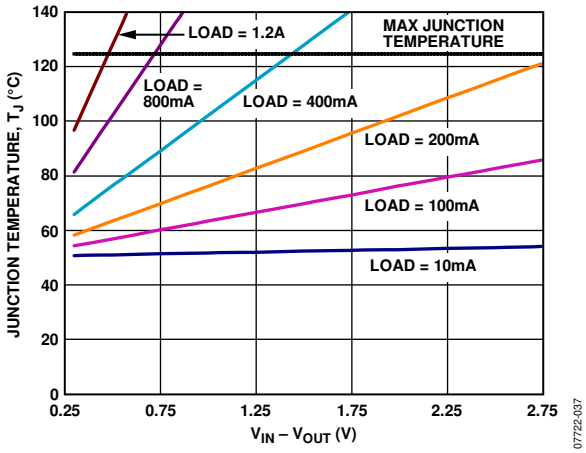


Figure 41. 0 mm² of PCB Copper, T_A = 50°C, LFCSP

In cases where the board temperature is known, the thermal characterization parameter, Ψ_{JB}, can be used to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (7)$$

Figure 42 through Figure 45 show junction temperature calculations for different board temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

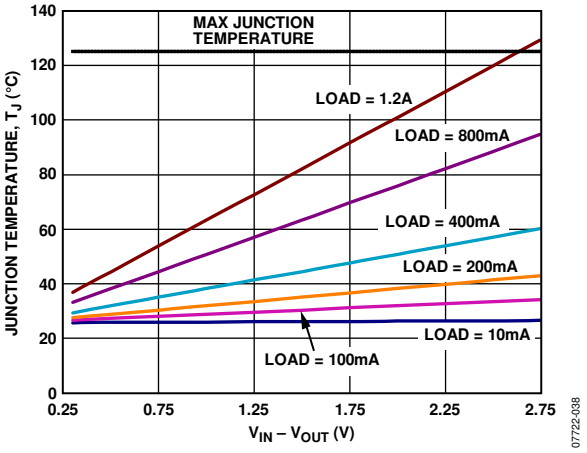


Figure 42. 500 mm² of PCB Copper, T_B = 25°C, LFCSP

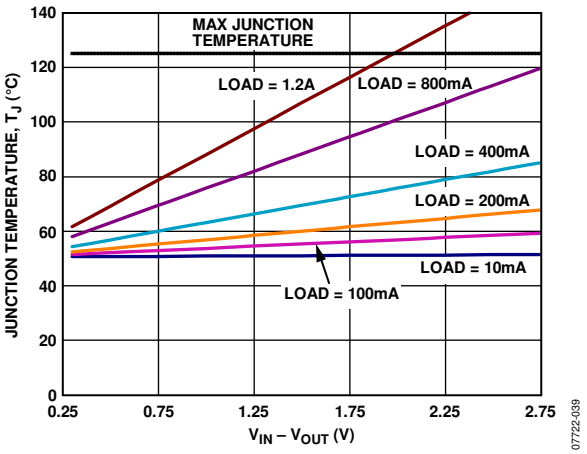


Figure 43. 500 mm² of PCB Copper, T_B = 50°C, LFCSP

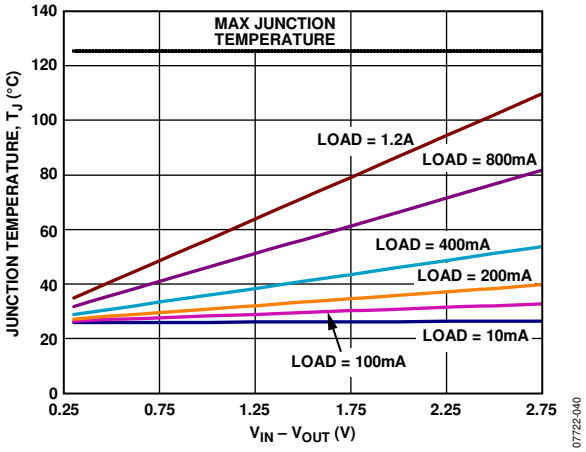


Figure 44. 1000 mm² of PCB Copper, T_B = 25°C, LFCSP

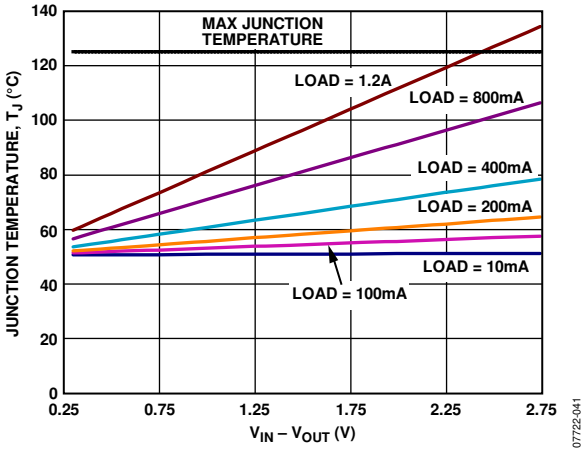


Figure 45. 1000 mm² of PCB Copper, T_B = 50°C, LFCSP

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP1754/ADP1755. However, as shown in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Here are a few general tips when designing PCBs:

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor as close as possible to the SS pin.
- Connect the load as close as possible to the VOUT and SENSE pins (ADP1754) or to the VOUT and ADJ pins (ADP1755).

Use of 0603 or 0805 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

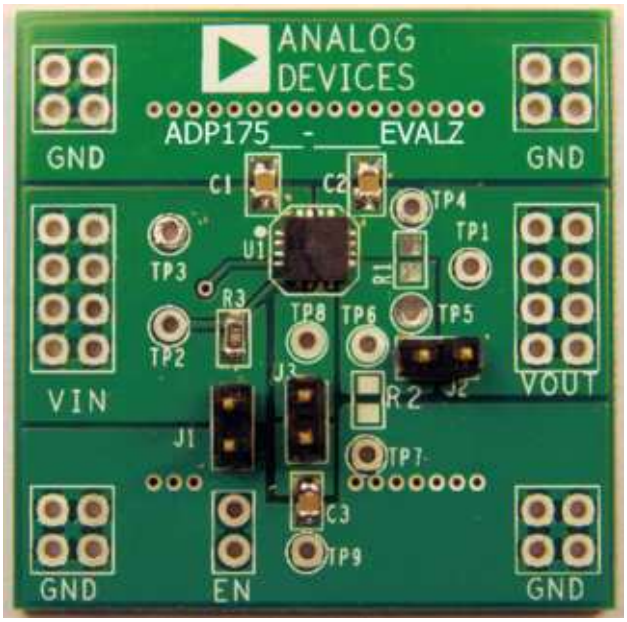


Figure 46. Evaluation Board

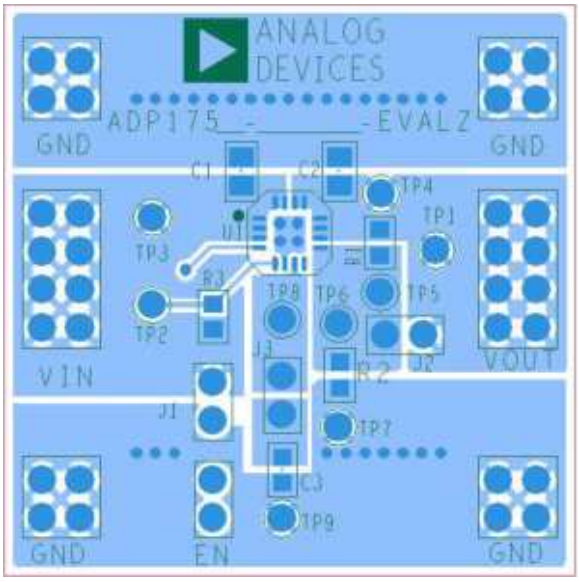


Figure 47. Typical Board Layout—Top Side

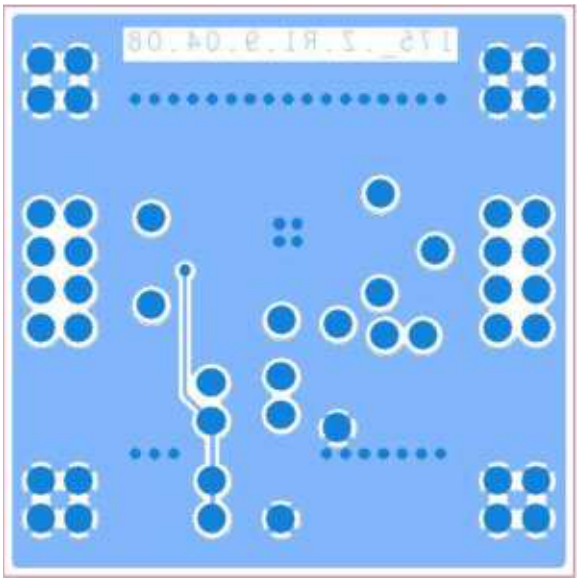


Figure 48. Typical Board Layout—Bottom Side

OUTLINE DIMENSIONS

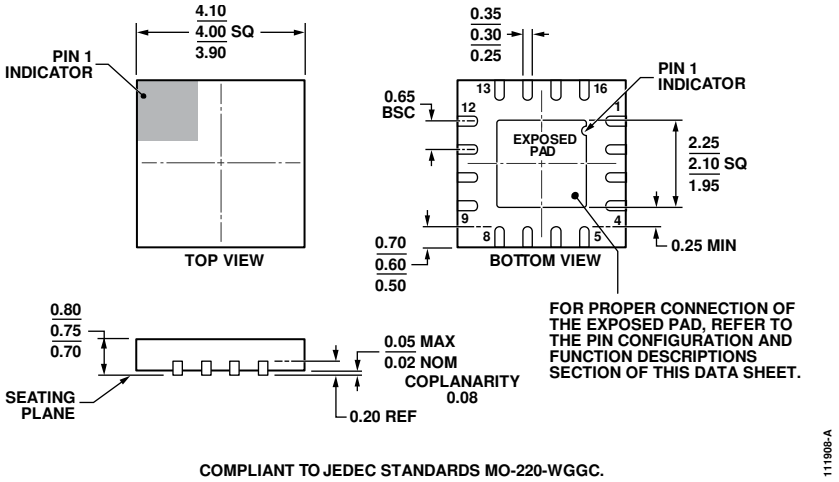


Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option
ADP1754ACPZ-0.75R7	−40°C to +125°C	0.75	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.0-R7	−40°C to +125°C	1.0	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.1-R7	−40°C to +125°C	1.1	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.2-R7	−40°C to +125°C	1.2	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.3-R7	−40°C to +125°C	1.3	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.5-R7	−40°C to +125°C	1.5	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.8-R7	−40°C to +125°C	1.8	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-2.5-R7	−40°C to +125°C	2.5	16-Lead LFCSP_WQ	CP-16-23
ADP1755ACPZ-R7	−40°C to +125°C	Adjustable from 0.75 to 3.3	16-Lead LFCSP_WQ	CP-16-23
ADP1754-1.5-EVALZ		1.5	Evaluation Board	
ADP1755-EVALZ		Adjustable	Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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