Low Profile, 500 mA, 6 MHz, Synchronous, Step-Down, DC-to-DC Converter

ADP2125

FEATURES

- 1.26 V fixed output voltage
- Clock signal enable
- 6 MHz (maximum) operating frequency
- 500 mA continuous output current
- Input voltage: 2.1 V to 5.5 V
- 0.3 µA (typical) shutdown supply current
- Compatible with tiny multilayer inductors
- Internal synchronous rectifier
- Internal compensation
- Internal soft start
- Output-to-ground short-circuit protection
- Current-limit protection
- Undervoltage lockout
- Thermal shutdown protection
- Ultrasmall, 0.405 mm height (maximum), 6-ball BUMPED_CHIP

APPLICATIONS

- Mobile phones
- Digital still/video cameras
- Digital audio
- Portable equipment
- Camera modules
- Image stabilization systems

GENERAL DESCRIPTION

The ADP2125 is a high frequency, step-down, dc-to-dc converter optimized for portable applications in which board area and battery life are critical constraints. Fixed frequency operation at 6 MHz enables the use of tiny ceramic inductors and capacitors. Additionally, the synchronous rectification improves efficiency and results in fewer external components. Over all load currents, the device uses a voltage regulating pulse-width modulation (PWM) mode that maintains a constant frequency with excellent stability and transient response. The ADP2125 is enabled by a 6 MHz to 27 MHz external clock signal applied to the EXTCLK pin. When the external clock is not switching and in a low state (EXTCLK ≤ 0.5 V), the input is disconnected from the output and draws less than 0.3 µA (typical) from the source.

The ADP2125 has an input voltage range of 2.1 V to 5.5 V, allowing the use of single Li+/Li polymer cell, three-cell alkaline, NiMH cell, and other standard power sources. The ADP2125 is internally compensated to minimize external components and can source up to 500 mA. Other key features such as cycle-by-cycle peak current limit, soft start, undervoltage lockout (UVLO), output-to-ground short-circuit protection, and thermal shutdown provide protection for internal and external circuit components.

TYPICAL APPLICATION CIRCUIT

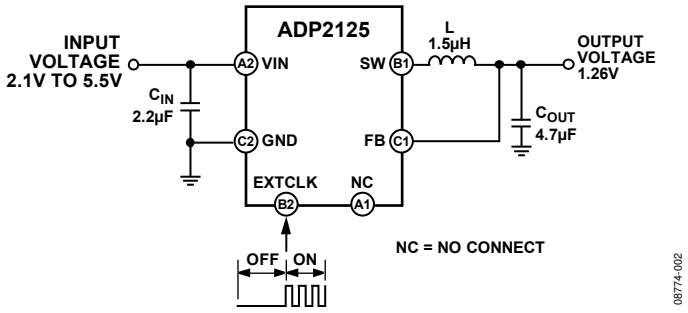


Figure 1.

Rev. A

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REVISION HISTORY

5/11—Rev. 0 to Rev. A

Changes to Ordering Guide ... 15

9/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 1.26 V, T_A = 25°C for typical specifications, and T_A = T_J = −40°C to +85°C for minimum and maximum specifications, unless otherwise noted. All specifications at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods. Typical specifications are not guaranteed.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Operating Input Voltage Range	V_{IN}		2.1		5.5	V
Quiescent Current		No load		8		mA
Shutdown Current		V_{EXTCLK} = 0 V, open-loop		0.3	1.5	µA
UNDERVOLTAGE LOCKOUT						
Rising V_{IN} Threshold				1.9	2.1	V
Falling V_{IN} Threshold			1.5	1.8		V
OUTPUT						
Continuous Output Current[1]	I_{LOAD}	V_{IN} = 2.1 V to 5.5 V	500			mA
Output Accuracy[2]	V_{OUT}	V_{IN} = 2.3 V to 4.8 V	V_{OUT} − 2%		V_{OUT} + 2%	V
FB Bias Current		V_{FB} = 1.2 V		4	9	µA
FB Pull-Down Resistance	R_{DSCHG}	V_{EXTCLK} = 0 V, I_{FB} = 10 mA		110	180	Ω
SWITCHING CHARACTERISTICS						
PMOS On Resistance				180	340	mΩ
NMOS On Resistance				250		mΩ
SW Leakage Current		V_{SW} = 0 V, V_{IN} = 5.5 V			10	µA
PMOS Switch Current Limit		Open-loop	770	1000	1291	mA
Oscillator Frequency	f_{SW}		4.83	5.52	6	MHz
SHORT-CIRCUIT PROTECTION						
Rising V_{OUT} Threshold				0.55	0.7	V
Falling V_{OUT} Threshold			0.4	0.52		V
EXTCLK INPUT						
High Threshold Voltage	$V_{EXTCLK(H)}$	V_{IN} = 2.5 V to 4.4 V	1.4			V
Low Threshold Voltage	$V_{EXTCLK(L)}$	V_{IN} = 2.5 V to 4.4 V			0.5	V
Leakage Current		V_{IN} = 5.5 V, V_{EXTCLK} = 2.1 V to 5.5 V		0.01	1	µA
Duty Cycle Operating Range	D_{EXTCLK}		40		60	%
Frequency Operating Range	f_{EXTCLK}		6		27	MHz
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				146		°C
Thermal Shutdown Hysteresis				13		°C
TIMING		See Figure 2				
VIN High to EXTCLK On[1]	t_1	V_{IN} = 2.1 V to 5.5 V	200			µs
EXTCLK On to V_{OUT} Rising	t_2	D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 6 MHz	17	23	32	µs
		D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 27 MHz	16	21	28	µs
V_{OUT} Power-Up Time (Soft Start)[1]	t_3	C_{OUT} = 4.7 µF, R_{LOAD} = 3.6 Ω		105	200	µs
EXTCLK Off to V_{OUT} Falling	t_5	D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 6 MHz to 27 MHz		4.1	11	µs
V_{OUT} Power-Down Time	t_6	C_{OUT} = 4.7 µF, R_{LOAD} = 3.6 Ω		36		µs
		C_{OUT} = 4.7 µF, no load		1070		µs
Minimum Shutdown Time[1]	$t_5 + t_6$	C_{OUT} = 4.7 µF, no load	1400			µs
Minimum Power-Off Time[1]	t_7		500			µs

[1] Guaranteed by design.
[2] Transients not included in voltage accuracy specifications.

TIMING DIAGRAM

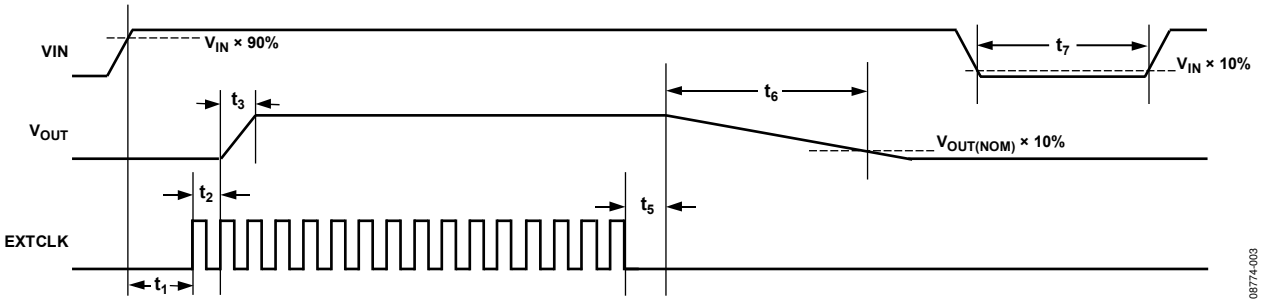


Figure 2. I/O Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +6 V
EXTCLK to GND	−0.3 V to +6 V
SW, NC to GND	−0.3 V to VIN
FB (VIN ≥ 3.6 V) to GND	−0.3 V to +3.6 V
FB (VIN < 3.6 V) to GND	−0.3 V to VIN
Operating Ambient Temperature (T_A)	−40°C to +85°C[1]
Operating Junction Temperature (T_J) at I_{LOAD} = 500 mA	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

[1] The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). See the Thermal Considerations section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL CONSIDERATIONS

The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$) because the ADP2125 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits.

In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and good PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The operating junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

See the Applications Information section for further information on calculating the operating junction temperature for a specific application.

THERMAL RESISTANCE

θ_{JA} of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions.

θ_{JA} is specified for worst-case conditions, that is, a device soldered on a circuit board for surface-mount packages. θ_{JA} is determined according to JEDEC Standard JESD51-9 on a 4-layer printed circuit board (PCB).

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Ball Bumped Bare Die, 4-Layer Board	120	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

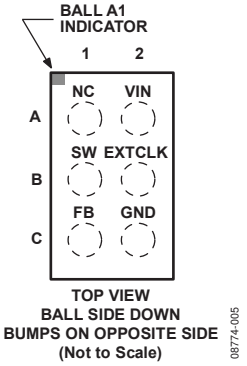


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	NC	No Connection. Any voltage applied to this pin must be between GND and VIN. Voltages above VIN or below GND exceed the absolute maximum ratings and may cause damage to the part.
B1	SW	Switch Node.
C1	FB	Feedback Divider Input. Connect the output capacitor from FB to GND to set the output voltage ripple and to complete the control loop.
A2	VIN	Power Supply Input.
B2	EXTCLK	External Clock Enable Signal. The ADP2125 powers up when a clock signal (6 MHz to 27 MHz) is detected on this pin.
C2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, f_{EXTCLK} = 10 MHz, V_{OUT} = 1.26 V, L = 1.8 µH (700 mA, 0603 package, LQM18PN1R8NC0), C_{IN} = 2.2 µF (6.3 V, 0402 package, X5R, GRM155R60J225ME15), C_{OUT} = 4.7 µF (4 V, 0402 package, X5R, GRM155R60G475ME47), and T_A = 25°C, unless otherwise noted.

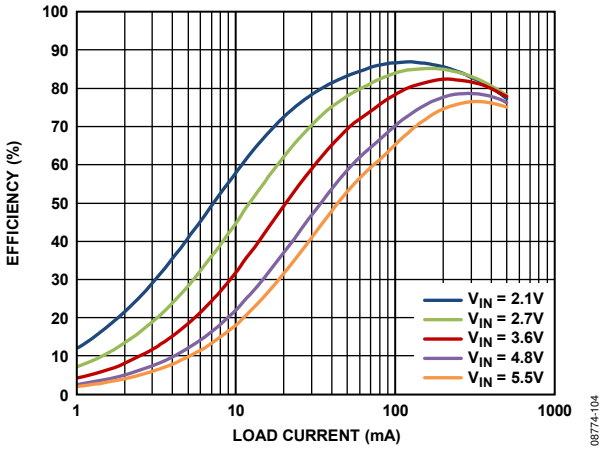


Figure 4. Efficiency vs. Load Current

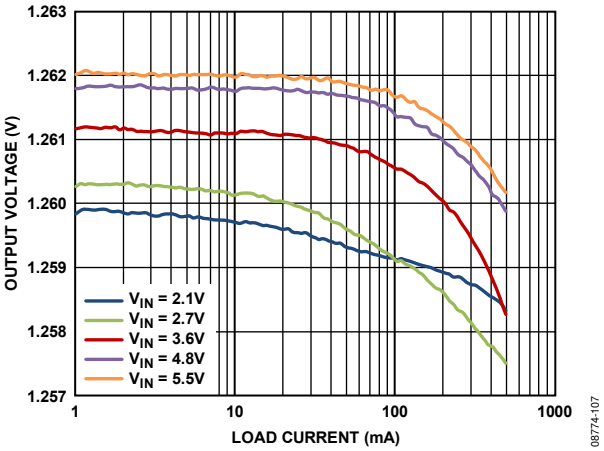


Figure 7. Output Voltage Accuracy

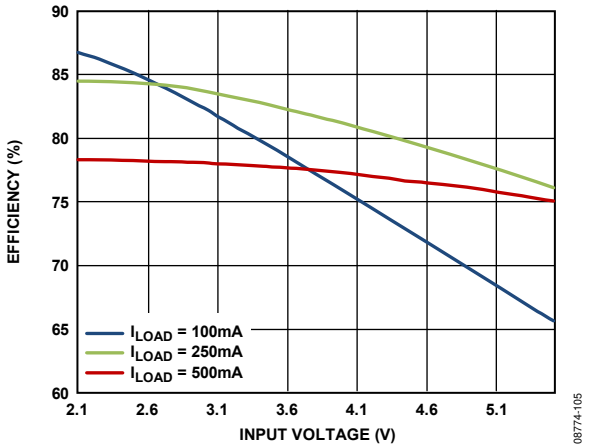


Figure 5. Efficiency vs. Input Voltage

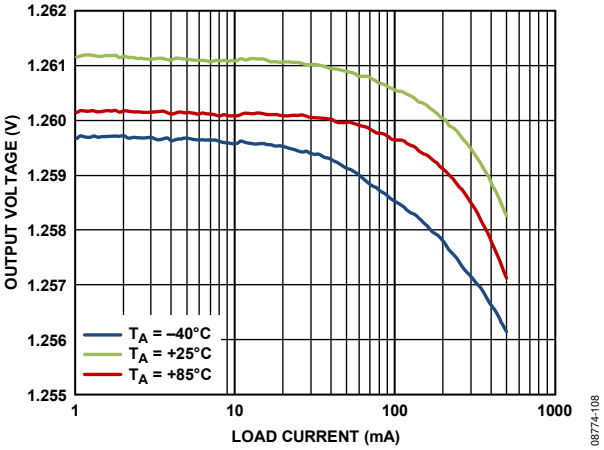


Figure 8. Output Voltage Accuracy over Temperature

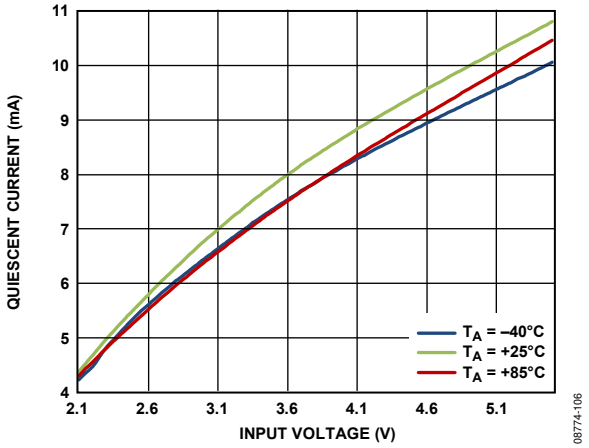


Figure 6. Quiescent Current vs. Input Voltage

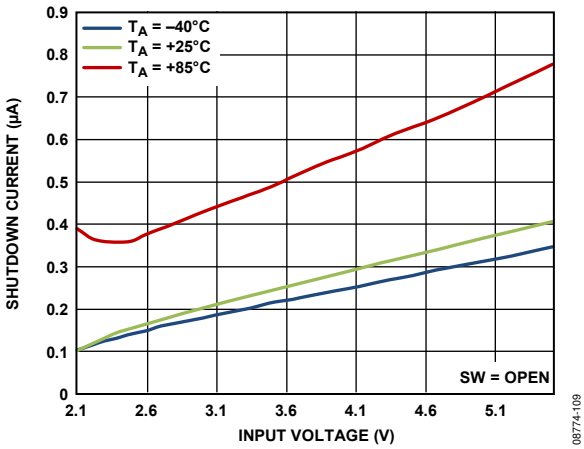


Figure 9. Shutdown Current vs. Input Voltage

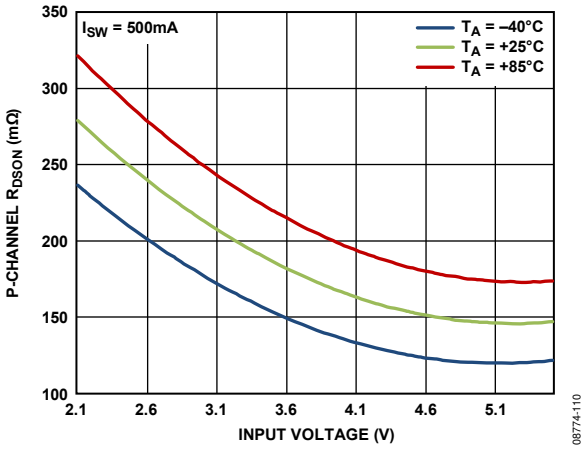


Figure 10. PMOS Drain-to-Source On Resistance

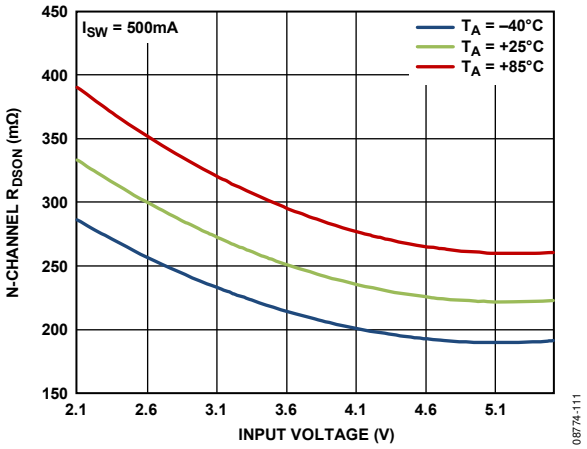


Figure 11. NMOS Drain-to-Source On Resistance

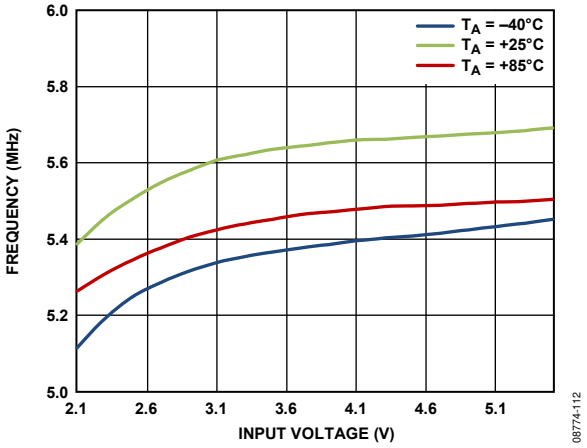


Figure 12. Switching Frequency vs. Input Voltage

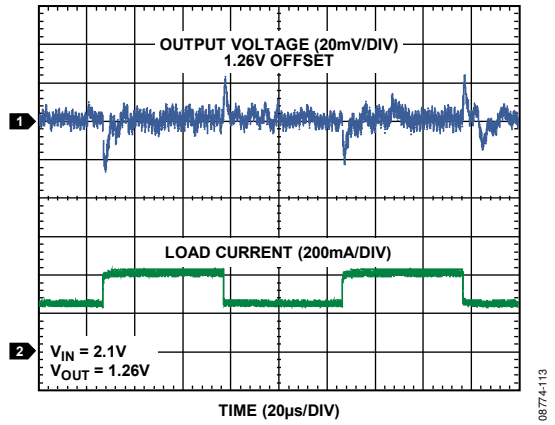


Figure 13. Load Transient Response, 250 mA to 420 mA, V_{IN} = 2.1 V

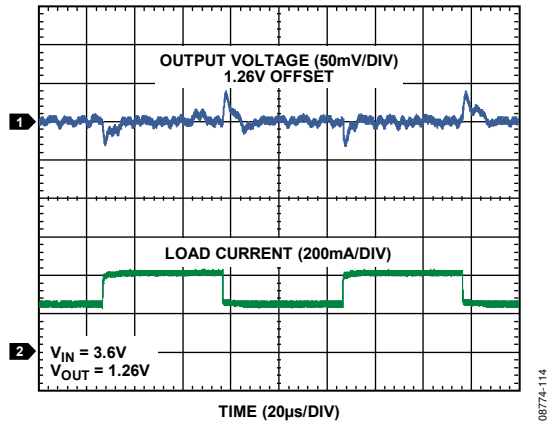


Figure 14. Load Transient Response, 250 mA to 420 mA, V_{IN} = 3.6 V

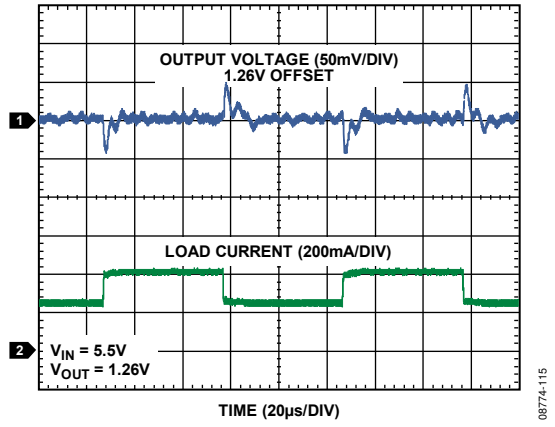


Figure 15. Load Transient Response, 250 mA to 420 mA, V_{IN} = 5.5 V

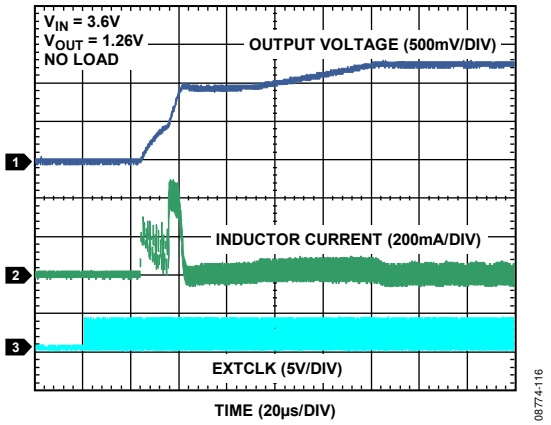


Figure 16. Startup, No Load

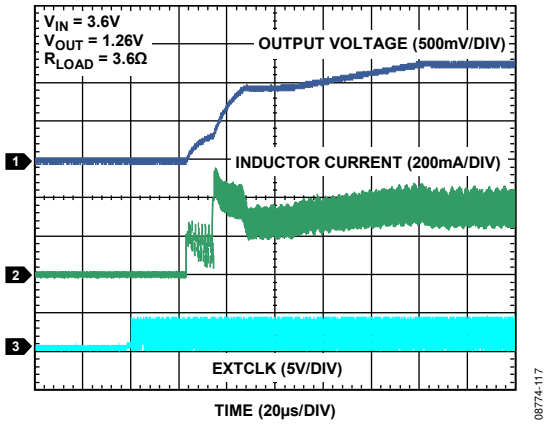


Figure 17. Startup, R_{LOAD} = 3.6 Ω

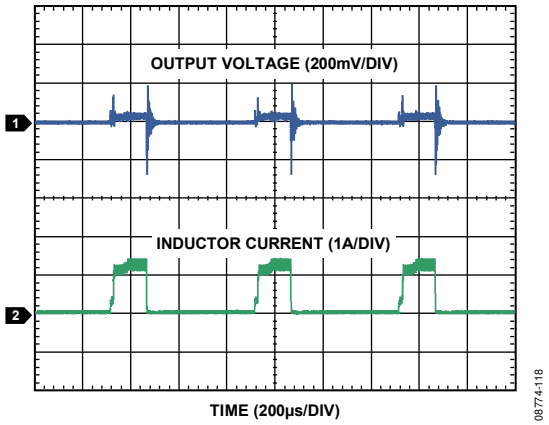


Figure 18. Output Short-Circuit Response

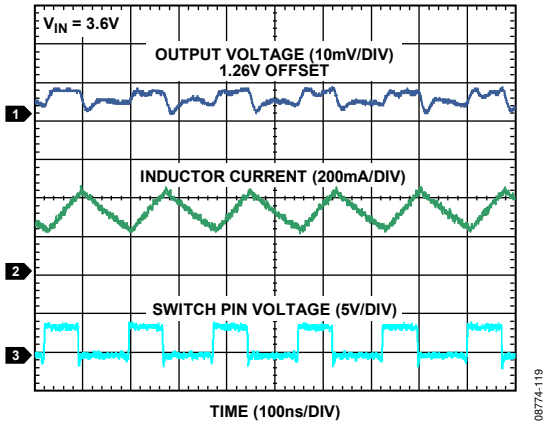


Figure 19. Standard Operation

THEORY OF OPERATION

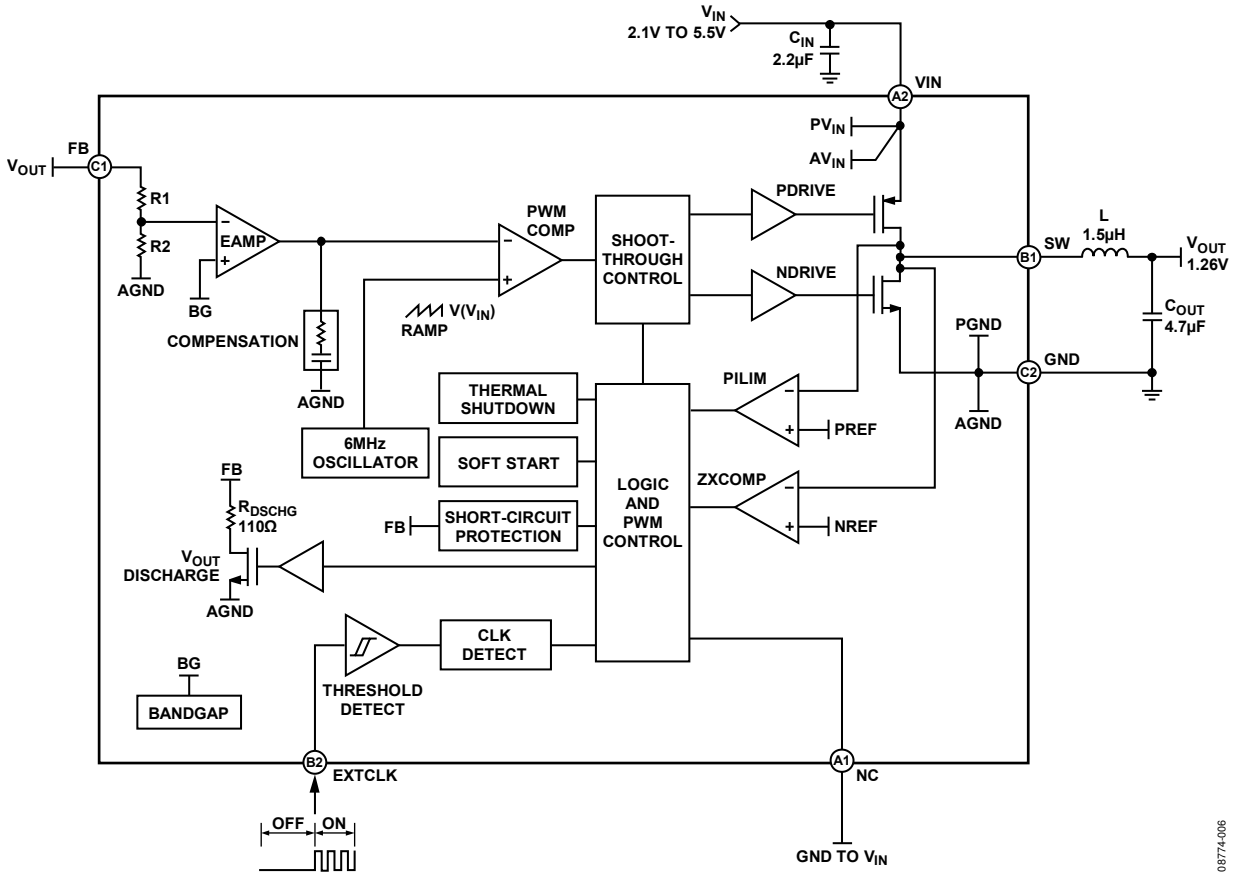


Figure 20. Internal Block Diagram

OVERVIEW

The ADP2125 is a high efficiency, synchronous, step-down, dc-to-dc converter that operates from a 2.1 V to 5.5 V input voltage. It provides up to 500 mA of continuous output current at a fixed output voltage. The 6 MHz operating frequency enables the use of tiny external components. The internal control schemes of the ADP2125 give excellent stability and transient response. Other internal features such as cycle-by-cycle peak current limiting, soft start, undervoltage lockout, output-to-ground short-circuit protection, and thermal shutdown provide protection for internal and external circuit components.

EXTERNAL CLOCK (EXTCLK) ENABLE

The ADP2125 is enabled by a 6 MHz to 27 MHz clock signal applied to the EXTCLK pin (see Figure 2 and Figure 20). The ADP2125 internally detects the clock signal and allows the converter to power up and the output voltage to rise to its nominal value.

The ADP2125 can detect a nonswitching state and disable the part whether the EXTCLK gates low or high. If the EXTCLK signal gates low, the part is shut down, reducing the current consumption to 0.3 µA (typical).

INTERNAL CONTROL FEATURES

Pulse-Width Modulation (PWM)

PWM forces the part to maintain a fixed frequency of 6 MHz (maximum) over all load conditions. The ADP2125 uses a hybrid proprietary voltage mode control scheme to control the duty cycle over load current and line voltage variation. This control provides excellent stability, transient response, and output regulation.

Synchronous Rectification

In addition to the P-channel MOSFET switch, the ADP2125 includes an N-channel MOSFET switch to build the synchronous rectifier. The synchronous rectifier improves efficiency, especially for small load currents, and reduces cost and board space by eliminating the need for an external rectifier.

Soft Start

To prevent excessive input inrush current at startup, the ADP2125 operates with an internal soft start. When EXTCLK begins to oscillate, or when the part recovers from a fault (UVLO, TSD, or SCP), a soft start timer begins. During this time, the peak current limit is gradually increased to its maximum. The output

voltage increases in stages to ensure that the converter is able to start up effectively and in proper sequence. After the soft start period expires, the peak PMOS switch current limit remains at 1 A (typical) and the part is able to operate.

PROTECTION FEATURES

Overcurrent Protection

To ensure that excessively high currents do not damage the inductor, the ADP2125 incorporates cycle-by-cycle overcurrent protection. This function is accomplished by monitoring the instantaneous peak current on the power PMOS switch. If this current exceeds the PMOS switch current limit (1 A typical), then the PMOS is immediately turned off. This minimizes the potential for damage to power components during certain faults and transient events.

Output Short-Circuit Protection (SCP)

If the output voltage is shorted to GND, a standard dc-to-dc controller delivers maximum power into that short. This may result in a potentially catastrophic failure. To prevent this, the ADP2125 senses when the output voltage is below the SCP threshold (typically 0.55 V). At this point, the controller turns off for approximately 450 µs and then automatically initiates a soft start sequence. This cycle repeats until the short is removed or the part is disabled. Figure 18 shows this operating behavior of the ADP2125 during a short-circuit fault. The SCP dramatically reduces the power delivered into the short circuit, yet still allows the converter to recover if the fault is removed.

Thermal Shutdown (TSD) Protection

The ADP2125 also includes TSD protection. If the die temperature exceeds 146°C (typical), the TSD protection activates and turns off the power devices. They remain off until the die temperature falls 13°C (typical), at which point the converter restarts.

Undervoltage Lockout (UVLO)

If the input voltage is below the UVLO threshold, the ADP2125 automatically turns off the power switches and places the part in a low power consumption mode. This prevents potentially erratic operation at low input voltages. The UVLO levels have approximately 100 mV of hysteresis to ensure glitch-free startup.

TIMING CONSTRAINTS

Shutdown Time

When the ADP2125 enters shutdown mode after the EXTCLK signal is removed, the ADP2125 must remain in shutdown for a minimum of 1400 µs, if no load is applied, before the EXTCLK signal can be reapplied. This allows all internal nodes to discharge to an off state.

Power-Off Time

When V_{IN} drops, thereby triggering UVLO, the ADP2125 has a minimum power-off time (t_7) of 500 µs that must elapse before V_{IN} can be reapplied. This allows all supplies to discharge enough power so that all internal devices are in an off state.

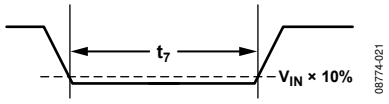


Figure 21. Power-Off Time

APPLICATIONS INFORMATION

The ADP2125 is designed to be compatible with chip inductors and multilayer ceramic capacitors that are ideal for their small footprint and low height. The recommended components for this application may change as this technology advances. Table 5, Table 6, and Table 7 list compatible inductors and capacitors.

This section describes the selection of external components. The component value ranges are limited to optimize efficiency and transient performance while maintaining stability over the full operating range.

INDUCTOR SELECTION

The high switching frequency of the ADP2125 allows for minimal output voltage ripple, even with small inductors. Inductor sizing is a trade-off between efficiency and transient response. A small value inductor leads to a larger inductor current ripple that provides excellent transient response, but degrades efficiency. A small footprint and low height chip inductor can be used for an overall smaller solution size but has a higher dc resistance (DCR) value and lower current rating that can degrade performance. Shielded ferrite core inductors are recommended for their low core losses and low electromagnetic interference (EMI). The recommended inductor for the ADP2125 is 1.5 µH.

The inductor peak-to-peak current ripple, ΔI_L, can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f_{SW}} \quad (2)$$

It is important that the inductor be capable of handling the maximum peak inductor current, I_{PK}, determined by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \Delta I_L/2 \quad (3)$$

The dc current rating of the inductor should be greater than the calculated I_{PK} to prevent core saturation.

INPUT CAPACITOR SELECTION

The input capacitor must be rated to support the maximum input operating voltage. Higher value input capacitors reduce the input voltage ripple caused by the switch currents on the VIN pin. Maximum rms input current for the application can be calculated using the following equation:

$$I_{RMS_MAX(CIN)} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (4)$$

Place the input capacitor as close as possible to the VIN pin to minimize supply noise.

In principle, different types of capacitors can be considered, but for battery-powered applications, the best choice is the multilayer ceramic capacitor, due to its small size, low equivalent series resistance (ESR), and low equivalent series inductance (ESL).

It is recommended that the VIN pin be bypassed with a 2.2 µF input capacitor. The input capacitor can be increased without any limit for better input voltage filtering. X5R or X7R dielectrics with a voltage rating of 6.3 V or higher are recommended.

Table 5. Inductor Selection

Manufacturer	Series	Inductance (µH)	DCR (mΩ) (typ)	Current Rating (mA)	Size (L × W × H) (mm)	Package
Murata	LQM18PN1R8NC0L	1.80	240	700	1.60 × 0.80 × 0.55	0603
	LQM18PN1R5NB0L	1.50	350	600	1.60 × 0.80 × 0.40	0603
Taiyo Yuden	CKP1608L1R5M	1.50	220	700	1.60 × 0.80 × 0.55	0603

Table 6. Input Capacitor Selection

Manufacturer	Part Number	Capacitance (µF)	Voltage Rating (V)	Temperature Coefficient	Size (L × W × H) (mm)	Package
Murata	GRM155R60J225ME95	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402
Taiyo Yuden	JMK105BJ225MV-F	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402
TDK	C1005X5R0J225M	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402

Table 7. Output Capacitor Selection

Manufacturer	Part Numbers	Capacitance (µF)	Voltage Rating (V)	Temperature Coefficient	Size (L × W × H) (mm)	Package
Murata	GRM155R60J475ME87	4.7	6.3	X5R	1.0 × 0.5 × 0.5	0402
	GRM155R60G475ME47	4.7	4	X5R	1.0 × 0.5 × 0.5	0402
Taiyo Yuden	AMK105BJ475MV-F	4.7	4	X5R	1.0 × 0.5 × 0.5	0402
TDK	C1005X5R0J475M	4.7	6.3	X5R	1.0 × 0.5 × 0.5	0402

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. For a given loop crossover frequency (the frequency at which the loop gain drops to 0 dB), the maximum voltage transient excursion (overshoot) is inversely proportional to the value of the output capacitor.

When choosing output capacitors, it is also important to account for the loss of capacitance due to output voltage dc bias. This may result in using a capacitor with a higher rated voltage to achieve the desired capacitance value. Additionally, if ceramic output capacitors are used, the capacitor rms ripple current rating should always meet the application requirements. The rms ripple current is calculated as follows:

$$I_{RMS(COUT)} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{L \times f_{SW} \times V_{IN(MAX)}} \quad (5)$$

At nominal load currents, the converter operates in forced PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor.

$$\Delta V_{OUT} = \Delta I_L \times (ESR + 1/(8 \times C_{OUT} \times f_{SW})) \quad (6)$$

The largest voltage ripple occurs at the highest input voltage.

The ADP2125 is designed to operate with small 4.7 µF ceramic capacitors that have low ESR and ESL. These components are therefore able to meet tight output voltage ripple specifications. X5R or X7R dielectrics with a voltage rating of 4 V or higher are recommended.

THERMAL LIMIT CALCULATIONS

The operating junction temperature (T_J) of the device is dependent on the ambient operating temperature (T_A) of the application, the power dissipation of the ADP2125 (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). The operating junction temperature (T_J) is calculated using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (7)$$

where θ_{JA} is 120°C/W, as provided in Table 3.

The ADP2125 can be damaged when the operating junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

- In applications with high P_D and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.
- In applications with moderate P_D and good PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The power dissipation (P_D) of the ADP2125 is only a portion of the power loss of the overall application. For a given application with known operating conditions, the application power loss can be calculated by combining the following equations for power loss (P_{LOSS}) and efficiency (η):

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (8)$$

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 \quad (9)$$

The resulting equation uses the output power and the efficiency to determine the P_{LOSS}.

$$P_{LOSS} = P_{OUT}\left(\frac{100}{\eta} - 1\right) \quad (10)$$

The power loss calculated using this approach is the combined loss of the ADP2125 device (P_D), the inductor (P_L), input capacitor (P_{CIN}), and the output capacitor (P_{COUT}), as shown in the following equation:

$$P_{LOSS} = P_D + P_L + P_{CIN} + P_{COUT} \quad (11)$$

The power loss for the inductor, input capacitor, and output capacitor can be calculated as follows:

$$P_L = I_{RMS}^2 \times DCR \quad (12)$$

$$P_{CIN} = \left(\frac{I_{RMS}}{2}\right)^2 \times ESR_{CIN} \quad (13)$$

$$P_{COUT} = (\Delta_{IOUT})^2 \times ESR_{COUT} \quad (14)$$

If multilayer chip capacitors with low ESR are used, the power loss in the input and output capacitors is negligible and

$$P_D + P_L >> P_{CIN} + P_{COUT} \quad (15)$$

$$P_{LOSS} \approx P_D + P_L \quad (16)$$

The final equation for calculating P_D can be used in Equation 7 to ensure that the operating junction temperature is not exceeded.

$$P_D \approx P_{LOSS} - P_L \approx P_{OUT}\left(\frac{100}{\eta} - 1\right) - P_L \quad (17)$$

PCB LAYOUT GUIDELINES

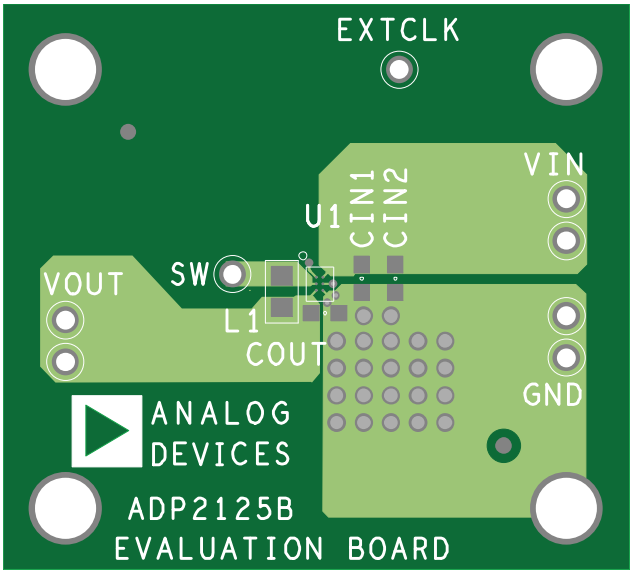


Figure 22. ADP2125 Recommended Top Layer Layout

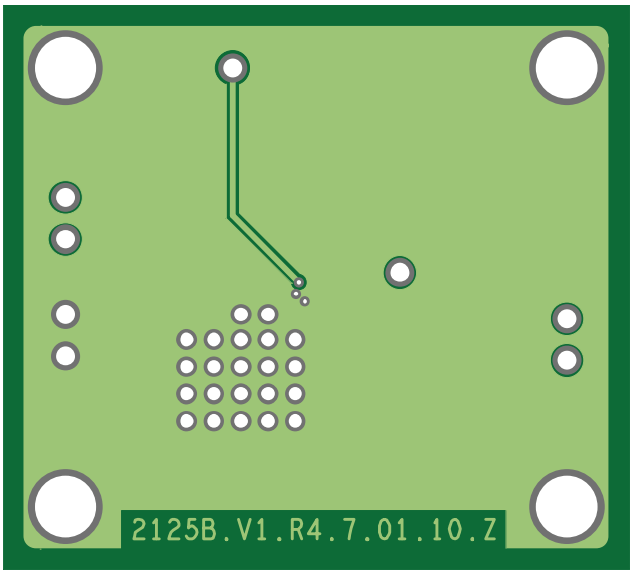


Figure 23. ADP2125 Recommended Bottom Layer Layout

For high efficiency, good regulation, and stability, a well-designed and manufactured PCB is required.

Use the following guidelines when designing PCBs:

- Keep the low ESR input capacitor, C_{IN}, close to VIN and GND.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, C_{OUT}, close to the FB and GND pins of the ADP2125. Long trace lengths from the part to the output capacitor add series inductance that may cause instability or increased ripple.

To ensure package reliability, consider the following guidelines when designing the footprint for the ADP2125. The BUMPED_CHIP device footprint must ultimately be determined according to application and customer specific reliability requirements, PCB fabrication quality, and PCB assembly capabilities.

- The Cu pad on the PCB for each solder bump should be 80% to 100% of the width of the solder bump. A smaller pad opening favors solder joint reliability (SJR) performance, whereas a larger pad opening favors drop test performance. The maximum pad size, including tolerance, should not exceed 180 µm.
- Electroplated nickel, immersion gold (ENIG) and organic solderability preservative (OSP) were used for internal reliability testing and are recommended.
- Nonsolder mask defined (NSMD) Cu pads are recommended for BUMPED_CHIP packages.
- The solder mask opening should be approximately 100 µm larger than the pad opening.
- The trace width should be less than two-thirds the size of the pad opening.
- The routing of traces from the Cu pads should be symmetrical in X and Y directions. Symmetrical routing of the traces prevents part rotation due to uneven solder wetting/surface tension forces.
- Stencil design is important for proper transfer of paste onto the Cu pads. Area ratio (AR), the relationship between the surface area of the stencil aperture and the inside surface area of the aperture walls, is critically important. Stencil thickness has the greatest impact on this ratio. AR values from 0.66 to 0.8 provide the best paste transfer efficiency and repeatability. The AR is calculated using the following equation:

$$AR = \frac{Ap}{Aw}$$

where:
Ap is the area of the aperture opening.
Aw is the wall area.

OUTLINE DIMENSIONS

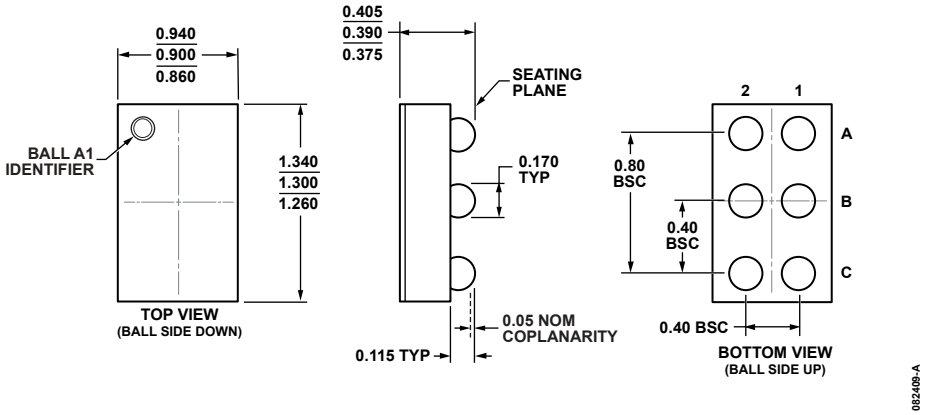


Figure 24. 6-Ball Bumped Bare Die Sales [BUMPED_CHIP]
(CD-6-2)
Dimensions shown in millimeters

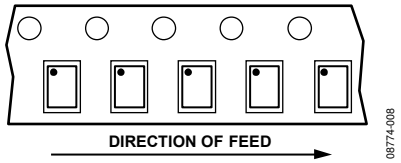


Figure 25. Tape and Reel Orientation for ADP2125

ORDERING GUIDE

Model[1]	Output Voltage	Pin A1 Function	Temperature Range	Package Description	Package Option[2]	Branding
ADP2125BCDZ-1.26R7	1.26 V	NC	−40°C to +85°C	6-Ball Bumped Bare Die [BUMPED_CHIP]	CD-6-2	LEP
ADP2125B-1.26EVALZ	1.26 V	NC		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] This package option is halide free.

NOTES

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