# 50 mA/500 mA, High Efficiency, Ultralow Power Step-Down Regulator

Data Sheet

# ADP5300

## FEATURES

- Input supply voltage range: 2.15 V to 6.50 V
- Operates down to 2.00 V voltage
- Ultralow 180 nA quiescent current
- Selectable output voltage of 0.8 V to 5.0 V
- ±1.5% output accuracy over full temperature range in PWM mode
- Selectable hysteresis mode or PWM operation mode
- Output current
  - Up to 50 mA in hysteresis mode
  - Up to 500 mA in PWM mode
- VOUTOK flag monitors the output voltage
- Ultrafast stop switching control
- 100% duty cycle operation mode
- 2.0 MHz typical switching frequency in PWM mode with optional SYNC clock range from 1.5 MHz to 2.5 MHz
- Quick output discharge (QOD) option
- UVLO, OCP, and TSD protection
- 10-lead, 3 mm × 3 mm LFCSP
- −40°C to +125°C operating temperature range

## APPLICATIONS

- Energy (gas and water) metering
- Portable and battery-powered equipment
- Medical applications
- Keep-alive power supplies

## TYPICAL APPLICATION CIRCUIT

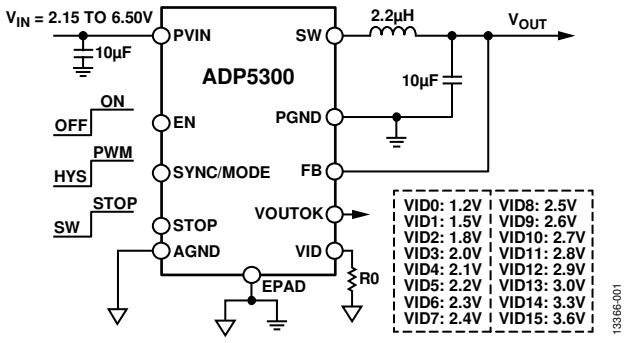



*Figure 1.*

## GENERAL DESCRIPTION

The ADP5300 is a high efficiency, ultralow quiescent current step-down regulator that draws only 180 nA quiescent current to regulate the output.

The ADP5300 runs from an input supply voltage range of 2.15 V to 6.50 V, allowing the use of multiple alkaline or NiMH, Li-Ion cells, or other power sources. The output voltage is selectable from 0.8 V to 5.0 V by an external VID resistor and factory fuse. The total solution requires only four tiny external components.

The ADP5300 can operate between hysteresis mode and pulse-width modulation (PWM) mode via the SYNC/MODE pin. The regulator in hysteresis mode achieves excellent efficiency at a power of less than 1 mW and provides up to 50 mA of output current. The regulator in PWM mode produces a lower output ripple and supplies up to 500 mA of output current. The flexible configuration capability during operation of the device enables very efficient power management to meet both the longest battery life and low system noise requirements.

The ADP5300 contains a VOUTOK flag, which monitors the output voltage and runs at a 2 MHz switching frequency in PWM mode. SYNC/MODE can be synchronized to an external clock from 1.5 MHz to 2.5 MHz.

The ADP5300 includes an STOP pin that can disable the regulator switching temporarily, in this way a quiet system environment can be achieved to benefit noise sensitive circuitry, such as data conversion, RF data transmission, and analog sensing.

Other key features in the ADP5300 include separate enabling, QOD, and safety features such as overcurrent protection (OCP), thermal shutdown (TSD), and input undervoltage lockout (UVLO).

The ADP5300 is available in a 10-lead, 3 mm × 3 mm LFCSP rated for a −40°C to +125°C operating temperature range.

Multifunction pin names may be referenced by their relevant function only.

Rev. B
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## REVISION HISTORY

**11/2017—Rev A. to Rev. B**

Change to Figure 44 ... 19
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 21

**6/2016—Rev. 0 to Rev. A**

Changes to Features Section and General Description Section ... 1
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**8/2015—Revision 0: Initial Version**

# DETAILED FUNCTIONAL BLOCK DIAGRAM

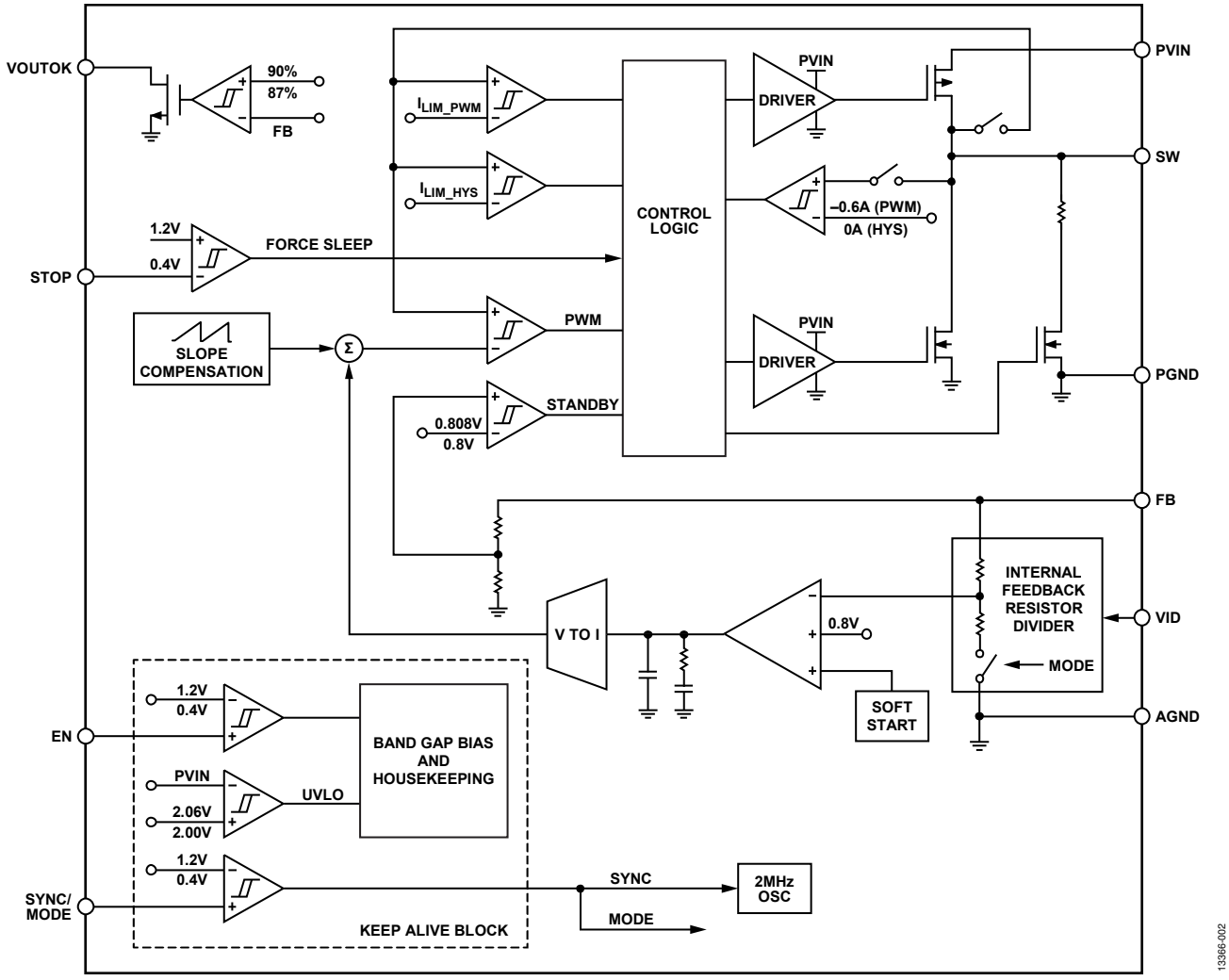



*Figure 2.*

# SPECIFICATIONS

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.5 V, $T_J$ = −40°C to +125°C for minimum and maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| INPUT SUPPLY VOLTAGE RANGE | $V_{IN}$ | 2.15 | | 6.50 | V | |
| SHUTDOWN CURRENT | $I_{SHUTDOWN}$ | | 18 | 40 | nA | $V_{EN}$ = 0 V, −40°C ≤ $T_J$ ≤ +85°C |
| | | | 18 | 130 | nA | $V_{EN}$ = 0 V, −40°C ≤ $T_J$ ≤ +125°C |
| QUIESCENT CURRENT | | | | | | |
| Operating Quiescent Current in Hysteresis Mode | $I_{Q_HYS}$ | | 180 | 260 | nA | −40°C ≤ $T_J$ ≤ +85°C |
| | | | 180 | 350 | nA | −40°C ≤ $T_J$ ≤ +125°C |
| | | | 570 | 1400 | nA | 100% duty cycle operation, $V_{IN}$ = 3.0 V, $V_{OUT}$ set to 3.3 V |
| Operating Quiescent Current in Hysteresis Mode | $I_{Q\text{-}HYS2}$ | | 2.3 | 3.2 | µA | $V_{IN}$ = 3.6 V, $V_{STOP}$ = 3.6 V |
| Operating Quiescent Current in PWM Mode | $I_{Q_PWM}$ | | 425 | 630 | µA | |
| UNDERVOLTAGE LOCKOUT | UVLO | | | | | |
| UVLO Threshold | | | | | | |
| Rising | $V_{UVLO_RISING}$ | | 2.06 | 2.14 | V | |
| Falling | $V_{UVLO_FALLING}$ | 1.90 | 2.00 | | V | |
| OSCILLATOR CIRCUIT | | | | | | |
| Switching Frequency in PWM Mode | $f_{SW}$ | 1.7 | 2.0 | 2.3 | MHz | |
| Feedback (FB) Threshold of Frequency Fold | $V_{OSC_FOLD}$ | | 0.3 | | V | |
| SYNCHRONIZATION THRESHOLD | | | | | | |
| SYNC Clock Range | $SYNC_{CLOCK}$ | 1.5 | | 2.5 | MHz | |
| SYNC High Level Threshold | $SYNC_{HIGH}$ | 1.2 | | | V | |
| SYNC Low Level Threshold | $SYNC_{LOW}$ | | | 0.4 | V | |
| SYNC Duty Cycle Range | $SYNC_{DUTY}$ | 100 | | $1/f_{SW}$ − 150 | ns | |
| SYNC/MODE Leakage Current | $I_{SYNC_LEAKAGE}$ | | 50 | 150 | nA | $V_{SYNC/MODE}$ = 3.6 V |
| MODE TRANSITION | | | | | | |
| Transition Delay from Hysteresis Mode to PWM Mode | $t_{HYS_TO_PWM}$ | | 20 | | Clock cycles | SYNC/MODE goes logic high from logic low |
| EN PIN | | | | | | |
| Input Voltage Threshold | | | | | | |
| High | $V_{IH}$ | 1.2 | | | V | |
| Low | $V_{IL}$ | | | 0.4 | V | |
| Input Leakage Current | $I_{EN_LEAKAGE}$ | | | 25 | nA | |
| STOP Switching | | | | | | |
| PWM Switching Stop Delay | $t_{STOP\text{-}RISE\text{-}DELAY}$ | | 10 | | ns | STOP goes logic high from low |
| PWM Switching Resume Delay | $t_{STOP\text{-}FALL\text{-}DELAY}$ | | 20 | | ns | STOP goes logic low from high |
| FB PIN | | | | | | |
| Output Options by VID Resistor | $V_{OUT_OPT}$ | 0.8 | | 5.0 | V | 0.8 V to 5.0 V in various factory options |
| PWM Mode | | | | | | |
| Fixed VID Code Voltage Accuracy | $V_{FB_PWM_FIX}$ | −0.6 | | +0.6 | % | $T_J$ = 25°C, output voltage setting via factory fuse |
| | | −1.2 | | +1.2 | % | −40°C ≤ $T_J$ ≤ +125°C |
| Adjustable VID Code Voltage Accuracy | $V_{FB_PWM_ADJ}$ | −1.5 | | +1.5 | % | Output voltage setting via VID resistor |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Hysteresis Mode | | | | | | |
| Fixed VID Code Threshold Accuracy from Active Mode to Standby Mode | $V_{FB_HYS_FIX}$ | −0.75 | | +0.75 | % | $T_J$ = 25°C |
| | | −2.5 | | +2.5 | % | −40°C ≤ $T_J$ ≤ +125°C |
| Adjustable VID Code Threshold Accuracy from Active Mode to Standby Mode | $V_{FB_HYS_ADJ}$ | −3 | | +3 | % | −40°C ≤ $T_J$ ≤ +125°C |
| Hysteresis of Threshold Accuracy from Active Mode to Standby Mode | $V_{FB_HYS\ (HYS)}$ | | 1 | | % | |
| Feedback Bias Current | $I_{FB}$ | | 66 | 95 | nA | Output Option 0, $V_{OUT}$ = 2.5 V |
| | | | 25 | 45 | nA | Output Option 1, $V_{OUT}$ = 1.3 V |
| SW PIN | | | | | | |
| High-Side Power FET On Resistance | $R_{DS\ (ON)\ H}$ | | 386 | 520 | mΩ | Pin to pin measurement |
| Low-Side Power FET On Resistance | $R_{DS\ (ON)\ L}$ | | 299 | 470 | mΩ | Pin to pin measurement |
| Current Limit in PWM Mode | $I_{LIM_PWM}$ | 800 | 1000 | 1200 | mA | SYNC/MODE = high |
| Peak Current in Hysteresis Mode | $I_{LIM_HYS}$ | | 265 | | mA | SYNC/MODE = low |
| Minimum On Time | $t_{MIN_ON}$ | | 40 | 70 | ns | |
| VOUTOK PIN | | | | | | |
| Monitor Threshold | $V_{OUTOK\ (RISE)}$ | 87 | 90 | 93 | % | |
| Monitor Hysteresis | $V_{OUTOK\ (HYS)}$ | | 3 | | % | |
| Monitor Rising Delay | $t_{VOUTOK_RISE}$ | | 40 | | µs | |
| Monitor Falling Delay | $t_{VOUTOK_FALL}$ | | 10 | | µs | |
| Leakage Current | $I_{VOUTOK_LEAKAGE}$ | | 0.1 | 1 | µA | |
| Output Low Voltage | $V_{OUTOK_LOW}$ | | 50 | 80 | mV | $I_{VOUTOK}$ = 100 µA |
| SOFT START | | | | | | |
| Default Soft Start Time | $t_{SS}$ | | 350 | | µs | Factory trim, 1 bit (350 µs and 2800 µs) |
| Start-Up Delay | $t_{START_DELAY}$ | | 2 | | ms | Delay from the EN pin being pulled high |
| $C_{OUT}$ DISCHARGE SWITCH ON RESISTANCE | $R_{DIS}$ | | 290 | | Ω | |
| THERMAL SHUTDOWN | | | | | | |
| Threshold | $T_{SHDN}$ | | 142 | | °C | |
| Hysteresis | $T_{HYS}$ | | 127 | | °C | |

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| PVIN to PGND | −0.3 V to +7 V |
| SW to PGND | −0.3 V to PVIN + 0.3 V |
| FB to AGND | −0.3 V to +7 V |
| VID to AGND | −0.3 V to +7 V |
| EN to AGND | −0.3 V to +7 V |
| VOUTOK to AGND | −0.3 V to +7 V |
| SYNC/MODE to AGND | −0.3 V to +7 V |
| STOP to AGND | −0.3 V to +7 V |
| PGND to AGND | −0.3 V to +0.3 V |
| Storage Temperate Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. $\theta_{JC}$ is the thermal resistance from the operating portion of the device to the outside surface of the package (case) closest to the device mounting area.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 10-Lead, 3 mm × 3 mm LFCSP | 57 | 0.86 | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

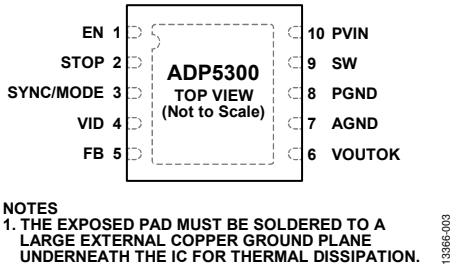



*Figure 3. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | EN | Enable Input for the Regulator. Set to logic low to disable the regulator. |
| 2 | STOP | Stop Switching Input Signal. When this pin is logic high, the regulator stops the regulator switching. When this pin is logic low, the regulator resumes the regulator switching. |
| 3 | SYNC/MODE | Synchronization Input Pin (SYNC). To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 1.5 MHz to 2.5 MHz.<br>PWM or Hysteresis Mode Selection Pin (MODE). When this pin is logic high, the regulator operates in PWM mode. When this pin is logic low, the regulator operates in hysteresis mode. |
| 4 | VID | Voltage Configuration Pin. Connect an external resistor ($R_{VID}$) from this pin to ground to configure the output voltage of the regulator (see Table 5). |
| 5 | FB | Feedback Sensing Input for the Regulator. |
| 6 | VOUTOK | Output Power-Good Signal. This open-drain output is the power-good signal for the output voltage. |
| 7 | AGND | Analog Ground. |
| 8 | PGND | Power Ground. |
| 9 | SW | Switching Node Output for the Regulator. |
| 10 | PVIN | Power Input for the Regulator. |
| | EPAD | Exposed Pad. The exposed pad must be soldered to a large external copper ground plane underneath the IC for thermal dissipation. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.5 V, L = 2.2 µH, $C_{IN}$ = $C_{OUT}$ = 10 µF, $f_{SW}$ = 2 MHz, $T_A$ = 25°C, unless otherwise noted.

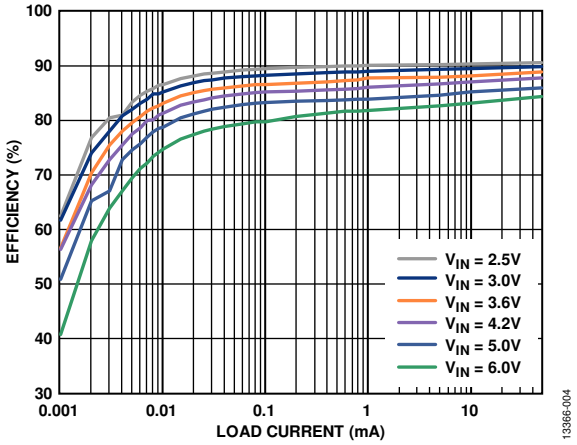



Figure 4. Hysteresis Efficiency vs. Load Current, $V_{OUT}$ = 1.2 V

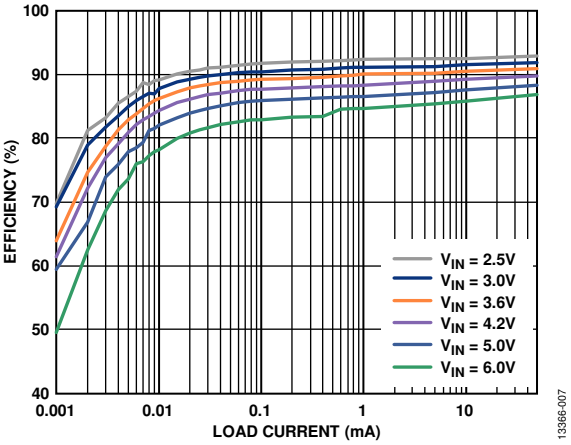



Figure 7. Hysteresis Efficiency vs. Load Current, $V_{OUT}$ = 1.5 V

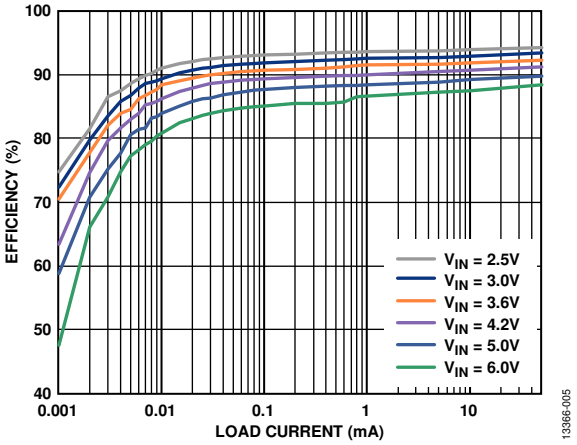



Figure 5. Hysteresis Efficiency vs. Load Current, $V_{OUT}$ = 1.8 V

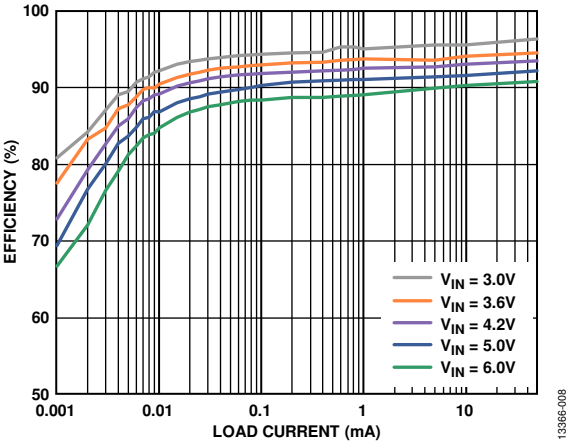



Figure 8. Hysteresis Efficiency vs. Load Current, $V_{OUT}$ = 2.5 V

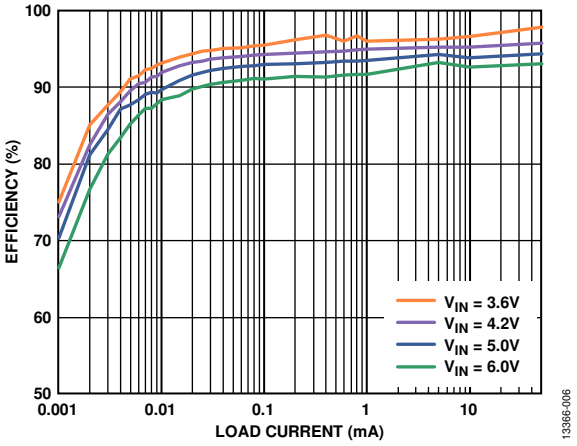



Figure 6. Hysteresis Efficiency vs. Load Current, $V_{OUT}$ = 3.3 V

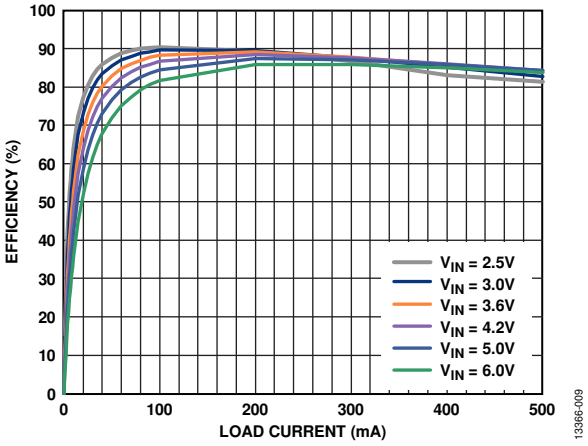



Figure 9. PWM Efficiency vs. Load Current, $V_{OUT}$ = 1.2 V

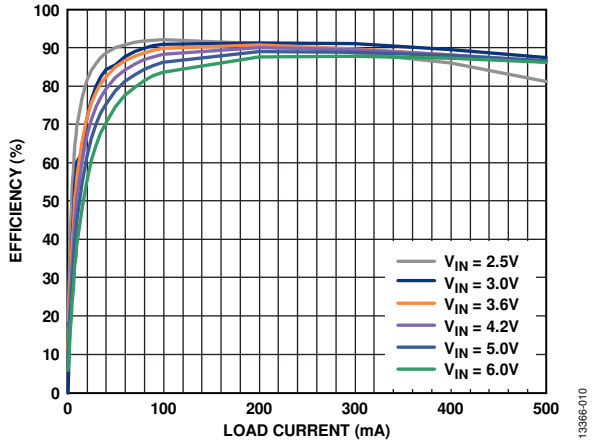



Figure 10. PWM Efficiency vs. Load Current, $V_{OUT}$ = 1.5 V

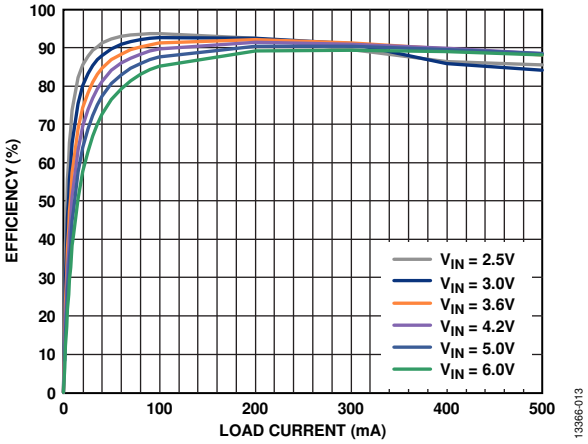



Figure 13. PWM Efficiency vs. Load Current, $V_{OUT}$ = 1.8 V

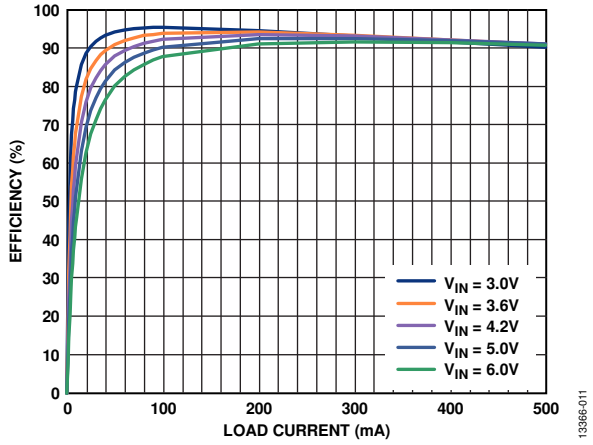



Figure 11. PWM Efficiency vs. Load Current, $V_{OUT}$ = 2.5 V

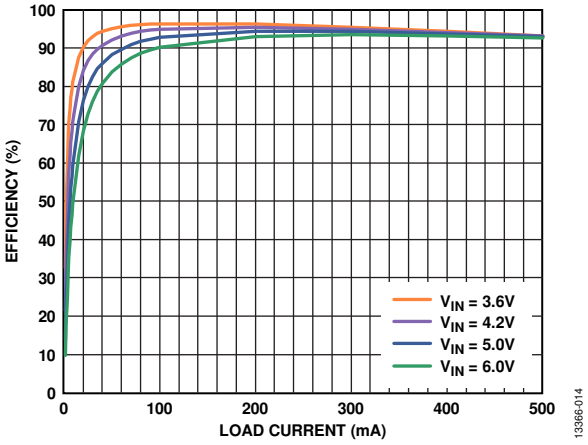



Figure 14. PWM Efficiency vs. Load Current, $V_{OUT}$ = 3.3 V

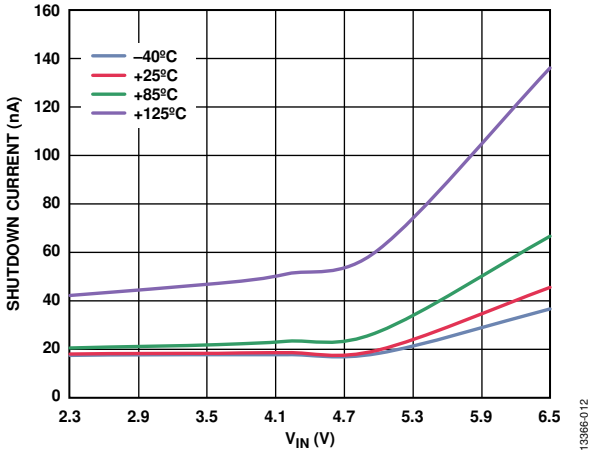



Figure 12. Shutdown Current vs. $V_{IN}$, EN = Low

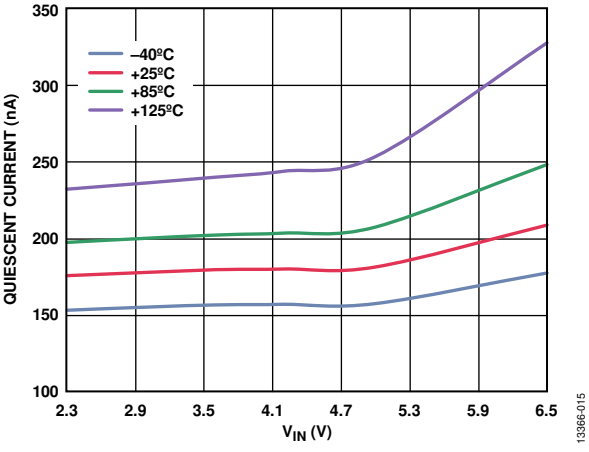



Figure 15. Hysteresis Quiescent Current vs. $V_{IN}$, SYNC/MODE = Low

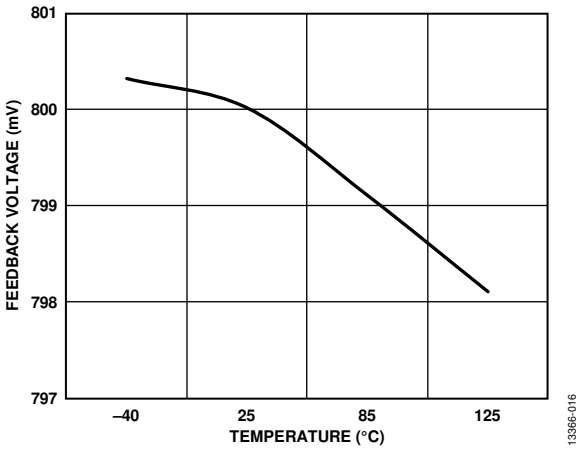



Figure 16. Feedback Voltage vs. Temperature, PWM Mode

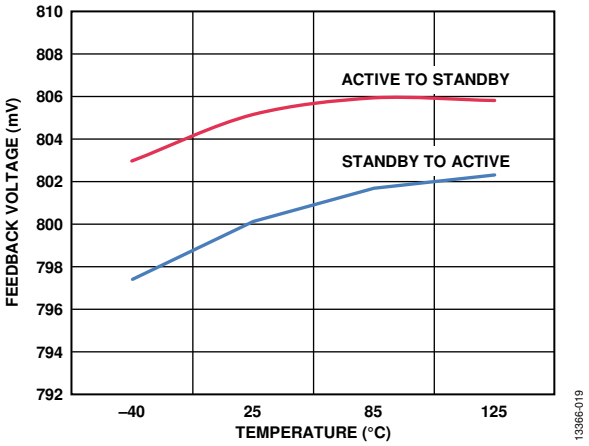



Figure 19. Feedback Voltage vs. Temperature, Hysteresis Mode

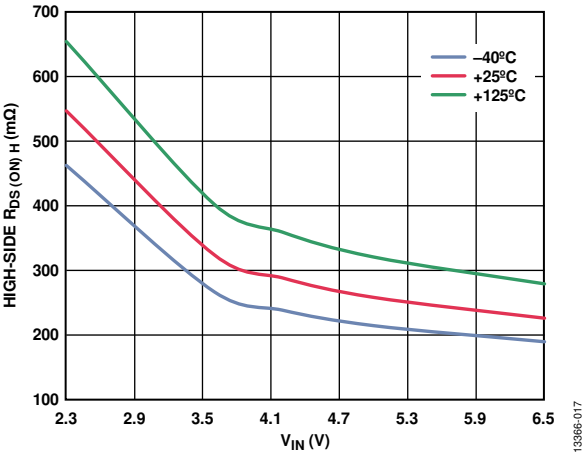



Figure 17. High-Side $R_{DS\ (ON)\ H}$ vs. $V_{IN}$

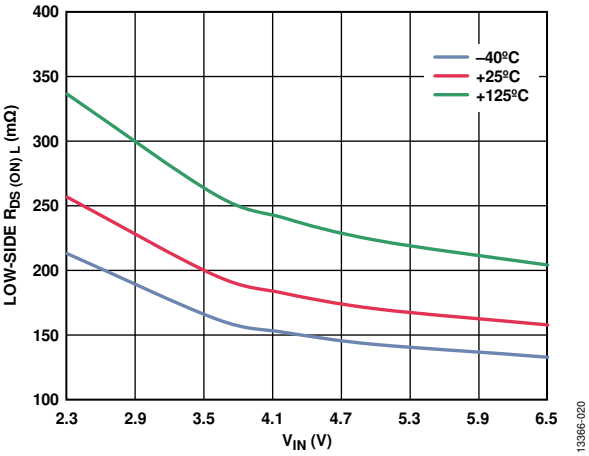



Figure 20. Low-Side $R_{DS\ (ON)\ L}$ vs. $V_{IN}$

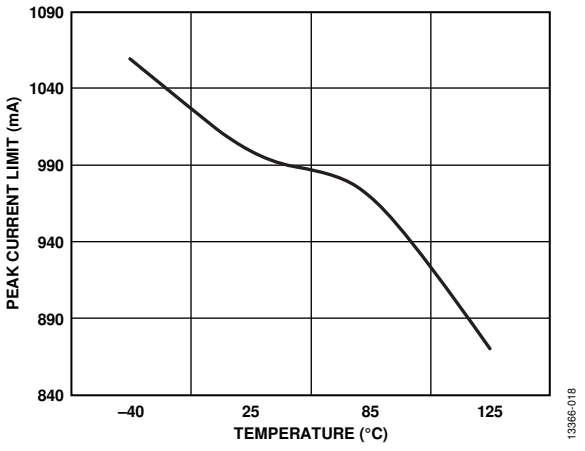



Figure 18. Peak Current Limit vs. Temperature

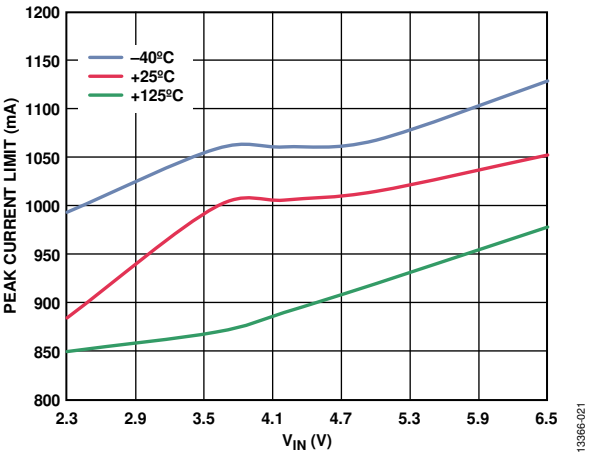



Figure 21. Peak Current Limit vs. $V_{IN}$

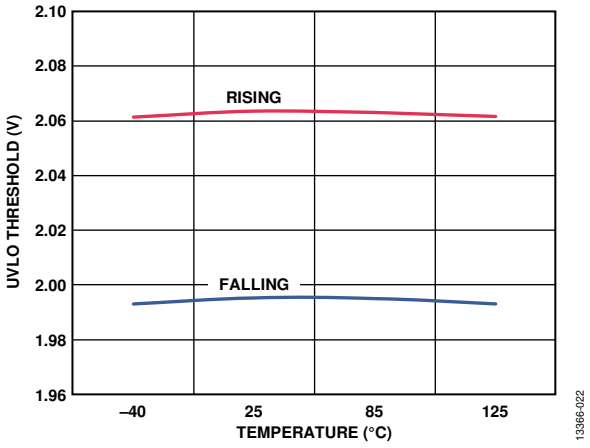



Figure 22. UVLO Threshold, Rising and Falling vs. Temperature

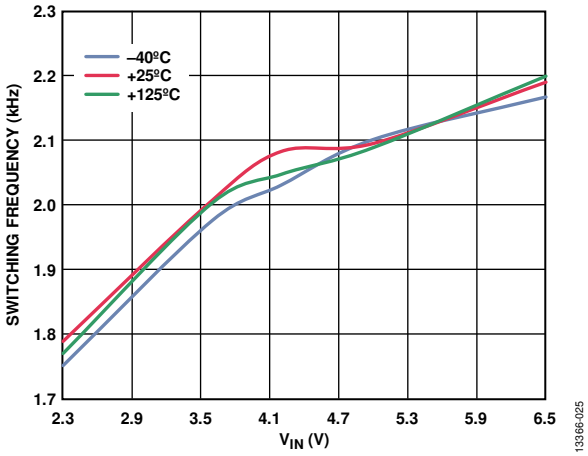



Figure 25. Switching Frequency vs. $V_{IN}$

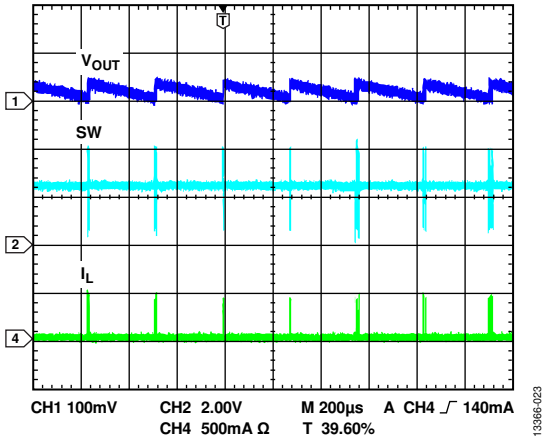



Figure 23. Steady Waveform of Hysteresis Mode, $I_{LOAD}$ = 1 mA ($I_L$ is the Inductor Current)

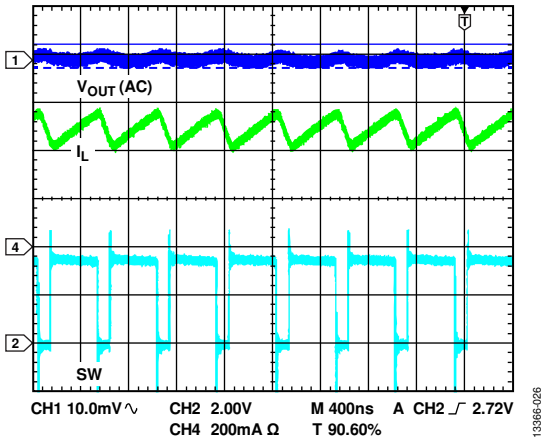



Figure 26. Steady Waveform of PWM Mode, $I_{LOAD}$ = 300 mA ($I_L$ is the Inductor Current)

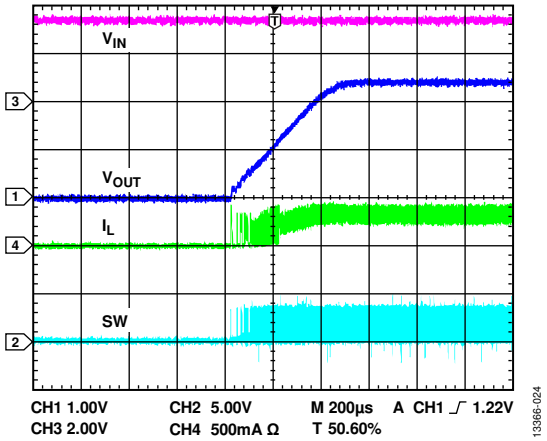



Figure 24. Soft Start, $I_{LOAD}$ = 300 mA ($I_L$ is the Inductor Current)

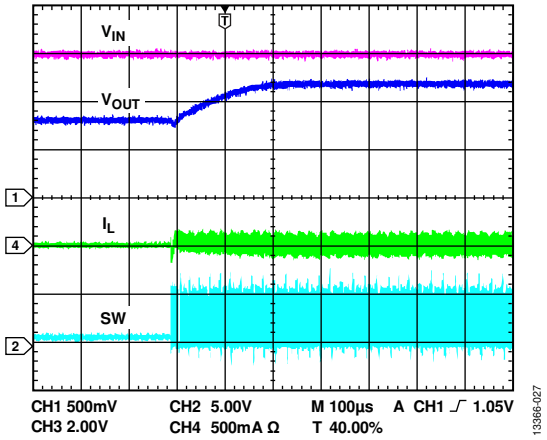



Figure 27. Soft Start with Precharge Function ($I_L$ is the Inductor Current)

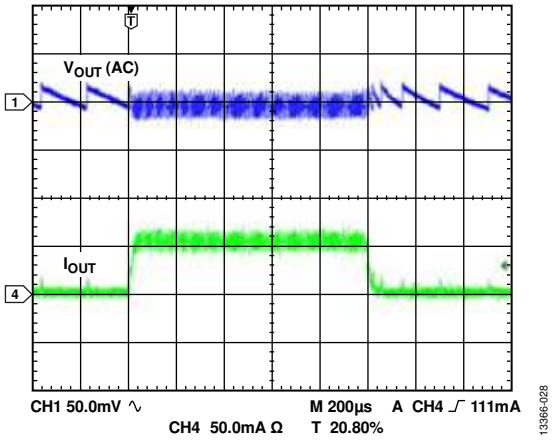



Figure 28. Load Transient of Hysteresis Mode, $I_{LOAD}$ from 0 mA to 50 mA

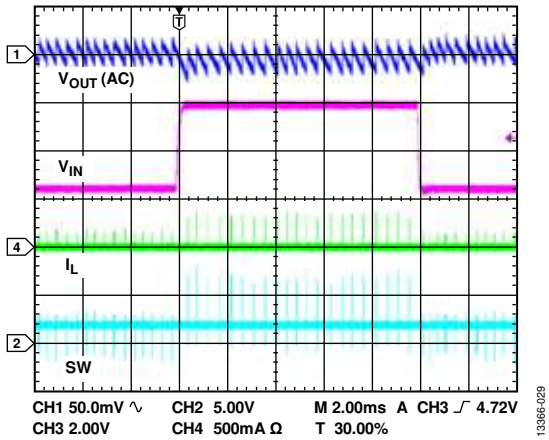



Figure 29. Line Transient of Hysteresis Mode, $I_{LOAD}$ = 10 µA ($I_L$ is the Inductor Current)

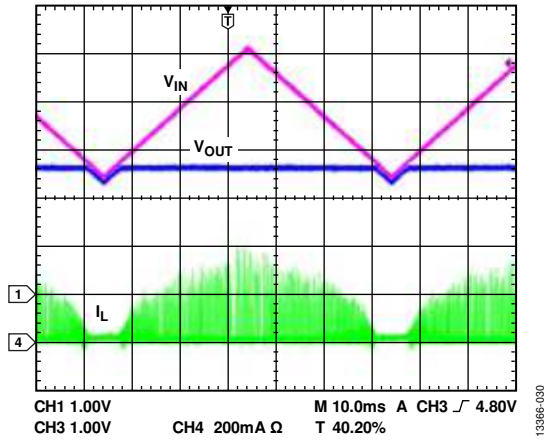



Figure 30. Input Voltage Ramp Up and Ramp Down in Hysteresis Mode ($I_L$ is the Inductor Current)

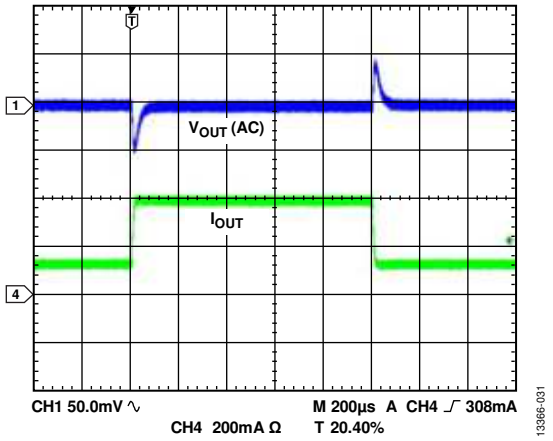



Figure 31. Load Transient of PWM Mode, $I_{LOAD}$ from 125 mA to 375 mA

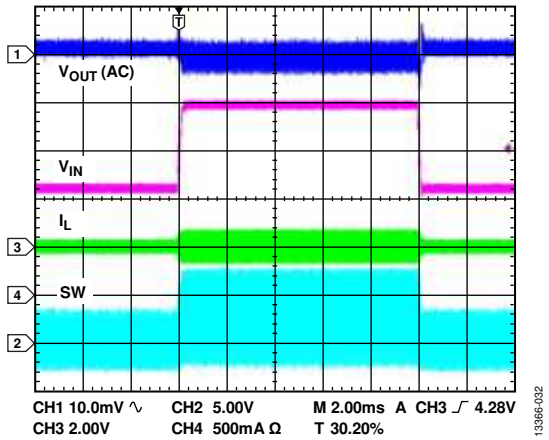



Figure 32. Line Transient of PWM Mode, $I_{LOAD}$ = 500 mA ($I_L$ is the Inductor Current)

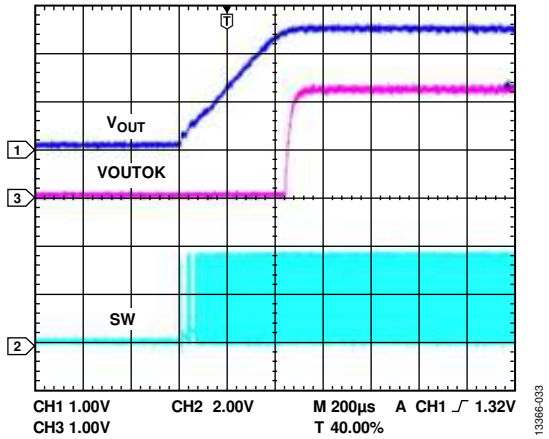



Figure 33. VOUTOK Function

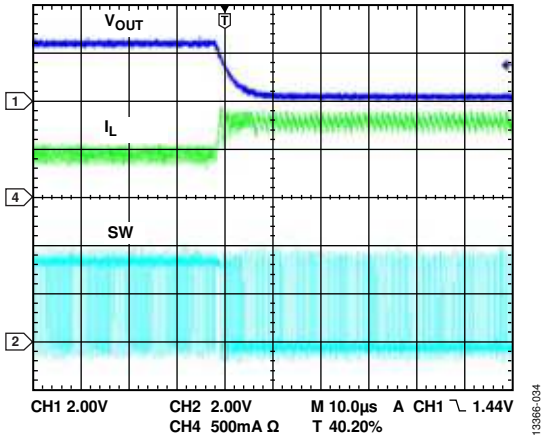



Figure 34. Output Short Protection
($I_L$ is the Inductor Current)

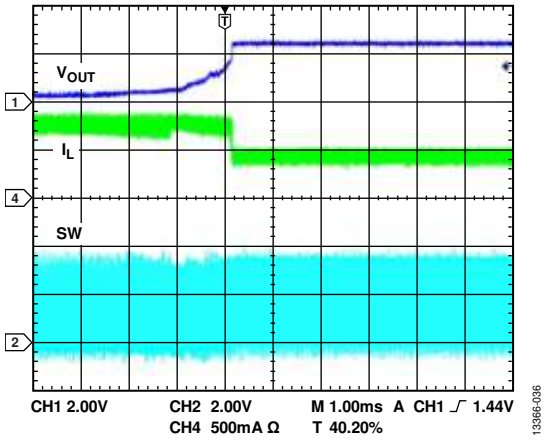



Figure 37. Output Short Recovery
($I_L$ is the Inductor Current)

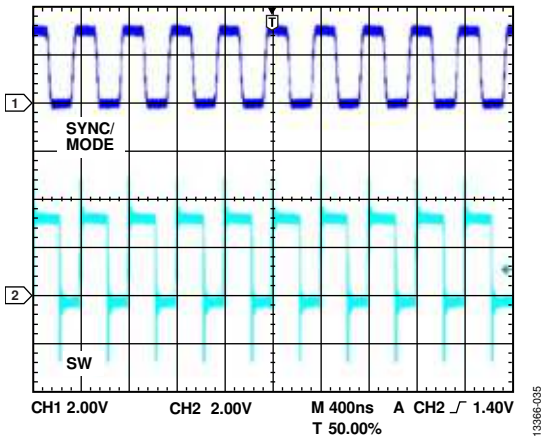



Figure 35. Synchronized to 2.5 MHz

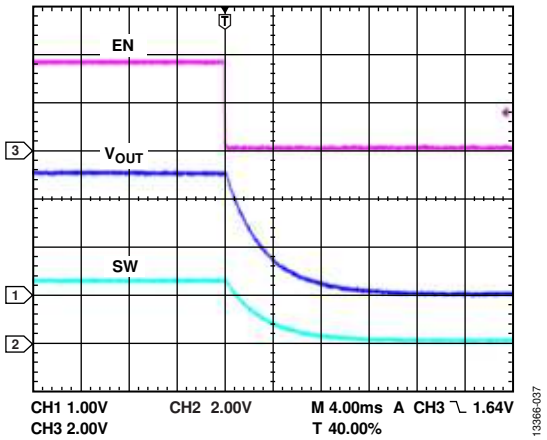



Figure 38. Quick Output Discharge Function

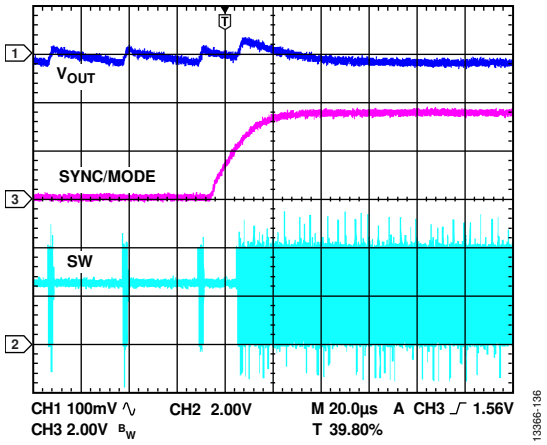



Figure 36. Hysteresis Mode to PWM Mode with 10 mA Load Current

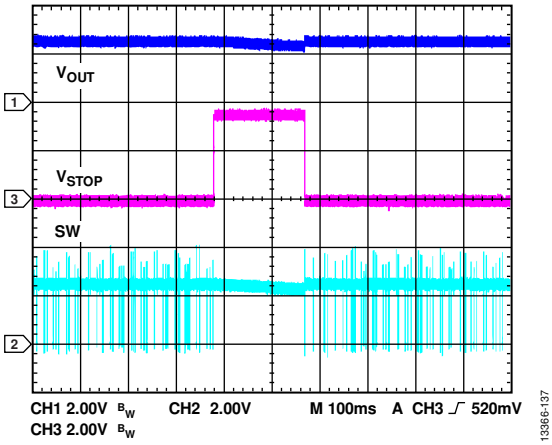



Figure 39. STOP Switching Function

# THEORY OF OPERATION

The ADP5300 is a high efficient, ultralow quiescent current, step-down regulator in a 10-lead LFCSP package to meet demanding performance and board space requirements. The device enables direct connection to a wide input voltage range of 2.15 V to 6.50 V, allowing the use of multiple alkaline/NiMH or, Li-Ion cells and other power sources.

## BUCK REGULATOR OPERATIONAL MODES

### *PWM Mode*

In PWM mode, the buck regulator in the ADP5300 operates at a fixed frequency that is set by an internal oscillator. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak inductor current threshold, which turns off the high-side MOSFET switch. This threshold is set by the error amplifier output. During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle.

### *Hysteresis Mode*

In hysteresis mode, the buck regulator in the ADP5300 charges the output voltage slightly higher than its nominal output voltage with PWM pulses by regulating the constant peak inductor current. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters standby mode. In standby mode, the high-side and low-side MOSFETs and a majority of the circuitry are disabled to allow a low quiescent current as well as high efficiency performance.

During standby mode, the output capacitor supplies energy into the load, and the output voltage decreases until it falls below the hysteresis comparator lower threshold. The buck regulator wakes up and generates the PWM pulses to charge the output again.

Because the output voltage occasionally enters standby mode and then recovers, the output voltage ripple in hysteresis mode is larger than the ripple in PWM mode.

### *Mode Selection*

The ADP5300 includes the SYNC/MODE pin to allow flexible configuration in hysteresis mode or PWM mode.

When a logic high level is applied to the SYNC/MODE pin, the buck regulator is forced to operate in PWM mode. In PWM mode, the regulator can supply up to 500 mA of output current. The regulator can provide lower output ripple and output noise in PWM mode, which is useful for noise sensitive applications.

When a logic low level is applied to the SYNC/MODE pin, the buck regulator is forced to operate in hysteresis mode. In hysteresis mode, the regulator draws only 180 nA of quiescent current typical to regulate the output under zero load, which allows the regulator to act as a keep-alive power supply in a battery-powered system. In hysteresis mode, the regulator supplies up to 50 mA of output current with a relatively large output ripple compared to PWM mode.

The user can alternate between hysteresis mode and PWM mode during operation. The flexible configuration capability during operation of the device enables efficient power management to meet high efficiency and low output ripple requirements when the system switches between active mode and standby mode.

## OSILLATOR AND SYNCHRONIZATION

The ADP5300 operates at a 2 MHz switching frequency typical in PWM operation mode.

The switching frequency of the ADP5300 can be synchronized to an external clock with a frequency range from 1.5 MHz to 2.5 MHz. The ADP5300 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock.

## ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The ADP5300 provides adjustable output voltage settings by connecting one resistor through the VID pin to AGND. The VID detection circuitry works in the start-up period, and the voltage ID code is sampled and held in the internal register and does not change until the next power recycle. Furthermore, the ADP5300 provides a fixed output voltage programmed via the factory fuse. In this condition, connect the VID pin to the PVIN pin.

For the output voltage settings, the feedback resistor divider is built into the ADP5300, and the feedback pin (FB) must be tied directly to the output. An ultralow power voltage reference and an integrated high impedance (50 MΩ typical) feedback divider network contribute to the low quiescent current. Table 5 lists the output voltage options by the VID pin configurations. A 1% accuracy resistor through VID to ground is recommended.

**Table 5. Output Voltage ($V_{OUT}$) Options by the VID Pin**

| | $V_{OUT}$ (V) | |
|---|---|---|
| **VID Configuration** | **Factory Option 0** | **Factory Option 1** |
| Short to Ground | 3.0 | 3.1 |
| Short to PVIN | 2.5 | 1.3 |
| $R_{VID}$ = 499 kΩ | 3.6 | 5.0 |
| $R_{VID}$ = 316 kΩ | 3.3 | 4.5 |
| $R_{VID}$ = 226 kΩ | 2.9 | 4.2 |
| $R_{VID}$ = 174 kΩ | 2.8 | 3.9 |
| $R_{VID}$ = 127 kΩ | 2.7 | 3.4 |
| $R_{VID}$ = 97.6 kΩ | 2.6 | 3.2 |
| $R_{VID}$ = 76.8 kΩ | 2.4 | 1.9 |
| $R_{VID}$ = 56.2 kΩ | 2.3 | 1.7 |
| $R_{VID}$ = 43 kΩ | 2.2 | 1.6 |
| $R_{VID}$ = 32.4 kΩ | 2.1 | 1.4 |
| $R_{VID}$ = 25.5 kΩ | 2.0 | 1.1 |
| $R_{VID}$ = 19.6 kΩ | 1.8 | 1.0 |
| $R_{VID}$ = 15 kΩ | 1.5 | 0.9 |
| $R_{VID}$ = 11.8 kΩ | 1.2 | 0.8 |

## UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout circuitry monitors the input voltage level on the PVIN pin. If the input voltage falls below 2.00 V (typical), the regulator turns off. After the input voltage rises above 2.06 V (typical), the soft start period initiates, and when the EN pin is high, the regulator enables.

## ENABLE/DISABLE

The ADP5300 includes a separate enable (EN) pin. A logic high on the EN pin starts the regulator. Due to the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from the EN pin being pulled high.

A logic low on the EN pin immediately disables the regulator and brings the regulator into extremely low current consumption.

## CURRENT LIMIT

The buck regulators in the ADP5300 have protection circuitry that limits the direction and the amount of current to a certain level that flows through the high-side MOSFET and the low-side MOSFET in cycle-by-cycle mode. The positive current limit on the high-side MOSFET limits the amount of current that can flow from the input to the output. The negative current limit on the low-side MOSFET prevents the inductor current from reversing direction and flowing out of the load.

## SHORT-CIRCUIT PROTECTION

The buck regulators in the ADP5300 include frequency foldback to prevent current runaway on a hard short. When the output voltage at the feedback (FB) pin falls below 0.3 V typical, indicating the possibility of a hard short at the output, the switching frequency (in PWM mode) is reduced to one-fourth of the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

## SOFT START

The ADP5300 has an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This feature prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default typical soft start time is 350 µs for the regulator.

A different soft start time (2800 µs) can be programmed for ADP5300 by the factory fuse.

## STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5300 include a precharged start-up feature to protect the low-side MOSFET from damage during startup. If the output voltage is precharged before the regulator turns on, the regulator prevents reverse inductor current, which discharges the output capacitor, until the internal soft start reference voltage exceeds the precharged voltage on the FB pin.

## 100% DUTY OPERATION

When the input voltage approaches the output voltage, the ADP5300 stops switching and enters 100% duty cycle operation. It connects the output via the inductor and the internal high-side power switch to the input. When the input voltage is charged again and the required duty cycle falls to 95% typical, the buck immediately restarts switching and regulation without allowing overshoot on the output voltage. In hysteresis mode, the ADP5300 draws an ultralow quiescent current of only 570 nA typical during 100% duty cycle operation.

## ACTIVE DISCHARGE

The regulator in the ADP5300 integrates an optional, factory programmable discharge switch from the switching node to ground. This switch turns on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is 290 Ω for the regulator.

By default, the discharge function is not enabled. The factory fuse can enable the active discharge function.

## VOUTOK FUNCTION

The ADP5300 includes an open-drain, power-good output (VOUTOK pin) that is active high when the buck regulator operates normally. By default, the VOUTOK pin monitors the output voltage. A logic high on the VOUTOK pin indicates that the regulated output voltage of the buck regulator is above 90% (typical) of its nominal output. When the regulated output voltage of the buck regulator falls below 87% (typical) of its nominal output for a delay time greater than approximately 10 µs, the VOUTOK pin goes low.

## STOP SWITCHING

The ADP5300 includes a stop input pin (STOP) that can temporarily stop the regulator switching in hysteresis mode.

When a logic high level is applied to the STOP pin, the buck regulator is forced to stop switching immediately. When a logic low level is applied to the STOP pin, the buck regulator resumes switching. Note that tens of nanoseconds delay time exists from when the STOP signal goes high to fully stop switching.

In some battery-powered systems, the microcontroller unit (MCU) can command the regulator to stop switching via the STOP signal, and the regulator then relies on the output capacitor to supply the load. In this period, a quiet system environment can be achieved which benefits the noise sensitive circuitry, such as data conversion, RF data transmission, and analog sensing. After the noise sensitive circuitry completes its task, the MCU can control the regulator and resume switching regulation mode. If needed, the VOUTOK signal can monitor the output voltage in the event it dips too low to latch up the system. Figure 40 shows the STOP switching operation status in ADP5300.

When the regulator is enabled with EN pin pulled high, the STOP signal control is valid, and when EN pin is logic low, the STOP signal is ignored.

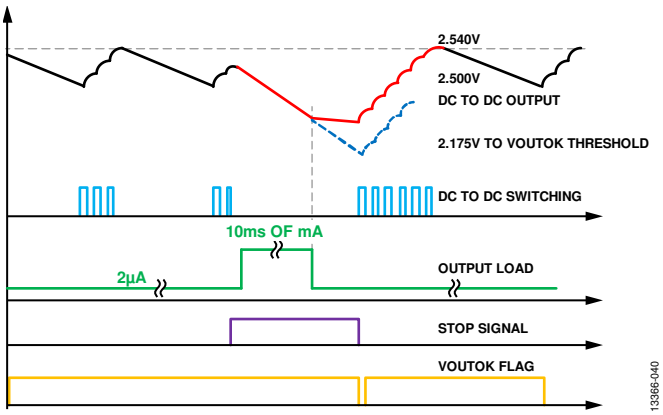



*Figure 40. STOP Switching Operation Status*

## THERMAL SHUTDOWN

If the ADP5300 junction temperature exceeds 142°C, the thermal shutdown circuit turns off the IC except for the internal linear regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5300 does not return to operation after thermal shutdown until the junction temperature falls below 127°C. When the device exits thermal shutdown, a soft start initiates for each enabled channel.

# APPLICATIONS INFORMATION

This section describes the external components selection for the ADP5300. The typical application circuit is shown in Figure 41.

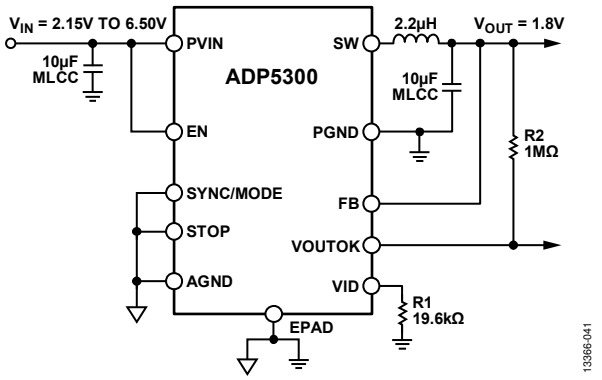



*Figure 41. Typical Application Circuit*

## EXTERNAL COMPONENT SELECTION

The ADP5300 is optimized for operation with a 2.2 µH inductor and 10 µF output capacitors for various output voltages using the closed-loop compensation and adaptive slope compensation circuits. The selection of components depends on the efficiency, the load current transient, and other application requirements. The trade-offs among performance parameters, such as efficiency and transient response, are made by varying the choice of external components.

## SELECTING THE INDUCTOR

The high switching frequency of the ADP5300 allows the use of small surface-mount power inductors. The dc resistance (DCR) value of the selected inductor affects efficiency. In addition, it is recommended to select a multilayer inductor rather than a magnetic iron inductor because the high switching frequency increases the core temperature rise and enlarges the core loss.

A minimum requirement of the dc current rating of the inductor is for it to be equal to the maximum load current plus half of the inductor current ripple ($\Delta I_L$), as shown by the following equations:

$$\Delta I_L = V_{OUT} + \left( \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \right)$$

$$I_{PK} = I_{LOAD(MAX)} + \left( \frac{\Delta I_L}{2} \right)$$

Use the inductor series from the different vendors shown in Table 6.

## OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot, the voltage undershoot, and the ripple voltage present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple. Furthermore, use capacitors such as X5R and X7R dielectric capacitors. Do not use Y5V and Z5U capacitors, because they are unsuitable choices due to their large capacitance variation over temperature and their dc bias voltage changes. Because ESR is important, select the capacitor using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

where:
$ESR_{COUT}$ is the ESR of the chosen capacitor.
$V_{RIPPLE}$ is the peak-to-peak output voltage ripple.

Increasing the output capacitor value has no effect on stability and may reduce output ripple and enhance load transient response. When choosing the output capacitor value, it is important to account for the loss of capacitance due to output voltage dc bias.

Use the capacitor series from the different vendors shown in Table 7.

**Table 6. Recommended Inductors**

| Vendor | Model | Inductance (µH) | Dimensions (mm) | DCR (mΩ) | $I_{SAT}$[1] (A) |
|---|---|---|---|---|---|
| TDK | MLP2016V2R2MT0S1 | 2.2 | 2.0 × 1.6 × 0.85 | 280 | 1.0 |
| Wurth | 74479889222 | 2.2 | 2.5 × 2.0 × 1.2 | 250 | 1.7 |
| Coilcraft | LPS3314-222MR | 2.2 | 3.3 × 3.3 × 1.3 | 100 | 1.5 |

[1] $I_{SAT}$ is the dc current at which the inductance drops 30% (typical) from its value without current.

**Table 7. Input and Output Capacitors**

| Vendor | Model | Capacitance (µF) | Size |
|---|---|---|---|
| Murata | GRM188D71A106MA73 | 10 | 0603 |
| Murata | GRM21BR71A106KE51 | 10 | 0805 |
| Murata | GRM31CR71A106KA01 | 10 | 1206 |

## INPUT CAPACITOR

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the PVIN pin. A low ESR X7R or X5R capacitor is highly recommended to minimize the input voltage ripple. Use the following equation to determine the rms input current:

$$I_{RMS} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

For most applications, a 10 µF capacitor is sufficient. The input capacitor can be increased without any limit for improved input voltage filtering.

## EFFICIENCY

Efficiency is the ratio of output power to input power. The high efficiency of the ADP5300 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package, which in turn reduces thermal constraints. Second, the high efficiency delivers the maximum output power for the given input power, thereby extending battery life in portable applications.

### *Power Switch Conduction Losses*

Power switch dc conduction losses are caused by the flow of output current through the high-side, P-channel power switch and the low-side, N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss is approximated by

$$P_{SW_COND} = (R_{DS(ON)H} \times D + R_{DS(ON)L} \times (1 - D)) \times I_{OUT}^2$$

where:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The internal resistance of the power switches increases with temperature and with the input voltage decrease.

### *Inductor Losses*

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal DCR associated with it. Larger size inductors have smaller DCR, which can decrease inductor conduction losses. Inductor core losses relate to the magnetic permeability of the core material. Because the ADP5300 is a high switching frequency dc-to-dc regulator, shielded ferrite core material is recommended because of its low core losses and low electromagnetic interference (EMI).

To estimate the total amount of power lost in the inductor, use the following equation:

$$P_L = DCR \times I_{OUT}^2 + Core\ Losses$$

### *Driver Losses*

Driver losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground.

Estimate driver losses using the following equation:

$$P_{DRIVER} = (C_{GATE_H} + C_{GATE_L}) \times V_{IN}^2 \times f_{SW}$$

where:

$C_{GATE_H}$ is the gate capacitance of the internal high-side switch.
$C_{GATE_L}$ is the gate capacitance of the internal low-side switch.
$f_{SW}$ is the switching frequency in PWM mode.

The typical values for the gate capacitances are 69 pF for $C_{GATE_H}$ and 31 pF for $C_{GATE_L}$.

### *Transition Losses*

Transition losses occur because the P-channel switch cannot turn on or turn off instantaneously. In the middle of a switch node transition, the power switch provides all of the inductor current. The source to drain voltage of the power switch is half of the input voltage, resulting in power loss. Transition losses increase with both load current and input voltage and occur twice for each switching cycle.

Use the following equation to estimate transition losses:

$$P_{TRAN} = V_{IN}/2 \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:

$t_R$ is the rise time of the SW node.
$t_F$ is the fall time of the SW node.

The typical value for the rise and fall times, $t_R$ and $t_F$, is 2 ns.

## CIRCUIT BOARD LAYOUT RECOMMENDATIONS

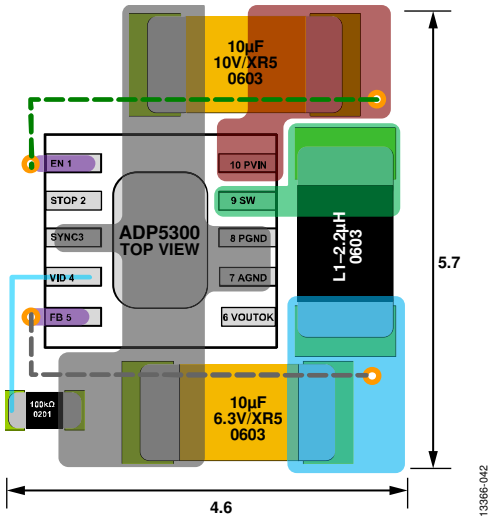



*Figure 42. Typical PCB Layout*

# TYPICAL APPLICATION CIRCUITS

The ADP5300 can be used as a keep-alive, ultralow power step-down regulator to extend the battery life (see Figure 43), and as a battery-powered equipment or wireless sensor network controlled by a microcontroller or a processor (see Figure 44). The STOP switching function can achieve a quiet system environment for a noise sensitive application.

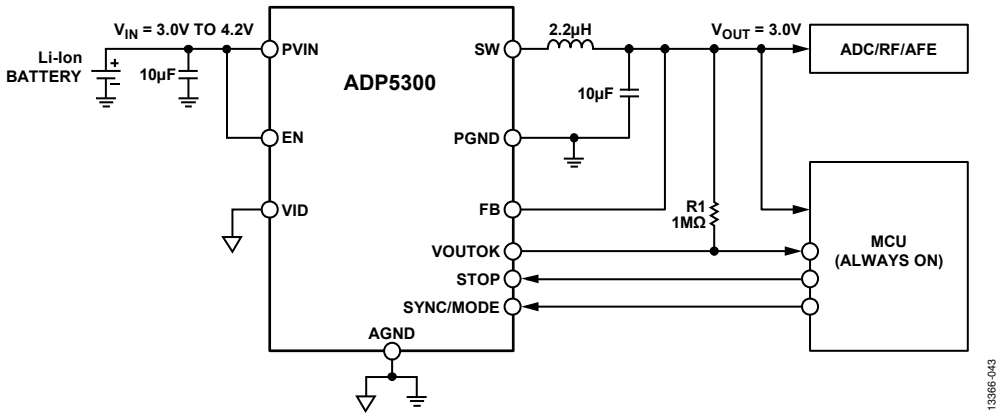



*Figure 43. Typical ADP5300 Application with Li-Ion Battery and STOP Switching Functionality*

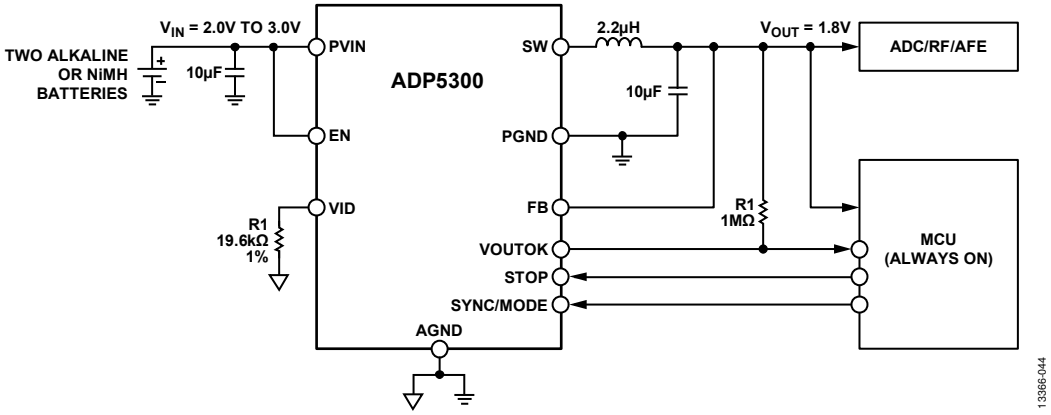



*Figure 44. Typical ADP5300 Application with Two Alkaline/NiMH Batteries*

# FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

**Table 8. Output Voltage VID Setting Options**

| Option | Description |
|---|---|
| Option 0 | VID resistor to set the output voltage as: 1.2 V, 1.5 V, 1.8 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.3 V, 3.6 V, or 3.3 V. |
| Option 1 | VID resistor to set the output voltage as: 0.8 V, 0.9 V, 1.0 V, 1.1 V, 1.3 V, 1.4 V, 1.6 V, 1.7 V, 1.9 V, 3.1 V, 3.2 V, 3.4 V, 3.9 V, 4.2 V, 4.5 V, or 5.0 V. |

**Table 9. Output Discharge Functionality Options**

| Option | Description |
|---|---|
| Option 0 | Output discharge function disabled for buck regulator (default) |
| Option 1 | Output discharge function enabled form buck regulator |

**Table 10. Soft-Start Timer Options**

| Option | Description |
|---|---|
| Option 0 | 350 µs (default) |
| Option 1 | 2800 µs |

# OUTLINE DIMENSIONS

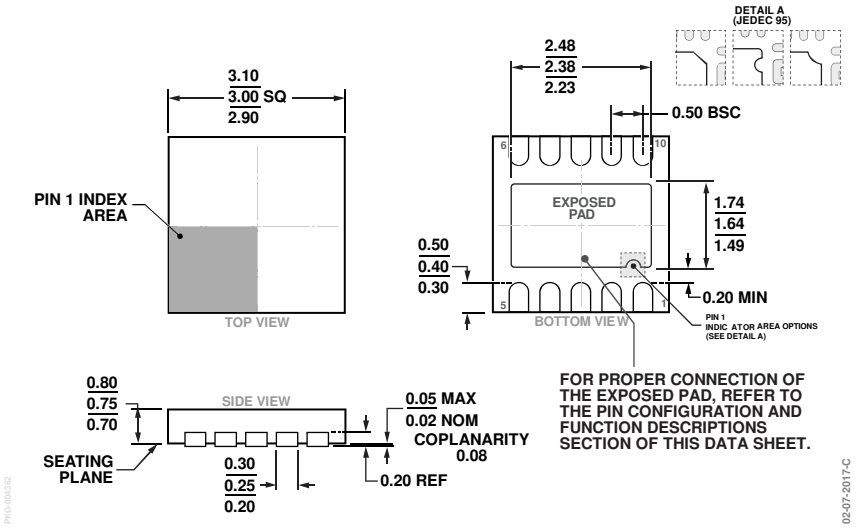



*Figure 45. 10-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-10-9)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADP5300ACPZ-1-R7 | −40°C to +125°C | 10-Lead LFCSP, Output Voltage Option 0 with Output Discharge | CP-10-9 |
| ADP5300ACPZ-2-R7 | −40°C to +125°C | 10-Lead LFCSP, Output Voltage Option 0 without Output Discharge | CP-10-9 |
| ADP5300ACPZ-3-R7 | −40°C to +125°C | 10-Lead LFCSP, Output Voltage Option 1 without Output Discharge | CP-10-9 |
| ADP5300ACPZ-4-R7 | −40°C to +125°C | 10-Lead LFCSP, 3.6 V Fixed Output without Output Discharge, 2800 µs Soft Start Time | CP-10-9 |
| ADP5300-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

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