SHARC
Digital Signal Processor

ADSP-21160M/ADSP-21160N

SUMMARY

High performance 32-bit DSP—applications in audio, medical, military, graphics, imaging, and communication

Super Harvard architecture—4 independent buses for dual data fetch, instruction fetch, and nonintrusive, zero-overhead I/O

Backward compatible—assembly source level compatible with code for ADSP-2106x DSPs

Single-instruction, multiple-data (SIMD) computational architecture—two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file

Integrated peripherals—integrated I/O processor, 4 M bits on-chip dual-ported SRAM, glueless multiprocessing features, and ports (serial, link, external bus, and JTAG)

FEATURES

100 MHz (10 ns) core instruction rate (ADSP-21160N)

Single-cycle instruction execution, including SIMD operations in both computational units

Dual data address generators (DAGs) with modulo and bit-reverse addressing

Zero-overhead looping and single-cycle loop setup, providing efficient program sequencing

IEEE 1149.1 JTAG standard Test Access Port and on-chip emulation

400-ball 27 mm × 27 mm PBGA package

Available in lead-free (RoHS compliant) package

200 million fixed-point MACs sustained performance (ADSP-21160N)

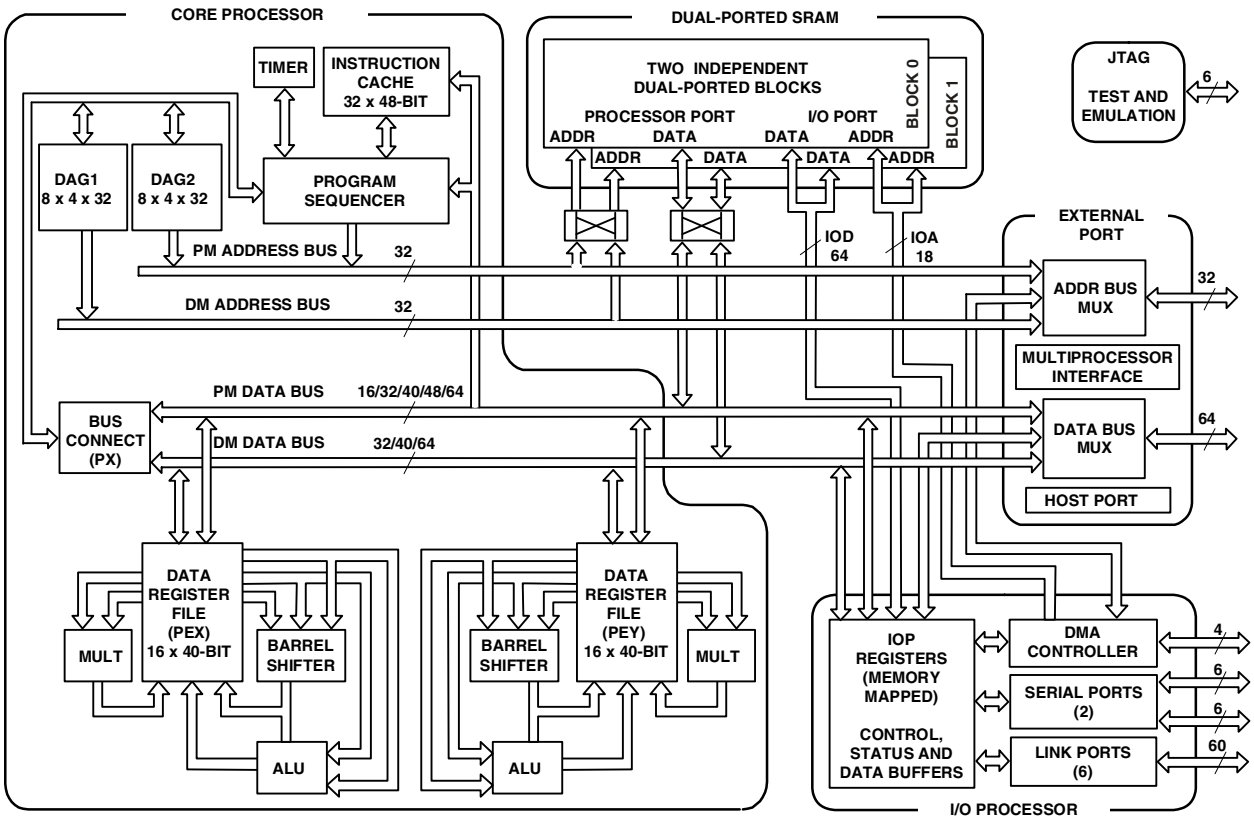


Figure 1. Functional Block Diagram

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- **Single-instruction, multiple-data (SIMD) architecture provides**
  - **Two computational processing elements**
  - **Concurrent execution—each processing element executes the same instruction, but operates on different data**
  - **Code compatibility—at assembly level, uses the same instruction set as the ADSP-2106x SHARC DSPs**
- **Parallelism in buses and computational units allows**
  - **Single-cycle execution (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch**
  - **Transfers between memory and core at up to four 32-bit floating- or fixed-point words per cycle**
  - **Accelerated FFT butterfly computation through a multiply with add and subtract**
- **Memory attributes**
  - **4M bits on-chip dual-ported SRAM for independent access by core processor, host, and DMA**
  - **4G word address range for off-chip memory**
  - **Memory interface supports programmable wait state generation and page-mode for off-chip memory**
- **DMA controller supports**
  - **14 zero-overhead DMA channels for transfers between ADSP-21160x internal memory and external memory, external peripherals, host processor, serial ports, or link ports**
  - **64-bit background DMA transfers at core clock speed, in parallel with full-speed processor execution**
  - **Host processor interface to 16- and 32-bit microprocessors**
- **Multiprocessing support provides**
  - **Glueless connection for scalable DSP multiprocessing architecture**
  - **Distributed on-chip bus arbitration for parallel bus connect of up to 6 ADSP-21160x processors plus host**
  - **6 link ports for point-to-point connectivity and array multiprocessing**
- **Serial ports provide**
  - **Two synchronous serial ports with companding hardware**
  - **Independent transmit and receive functions**
  - **TDM support for T1 and E1 interfaces**
- **64-bit-wide synchronous external port provides**
  - **Glueless connection to asynchronous and SBSRAM external memories**

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REVISION HISTORY

9/15—Rev. C to Rev. D

Removed model ADSP-21160NKB-100 (no longer available) from Ordering Guide 58

GENERAL DESCRIPTION

The ADSP-21160x SHARC® DSP family has two members: ADSP-21160M and ADSP-21160N. The ADSP-21160M is fabricated in a 0.25 micron CMOS process. The ADSP-21160N is fabricated in a 0.18 micron CMOS process. The ADSP-21160N offers higher performance and lower power consumption than the ADSP-21160M. Easing portability, the ADSP-21160x is application source code compatible with first generation ADSP-2106x SHARC DSPs in SISD (single instruction, single data) mode. To take advantage of the processor's SIMD (single-instruction, multiple-data) capability, some code changes are needed. Like other SHARC DSPs, the ADSP-21160x is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21160x includes a core running up to 100 MHz, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

Table 1 shows major differences between the ADSP-21160M and ADSP-21160N processors.

Table 1. ADSP-21160x SHARC Processor Family Features

Feature	ADSP-21160M	ADSP-21160N
SRAM	4 Mbits	4 Mbits
Operating Voltage	3.3 V I/O 2.5 V Core	3.3 V I/O 1.9 V Core
Instruction Rate	80 MHz	100 MHz
Link Port Transfer Rate (6)	80 MBytes/s	100 MBytes/s
Serial Port Transfer Rate (2)	40 Mbits/s	50 Mbits/s

The ADSP-21160x introduces single-instruction, multiple-data (SIMD) processing. Using two computational units (ADSP-2106x SHARC DSPs have one), the ADSP-21160x can double performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state-of-the-art, high speed, low power CMOS process, the ADSP-21160N has a 10 ns instruction cycle time. With its SIMD computational hardware running at 100 MHz, the ADSP-21160N can perform 600 million math operations per second (480 million operations for ADSP-21160M at a 12.5 ns instruction cycle time).

Table 2 shows performance benchmarks for the ADSP-21160x.

These benchmarks provide single-channel extrapolations of measured dual-channel (SIMD) processing performance. For more information on benchmarking and optimizing DSP code for single- and dual-channel processing, see the Analog Devices website (www.analog.com).

The ADSP-21160x continues the SHARC family's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 4M-bit dual-ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, two serial ports, six link ports, external parallel bus, and glueless multiprocessing.

Table 2. ADSP-21160x Benchmarks

Benchmark Algorithm	ADSP-21160M 80 MHz	ADSP-21160N 100 MHz
1024 Point Complex FFT (Radix 4, with reversal)	115 µs	92 µs
FIR Filter (per tap)	6.25 ns	5 ns
IIR Filter (per biquad)	25 ns	20 ns
Matrix Multiply (pipelined)		
[3×3] × [3×1]	56.25 ns	45 ns
[4×4] × [4×1]	100 ns	80 ns
Divide (y/x)	37.5 ns	30 ns
Inverse Square Root	56.25 ns	45 ns
DMA Transfer Rate	560M bytes/s	800M bytes/s

The functional block diagram (Figure 1 on Page 1) of the ADSP-21160x illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-chip SRAM (4M bits)
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21160x SHARC DSPs
  - Host port
- DMA controller
- Serial ports and link ports
- JTAG test access port

Figure 2 shows a typical single-processor system. A multiprocessing system appears in Figure 3 on Page 6.

ADSP-21160X FAMILY CORE ARCHITECTURE

The ADSP-21160x processor includes the following architectural features of the ADSP-2116x family core. The ADSP-21160x is code compatible at the assembly level with the ADSP-2106x and ADSP-21161.

SIMD Computational Engine

The ADSP-21160x contains two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is

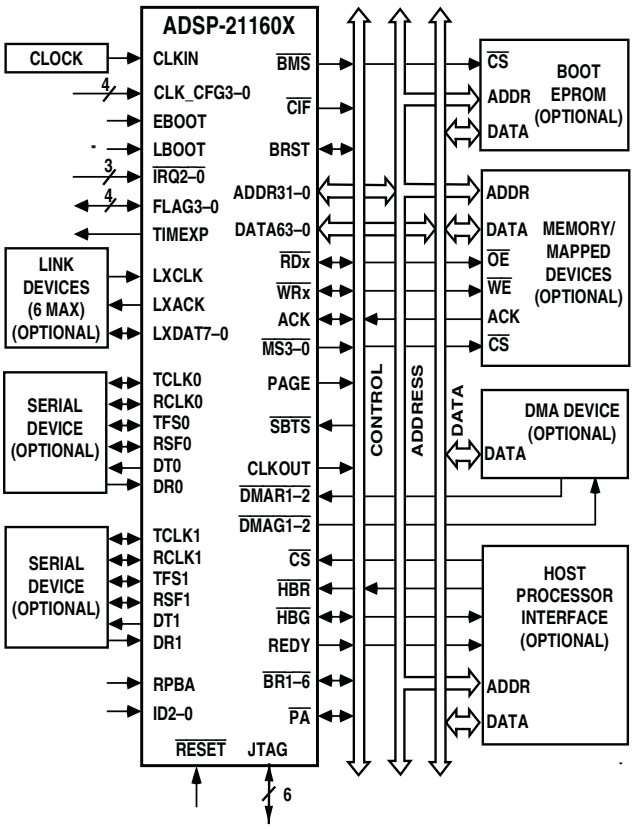


Figure 2. Single-Processor System

enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math-intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. In SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2116x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data, and the program memory (PM) bus transfers both instructions and data (see the functional block diagram 1). With the ADSP-21160x DSP's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21160x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, providing looped operations, such as digital filter multiply- accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21160x DSP's two data address generators (DAGs) are used for indirect addressing and provide for implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the product contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and subtract, in both processing elements, while branching, all in a single instruction.

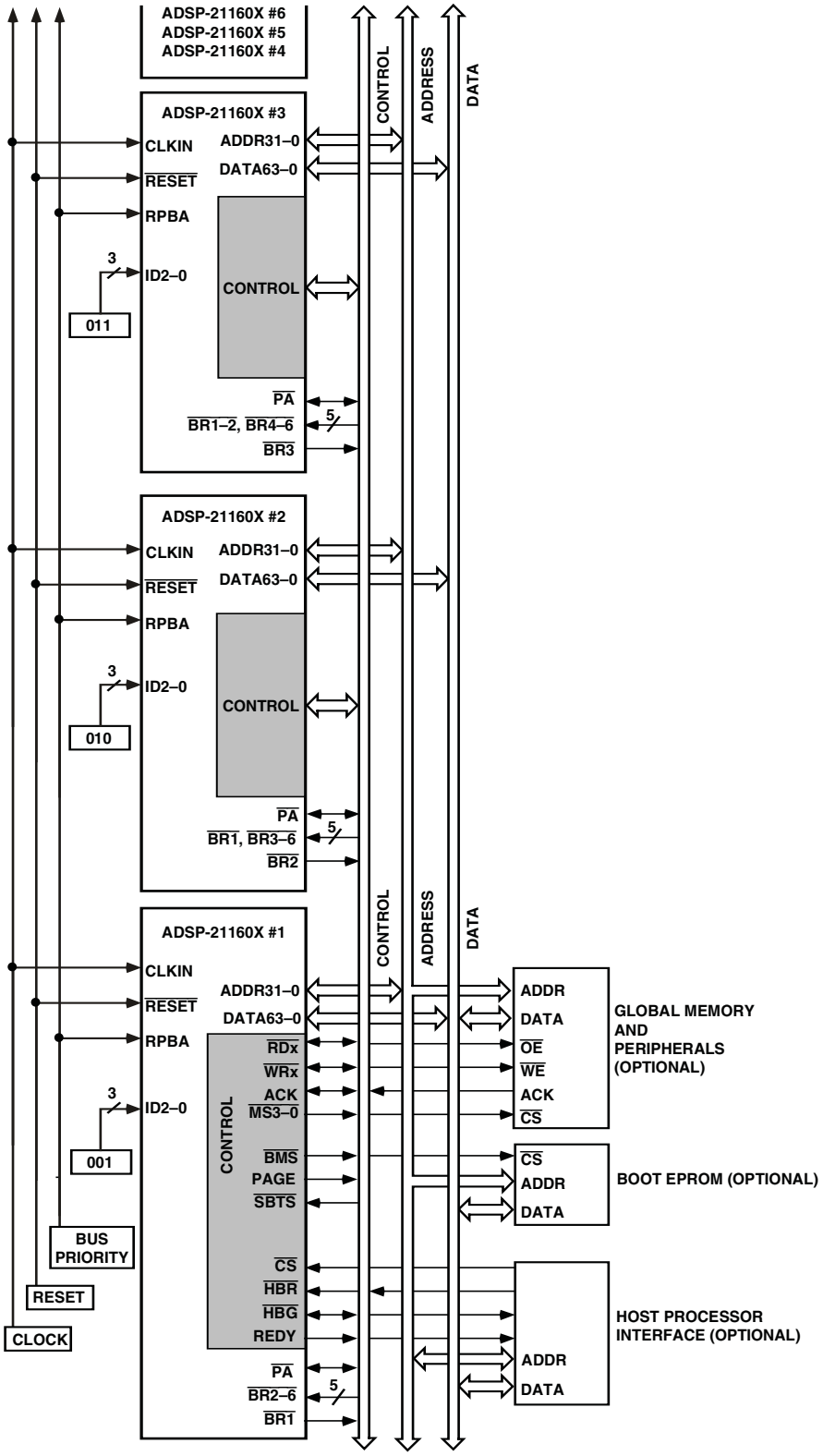


Figure 3. Shared Memory Multiprocessing System

MEMORY AND I/O INTERFACE FEATURES

Augmenting the ADSP-2116x family core, the ADSP-21160x adds the following architectural features.

Dual-Ported On-Chip Memory

The ADSP-21160x contains four megabits of on-chip SRAM, organized as two blocks of 2M bits each, which can be configured for different combinations of code and data storage (Figure 4). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allows two data transfers from the core and one from I/O processor, in a single cycle. The ADSP-21160x memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 85K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-, 32-, 48-, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21160x DSP's external port provides the processor's interface to off-chip memory and peripherals. The 4G word off-chip address space is included in the processor's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 64-bit data bus. The lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits of the 64 connect to odd addresses. Every access to external memory is based on an address that fetches a 32-bit word, and with the 64-bit bus, two address locations can be accessed at once. When fetching an instruction from external memory, two 32-bit data locations are being accessed (16 bits are unused). Figure 5 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. ZBT synchronous burst SRAM can be interfaced gluelessly. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21160x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

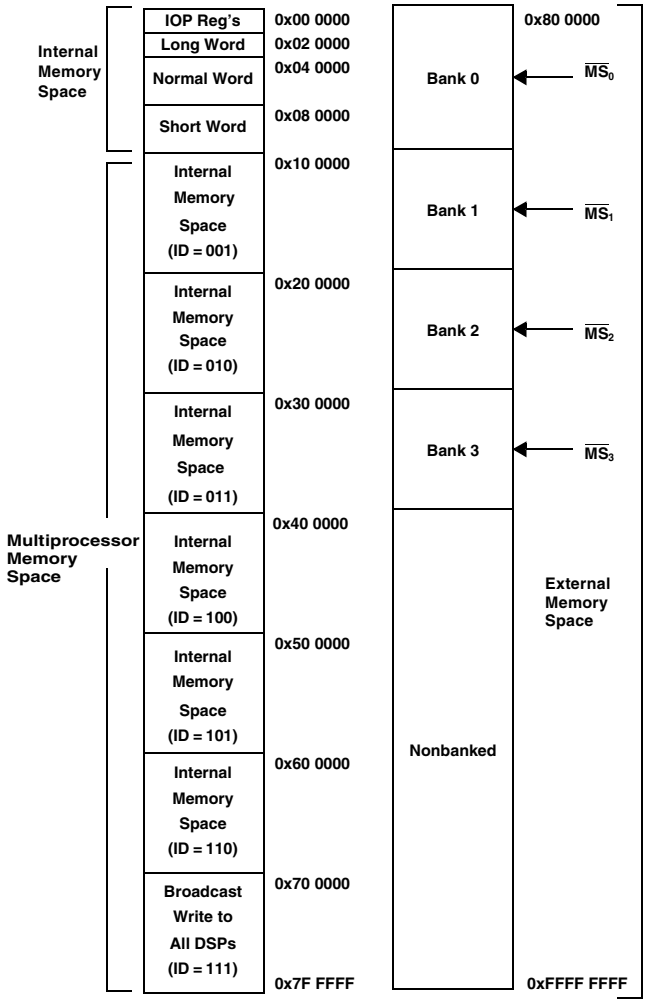


Figure 4. Memory Map

DMA Controller

The ADSP-21160x DSP's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the product's DSP's internal memory and its serial ports or link ports. External bus packing to 16-, 32-, 48-, or 64-bit words is performed during DMA transfers. Fourteen channels of DMA are available on the ADSP-21160x—six via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-21160x processors, memory or I/O transfers). Programs can be downloaded to the processor using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include

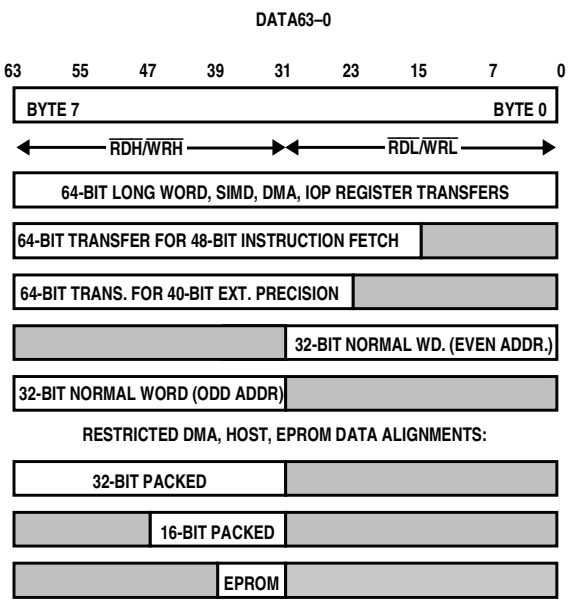


Figure 5. External Data Alignment Options

interrupt generation upon completion of DMA transfers, two-dimensional DMA, and DMA chaining for automatic linked DMA transfers.

Multiprocessing

The ADSP-21160x offers powerful features tailored to multiprocessing DSP systems as shown in M. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 4) that allows direct interprocessor accesses of each processor's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21160x processors and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 400M bytes/s (ADSP-21160N) over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21160x DSPs and can be used to implement reflective semaphores.

Six link ports provide for a second method of multiprocessing communications. Each link port can support communications to another ADSP-21160x. Using the links, a large multiprocessor system can be constructed in a 2D or 3D fashion. Systems can use the link ports and cluster multiprocessing concurrently or independently.

Link Ports

The processor features six 8-bit link ports that provide additional I/O capabilities. With the capability of running at 100 MHz rates, each link port can support 100M bytes/s (ADSP-21160N). Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously. Link port data is packed into 48- or 32-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as transmit or receive.

Serial Ports

The processor features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate up to half the clock rate of the core, providing each with a maximum data rate of 50M bits/s (ADSP-21160N). Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports offers a TDM multichannel mode. The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be generated internally or externally.

Host Processor Interface

The ADSP-21160x host interface allows easy connection to standard microprocessor buses, both 16- and 32-bit, with little additional hardware required. The host interface is accessed through the ADSP-21160x DSP's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor communicates with the ADSP-21160x DSP's external bus with host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), ready (REDY), acknowledge (ACK), and chip select (CS) signals. The host can directly read and write the internal memory of the processor, and can access the DMA channel setup and mailbox registers. Vector interrupt support provides efficient execution of host commands.

The host processor interface can be used in either multiprocessor or uniprocessor systems. For multiprocessor systems, host access to the SHARC requires that address pins ADDR17, ADDR18, ADDR19, and ADDR20 be driven low. It is not enough to tie these pins to ground through a resistor (for example, 10 kΩ). These pins must be driven low with a strong enough drive strength (10 Ω to 50 Ω) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For uniprocessor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example, through a 10 kΩ ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

Program Booting

The internal memory of the ADSP-21160x can be booted at system power-up from an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (Boot Memory Select), EBOOT (EPROM Boot), and LBOOT (Link/Host Boot) pins. 32-bit and 16-bit host processors can be used for booting.

Phase-Locked Loop

The processor uses an on-chip PLL to generate the internal clock for the core. Ratios of 2:1, 3:1, and 4:1 between the core and CLKIN are supported. The CLK_CFG pins are used to select the ratio. The CLKIN rate is the rate at which the synchronous external port operates.

Power Supplies

The processor has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (AV_{DD} and AGND) power supplies. The internal and analog supplies must meet the V_{DDINT} and AV_{DD} requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

The PLL filter, Figure 6, must be added for each ADSP-21160x in the system. V_{DDINT} is the digital core supply. It is recommended that the capacitors be connected directly to AGND using short thick trace. It is recommended that the capacitors be placed as close to AV_{DD} and AGND as possible. The connection from AGND to the (digital) ground plane should be made after the capacitors. The use of a thick trace for AGND is reasonable only because the PLL is a relatively low power circuit—it does not apply to any other ADSP-21160x GND connection.

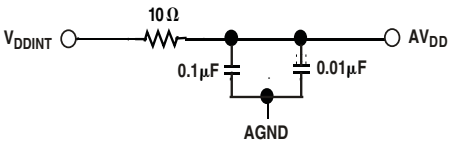


Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21160x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Tie or pull unused inputs to V_{DD} or GND, except for the following:

- ADDR31–0, DATA63–0, PAGE, BRST, CLKOUT (ID2–0 = 00x) (Note: These pins have a logic-level hold circuit enabled on the ADSP-21160x DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{MS3–0}}$, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{CIF}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$ (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21160x with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the *ADSP-21160 SHARC DSP Hardware Reference*.)
- DTx, DRx, TCLKx, RCLKx, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 3: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21160x is a bus slave).

Table 3. Pin Function Descriptions

Pin	Type	Function
ADDR31–0	I/O/T	External Bus Address. The ADSP-21160x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-21160x DSPs. The ADSP-21160x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers. A keeper latch on the DSP's ADDR31–0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
DATA63–0	I/O/T	External Bus Data. The ADSP-21160x inputs and outputs data and instructions on these pins. Pull-up resistors on unused DATA pins are not necessary. A keeper latch on the DSP's DATA63-0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
$\overline{\text{MS3–0}}$	O/T	Memory Select Lines. These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the SYSCON control register. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. $\overline{\text{MS3–0}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{\text{RDL}}$	I/O/T	Memory Read Low Strobe. $\overline{\text{RDL}}$ is asserted whenever ADSP-21160x reads from the low word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDL}}$ for reading from the low word of processor internal memory. In a multiprocessing system, $\overline{\text{RDL}}$ is driven by the bus master. $\overline{\text{RDL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{RDH}}$	I/O/T	Memory Read High Strobe. $\overline{\text{RDH}}$ is asserted whenever ADSP-21160x reads from the high word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDH}}$ for reading from the high word of ADSP-21160x internal memory. In a multiprocessing system, $\overline{\text{RDH}}$ is driven by the bus master. $\overline{\text{RDH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRL}}$	I/O/T	Memory Write Low Strobe. $\overline{\text{WRL}}$ is asserted when ADSP-21160x writes to the low word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRL}}$ for writing to ADSP-21160x DSP's low word of internal memory. In a multiprocessing system, $\overline{\text{WRL}}$ is driven by the bus master. $\overline{\text{WRL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRH}}$	I/O/T	Memory Write High Strobe. $\overline{\text{WRH}}$ is asserted when ADSP-21160x writes to the high word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRH}}$ for writing to ADSP-21160x DSP's high word of internal memory. In a multiprocessing system, $\overline{\text{WRH}}$ is driven by the bus master. $\overline{\text{WRH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
PAGE	O/T	DRAM Page Boundary. The processor asserts this pin to an external DRAM controller, to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the processor's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master. A keeper latch on the DSP's PAGE pin maintains the output at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
BRST	I/O/T	Sequential Burst Access. BRST is asserted by ADSP-21160x or a host to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. If the burst access is a read from the host to the processor, the processor automatically increments the address as long as BRST is asserted. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{RDx}$ or $\overline{WRx}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
ACK	I/O/S	Memory Acknowledge. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21160x deasserts ACK as an output to add wait states to a synchronous access of its internal memory, by a synchronous host or another DSP in a multiprocessor configuration. ACK has a 2 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{SBTS}$	I/S	Suspend Bus and Three-State. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high-impedance state for the following cycle. If the ADSP-21160x attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor and/or ADSP-21160x deadlock or used with a DRAM controller.
$\overline{IRQ2–0}$	I/A	Interrupt Request Lines. These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG3–0	I/O/A	Flag Pins. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	Timer Expired. Asserted for four processor core clock (CCLK) cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	Host Bus Request. Must be asserted by a host processor to request control of the ADSP-21160x DSP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the processor that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the processor places the address, data, select, and strobe lines in a high-impedance state. $\overline{HBR}$ has priority over all processor bus requests ($\overline{BR6–1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	Host Bus Grant. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-21160x until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the processor bus master and is monitored by all others. After $\overline{HBR}$ is asserted, and before $\overline{HBG}$ is given, $\overline{HBG}$ will float for 1 t_{CLK} (1 CLKIN cycle). To avoid erroneous grants, $\overline{HBG}$ should be pulled up with a 20 kΩ to 50 kΩ external resistor.
$\overline{CS}$	I/A	Chip Select. Asserted by host processor to select the ADSP-21160x, for asynchronous transfer protocol.
REDY	O (O/D)	Host Bus Acknowledge. The ADSP-21160x deasserts REDY (low) to add wait states to an asynchronous host access when $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	DMA Request 1 (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{DMAR1}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{DMAR2}$	I/A	DMA Request 2 (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{DMAR2}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
ID2–0	I	Multiprocessing ID. Determines which multiprocessing bus request ($\overline{BR1}$–$\overline{BR6}$) is used by the ADSP-21160x. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, and so on. Use ID = 000 or ID = 001 in single-processor systems. These lines are a system configuration selection which should be hardwired or only changed at reset.
$\overline{DMAG1}$	O/T	DMA Grant 1 (DMA Channel 11). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG1}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{DMAG2}$	O/T	DMA Grant 2 (DMA Channel 12). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG2}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{BR6–1}$	I/O/S	Multiprocessing Bus Requests. Used by multiprocessing ADSP-21160x DSPs to arbitrate for bus mastership. An ADSP-21160x only drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21160x DSPs, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
RPBA	I/S	Rotating Priority Bus Arbitration Select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21160x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{PA}$	I/O/T	Priority Access. Asserting its $\overline{PA}$ pin allows an ADSP-21160x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{PA}$ is connected to all ADSP-21160x DSPs in the system. If access priority is not required in a system, the $\overline{PA}$ pin should be left unconnected. $\overline{PA}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
DTx	O	Data Transmit (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	Data Receive (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	Transmit Frame Sync (Serial Ports 0, 1).
RFSx	I/O	Receive Frame Sync (Serial Ports 0, 1).
LxDAT7–0	I/O	Link Port Data (Link Ports 0–5). Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxCLK	I/O	Link Port Clock (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxACK	I/O	Link Port Acknowledge (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	EPROM Boot Select. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
LBOOT	I	Link Boot. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
$\overline{BMS}$	I/O/T	Boot Memory Select. Serves as an output or input as selected with the EBOOT and LBOOT pins; see Table 4. This input is a system configuration selection that should be hardwired.
CLKIN	I	Local Clock In. CLKIN is the ADSP-21160x clock input. The ADSP-21160x external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up. CLKIN may not be halted, changed, or operated below the specified frequency.
CLK_CFG3–0	I	Core/CLKIN Ratio Control. ADSP-21160x core clock (instruction cycle) rate is equal to n x CLKIN where n is user-selectable to 2, 3, or 4, using the CLK_CFG3–0 inputs. For clock configuration definitions, see the *$\overline{RESET}$ & CLKIN* section of the *System Design* chapter of the *ADSP-21160 SHARC DSP Hardware Reference*.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
CLKOUT	O/T	Local Clock Out. CLKOUT is driven at the CLKIN frequency by the processor. This output can be three-stated by setting the COD bit in the SYSCON register. A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven (only enabled on the processor with ID2-0 = 00x). Do not use CLKOUT in multiprocessing systems; use CLKIN instead.
$\overline{\text{RESET}}$	I/A	Processor Reset. Resets the ADSP-21160x to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21160x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Emulation Status. Must be connected to the ADSP-21160x emulator target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
$\overline{\text{CIF}}$	O/T	Core Instruction Fetch. Signal is active low when an external instruction fetch is performed. Driven by bus master only. Three-state when host is bus master. $\overline{\text{CIF}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
V_{DDINT}	P	Core Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's core processor
V_{DDEXT}	P	I/O Power Supply. Nominally 3.3 V dc.
AV_{DD}	P	Analog Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on page 9.
AGND	G	Analog Power Supply Return.
GND	G	Power Supply Return.
NC		Do Not Connect. Reserved pins that must be left open and unconnected.

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
0	1	0 (Input)	Reserved
1	1	x (Input)	Reserved

SPECIFICATIONS

OPERATING CONDITIONS—ADSP-21160M

Table 5 shows the recommended operating conditions for the ADSP-21160M. Specifications are subject to change without notice.

Table 5. Operating Conditions—ADSP-21160M

		K Grade		
Parameter		**Min**	**Max**	**Unit**
V_{DDINT}	Internal (Core) Supply Voltage	2.37	2.63	V
AV_{DD}	Analog (PLL) Supply Voltage	2.37	2.63	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.2	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.3	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	−0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.

[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.

[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS—ADSP-21160M

Table 6 shows ADSP-21160M electrical characteristics. These specifications are subject to change without notification.

Table 6. Electrical Characteristics—ADSP-21160M

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU1}	Low Level Input Current Pull-Up1[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{ILPU2}	Low Level Input Current Pull-Up2[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZH}	Three-State Leakage Current[6, 7, 8, 9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZHPD}	Three-State Leakage Current Pull-Down[9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		250	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[8]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZHA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		25	µA
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		4	mA
$I_{DD-INPEAK}$	Supply Current (Internal)[11]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		1400	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[12]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		875	mA
$I_{DD-INLOW}$	Supply Current (Internal)[13]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		625	mA
$I_{DD-IDLE}$	Supply Current (Idle)[14]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		400	mA
AI_{DD}	Supply Current (Analog)[15]	@AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[16, 17]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, PAGE, CLKOUT, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{BMS}$, TDO, and $\overline{EMU}$.

[2] See Output Drive Currents—ADSP-21160M on Page 47 for typical drive current capabilities.

[3] Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK, and CLK_CFG3-0.

[4] Applies to input pins with internal pull-ups: DR0, and DR1.

[5] Applies to input pins with internal pull-ups: $\overline{DMARx}$, TMS, TDI, and $\overline{TRST}$.

[6] Applies to three-statable pins: DATA63–0, ADDR31–0, PAGE, CLKOUT, ACK, FLAG3–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, and TDO.

[7] Applies to three-statable pins with internal pull-ups: DTx, TCLKx, RCLKx, and $\overline{EMU}$.

[8] Applies to three-statable pins with internal pull-ups: $\overline{MS3–0}$,$\overline{RDx}$, $\overline{WRx}$, $\overline{DMAGx}$, $\overline{PA}$, and $\overline{CIF}$.

[9] Applies to three-statable pins with internal pull-downs: LxDAT7–0, LxCLK, and LxACK.

[10] Applies to ACK pulled up internally with 2 kΩ during reset or ID2–0 = 00x.

[11] The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 47.

[12] $I_{DD-INHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 47.

[13] $I_{DD-INLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 47.

[14] Idle denotes ADSP-21160M state during execution of IDLE instruction. For more information, see Power Dissipation on Page 47.

[15] Characterized, but not tested.

[16] Applies to all signal pins.

[17] Guaranteed, but not tested.

OPERATING CONDITIONS—ADSP-21160N

Table 7 shows recommended operating conditions for the ADSP-21160N. These specifications are subject to change without notice.

Table 7. Operating Conditions—ADSP-21160N

Parameter		C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.8	2.0	1.8	2.0	V
AV_{DD}	Analog (PLL) Supply Voltage	1.8	2.0	1.8	2.0	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	–40	+100	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	–0.5	+0.8	–0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.
[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, $\overline{ACK}$, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{FLAG3–0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.
[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS—ADSP-21160N

Table 8 shows the electrical characteristics. Note that these specifications are subject to change without notification.

Table 8. Electrical Characteristics—ADSP-21160N

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{IHC}	CLKIN High Level Input Current[6]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		25	µA
I_{ILC}	CLKIN Low Level Input Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		25	µA
I_{IKH}	Keeper High Load Current[7]	@ V_{DDEXT} = Max, V_{IN} = 2.0 V	–250	–50	µA
I_{IKL}	Keeper Low Load Current[7]	@ V_{DDEXT} = Max, V_{IN} = 0.8 V	50	200	µA
I_{IKH-OD}	Keeper High Overdrive Current[7, 8, 9]	@ V_{DDEXT} = Max	–300		µA
I_{IKL-OD}	Keeper Low Overdrive Current[7, 8, 9]	@ V_{DDEXT} = Max	300		µA
I_{ILPU1}	Low Level Input Current Pull-Up1[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{ILPU2}	Low Level Input Current Pull-Up2[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZH}	Three-State Leakage Current[10, 11, 12, 13]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZHPD}	Three-State Leakage Current Pull-Down[13]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		250	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[11]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[12]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZHA}	Three-State Leakage Current[14]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		25	µA
I_{OZLA}	Three-State Leakage Current[14]	@ V_{DDEXT} = Max, V_{IN} = 0 V		4	mA
$I_{DD-INPEAK}$	Supply Current (Internal)[15]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		960	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[16]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		715	mA
$I_{DD-INLOW}$	Supply Current (Internal)[17]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		550	mA
$I_{DD-IDLE}$	Supply Current (Idle)[18]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		450	mA
AI_{DD}	Supply Current (Analog)[9]	@AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[19, 20]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, PAGE, CLKOUT, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{BMS}$, TDO, and $\overline{EMU}$.

[2] See Output Drive Currents 47 for typical drive current capabilities.

[3] Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK, and CLK_CFG3-0.

[4] Applies to input pins with internal pull-ups: DR0, and DR1.

[5] Applies to input pins with internal pull-ups: $\overline{DMARx}$, TMS, TDI, and $\overline{TRST}$.

[6] Applies to CLKIN only.

[7] Applies to all pins with keeper latches: ADDR31–0, DATA63–0, PAGE, BRST, and CLKOUT.

[8] Current required to switch from kept high to low, or from kept low to high.

[9] Characterized, but not tested.

[10] Applies to three-statable pins: DATA63–0, ADDR31–0, PAGE, CLKOUT, ACK, FLAG3–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, and TDO.

[11] Applies to three-statable pins with internal pull-ups: DTx, TCLKx, RCLKx, and $\overline{EMU}$.

[12] Applies to three-statable pins with internal pull-ups: $\overline{MS3–0}$,$\overline{RDx}$, $\overline{WRx}$, $\overline{DMAGx}$, $\overline{PA}$, and $\overline{CIF}$.

[13] Applies to three-statable pins with internal pull-downs: LxDAT7–0, LxCLK, and LxACK.

[14] Applies to ACK pulled up internally with 2 kΩ during reset or ID2–0 = 00x.

[15] The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 47.

[16] $I_{DD-INHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 47.

[17] $I_{DD-INLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 47.

[18] Idle denotes ADSP-21160N state during execution of IDLE instruction. For more information, see Power Dissipation on Page 47.

[19] Applies to all signal pins.

[20] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 9 (ADSP-21160M) and Table 10 (ADSP-21160N) may cause permanent damage to the product. These are stress ratings only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings—ADSP-21160M

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +3.0 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +3.0 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

Table 10. Absolute Maximum Ratings—ADSP-21160N

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.3 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.3 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD SENSITIVITY



ESD (electrostatic discharge sensitive device)
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about the package branding for the ADSP-21160M/ADSP-21160N processor. For a complete listing of product availability, see Ordering Guide on Page 58.



Figure 7. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
a	ADSP-21160 Model (M or N)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

TIMING SPECIFICATIONS

The ADSP-21160x DSP's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21160x DSP's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG3–0 pins. Even though the internal clock is the clock source for the external port, the external port clock always switches at the CLKIN frequency. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (TDIVx/RDIVx for the serial ports and LxCLKD1–0 for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control:

- $t_{CCLK} = (t_{CK}) / CR$
- $t_{LCLK} = (t_{CCLK}) \times LR$
- $t_{SCLK} = (t_{CCLK}) \times SR$

where:

- LCLK = Link Port Clock
- SCLK = Serial Port Clock
- t_{CK} = CLKIN Clock Period
- t_{CCLK} = (Processor) Core Clock Period
- t_{LCLK} = Link Port Clock Period
- t_{SCLK} = Serial Port Clock Period
- CR = Core/CLKIN Ratio (2, 3, or 4:1, determined by CLK_CFG3–0 at reset)
- LR = Link Port/Core Clock Ratio (1, 2, 3, or 4:1, determined by LxCLKD)
- SR = Serial Port/Core Clock Ratio (wide range, determined by × CLKDIV)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 33 on Page 49 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

During processor reset ($\overline{RESET}$ pin low) or software reset (SRST bit in SYSCON register = 1), deassertion ($\overline{MS3–0}$, $\overline{HBG}$, $\overline{DMAGx}$, $\overline{RDx}$, $\overline{WRx}$, $\overline{CIF}$, PAGE, BRST) and three-state (FLAG3-0, LxCLK, LxACK, LxDAT7-0, ACK, REDY, $\overline{PA}$, TFSx, RFSx, TCLKx, RCLKx, DTx, $\overline{BMS}$, TDO, $\overline{EMU}$, DATA) timings differ. These occur asynchronously to CLKIN, and may not meet the specifications published in the timing requirements and switching characteristics tables. The maximum delay for deassertion and three-state is one t_{CK} from $\overline{RESET}$ pin assertion low or setting the SRST bit in SYSCON. During reset the DSP will not respond to $\overline{SBTS}$, $\overline{HBR}$, and MMS accesses. $\overline{HBR}$ asserted before reset will be recognized, but an $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP has completed bus synchronization.

Unless otherwise noted, all timing specifications (*Timing Requirements* and *Switching Characteristics*) listed on pages 21 through 46 apply to both ADSP-21160M and ADSP-21160N.

Power-Up Sequencing

For power-up sequencing, see Table 12 and Figure 8. During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two power supplies can cause current to flow in the I/O ESD protection circuitry. To prevent this damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode (see Figure 9). The bootstrap Schottky diode connected between the V_{DDINT} and V_{DDEXT} power supplies protects the ADSP-21160x from partially powering the V_{DDEXT} supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the V_{DDINT} rail rises ahead of the V_{DDEXT} rail, the Schottky diode pulls the V_{DDEXT} rail along with the V_{DDINT} rail.

Table 12. Power-Up Sequencing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	– 50	+200	ms
t_{CLKVDD}	CLKIN Running After valid V_{DDINT}/V_{DDEXT}[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristics				
$t_{CORERST}$	DSP Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK}$[3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their V_{DDINT} and V_{DDEXT} rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal after meeting worst-case start-up timing of oscillators. Refer to your oscillator manufacturer's data sheet for start-up time.

[3] Based on CLKIN cycles.

[4] $\overline{\text{CORERST}}$ is an internal signal only. The 4096 cycle count is dependent on t_{SRST} specification. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

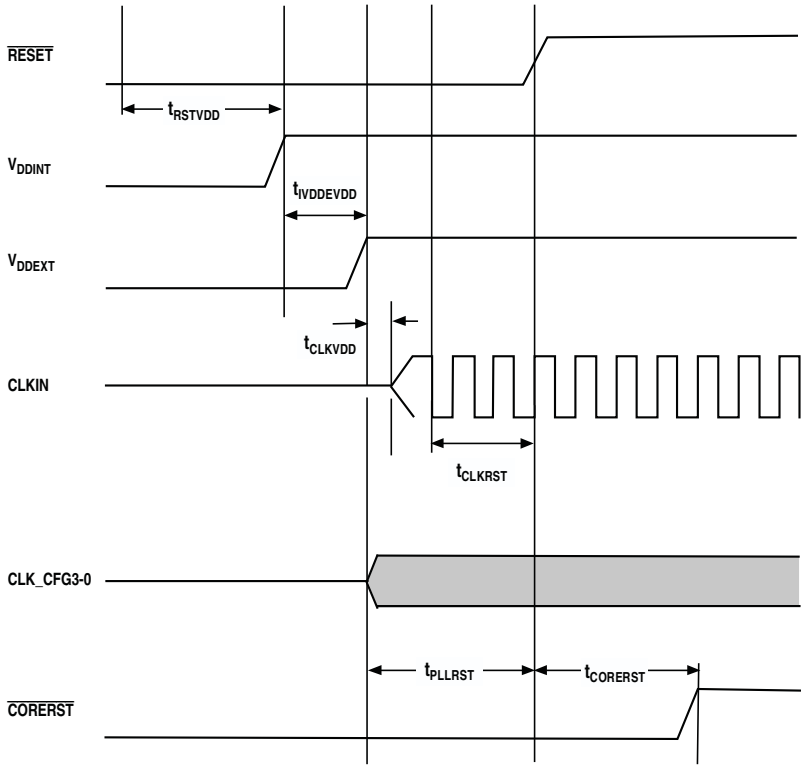


Figure 8. Power-Up Sequencing

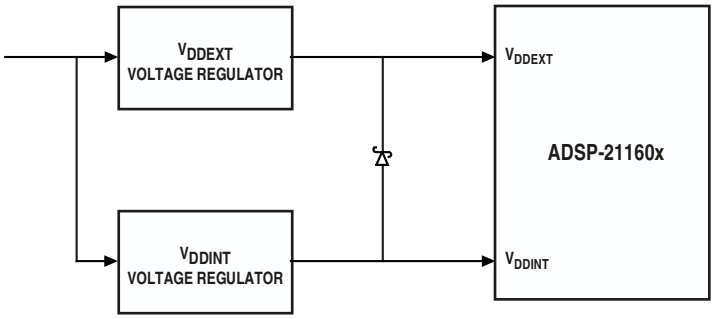


Figure 9. Dual Voltage Schottky Diode

Clock Input

For clock input, see Table 13 and Figure 10.

Table 13. Clock Input

Parameter		ADSP-21160M 80 MHz		ADSP-21160N 100 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	25	80	20	80	ns
t_{CKL}	CLKIN Width Low	10.5	40	7.5	40	ns
t_{CKH}	CLKIN Width High	10.5	40	7.5	40	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	Core Clock Period	12.5	40	10	30	ns

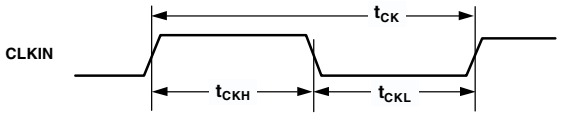


Figure 10. Clock Input

Reset

For reset, see Table 14 and Figure 11.

Table 14. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-21160x DSPs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21160x DSPs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

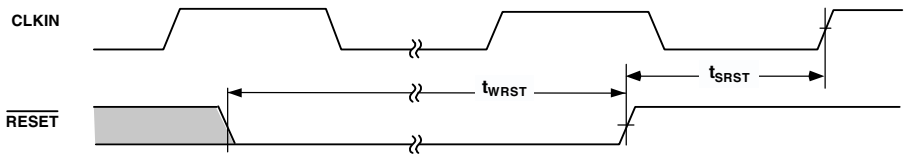


Figure 11. Reset

Interrupts

For interrupts, see Table 15 and Figure 12.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN High[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

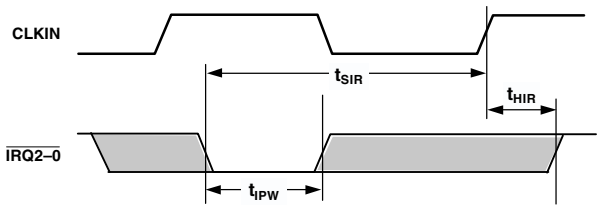


Figure 12. Interrupts

Timer

For timer, see Table 16 and Figure 13.

Table 16. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP[1]	1	9	ns

[1] For ADSP-21160M, specification is 7 ns, maximum.

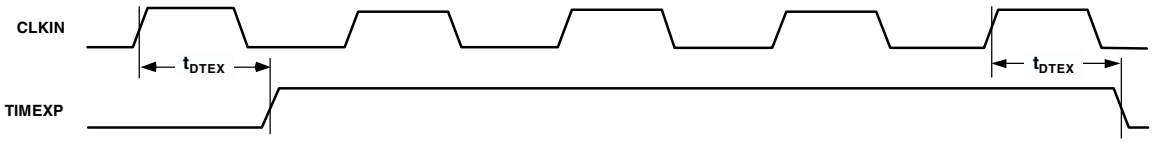


Figure 13. Timer

Flags

For flags, see Table 17 and Figure 14.

Table 17. Flags

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	4		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	1		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RDx}$/$\overline{WRx}$ Low[1, 2]		10	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RDx}$/$\overline{WRx}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		9	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	1		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	1		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable[3]		$t_{CK} - t_{CCLK} + 5$	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N + 2.
[2] For ADSP-21160M, specification is 12 ns, maximum.
[3] For ADSP-21160M, specification is 5 ns, maximum.

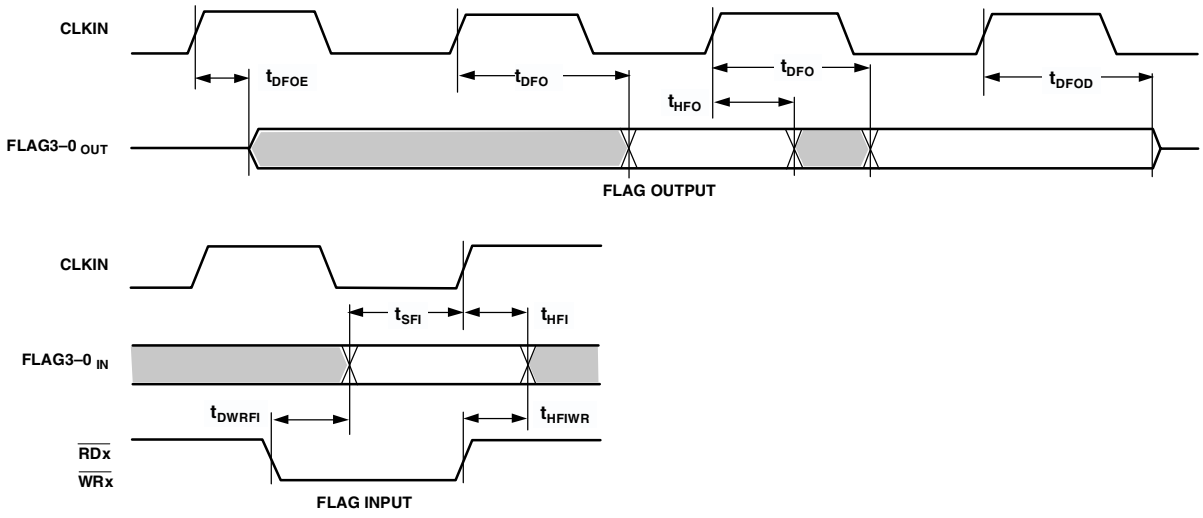


Figure 14. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 6 of Table 18. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 18. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, $\overline{CIF}$, Selects Delay to Data Valid[1, 2, 3, 4]		$t_{CK} - 0.25t_{CCLK} - 8.5 + W$	ns
t_{DRLD}	$\overline{RDx}$ Low to Data Valid[1, 4, 5]		$t_{CK} - 0.5t_{CCLK} + W$	ns
t_{HDA}	Data Hold from Address, Selects[6]	0		ns
t_{SDS}	Data Setup to $\overline{RDx}$ High[1]	8		ns
t_{HDRH}	Data Hold from $\overline{RDx}$ High[6]	1		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 7]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{RDx}$ Low[7]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[7]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DRHA}	Address, $\overline{CIF}$, Selects Hold After $\overline{RDx}$ High	$0.25t_{CCLK} - 1 + H$		ns
t_{DARL}	Address, $\overline{CIF}$, Selects to $\overline{RDx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{RW}	$\overline{RDx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{RWR}	$\overline{RDx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is t_{CK}–$0.25t_{CCLK}$–11+W ns, maximum.
[4] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high.
[5] For ADSP-21160M, specification is $0.75t_{CK}$–11+W ns, maximum.
[6] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Example System Hold Time Calculation on page 49 for the calculation of hold times given capacitive and dc loads.
[7] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.

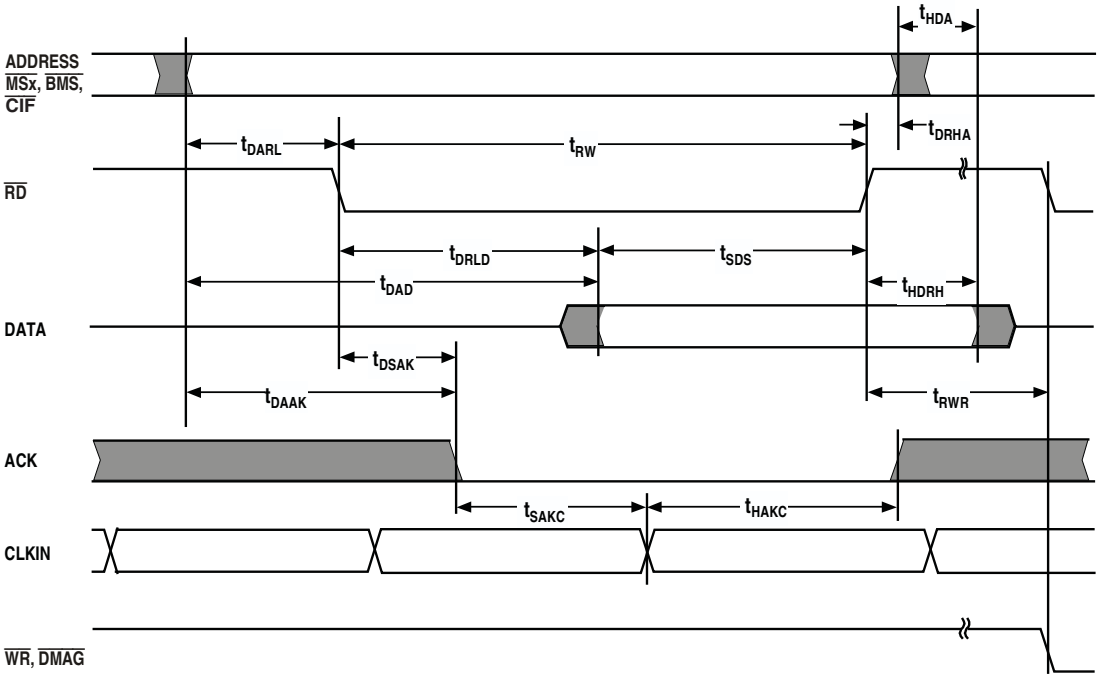


Figure 15. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 1 of Table 19. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 19. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{WRx}$ Low[1]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[1]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Deasserted[2]	$t_{CK} - 0.25t_{CCLK} - 3 + W$		ns
t_{DAWL}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{WW}	$\overline{WRx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DDWH}	Data Setup before $\overline{WRx}$ High[3]	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DWHA}	Address Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DWHD}	Data Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DATRWH}	Data Disable after $\overline{WRx}$ Deasserted[4]	$0.25t_{CCLK} - 2 + H$	$0.25t_{CCLK} + 2 + H$	ns
t_{WWR}	$\overline{WRx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns
t_{DDWR}	Data Disable before $\overline{WRx}$ or $\overline{RDx}$ Low	$0.25t_{CCLK} - 1 + I$		ns
t_{WDE}	$\overline{WRx}$ Low to Data Enabled	$-0.25t_{CCLK} - 1$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK} or t_{DSAK} or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is $t_{CK} - 0.25t_{CCLK} - 12.5 + W$ ns, minimum.
[4] See Example System Hold Time Calculation on Page 49 for calculation of hold times given capacitive and dc loads.

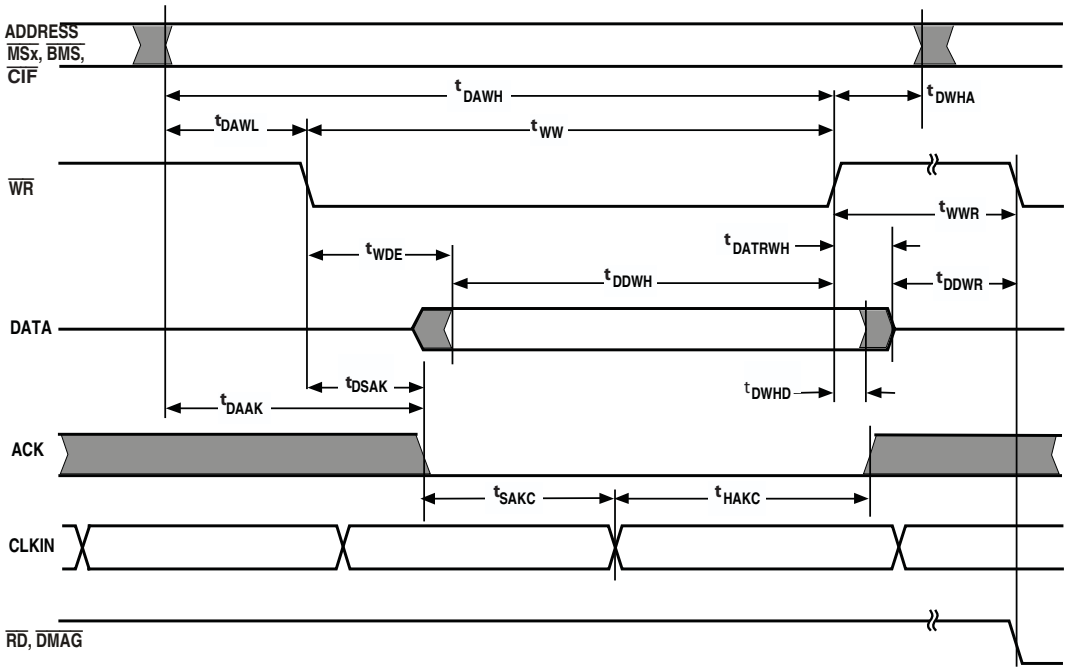


Figure 16. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

See Table 20 and Figure 17. Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-21160x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read–Bus Master on page 26 and Memory Write–Bus Master on page 28).

When accessing a slave ADSP-21160x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write–Bus Slave on page 32). The slave ADSP-21160x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 20. Synchronous Read/Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
t_{SACKC}	ACK Setup Before CLKIN	$0.5t_{CCLK}+3$		ns
t_{HACKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, $\overline{CIF}$ Delay After CLKIN		10	ns
t_{HADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, $\overline{CIF}$ Hold After CLKIN	1.5		ns
t_{DPGO}	PAGE Delay After CLKIN	1.5	11	ns
t_{DRDO}	$\overline{RDx}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DWRO}	$\overline{WRx}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DRWL}	$\overline{RDx}$/$\overline{WRx}$ Low Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DDATO}	Data Delay After CLKIN[1]		$0.25t_{CCLK}+9$	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns
t_{DACKMO}	ACK Delay After CLKIN[2, 3]	3	9	ns
t_{ACKMTR}	ACK Disable Before CLKIN[2]	−3		ns
t_{DCKOO}	CLKOUT Delay After CLKIN[4]	0.5	5	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	t_{CK}[5] $+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CK}/2-2$	$t_{CK}/2+2$[2]	ns
t_{CKWL}	CLKOUT Width Low	$t_{CK}/2-2$	$t_{CK}/2+2$[2]	ns

[1] For ADSP-21160M, specification is 12.5 ns, maximum.
[2] Applies to broadcast write, master precharge of ACK.
[3] For ADSP-21160M, specification is $0.25t_{CCLK}+3$ ns (minimum) and $.25t_{CCLK}+9$ ns (maximum).
[4] For ADSP-21160M, specification is 2 ns, minimum.
[5] Applies only when the DSP drives a bus operation; CLKOUT held inactive or three-state otherwise. For more information, see the System Design chapter in the *ADSP-21160 SHARC DSP Hardware Reference*.

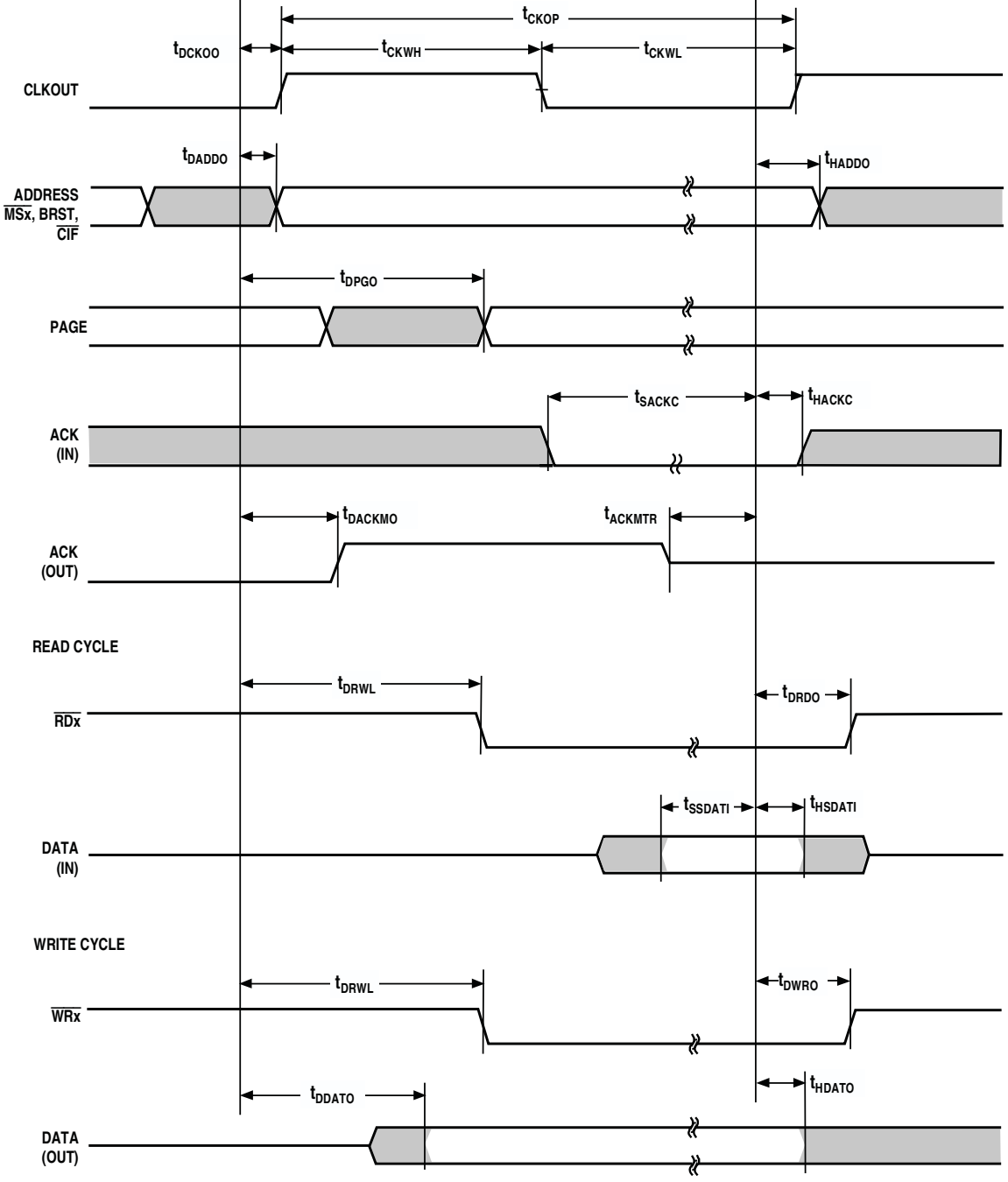


Figure 17. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

See Table 21 and Figure 18. Use these specifications for ADSP-21160x bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Table 21. Synchronous Read/Write—Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADDI}	Address, BRST Setup Before CLKIN	5		ns
t_{HADDI}	Address, BRST Hold After CLKIN	1		ns
t_{SRWI}	$\overline{RDx}$/$\overline{WRx}$ Setup Before CLKIN	5		ns
t_{HRWI}	$\overline{RDx}$/$\overline{WRx}$ Hold After CLKIN	1		ns
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
Switching Characteristics				
t_{DDATO}	Data Delay After CLKIN[1]		0.25 t_{CCLK} + 9	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns
t_{DACKC}	ACK Delay After CLKIN		10	ns
t_{HACKO}	ACK Hold After CLKIN	1.5		ns

[1] For ADSP-21160M, specification is 12.5 ns, maximum.

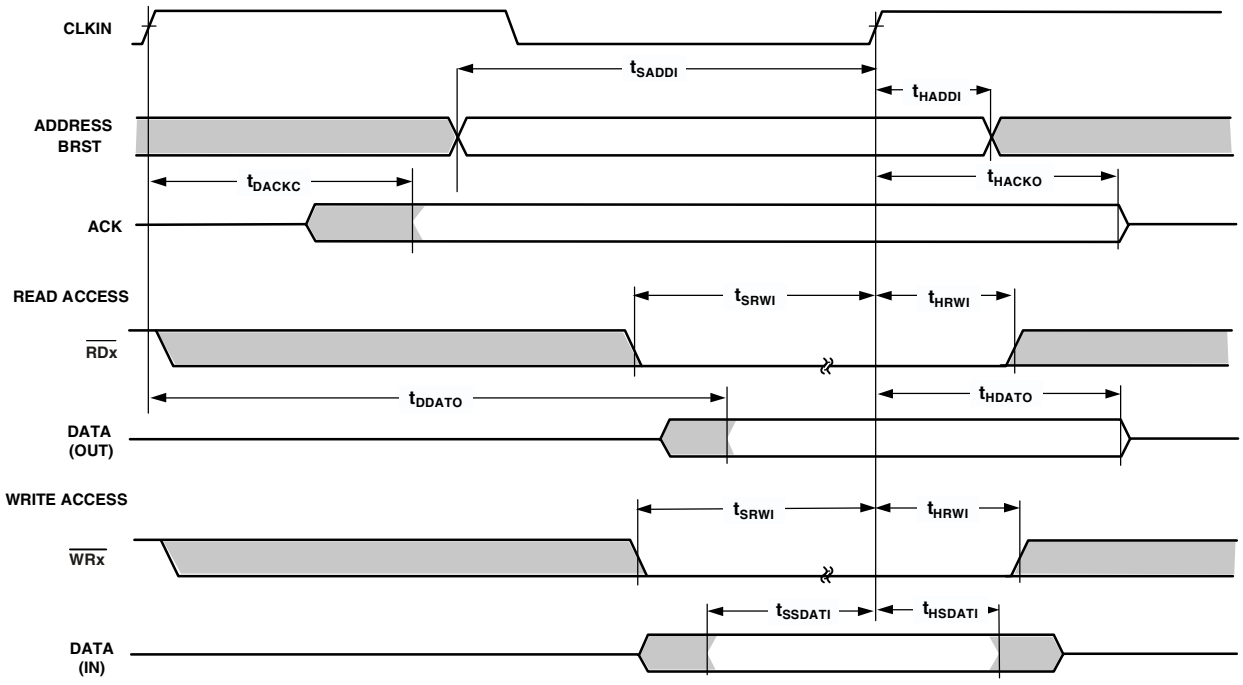


Figure 18. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request

See Table 22 and Figure 19. Use these specifications for passing of bus mastership between multiprocessing ADSP-21160x DSPs ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 22. Multiprocessor Bus Request and Host Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RDx}$/$\overline{WRx}$/$\overline{CS}$ Valid[1]		$6.5 + t_{CK} + t_{CCLK} - 12.5CR$	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	6		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]	1		ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High	1		ns
t_{SBRI}	$\overline{BRx}$, $\overline{PA}$ Setup Before CLKIN	9		ns
t_{HBRI}	$\overline{BRx}$, $\overline{PA}$ Hold After CLKIN High	1		ns
t_{SRPBAI}	RPBA Setup Before CLKIN	6		ns
t_{HRPBAI}	RPBA Hold After CLKIN	2		ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN[3]	1.5		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	1.5		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKIN, Slave		8	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKIN, Slave	1.5		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKIN, Master		$0.25t_{CCLK}+9$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKIN, Master[4]	$0.25t_{CCLK} - 5.5$		ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		$0.5t_{CK}+1.0$	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[5, 7]	$t_{CK}+15$		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[5]		11	ns

[1] For ADSP-21160M, specification is 19 ns, maximum.
[2] Only required for recognition in the current cycle.
[3] For ADSP-21160M, specification is 2 ns, maximum.
[4] For ADSP-21160M, specification is $0.25t_{CK}-5$ ns, minimum.
[5] (O/D) = open drain, (A/D) = active drive.
[6] For ADSP-21160M, specification is $0.5t_{CK}$ ns, maximum.
[7] For ADSP-21160M, specification is $t_{CK}+25$ ns, maximum.

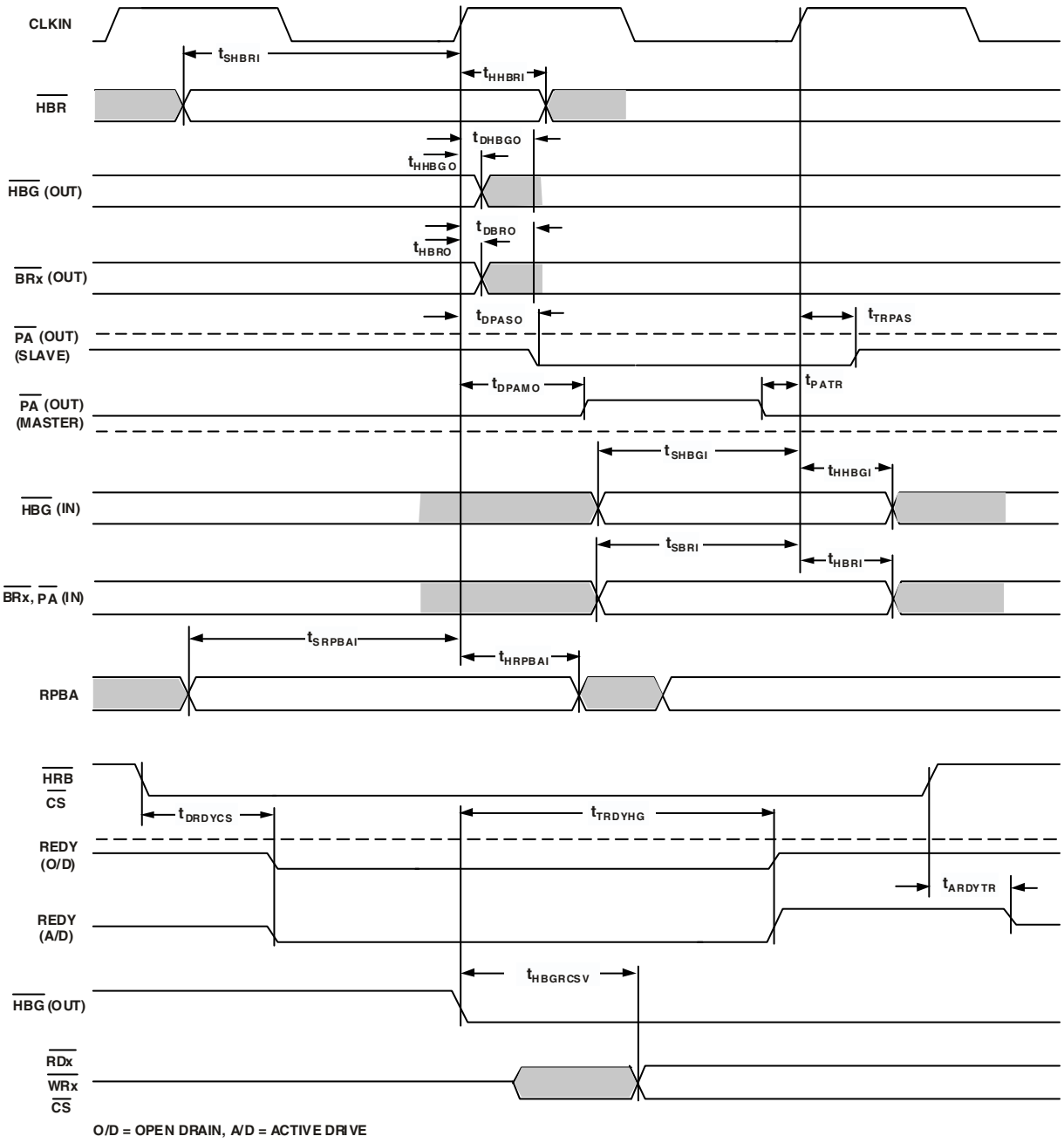


Figure 19. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-21160x

Use these specifications (Table 23, Table 24, Figure 20, and Figure 21) for asynchronous host processor accesses of an ADSP-21160x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21160x, the host can drive the $\overline{RDx}$ and $\overline{WRx}$ pins to access the ADSP-21160x DSP's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 23. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RDx}$ Low	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RDx}$	2		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RDx}$ Low[1]		11	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read[2]	t_{CK} – 4		ns
t_{HDARWH}	Data Disable After $\overline{RDx}$ High[3]	1.5	6	ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is t_{CK} ns, minimum.
[3] For ADSP-21160M, specification is 2 ns, minimum.

Table 24. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WRx}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WRx}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WRx}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WRx}$ High	2		ns
t_{WWRL}	$\overline{WRx}$ Low Width[1]	t_{CCLK}+1		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DWRHRDY}$	$\overline{WRx}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WRx}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WRx}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WRx}$/$\overline{CS}$ Low		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[2]	5.75 + 0.5t_{CCLK}		ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is 12 ns, minimum.

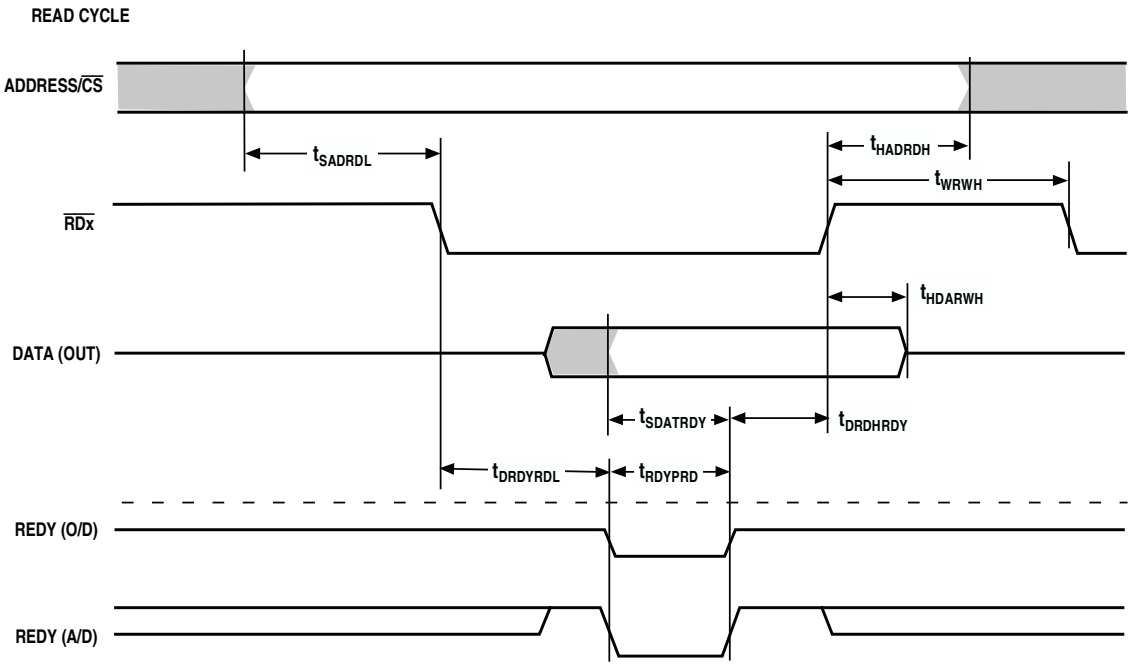


Figure 20. Asynchronous Read—Host to ADSP-21160x

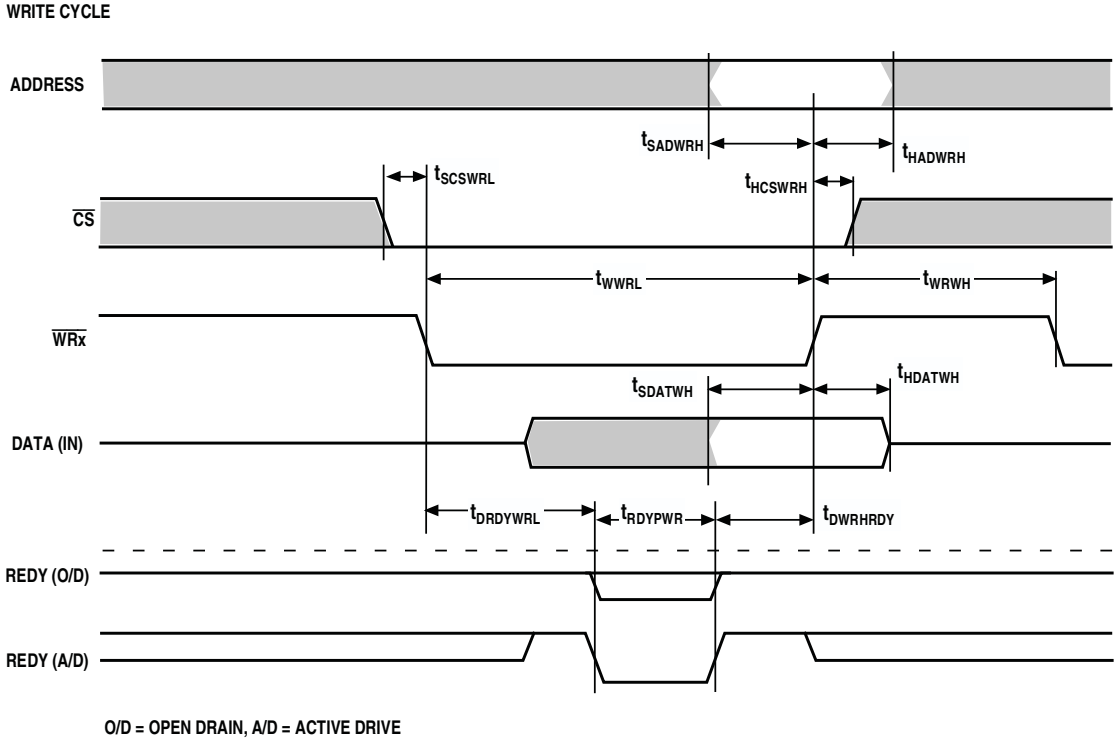


Figure 21. Asynchronous Write—Host to ADSP-21160x

Three-State Timing—Bus Master, Bus Slave

See Table 25 and Figure 22. These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Table 25. Three-State Timing—Bus Master, Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	6		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold After CLKIN[1]	2		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN	1.5	9	ns
t_{MIENS}	Strobes Enable After CLKIN[2]	1.5	9	ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	1.5	9	ns
t_{MITRA}	Address/Select Disable After CLKIN[3]	0.5	9	ns
t_{MITRS}	Strobes Disable After CLKIN[2, 4, 5]	$0.25t_{CCLK} - 4$	$0.25t_{CCLK}+1.5$	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN[6]	0.5	8	ns
t_{DATEN}	Data Enable After CLKIN[7, 8]	$0.25t_{CCLK} + 1$	$0.25t_{CCLK} + 7$	ns
t_{DATTR}	Data Disable After CLKIN[7, 9]	0.5	5	ns
t_{ACKEN}	ACK Enable After CLKIN[7]	1.5	9	ns
t_{ACKTR}	ACK Disable After CLKIN[7]	1.5	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN[10]	0.5	9	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	$t_{CCLK} - 3$	$t_{CCLK}+1$	ns
t_{ATRHBG}	Address, $\overline{\text{MSx}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$1.5t_{CK} - 6$	$1.5t_{CK} + 5$	ns
t_{STRHBG}	$\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{DMAGx}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$t_{CK} + 0.25t_{CCLK} - 6$	$t_{CK} + 0.25t_{CCLK} + 5$	ns
t_{PTRHBG}	Page Disable Before $\overline{\text{HBG}}$ Low[11]	$t_{CK} - 6$	$t_{CK} + 5$	ns
t_{BTRHBG}	$\overline{\text{BMS}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$0.5t_{CK} - 6.5$	$0.5t_{CK} + 1.5$	ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[12, 13]	$t_{CK} - 5$	$t_{CK}+6$	ns

[1] For ADSP-21160M, specification is 1 ns, minimum.
[2] Strobes = $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, and $\overline{\text{DMAGx}}$.
[3] For ADSP-21160M, specification is $0.25t_{CCLK}$–1 ns (minimum) and $0.25t_{CCLK}$+4 ns (maximum).
[4] If access aborted by $\overline{\text{SBTS}}$, then strobes disable *before* CLKIN [$0.25t_{CCLK}$ + 1.5 (min.), $0.25t_{CCLK}$ + 5 (max.)]
[5] For ADSP-21160M, specification is $0.25t_{CCLK}$ ns (maximum).
[6] For ADSP-21160M, specification is 3.5 ns (minimum).
[7] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[8] For ADSP-21160M, specification is 1.5 ns (minimum) and 10 ns (maximum).
[9] For ADSP-21160M, specification is 1.5 ns (minimum).
[10] For ADSP-21160M, specification is 0.5 ns (minimum).
[11] Not specified for ADSP-21160M.
[12] Memory Interface = Address, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MSx}}$, PAGE, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode).
[13] For ADSP-21160M, specification is t_{CK}+5 ns (maximum).

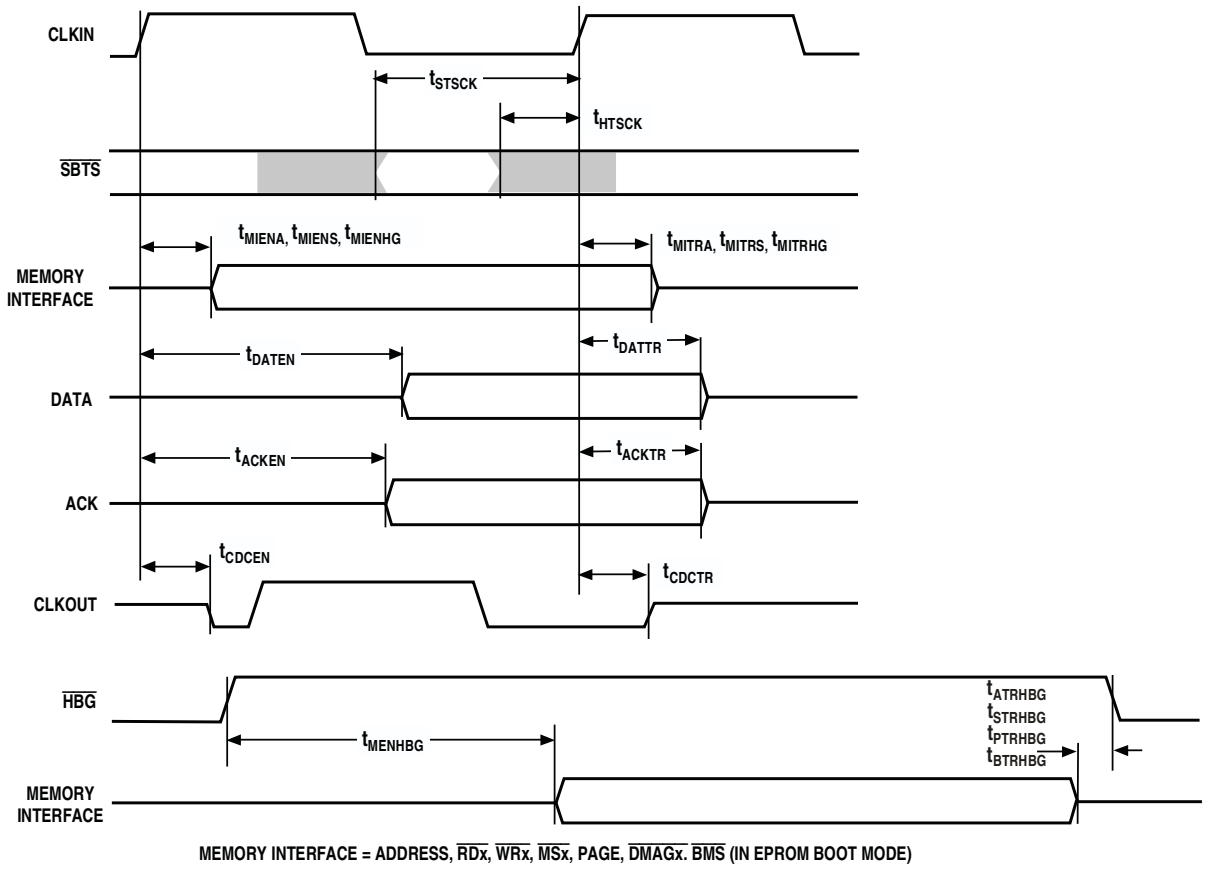


Figure 22. Three-State Timing—Bus Master, Bus Slave

DMA Handshake

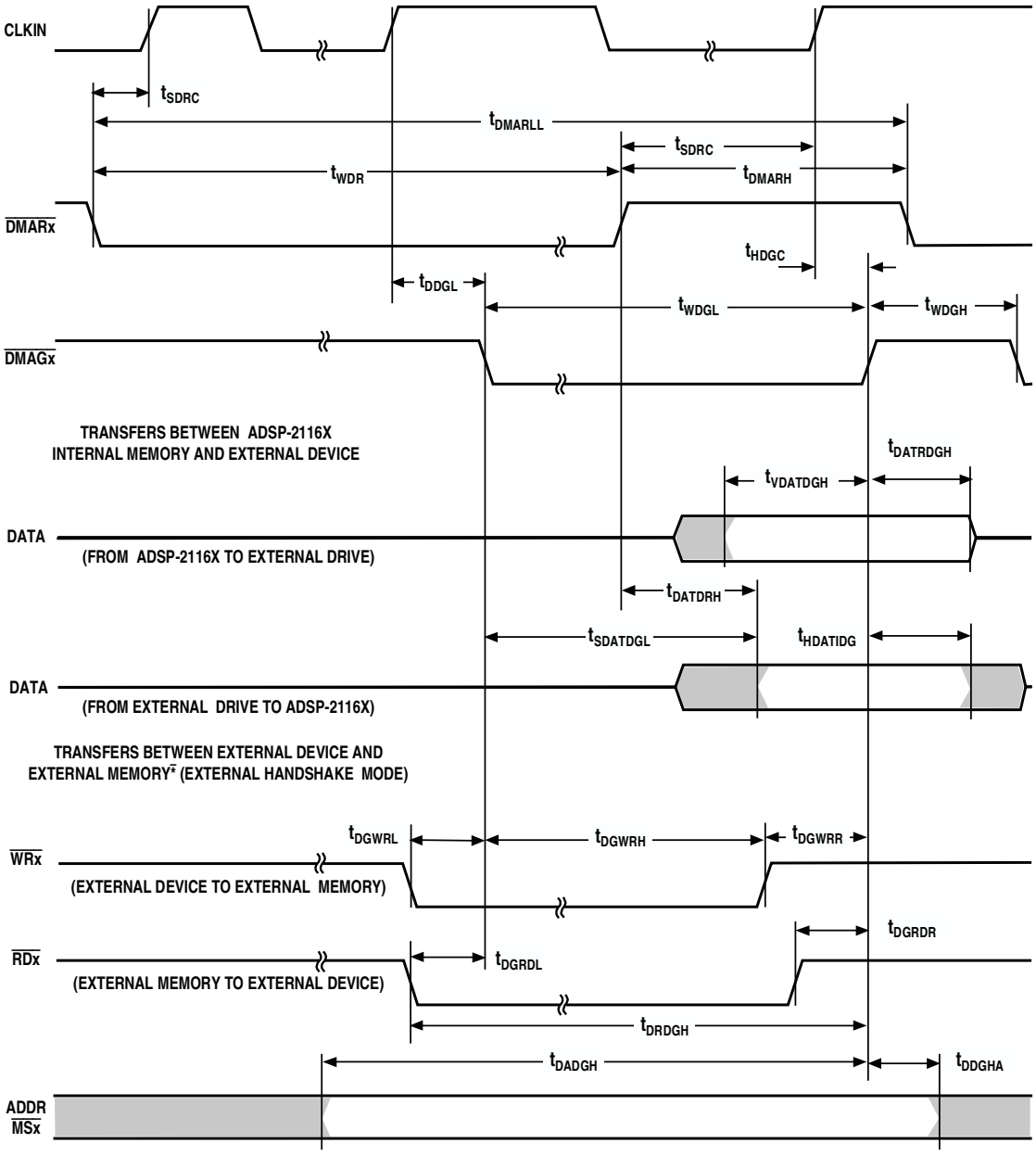
See Table 26 and Figure 23. These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAGx}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MS3–0}}$, PAGE, DATA63–0, and ACK also apply.

Table 26. DMA Handshake

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDRC}	$\overline{\text{DMARx}}$ Setup Before CLKIN[1]	3		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)[2, 3]	$0.5t_{CCLK}+2.5$		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[4, 5]		$t_{CK}-0.5t_{CCLK}-7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[4, 6]		$t_{CK}+3$	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[7]	t_{CK}		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High[2, 8]	$0.5t_{CCLK}+1$		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	$0.5t_{CCLK}-1+\text{HI}$		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	$t_{CK}-0.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	$t_{CK}-0.25t_{CCLK}+1.5$	$t_{CK}-0.25t_{CCLK}+9$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[9]	$t_{CK}-0.25t_{CCLK}-8$	$t_{CK}-0.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[10]	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+1.5$	ns
t_{DGWRL}	$\overline{\text{WRx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WRx}}$ High	$t_{CK}-0.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{\text{WRx}}$ High Before $\overline{\text{DMAGx}}$ High[11]	–1.5	2	ns
t_{DGRDL}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	2	ns
t_{DRDGH}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ High	$t_{CK}-0.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{\text{RDx}}$ High Before $\overline{\text{DMAGx}}$ High[11]	–1.5	2	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WRx}}$, $\overline{\text{RDx}}$, $\overline{\text{DMAGx}}$ Low	$0.5t_{CCLK}-2+\text{HI}$		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High[12]	15.5		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High	1		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] Maximum throughput using $\overline{\text{DMARx}}$ / $\overline{\text{DMAGx}}$ handshaking equals $t_{WDR} + t_{DMARH} = (0.5t_{CCLK}+1) + (0.5t_{CCLK}+1) = 10.0$ ns (100 MHz). This throughput limit applies to non-synchronous access mode only.
[3] For ADSP-21160M, specification is t_{CCLK}+4.5 ns, minimum.
[4] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[5] For ADSP-21160M, specification is $0.75t_{CCLK}$–7 ns, maximum.
[6] For ADSP-21160M, specification is t_{CLK}+10 ns, maximum.
[7] Use t_{DMARLL} if $\overline{\text{DMARx}}$ transitions synchronous with CLKIN. Otherwise, use t_{WDR} and t_{DMARH}.
[8] For ADSP-21160M, specification is t_{CCLK}+4.5 ns, minimum.
[9] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - 0.25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[10] See Example System Hold Time Calculation on page 49 for calculation of hold times given capacitive and dc loads.
[11] This parameter applies for synchronous access mode only.
[12] For ADSP-21160M, specification is 18 ns, minimum.



* MEMORY READ BUS MASTER, MEMORY WRITE BUS MASTER, OR SYNCHRONOUS READ/WRITE BUS MASTER TIMING SPECIFICATIONS FOR ADDR31–0, RDx, WRx, MS3–0 AND ACK ALSO APPLY HERE.

Figure 23. DMA Handshake

Link Ports—Receive, Transmit

For link ports, see Table 27, Table 28, Figure 24, and Figure 25. Calculation of link receiver data setup and hold, relative to link clock, is required to determine the maximum allowable skew that can be introduced in the transmission path, between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA, relative to LCLK (setup skew = $t_{LCLKTWH}$ minimum – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK, relative to LDATA (hold skew = $t_{LCLKTWL}$ minimum + t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications result in unrealistically small skew times, because they include multiple tester guardbands.

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 27. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	2.5		ns
t_{HLDCL}	Data Hold After LCLK Low[1]	3		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low[2]	4		ns
$t_{LCLKRWH}$	LCLK Width High[3]	4		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[4, 5]	9	17	ns

[1] For ADSP-21160M, specification is 2.5 ns, minimum.
[2] For ADSP-21160M, specification is 6 ns, minimum.
[3] For ADSP-21160M, specification is 6 ns, minimum.
[4] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[5] For ADSP-21160M, specification is 12 ns, minimum.

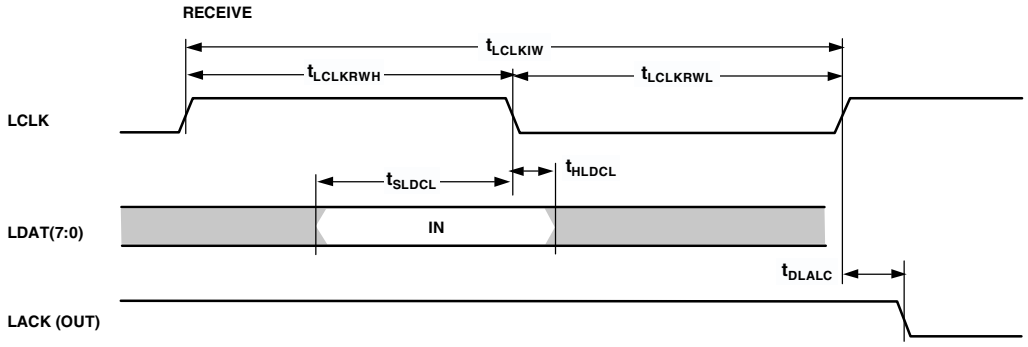


Figure 24. Link Ports—Receive

Table 28. Link Ports—Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	14		ns
t_{HLACH}	LACK Hold After LCLK High	–2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		4	ns
t_{HLDCH}	Data Hold After LCLK High	–2		ns
$t_{LCLKTWL}$	LCLK Width Low[1]	$0.5t_{LCLK} - 0.5$	$0.5t_{LCLK} + 0.5$	ns
$t_{LCLKTWH}$	LCLK Width High[2]	$0.5t_{LCLK} - 0.5$	$0.5t_{LCLK} + 0.5$	ns
t_{DLACLK}	LCLK Low Delay After LACK High[3]	$0.5t_{LCLK} + 4$	$3/2t_{LCLK} + 11$	ns

[1] For ADSP-21160M, specification is $0.5t_{LCLK}$–1.5 ns (minimum) and $0.5t_{LCLK}$+1.5 ns (maximum).
[2] For ADSP-21160M, specification is $0.5t_{LCLK}$–1.5 ns (minimum) and $0.5t_{LCLK}$+1.5 ns (maximum).
[3] For ADSP-21160M, specification is $0.5t_{LCLK}$+5 ns (minimum) and $3t_{LCLK}$+11 ns (maximum).

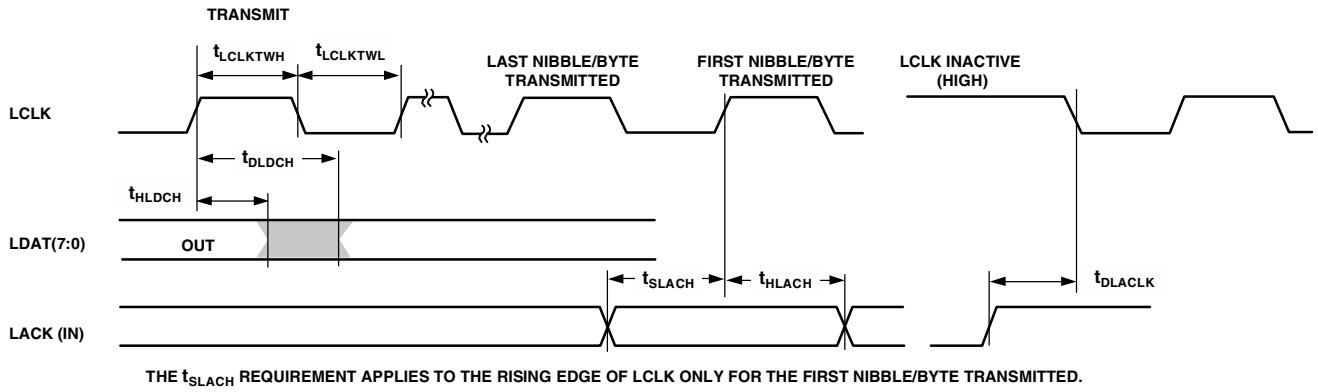


Figure 25. Link Ports—Transmit

Serial Ports

For serial ports, see Table 29, Table 30, Table 31, Table 32, Table 33, Table 34, Table 35, Figure 26, and Figure 27. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 29. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1, 2]	6.5		ns
t_{SCLKW}	TCLK/RCLK Width[3]	8		ns
t_{SCLK}	TCLK/RCLK Period	$2t_{CCLK}$		ns

[1] Referenced to sample edge.
[2] For ADSP-21160M, specification is 4 ns, minimum.
[3] For ADSP-21160M, specification is 14 ns, minimum.

Table 30. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	$t_{CCLK}/2 + 1$		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	6.5		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] For ADSP-21160M, specification is 1 ns, minimum.

Table 31. Serial Ports—External or Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 32. Serial Ports—External Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HDTE}	Transmit Data Hold After TCLK[1]	0		ns

[1] Referenced to drive edge.

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns

[1] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –1.5	$0.5t_{SCLK}$+1.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21160M, specification is $0.5t_{SCLK}$–2.5 ns (minimum) and $0.5t_{SCLK}$+2 ns (maximum)

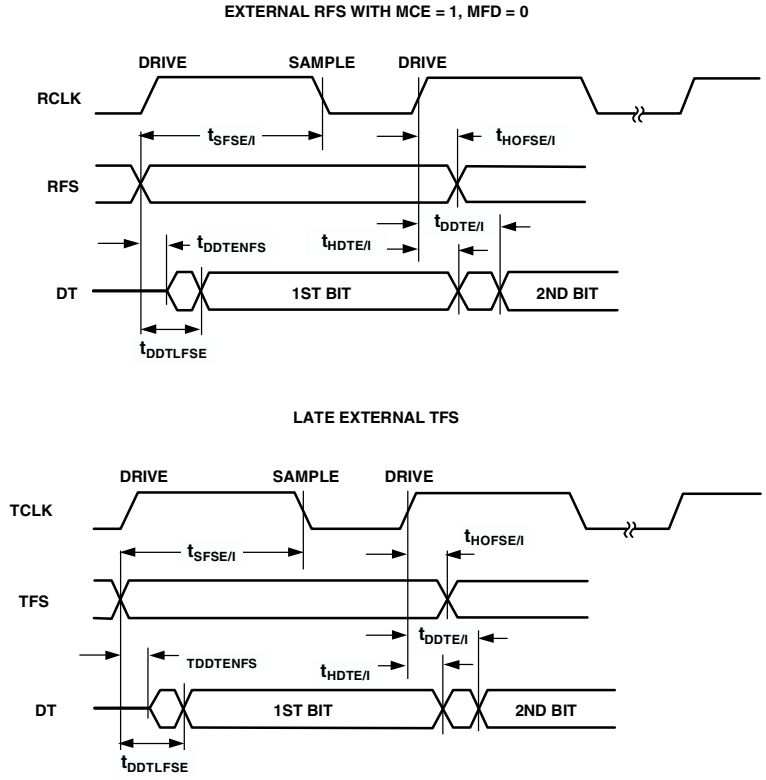


Figure 26. Serial Ports—External Late Frame Sync

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	1.0		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

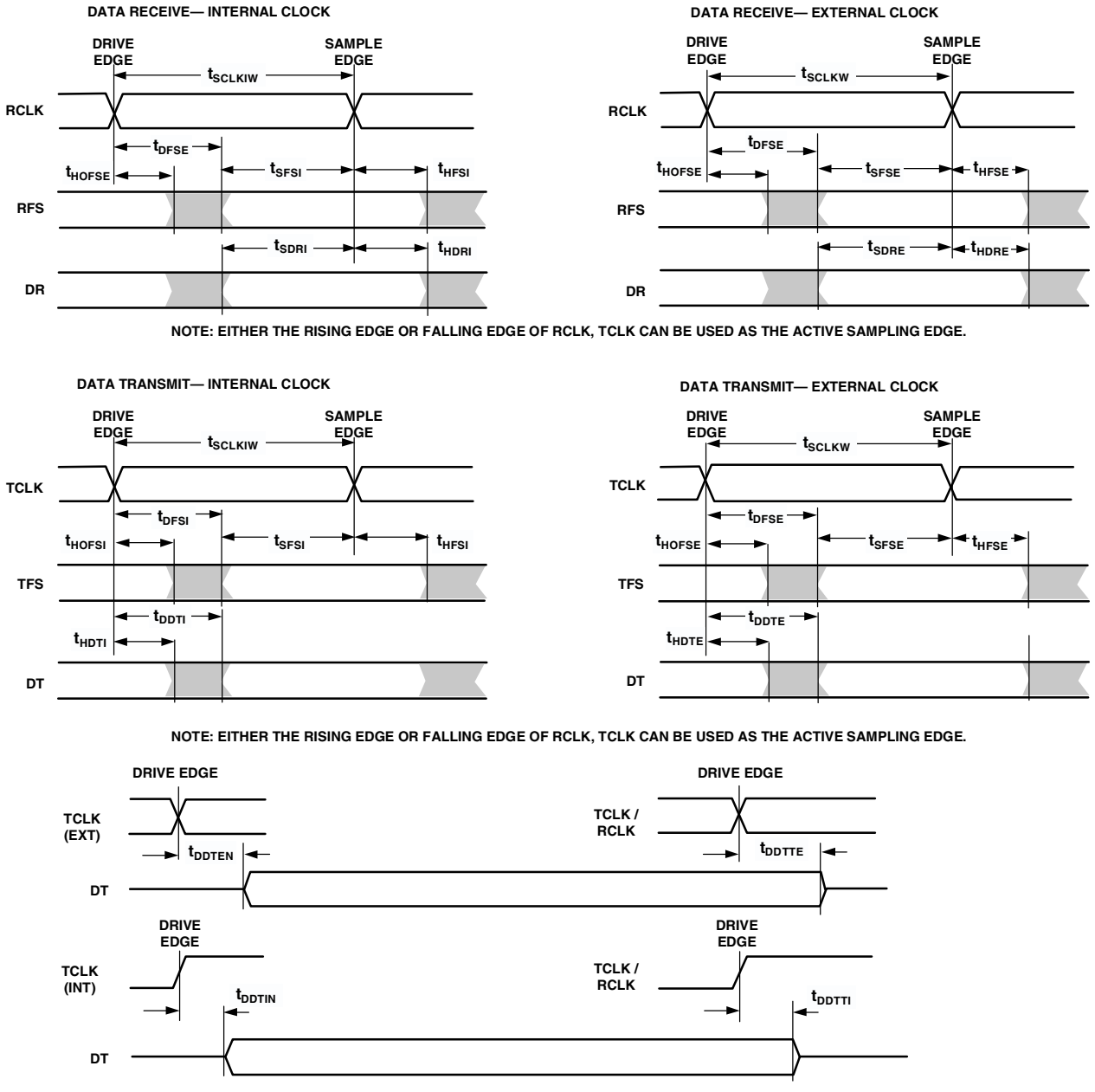


Figure 27. Serial Ports

JTAG Test Access Port and Emulation

For JTAG Test Access Port and emulation, see Table 36 and Figure 28.

Table 36. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulsewidth	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = DATA63–0, ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, ACK, $\overline{\text{SBTS}}$, $\overline{\text{HBR}}$, $\overline{\text{HBG}}$, $\overline{\text{CS}}$, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{BR6–1}}$, ID2–0, RPBA, $\overline{\text{IRQ2–0}}$, FLAG3–0, $\overline{\text{PA}}$, BRST, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{\text{BMS}}$, CLKIN, and $\overline{\text{RESET}}$.

[2] System Outputs = DATA63–0, ADDR31–0, $\overline{\text{MS3–0}}$, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, ACK, PAGE, CLKOUT, $\overline{\text{HBG}}$, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BR6–1}}$, $\overline{\text{PA}}$, BRST, $\overline{\text{CIF}}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, and $\overline{\text{BMS}}$.

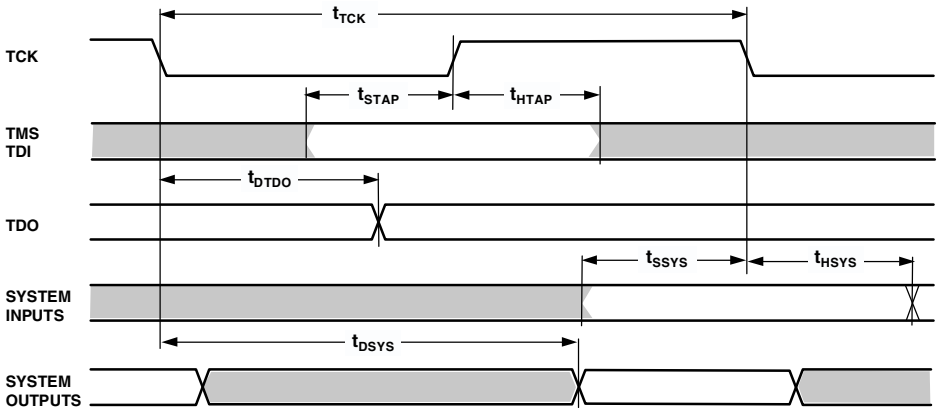


Figure 28. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENTS—ADSP-21160M

Figure 29 shows typical I–V characteristics for the output drivers of the ADSP-21160M. The curves represent the current drive capability of the output drivers as a function of output voltage.

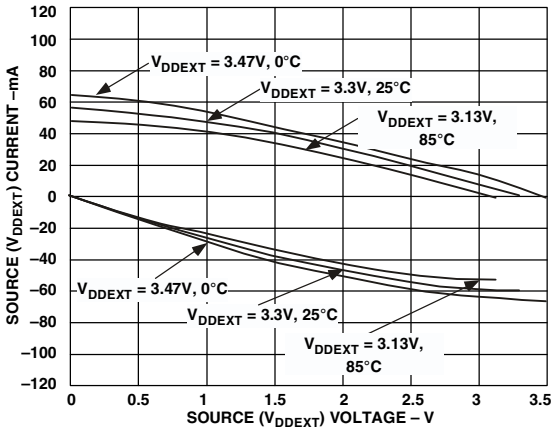


Figure 29. ADSP-21160M Typical Drive Currents

OUTPUT DRIVE CURRENTS—ADSP-21160N

Figure 30 shows typical I–V characteristics for the output drivers of the ADSP-21160N. The curves represent the current drive capability of the output drivers as a function of output voltage.

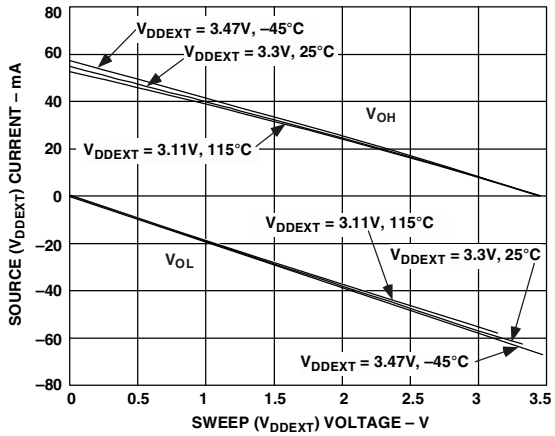


Figure 30. ADSP-21160N Typical Drive Currents

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DD\text{-}INPEAK}$, $I_{DD\text{-}INHIGH}$, $I_{DD\text{-}INLOW}$, and $I_{DD\text{-}IDLE}$) from Electrical Characteristics—ADSP-21160M on Page 16 and Electrical Characteristics—ADSP-21160N on Page 18 and the current-versus-operation information in Table 37, engineers can estimate the ADSP-21160x DSP's internal power supply (V_{DDINT}) input current for a specific application, according to the formula:

$$\begin{aligned} &\%\ \text{Peak} \times I_{DD\text{-}INPEAK} \\ &\%\ \text{High} \times I_{DD\text{-}INHIGH} \\ &\%\ \text{Low} \times I_{DD\text{-}INLOW} \\ +\ &\%\ \text{Peak} \times I_{DD\text{-}IDLE} \\ &= I_{DDINT} \end{aligned}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle (*O*)
- The maximum frequency at which they can switch (*f*)
- Their load capacitance (*C*)
- Their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example for ADSP-21160N: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory—asynchronous RAM (64-bit)
- Four 64K × 16 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(2\ t_{CK})$, with 50% of the pins switching
- The bus cycle time is 50 MHz (t_{CK} = 20 ns).

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 38.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

where:

- P_{EXT} is from Table 38
- P_{INT} is $I_{DDINT} \times 1.9$ V, using the calculation I_{DDINT} listed in Power Dissipation on page 47
- P_{PLL} is $AI_{DD} \times 1.9$ V, using the value for AI_{DD} listed in Electrical Characteristics—ADSP-21160M on Page 16 and Electrical Characteristics—ADSP-21160N on Page 18

Table 37. ADSP-21160x Operation Types vs. Input Current

Operation	Peak Activity[1]	High Activity[1]	Low Activity[1]
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access[2]	2 per t_{CK} Cycle (DM 3 64 and PM 3 64)	1 per t_{CK} Cycle (DM 3 64)	None
Internal Memory DMA	1 per 2 t_{CCLK} Cycles	1 per 2 t_{CCLK} Cycles	None
External Memory DMA	1 per External Port Cycle (364)	1 per External Port Cycle (3 64)	None
Data Bit Pattern for Core Memory Access and DMA	Worst Case	Random	N/A

[1] Peak activity = $I_{DD\text{-}INPEAK}$, high activity = $I_{DD\text{-}INHIGH}$, and low activity = $I_{DD\text{-}INLOW}$. The state of the PEYEN bit (SIMD versus SISD mode) does not influence these calculations.
[2] These assume a 2:1 core clock ratio. For more information on ratios and clocks (t_{CK} and t_{CCLK}), see the timing ratio definitions on page 20.

Table 38. External Power Calculations (ADSP-21160N Example)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 24 MHz	× 10.9 V	= 0.088 W
$\overline{MS0}$	1	0	× 44.7 pF	× 24 MHz	× 10.9 V	= 0.000 W
$\overline{WRx}$	2		× 44.7 pF	× 24 MHz	× 10.9 V	= 0.023 W
Data	64	50	× 14.7 pF	× 24 MHz	× 10.9 V	= 0.123 W
CLKOUT	1		× 4.7 pF	× 48 MHz	× 10.9 V	= 0.003 W
				P_{EXT}		= 0.237 W

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

The test conditions for timing parameters appearing in ADSP-21160x specifications on page 17 include output disable time, output enable time, and capacitive loading.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 31. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

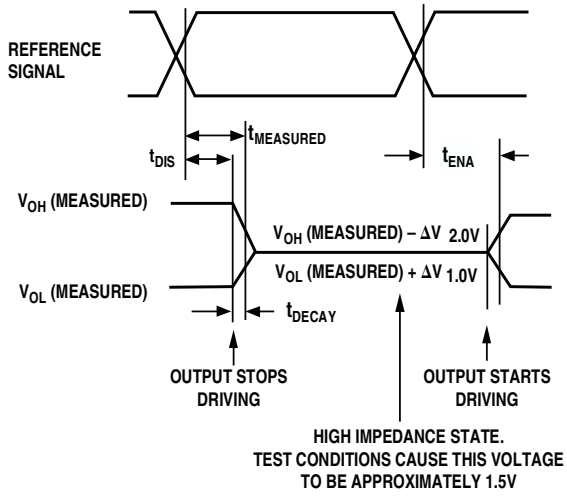


Figure 31. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 31). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21160x DSP's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

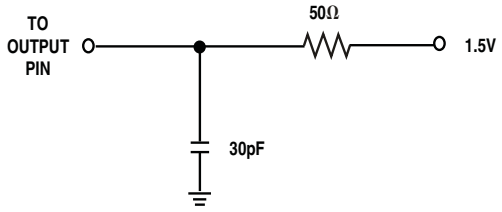


Figure 32. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

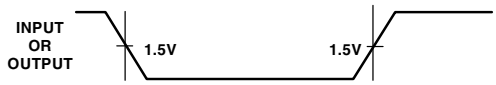


Figure 33. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 32). Figure 34, Figure 35, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 36 and Figure 39 graphically show how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 48.) The graphs of Figure 34 through Figure 39 may not be linear outside the ranges shown.

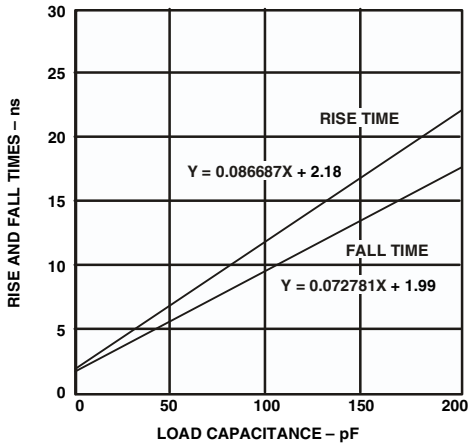


Figure 34. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Max) vs. Load Capacitance

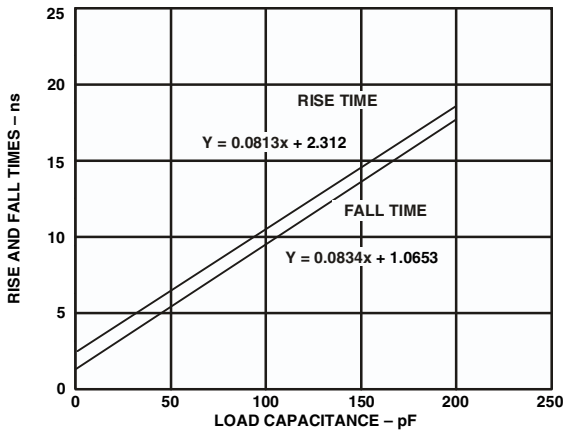


Figure 35. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Min) vs. Load Capacitance

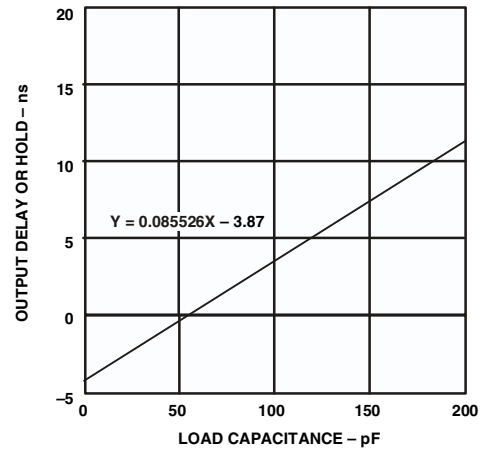


Figure 36. ADSP-21160M Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

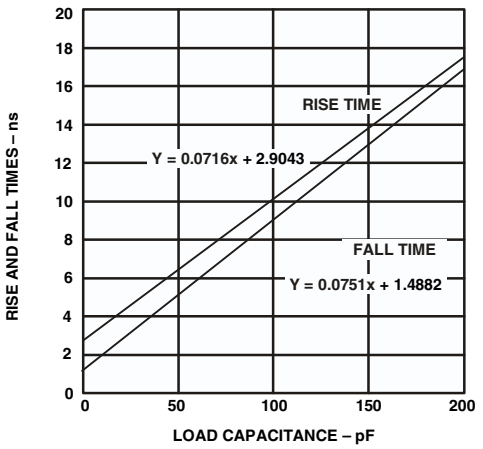


Figure 37. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Max) vs. Load Capacitance

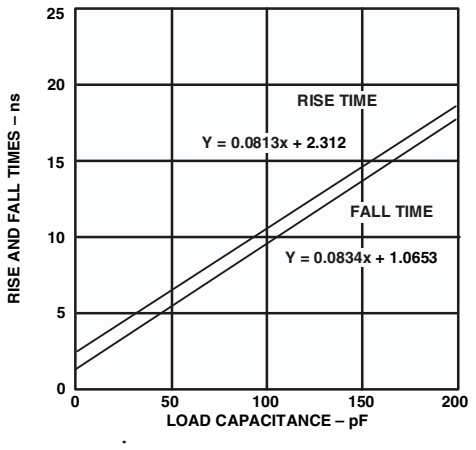


Figure 38. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Min) vs. Load Capacitance

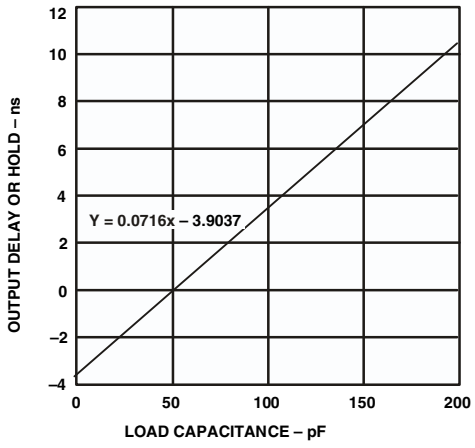


Figure 39. ADSP-21160N Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21160x DSPs are provided in a 400-Ball PBGA (Plastic Ball Grid Array) package.

The ADSP-21160x is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the centerblock of ground pins (for ADSP-21160M, PBGA balls: H8-13, J8-13, K8-13, L8-13, M8-13, N8-13; for ADSP-21160N, PBGA balls: F7-14, G7-14, H7-14, J7-14, K7-14, L7-14, M-14, N7-14, P7-14, R7-15) to provide thermal pathways to the printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

- T_{CASE} = Case temperature (measured on top surface of package)
- T_{AMB} = Ambient temperature °C
- PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
- θ_{CA} = Value from Table 39.
- θ_{JB} = 6.46°C/W

Table 39. Airflow Over Package Versus θ_{CA}

Airflow (Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)[1]	12.13	9.86	8.7

[1] θ_{JC} = 3.6 °C/W

400-BALL PBGA PIN CONFIGURATIONS

Table 40 lists the pin assignments for the PBGA package, and the pin configurations diagram in Figure 40 (ADSP-21160M) and Figure 41 (ADSP-21160N) show the pin assignment summary.

Table 40. 400-Ball PBGA Pin Assignments

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[14]	A01	DATA[22]	B01	DATA[24]	C01	DATA[28]	D01
DATA[13]	A02	DATA[16]	B02	DATA[18]	C02	DATA[25]	D02
DATA[10]	A03	DATA[15]	B03	DATA[17]	C03	DATA[20]	D03
DATA[8]	A04	DATA[9]	B04	DATA[11]	C04	DATA[19]	D04
DATA[4]	A05	DATA[6]	B05	DATA[7]	C05	DATA[12]	D05
DATA[2]	A06	DATA[3]	B06	DATA[5]	C06	V_{DDEXT}	D06
TDI	A07	DATA[0]	B07	DATA[1]	C07	V_{DDINT}	D07
$\overline{TRST}$	A08	TCK	B08	TMS	C08	V_{DDEXT}	D08
$\overline{RESET}$	A09	$\overline{EMU}$	B09	TD0	C09	V_{DDEXT}	D09
RPBA	A10	$\overline{IRQ2}$	B10	$\overline{IRQ1}$	C10	V_{DDEXT}	D10
$\overline{IRQ0}$	A11	FLAG3	B11	FLAG2	C11	V_{DDEXT}	D11
FLAG1	A12	FLAG0	B12	NC[1]	C12	V_{DDEXT}	D12
TIMEXP	A13	NC[1]	B13	NC	C13	V_{DDINT}	D13
NC[1]	A14	NC	B14	TCLK1	C14	V_{DDEXT}	D14
NC	A15	DT1	B15	DR1	C15	TFS0	D15
TFS1	A16	RCLK1	B16	DR0	C16	L1DAT[7]	D16
RFS1	A17	RFS0	B17	L0DAT[7]	C17	L0CLK	D17
RCLK0	A18	TCLK0	B18	L0DAT[6]	C18	L0DAT[3]	D18
DT0	A19	L0DAT[5]	B19	L0ACK	C19	L0DAT[1]	D19
L0DAT[4]	A20	L0DAT[2]	B20	L0DAT[0]	C20	L1CLK	D20
DATA[30]	E01	DATA[34]	F01	DATA[38]	G01	DATA[40]	H01
DATA[29]	E02	DATA[33]	F02	DATA[35]	G02	DATA[39]	H02
DATA[23]	E03	DATA[27]	F03	DATA[32]	G03	DATA[37]	H03
DATA[21]	E04	DATA[26]	F04	DATA[31]	G04	DATA[36]	H04
V_{DDEXT}	E05	V_{DDEXT}	F05	V_{DDEXT}	G05	V_{DDEXT}	H05
V_{DDINT}	E06	V_{DDINT}	F06	V_{DDINT}	G06	V_{DDINT}	H06
V_{DDINT}	E07	GND	F07	GND	G07	GND	H07
V_{DDINT}	E08	GND	F08	GND	G08	GND	H08
V_{DDINT}	E09	GND	F09	GND	G09	GND	H09
V_{DDINT}	E10	GND	F10	GND	G10	GND	H10
GND	E11	GND	F11	GND	G11	GND	H11
V_{DDINT}	E12	GND	F12	GND	G12	GND	H12
V_{DDINT}	E13	GND	F13	GND	G13	GND	H13
V_{DDINT}	E14	GND	F14	GND	G14	GND	H14
V_{DDINT}	E15	V_{DDINT}	F15	V_{DDINT}	G15	V_{DDINT}	H15
V_{DDEXT}	E16	V_{DDEXT}	F16	V_{DDEXT}	G16	V_{DDEXT}	H16
L1DAT[6]	E17	L1DAT[4]	F17	L1DAT[2]	G17	L2DAT[5]	H17
L1DAT[5]	E18	L1DAT[3]	F18	L2DAT[6]	G18	L2ACK	H18
L1ACK	E19	L1DAT[0]	F19	L2DAT[4]	G19	L2DAT[3]	H19
L1DAT[1]	E20	L2DAT[7]	F20	L2CLK	G20	L2DAT[1]	H20

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[44]	J01	CLK_CFG_0	K01	CLKIN	L01	AV_{DD}	M01
DATA[43]	J02	DATA[46]	K02	CLK_CFG_1	L02	CLK_CFG_3	M02
DATA[42]	J03	DATA[45]	K03	AGND	L03	CLKOUT	M03
DATA[41]	J04	DATA[47]	K04	CLK_CFG_2	L04	NC[2]	M04
V_{DDEXT}	J05	V_{DDEXT}	K05	V_{DDEXT}	L05	V_{DDEXT}	M05
V_{DDINT}	J06	V_{DDINT}	K06	V_{DDINT}	L06	V_{DDINT}	M06
GND	J07	GND	K07	GND	L07	GND	M07
GND	J08	GND	K08	GND	L08	GND	M08
GND	J09	GND	K09	GND	L09	GND	M09
GND	J10	GND	K10	GND	L10	GND	M10
GND	J11	GND	K11	GND	L11	GND	M11
GND	J12	GND	K12	GND	L12	GND	M12
GND	J13	GND	K13	GND	L13	GND	M13
GND	J14	GND	K14	GND	L14	GND	M14
V_{DDINT}	J15	V_{DDINT}	K15	V_{DDINT}	L15	V_{DDINT}	M15
V_{DDEXT}	J16	V_{DDEXT}	K16	V_{DDEXT}	L16	V_{DDEXT}	M16
L2DAT[2]	J17	$\overline{BR6}$	K17	$\overline{BR2}$	L17	PAGE	M17
L2DAT[0]	J18	$\overline{BR5}$	K18	$\overline{BR1}$	L18	$\overline{SBTS}$	M18
$\overline{HBG}$	J19	$\overline{BR4}$	K19	ACK	L19	$\overline{PA}$	M19
$\overline{HBR}$	J20	$\overline{BR3}$	K20	REDY	L20	L3DAT[7]	M20
NC	N01	DATA[49]	P01	DATA[53]	R01	DATA[56]	T01
NC	N02	DATA[50]	P02	DATA[54]	R02	DATA[58]	T02
DATA[48]	N03	DATA[52]	P03	DATA[57]	R03	DATA[59]	T03
DATA[51]	N04	DATA[55]	P04	DATA[60]	R04	DATA[63]	T04
V_{DDEXT}	N05	V_{DDEXT}	P05	V_{DDEXT}	R05	V_{DDEXT}	T05
V_{DDINT}	N06	V_{DDINT}	P06	V_{DDINT}	R06	V_{DDINT}	T06
GND	N07	GND	P07	GND	R07	V_{DDINT}	T07
GND	N08	GND	P08	GND	R08	V_{DDINT}	T08
GND	N09	GND	P09	GND	R09	V_{DDINT}	T09
GND	N10	GND	P10	GND	R10	V_{DDINT}	T10
GND	N11	GND	P11	GND	R11	V_{DDINT}	T11
GND	N12	GND	P12	GND	R12	V_{DDINT}	T12
GND	N13	GND	P13	GND	R13	V_{DDINT}	T13
GND	N14	GND	P14	GND	R14	V_{DDINT}	T14
V_{DDINT}	N15	V_{DDINT}	P15	GND	R15	V_{DDINT}	T15
V_{DDEXT}	N16	V_{DDEXT}	P16	V_{DDEXT}	R16	V_{DDEXT}	T16
L3DAT[5]	N17	L3DAT[2]	P17	L4DAT[5]	R17	L4DAT[3]	T17
L3DAT[6]	N18	L3DAT[1]	P18	L4DAT[6]	R18	L4ACK	T18
L3DAT[4]	N19	L3DAT[3]	P19	L4DAT[7]	R19	L4CLK	T19
L3CLK	N20	L3ACK	P20	L3DAT[0]	R20	L4DAT[4]	T20
DATA[61]	U01	ADDR[4]	V01	ADDR[5]	W01	ADDR[8]	Y01
DATA[62]	U02	ADDR[6]	V02	ADDR[9]	W02	ADDR[11]	Y02
ADDR[3]	U03	ADDR[7]	V03	ADDR[12]	W03	ADDR[13]	Y03
ADDR[2]	U04	ADDR[10]	V04	ADDR[15]	W04	ADDR[16]	Y04
V_{DDEXT}	U05	ADDR[14]	V05	ADDR[17]	W05	ADDR[19]	Y05
V_{DDEXT}	U06	ADDR[18]	V06	ADDR[20]	W06	ADDR[21]	Y06

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
V_{DDEXT}	U07	ADDR[22]	V07	ADDR[23]	W07	ADDR[24]	Y07
V_{DDEXT}	U08	ADDR[25]	V08	ADDR[26]	W08	ADDR[27]	Y08
V_{DDEXT}	U09	ADDR[28]	V09	ADDR[29]	W09	ADDR[30]	Y09
V_{DDEXT}	U10	ID0	V10	ID1	W10	ADDR[31]	Y10
V_{DDEXT}	U11	ADDR[1]	V11	ADDR[0]	W11	ID2	Y11
V_{DDEXT}	U12	$\overline{MS1}$	V12	$\overline{BMS}$	W12	BRST	Y12
V_{DDEXT}	U13	$\overline{CS}$	V13	$\overline{MS2}$	W13	$\overline{MS0}$	Y13
V_{DDEXT}	U14	$\overline{RDL}$	V14	$\overline{CIF}$	W14	$\overline{MS3}$	Y14
V_{DDEXT}	U15	$\overline{DMAR2}$	V15	$\overline{RDH}$	W15	$\overline{WRH}$	Y15
V_{DDEXT}	U16	L5DAT[0]	V16	$\overline{DMAG2}$	W16	$\overline{WRL}$	Y16
L5DAT[7]	U17	L5DAT[2]	V17	LBOOT	W17	$\overline{DMAG1}$	Y17
L4DAT[0]	U18	L5ACK	V18	L5DAT[1]	W18	$\overline{DMAR1}$	Y18
L4DAT[1]	U19	L5DAT[4]	V19	L5DAT[3]	W19	EBOOT	Y19
L4DAT[2]	U20	L5DAT[6]	V20	L5DAT[5]	W20	L5CLK	Y20

[1] For ADSP-21160M, Pin Name and function is defined as V_{DDEXT}. For ADSP-21160N, Pin Name and function is defined as No Connect (NC).
[2] For ADSP-21160M, Pin Name and function is defined as GND. For ADSP-21160N, Pin Name and function is defined as No Connect (NC).

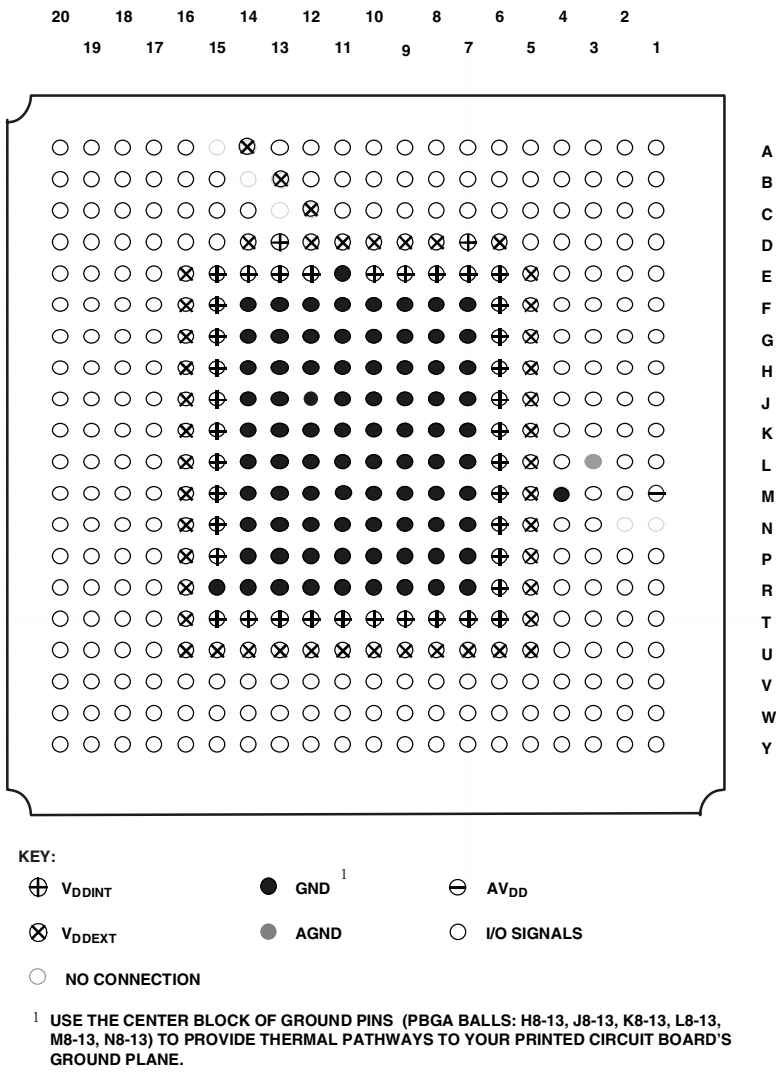


Figure 40. ADSP-21160M 400-Ball PBGA Pin Configurations (Bottom View, Summary)

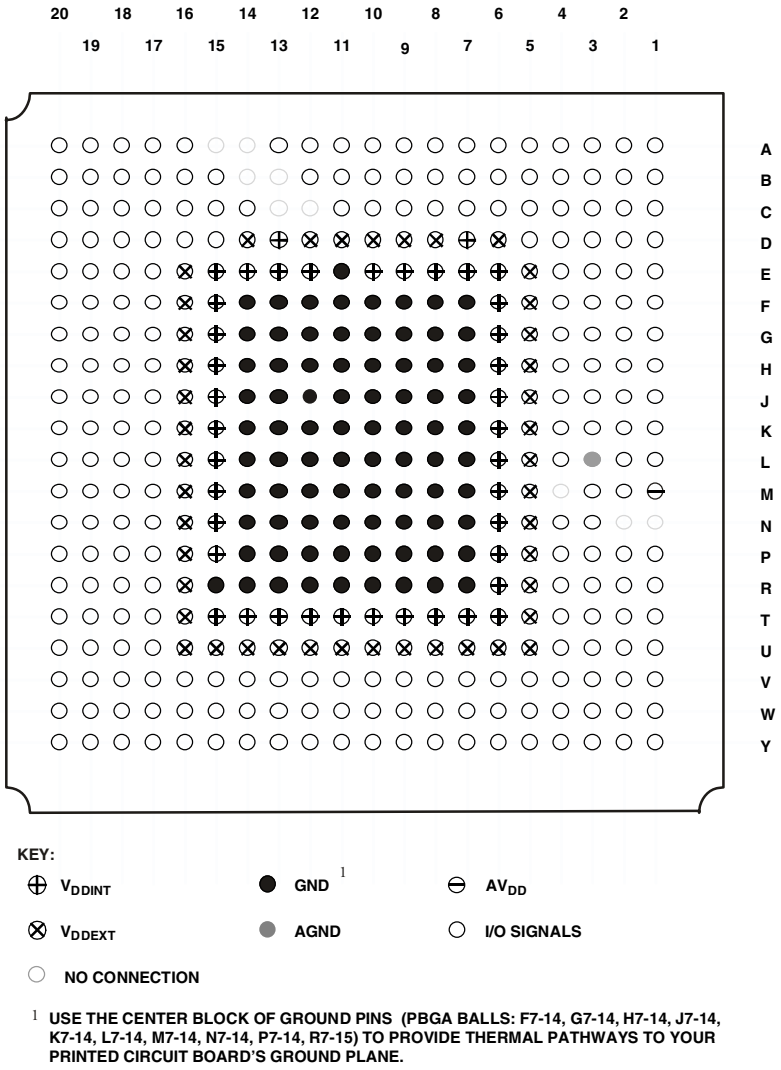


Figure 41. ADSP-21160N 400-Ball PBGA Pin Configurations (Bottom View, Summary)

OUTLINE DIMENSIONS

The ADSP-21160x processors are available in a 27 mm × 27 mm, 400-ball PBGA lead-free package.

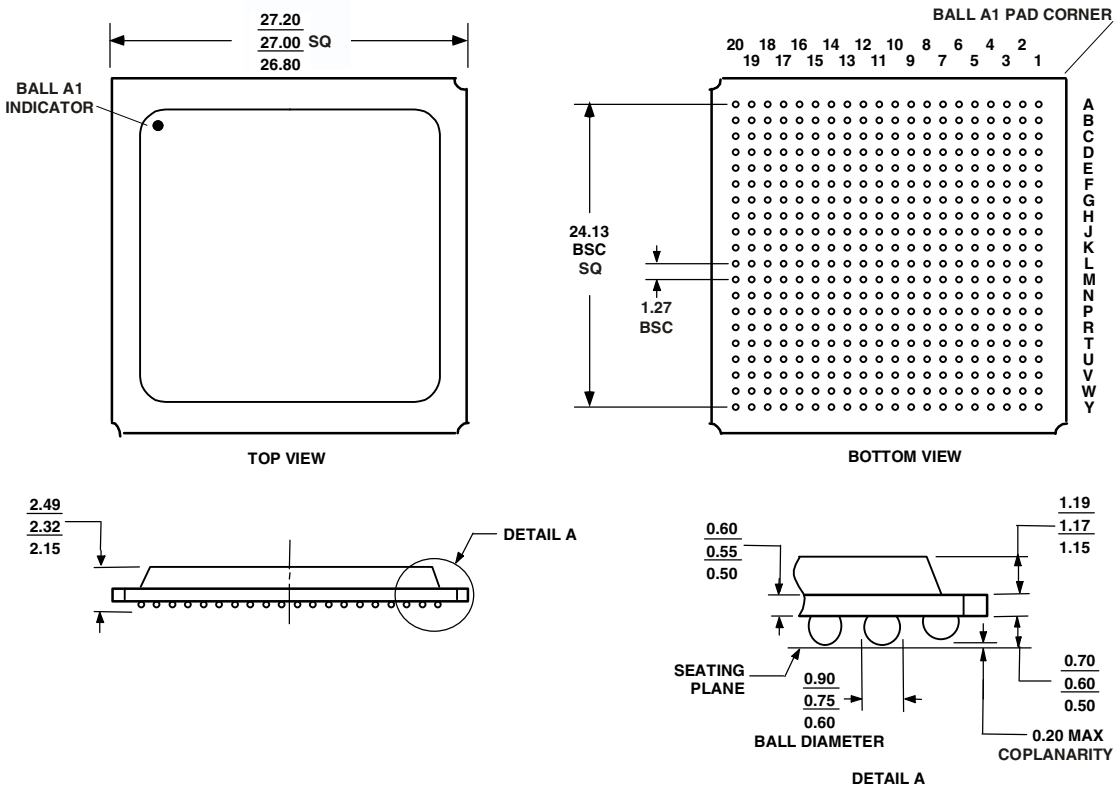


Figure 42. 400-Ball Plastic Grid Array (PBGA) (B-400) Compliant to JEDEC Standards MS-034-BAL-2 (Dimensions in Millimeters)

SURFACE-MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
400-Ball Grid Array (PBGA)	Solder Mask Defined (SMD)	0.63 mm diameter	0.76 mm diameter

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21160MKBZ-80	[1]	0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160MKB-80		0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCBZ-100	[1]	–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCB-100		–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NKBZ-100	[1]	0°C to +85°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400

[1] Z = RoHS Compliant Part.

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