Low Power, Precision Analog Microcontroller with Dual Sigma-Delta ADCs, ARM Cortex-M3

Data Sheet

ADuCM360/ADuCM361

FEATURES

- Analog input/output
  - Dual 24-bit ADCs (ADuCM360)
  - Single 24-bit ADC (ADuCM361)
  - Programmable ADC output rate (3.5 Hz to 3.906 kHz)
  - Simultaneous 50 Hz/60 Hz noise rejection
    - At 50 SPS continuous conversion mode
    - At 16.67 SPS single conversion mode
- Flexible input mux for input channel selection to both ADCs
- Two 24-bit multichannel ADCs (ADC0 and ADC1)
  - 6 differential or 12 single-ended input channels
  - 4 internal channels for monitoring DAC, temperature sensor, IOVDD/4, and AVDD/4 (ADC1 only)
  - Programmable gain (1 to 128)
  - RMS noise: 52 nV at 3.53 Hz, 200 nV at 50 Hz
- Programmable sensor excitation current sources
- On-chip precision voltage reference
- Single 12-bit voltage output DAC
  - NPN mode for 4 mA to 20 mA loop applications
- Microcontroller
  - ARM Cortex-M3 32-bit processor
  - Serial wire download and debug
  - Internal watch crystal for wake-up timer
  - 16 MHz oscillator with 8-way programmable divider
- Memory
  - 128 kB Flash/EE memory, 8 kB SRAM
  - In-circuit debug/download via serial wire and UART
- Power supply range: 1.8 V to 3.6 V (maximum)
- Power consumption, MCU active mode
  - Core consumes 290 µA/MHz
  - Overall system current consumption of 1.0 mA with core operating at 500 kHz (both ADCs on, input buffers off, PGA gain of 4, one SPI port on, and all timers on)
- Power consumption, power-down mode: 4 µA (wake-up timer active)
- On-chip peripherals
  - UART, I^2C, and 2 × SPI serial I/O
  - 16-bit PWM controller
  - 19-pin multifunction GPIO port
  - 2 general-purpose timers
  - Wake-up timer/watchdog timer
  - Multichannel DMA and interrupt controller
- Package and temperature range
  - 48-lead, 7 mm × 7 mm LFCSP
  - Specified for −40°C to +125°C operation
- Development tools
  - Low cost QuickStart Development System
  - Third-party compiler and emulator tool support
- Multiple functional safety features for improved diagnostics

APPLICATIONS

- Industrial automation and process control
- Intelligent precision sensing systems
- 4 mA to 20 mA loop-powered smart sensor systems
- Medical devices, patient monitoring

Rev. D
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Revision History ... 2
General Description ... 3
Functional Block Diagrams ... 4
Specifications ... 6
Microcontroller Electrical Specifications ... 6
RMS Noise Resolution of ADC0 and ADC1 ... 11
I²C Timing Specifications ... 15
SPI Timing Specifications ... 16
Absolute Maximum Ratings ... 18
Thermal Resistance ... 18
ESD Caution ... 18
Pin Configuration and Function Descriptions ... 19
Typical Performance Characteristics ... 22
Typical System Configuration ... 23
Outline Dimensions ... 24
Ordering Guide ... 24

REVISION HISTORY

6/2016—Rev. C to Rev. D

Change to Features Section ... 1
Added Note 12 and Note 13, Table 1 ... 6
Change to Internal Reference (1.2 V) Section, Table 2, and Table 3 ... 11
Changes to External Reference (2.5 V) Section, Table 6, and Table 7 ... 13
Change to Human Body Model Parameter, Table 14 ... 18
Changes to Figure 15 ... 23

10/2014—Rev. B to Rev. C

Changes to Table 1 ... 6
Changes to Table 3 ... 11
Changes to Table 5 ... 12
Changes to Table 7 ... 13
Changes to Table 9 ... 14
Changes to Table 14 ... 18
Changes to Pin 35 and Pin 36 Descriptions; Table 16 ... 20
Changes to Figure 11 ... 22

7/2013—Rev. A to Rev. B

Changes to Features Section and General Description Section ... 3
Changes to Figure 1 ... 4
Added Figure 2, Renumbered Sequentially ... 5
Changes to Table 1 ... 6
Changes to Table 2 and Table 3 ... 10
Changes to Table 4 and Table 5 ... 11
Changes to Table 6 and Table 7 ... 12
Changes to Table 8 and Table 9 ... 13
Changes to Table 16 ... 17
Changes to Figure 14 ... 21

11/2012—Rev. 0 to Rev. A

Changes to Pin 35 and Pin 36 in Table 16 ... 18

9/2012—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM360 is a fully integrated, 3.9 kSPS, 24-bit data acquisition system that incorporates dual high performance, multichannel sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a 32-bit ARM Cortex™-M3 processor, and Flash/EE memory on a single chip. The ADuCM360 is designed for direct interfacing to external precision sensors in both wired and battery-powered applications. The ADuCM361 contains all the features of the ADuCM360 except that only one 24-bit Σ-Δ ADC (ADC1) is available.

The ADuCM360/ADuCM361 contain an on-chip 32 kHz oscillator and an internal 16 MHz high frequency oscillator. The high frequency oscillator is routed through a programmable clock divider from which the operating frequency of the processor core clock is generated. The maximum core clock speed is 16 MHz; this speed is not limited by operating voltage or temperature.

The microcontroller core is a low power ARM Cortex-M3 processor, a 32-bit RISC machine that offers up to 20 MIPS peak performance. The Cortex-M3 processor incorporates a flexible, 11-channel DMA controller that supports all wired communication peripherals (SPI, UART, and I²C). Also integrated on chip are 128 kB of nonvolatile Flash/EE memory and 8 kB of SRAM.

The analog subsystem consists of dual ADCs, each connected to a flexible input mux. Both ADCs can operate in fully differential and single-ended modes. Other on-chip ADC features include dual programmable excitation current sources, diagnostic current sources, and a bias voltage generator of AVDD_REG/2 (900 mV) to set the common-mode voltage of an input channel. A low-side internal ground switch is provided to allow power-down of an external circuit (for example, a bridge circuit) between conversions.

The ADCs contain two parallel filters: a sinc3 or sinc4 filter in parallel with a sinc2 filter. The sinc3 or sinc4 filter is used for precision measurements. The sinc2 filter is used for fast measurements and for the detection of step changes in the input signal.

The devices contain a low noise, low drift internal band gap reference, but they can be configured to accept one or two external reference sources in ratiometric measurement configurations. An option to buffer the external reference inputs is provided on chip. A single-channel buffered voltage output DAC is also provided on chip.

The ADuCM360/ADuCM361 integrate a range of on-chip peripherals, which can be configured under microcontroller software control as required in the application. The peripherals include UART, I²C, and dual SPI serial I/O communication controllers; a 19-pin GPIO port; two general-purpose timers; a wake-up timer; and a system watchdog timer. A 16-bit PWM controller with six output channels is also provided.

The ADuCM360/ADuCM361 are specifically designed to operate in battery-powered applications where low power operation is critical. The microcontroller core can be configured in a normal operating mode that consumes 290 μA/MHz (including flash/ SRAM I_{DD}). An overall system current consumption of 1 mA can be achieved with both ADCs on (input buffers off), PGA gain of 4, one SPI port on, and all timers on.

The ADuCM360/ADuCM361 can be configured in a number of low power operating modes under direct program control, including a hibernate mode (internal wake-up timer active) that consumes only 4 μA. In hibernate mode, peripherals such as external interrupts or the internal wake-up timer can wake up the device. This mode allows the part to operate with ultralow power and still respond to asynchronous external or periodic events.

On-chip factory firmware supports in-circuit serial download via a serial wire interface (2-pin JTAG system) and UART; non-intrusive emulation is also supported via the serial wire interface. These features are incorporated into a low cost QuickStart™ Development System that supports this precision analog microcontroller family.

The parts operate from an external 1.8 V to 3.6 V voltage supply and are specified over an industrial temperature range of −40°C to +125°C.

More information on the ADuCM360/ADuCM361, see the UG-367 user guide.

FUNCTIONAL BLOCK DIAGRAMS

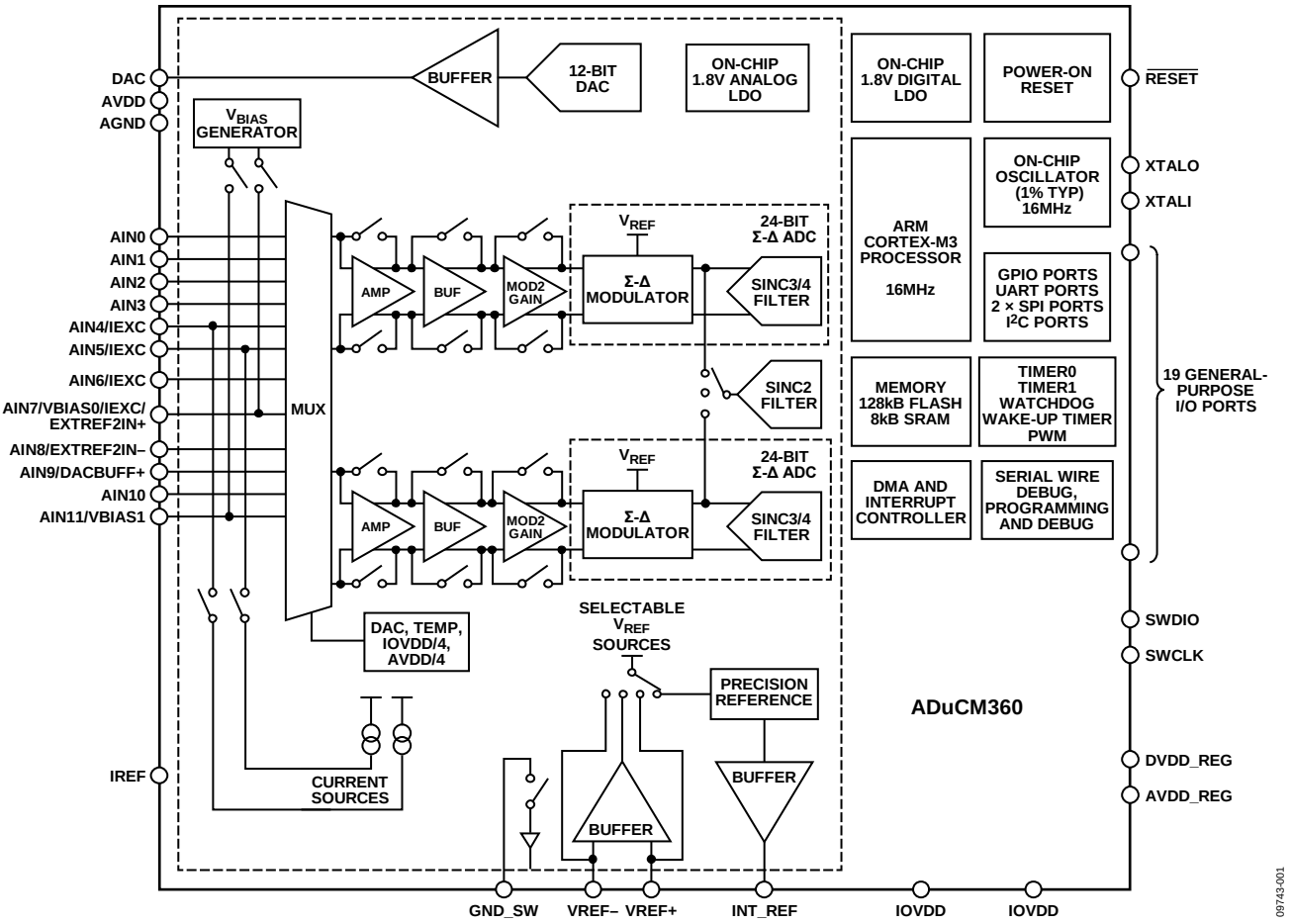


Figure 1. ADuCM360 Functional Block Diagram

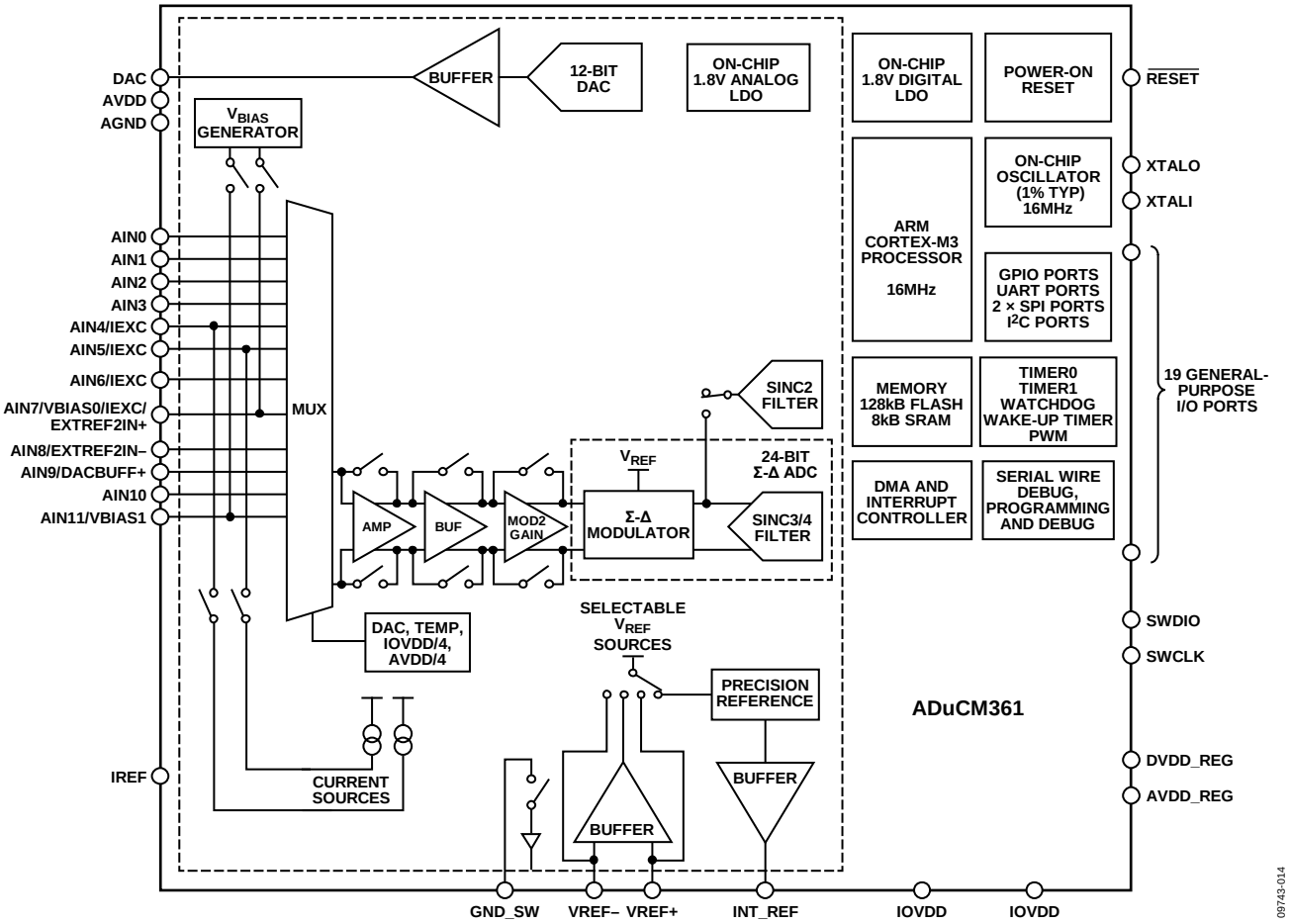


Figure 2. ADuCM361 Functional Block Diagram

SPECIFICATIONS

MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD/IOVDD = 1.8 V to 3.6 V. The difference between AVDD and IOVDD must be ≤0.3 V. Internal 1.2 V reference, f_{CORE} = 16 MHz, all specifications at T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS	ADC0 and ADC1				
Conversion Rate[1]	Chop off	3.5		3906	Hz
	Chop on	3.5		1302	Hz
No Missing Codes[1]	Chop off, f_{ADC} ≤ 500 Hz	24			Bits
	Chop on, f_{ADC} ≤ 250 Hz	24			Bits
RMS Noise and Data Output Rates	See Table 2 through Table 9				
Integral Nonlinearity[1]	Gain = 1, input buffer off		±10		ppm of FSR
	Gain = 2, 4, 8, or 16		±15		ppm of FSR
	Gain = 32, 64, or 128		±20		ppm of FSR
Offset Error[2, 3, 4, 6, 7]	Chop off; offset error is in the order of the noise for the programmed gain and update rate following calibration		±100/gain		µV
	Chop on[1]		±1.0		µV
Offset Error Drift vs. Temperature[1, 4, 6]	Chop off, gain ≤ 4		1/gain		µV/°C
	Chop off, gain ≥ 8		230		nV/°C
	Chop on		10		nV/°C
Offset Error Lifetime Stability[5]	Gain = 128		1		µV/1000Hr
Full-Scale Error[1, 4, 6, 7, 8]			±0.5/gain		mV
Full-Scale Error Lifetime Stability[5]	Gain = 128		±25		µV/1000Hr
Gain Error Drift vs. Temperature[1, 4, 6]	External reference				
	Gain = 1, 2, 4, 8, or 16		±3		ppm/°C
	Gain = 32, 64, or 128		±6		ppm/°C
PGA Gain Mismatch Error			±0.15		%
Power Supply Rejection[1]	External reference				
	Chop on, ADC input = 0.25 V, gain = 4	95			dB
	Chop off, ADC input = 7.8 mV, gain = 128	80			dB
	Chop off, ADC input = 1 V, gain = 1	90			dB
Absolute Input Voltage Range					
Unbuffered Mode		AGND		AVDD	V
Buffered Mode	Gain = 1 is not available; see the information about silicon anomalies on the ADuCM360/ADuCM361 product page				
	Gain ≥ 2	AGND + 0.1		AVDD − 0.1	V
Differential Input Voltage Ranges[1]	For gain = 32, 64, and 128, see Table 3 and Table 7 for allowable input ranges and noise values				
	Gain = 1			±V_{REF}	V
	Gain = 2			±500	mV
	Gain = 4			±250	mV
	Gain = 8			±125	mV
	Gain = 16			±62.5	mV
Common-Mode Voltage, V_{CM}[1]	Ideally, V_{CM} = ((AIN+) + (AIN−))/2; gain = 2 to 128; input current varies with V_{CM} (see Figure 9 and Figure 10)	AGND		AVDD	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Current[9]					
Buffered Mode	Gain > 1 (excluding AIN4, AIN5, AIN6, and AIN7 pins)		1		nA
	Gain > 1 (AIN4, AIN5, AIN6, and AIN7 pins)		2		nA
Unbuffered Mode	Input current varies with input voltage		500		nA/V
Average Input Current Drift[1]					
Buffered Mode	AIN0, AIN1, AIN2, AIN3		±5		pA/°C
	AIN4, AIN5, AIN6, AIN7		±16		pA/°C
	AIN8, AIN9, AIN10, AIN11		±9		pA/°C
Unbuffered Mode			±250		pA/V/°C
Common-Mode Rejection, DC[1]	On ADC input				
	ADC gain = 1, AVDD < 2 V	65	100		dB
	ADC gain = 1, AVDD > 2 V	80	100		dB
	ADC gain = 2 to 128	80			dB
Common-Mode Rejection, 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz; f_{ADC} = 16.7 Hz, chop on; f_{ADC} = 50 Hz, chop off				
	ADC gain = 1	97			dB
	ADC gain = 2 to 128	90			dB
Normal-Mode Rejection, 50 Hz/60 Hz[1]	On ADC input				
	50 Hz/60 Hz ± 1 Hz; f_{ADC} = 16.7 Hz, chop on; f_{ADC} = 50 Hz, chop off	60	80		dB
TEMPERATURE SENSOR[1]	After user calibration				
Voltage Output at 25°C	Processor powered down or in standby mode before measurement		82.1		mV
Voltage Temperature Coefficient (TC)			250		µV/°C
Accuracy			6		°C
GROUND SWITCH					
R_{ON}		3.7	10	19	Ω
Allowable Current[1]	20 kΩ resistor off, direct short to ground			20	mA
VOLTAGE REFERENCE	ADC internal reference				
Internal V_{REF}			1.2		V
Initial Accuracy	Measured at T_A = 25°C	−0.1		+0.1	%
Reference Temperature Coefficient (TC)[1, 10]		−15	±5	+15	ppm/°C
Power Supply Rejection[1]		82	90		dB
EXTERNAL REFERENCE INPUTS					
Input Range					
Buffered Mode		AGND + 0.1		AVDD − 0.1	V
Unbuffered Mode	Minimum differential voltage between VREF+ and VREF− pins is 400 mV	0		AVDD	V
Input Current					
Buffered Mode		−20	+4	+27	nA
Unbuffered Mode			500		nA/V
Normal-Mode Rejection[1]			80		dB
Common-Mode Rejection[1]		85	100		dB
Reference Detect Levels[1]			400		mV
EXCITATION CURRENT SOURCES					
Output Current	Available from each current source; value programmable from 10 µA to 1 mA	10	50	1000	µA
Initial Tolerance at 25°C[1]	I_{OUT} ≥ 50 µA		±5		%
Drift[1]	Using internal reference resistor		100	400	ppm/°C
	Using external 150 kΩ reference resistor between IREF pin and AGND; resistor must have drift specification of 5 ppm/°C		75	400	ppm/°C
Initial Current Matching at 25°C[1]	Matching between both current sources		±0.5		%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Drift Matching[1]			50		ppm/°C
Load Regulation, AVDD[1]	AVDD = 3.3 V		0.2		%/V
Output Compliance[1]	I_{OUT} = 10 µA to 210 µA	AGND – 0.03	AVDD – 0.45	AVDD – 0.85	V
	I_{OUT} > 210 µA	AGND – 0.03	AVDD – 0.55	AVDD – 1.1	V
DAC CHANNEL SPECIFICATIONS	R_L = 5 kΩ, C_L = 100 pF				
Voltage Range	Internal reference	0		V_{REF}	V
	External reference	0		1.8	V
DC Specifications[11]					
Resolution		12			Bits
Relative Accuracy			±3		LSB
Differential Nonlinearity	Guaranteed monotonic		±0.5	±1	LSB
Offset Error	1.2 V internal reference		±2	±10	mV
Gain Error	V_{REF} range (reference = 1.2 V)			±0.5	%
NPN Mode[1]					
Resolution		12			Bits
Relative Accuracy			±3		LSB
Differential Nonlinearity			±0.85		LSB
Offset Error			±0.35		mA
Gain Error			±0.75		mA
Output Current Range		0.008		23.6	mA
Interpolation Mode[1, 12]	Only monotonic to 14 bits				
Resolution			14		Bits
Relative Accuracy[13]	For 14-bit resolution		−4 to +13		LSB
Differential Nonlinearity	Monotonic (14 bits)		±0.5		LSB
Offset Error	1.2 V internal reference		±2		mV
Gain Error	V_{REF} range (reference = 1.2 V)		±1		%
	AVDD range		±1		%
DAC AC CHARACTERISTICS[1]					
Voltage Output Settling Time			10		µs
Digital-to-Analog Glitch Energy	1 LSB change at major carry (maximum number of bits changes simultaneously in the DAC0DAT register)		±20		nV-sec
POWER-ON RESET (POR)					
POR Trip Level	Voltage at DVDD pin				
	Power-on level		1.6		V
	Power-down level		1.6		V
Timeout from POR[1]			50		ms
WATCHDOG TIMER (WDT)[1]					
Timeout Period		0.00003		8192	sec
Timeout Step Size	T3CON[3:2] = 10		7.8125		ms
FLASH/EE MEMORY[1]					
Endurance[14]		10,000			Cycles
Data Retention[15]	T_J = 85°C	10			Years
DIGITAL INPUTS	All digital inputs				
Input Leakage Current	Digital inputs except for the $\overline{\text{RESET}}$, SWCLK, and SWDIO pins				
Logic 1	V_{INH} = IOVDD or V_{INH} = 1.8 V		140		µA
	Internal pull-up disabled		1		nA
Logic 0	V_{INL} = 0 V		160		µA
	Internal pull-up disabled		10		nA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Leakage Current	$\overline{\text{RESET}}$, SWCLK, and SWDIO pins				
Logic 1			140		µA
Logic 0			160		µA
Input Capacitance[1]			10		pF
Logic Inputs					
Input Low Voltage, V_{INL}				0.2 × IOVDD	V
Input High Voltage, V_{INH}		0.7 × IOVDD			V
Logic Outputs					
Output High Voltage, V_{OH}	I_{SOURCE} = 1 mA	IOVDD − 0.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1 mA			0.4	V
CRYSTAL OSCILLATOR[1]	32.768 kHz crystal inputs				
Logic Inputs, XTALI Only[16]					
Input Low Voltage, V_{INL}				0.8	V
Input High Voltage, V_{INH}		1.7			V
XTALI Capacitance			6		pF
XTALO Capacitance			6		pF
ON-CHIP LOW POWER OSCILLATOR					
Oscillator Frequency			32.768		kHz
Accuracy		−30	±10	+30	%
ON-CHIP HIGH FREQUENCY OSCILLATOR					
Oscillator Frequency			16		MHz
Accuracy	−40°C to +125°C	−1.8		+1.4	%
Long Term Stability[5]			0.8		%/1000 Hr
PROCESSOR CLOCK RATE[1]	Nine programmable core clock selections within specified range	0.0625	0.5	16	MHz
Using an External Clock		0.032768		16	MHz
PROCESSOR START-UP TIME[1]					
At Power-On	Includes kernel power-on execution time		41		ms
After Reset Event	Includes kernel power-on execution time		1.44		ms
From Processor Power-Down (Mode 1, Mode 2, and Mode 3)	f_{CLK} is the Cortex-M3 core clock		3 to 5		f_{CLK}
From Total Halt or Hibernate Mode (Mode 4 or Mode 5)			30.8		µs
POWER REQUIREMENTS					
Power Supply Voltages, V_{DD}	AVDD, IOVDD	1.8		3.6	V
Power Consumption					
I_{DD} (MCU Active Mode)[17, 18]	Processor clock rate = 16 MHz; all peripherals on (CLKSYSDIV = 0)		5.5		mA
	Processor clock rate = 8 MHz; all peripherals on (CLKSYSDIV = 1)		3		mA
	Processor clock rate = 500 kHz; both ADCs on (input buffers off) with PGA gain = 4, 1 × SPI port on, all timers on		1		mA
I_{DD} (MCU Powered Down)	Full temperature range, total halt mode (Mode 4)		4		µA
	Reduced temperature range, −40°C to +85°C		4		µA
I_{DD}, Total (ADC0)[18]	PGA enabled, gain ≥ 32		320		µA
PGA	Gain = 4, 8, or 16, PGA only		130		µA
	Gain = 32, 64, or 128, PGA only		180		µA
Input Buffers	2 × input buffers = 70 µA		70		µA
Digital Interface and Modulator			70		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I_{DD} (ADC1)	Input buffers off, gain = 4, 8, or 16 only		200		μA
External Reference Input Buffers	60 μA each		120		μA

[1] These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.
[2] Tested at gain = 4 after initial offset calibration.
[3] Measured with an internal short. A system zero-scale calibration removes this error.
[4] A recalibration at any temperature removes these errors.
[5] The long term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[6] These numbers do not include internal reference temperature drift.
[7] Factory calibrated at gain = 1.
[8] System calibration at a specific gain removes the error at this gain.
[9] Input current measured with one ADC measuring a channel. If both ADCs measure the same input channel, the input current increases (approximately doubles).
[10] Measured using the box method.
[11] Reference DAC linearity is calculated using a reduced code range of 0x0AB to 0xF30.
[12] Measured using a low-pass filter with R = 1 kΩ, C = 100 nF.
[13] A closed loop control with the ADC improves DAC accuracy.
[14] Endurance is qualified to 10,000 cycles as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[15] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.
[16] Voltage input levels are relevant only if driving XTAL input from a voltage source. If a crystal is connected directly, the internal crystal interface determines the common-mode voltage.
[17] Typical additional supply current consumed during Flash/EE memory program and erase cycles is 7 mA.
[18] Total I_{DD} for ADC includes figures for PGA ≥ 32, input buffers, digital interface, and the Σ-Δ modulator.

RMS NOISE RESOLUTION OF ADC0 AND ADC1

Internal Reference (1.2 V)

Table 2 through Table 5 provide rms noise specifications for ADC0 and ADC1 using the internal reference (1.2 V). Table 2 and Table 3 list the rms noise for both ADCs with various gain and output update rate values. Table 4 and Table 5 list the typical output rms noise effective number of bits (ENOB) in normal mode for both ADCs with various gain and output update rate values. (Peak-to-peak ENOB is shown in parentheses.) These results are taken with the input buffers off.

Table 2. RMS Noise vs. Gain and Output Update Rate, Internal Reference (1.2 V), Gain = 1, 2, 4, 8, and 16

			RMS Noise (µV)				
Update Rate (Hz)	**Chop/Sinc**	**ADCFLT Register Value**	**Gain = 1, ±V_{REF}, ADCxMDE = 0x01**	**Gain = 2, ±500 mV, ADCxMDE = 0x11**	**Gain = 4, ±250 mV, ADCxMDE = 0x21**	**Gain = 8, ±125 mV, ADCxMDE = 0x31**	**Gain = 16, ±62.5 mV, ADCxMDE = 0x41**
3.53	On/Sinc3	0x8E7C	1.05	0.45	0.23	0.135	0.072
30	Off/Sinc3	0x007E	2.1	1.37	0.63	0.37	0.22
50	Off/Sinc3	0x007D	3.7	1.6	0.83	0.47	0.29
100	Off/Sinc3	0x004D	5.45	2.41	1.13	0.63	0.38
488	Off/Sinc4	0x100F	10	4.7	2.2	1.3	0.79
976	Off/Sinc4	0x1007	13.5	6.5	3.3	1.7	1.1
1953	Off/Sinc4	0x1003	19.3	10	4.7	2.6	1.55
3906	Off/Sinc4	0x1001	67.0	36	16.6	8.8	4.9

Table 3. RMS Noise vs. Gain and Output Update Rate, Internal Reference (1.2 V), Gain = 32, 64, and 128

			RMS Noise (µV)					
Update Rate (Hz)	**Chop/Sinc**	**ADCFLT Register Value**	**Gain = 32,[1] ±37.5 mV, ADCxMDE = 0x49**	**Gain = 32,[1, 2] ±22.18 mV, ADCxMDE = 0x51**	**Gain = 64,[3] ±18.75 mV, ADCxMDE = 0x59**	**Gain = 64,[3, 4] ±10.3125 mV, ADCxMDE = 0x61**	**Gain = 128,[5] ±9.375 mV, ADCxMDE = 0x69**	**Gain = 128,[5, 6] ±3.98 mV, ADCxMDE = 0x71**
3.53	On/Sinc3	0x8E7C	0.067	0.064	0.073	0.055	0.058	0.052
30	Off/Sinc3	0x007E	0.202	0.2	0.196	0.16	0.174	0.155
50	Off/Sinc3	0x007D	0.24	0.24	0.25	0.21	0.21	0.2
100	Off/Sinc3	0x004D	0.35	0.32	0.36	0.27	0.31	0.25
488	Off/Sinc4	0x100F	0.7	0.67	0.71	0.58	0.62	0.57
976	Off/Sinc4	0x1007	0.99	0.91	1.01	0.74	0.83	0.7
1953	Off/Sinc4	0x1003	1.78	1.3	1.48	1.15	1.25	1.0
3906	Off/Sinc4	0x1001	6.44	2.68	3.59	1.4	2.2	1.4

[1] ADCxMDE = 0x49 sets the PGA for a gain of 16 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x51 sets the PGA for a gain of 32 with the modulator gain off. ADCxMDE = 0x49 has slightly higher noise but supports a wider input range.
[2] If AVDD < 2.0 V and ADCxMDE = 0x51, the input range is ±17.5 mV.
[3] ADCxMDE = 0x59 sets the PGA for a gain of 32 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x61 sets the PGA for a gain of 64 with the modulator gain off. ADCxMDE = 0x59 has slightly higher noise but supports a wider input range.
[4] If AVDD < 2.0 V and ADCxMDE = 0x61, the input range is ±8.715 mV.
[5] ADCxMDE = 0x69 sets the PGA for a gain of 64 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x71 sets the PGA for a gain of 128 with the modulator gain off. ADCxMDE = 0x69 has slightly higher noise but supports a wider input range.
[6] If AVDD < 2.0 V and ADCxMDE = 0x71, the input range is ±3.828 mV.

Table 4. Typical Output RMS Noise Effective Number of Bits in Normal Mode, Internal Reference (1.2 V), Gain = 1, 2, 4, 8, and 16

		Effective Number of Bits (ENOB) by Input Voltage Range and Gain[1]				
Update Rate (Hz)	**Chop/Sinc**	**Gain = 1, ±V_{REF}, ADCxMDE = 0x01**	**Gain = 2, ±500 mV, ADCxMDE = 0x11**	**Gain = 4, ±250 mV, ADCxMDE = 0x21**	**Gain = 8, ±125 mV, ADCxMDE = 0x31**	**Gain = 16, ±62.5 mV, ADCxMDE = 0x41**
3.53	On/Sinc3	21.1 (18.4 p-p)	21.1 (18.4 p-p)	21.1 (18.3 p-p)	20.8 (18.1 p-p)	20.7 (18.0 p-p)
30	Off/Sinc3	20.1 (17.4 p-p)	19.5 (16.8 p-p)	19.6 (16.9 p-p)	19.4 (16.6 p-p)	19.1 (16.4 p-p)
50	Off/Sinc3	19.3 (16.6 p-p)	19.25 (16.5 p-p)	19.2 (16.5 p-p)	19.0 (16.3 p-p)	18.7 (16.0 p-p)
100	Off/Sinc3	18.7 (16.0 p-p)	18.66 (15.9 p-p)	18.75 (16.0 p-p)	18.6 (15.9 p-p)	18.3 (15.6 p-p)
488	Off/Sinc4	17.9 (15.2 p-p)	17.7 (15.0 p-p)	17.8 (15.1 p-p)	17.55 (14.8 p-p)	17.3 (14.5 p-p)
976	Off/Sinc4	17.4 (14.7 p-p)	17.2 (14.5 p-p)	17.2 (14.5 p-p)	17.2 (14.4 p-p)	16.8 (14.1 p-p)
1953	Off/Sinc4	16.9 (14.2 p-p)	16.6 (13.9 p-p)	16.7 (14.0 p-p)	16.55 (13.8 p-p)	16.3 (13.6 p-p)
3906	Off/Sinc4	15.1 (12.4 p-p)	14.8 (12.0 p-p)	14.9 (12.2 p-p)	14.8 (12.1 p-p)	14.6 (11.9 p-p)

[1] RMS bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/\textit{RMS Noise})$; peak-to-peak (p-p) bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/(6.6 \times \textit{RMS Noise}))$.

Table 5. Typical Output RMS Noise Effective Number of Bits in Normal Mode, Internal Reference (1.2 V), Gain = 32, 64, and 128

		Effective Number of Bits (ENOB) by Input Voltage Range and Gain[1]					
Update Rate (Hz)	**Chop/Sinc**	**Gain = 32, ±37.5 mV, ADCxMDE = 0x49**	**Gain = 32, ±22.18 mV, ADCxMDE = 0x51**	**Gain = 64, ±18.75 mV, ADCxMDE = 0x59**	**Gain = 64, ±10.3125 mV, ADCxMDE = 0x61**	**Gain = 128, ±9.375 mV, ADCxMDE = 0x69**	**Gain = 128, ±3.98 mV, ADCxMDE = 0x71**
3.53	On/Sinc3	19.8 (17.1 p-p)	19.4 (16.7 p-p)	18.7 (16.0 p-p)	18.5 (15.8 p-p)	18.0 (15.3 p-p)	17.2 (14.5 p-p)
30	Off/Sinc3	18.2 (15.5 p-p)	17.75 (15.0 p-p)	17.3 (14.6 p-p)	17.0 (14.25 p-p)	16.45 (13.7 p-p)	15.6 (12.9 p-p)
50	Off/Sinc3	18.0 (15.2 p-p)	17.5 (14.8 p-p)	16.93 (14.2 p-p)	16.6 (13.86 p-p)	16.2 (13.5 p-p)	15.3 (12.55 p-p)
100	Off/Sinc3	17.4 (14.7 p-p)	17.1 (14.35 p-p)	16.4 (13.7 p-p)	16.2 (13.5 p-p)	15.6 (12.9 p-p)	15.0 (12.2 p-p)
488	Off/Sinc4	16.4 (13.7 p-p)	16.0 (13.3 p-p)	15.4 (12.7 p-p)	15.1 (12.4 p-p)	14.6 (11.9 p-p)	13.8 (11.0 p-p)
976	Off/Sinc4	15.9 (13.2 p-p)	15.6 (12.85 p-p)	14.91 (12.2 p-p)	14.8 (12.0 p-p)	14.2 (11.5 p-p)	13.4 (10.75 p-p)
1953	Off/Sinc4	15.1 (12.4 p-p)	15.05 (12.3 p-p)	14.4 (11.6 p-p)	14.1 (11.4 p-p)	13.6 (10.9 p-p)	13.0 (10.2 p-p)
3906	Off/Sinc4	13.2 (10.5 p-p)	14.0 (11.3 p-p)	13.1 (10.4 p-p)	13.8 (11.1 p-p)	12.8 (10.1 p-p)	12.5 (9.75 p-p)

[1] RMS bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/\textit{RMS Noise})$; peak-to-peak (p-p) bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/(6.6 \times \textit{RMS Noise}))$.

External Reference (2.5 V)

Table 6 through Table 9 provide rms noise specifications for ADC0 and ADC1 using the external reference (2.5 V). Table 6 and Table 7 list the rms noise for both ADCs with various gain and output update rate values. Table 8 and Table 9 list the typical output rms noise effective number of bits (ENOB) in normal mode for both ADCs with various gain and output update rate values. (Peak-to-peak ENOB is shown in parentheses.) These results are taken with the input buffers off.

Table 6. RMS Noise vs. Gain and Output Update Rate, External Reference (2.5 V), Gain = 1, 2, 4, 8, and 16

			RMS Noise (µV)				
Update Rate (Hz)	**Chop/Sinc**	**ADCFLT Register Value**	**Gain = 1, ±V_{REF}, ADCxMDE = 0x01**	**Gain = 2, ±500 mV, ADCxMDE = 0x11**	**Gain = 4, ±250 mV, ADCxMDE = 0x21**	**Gain = 8, ±125 mV, ADCxMDE = 0x31**	**Gain = 16, ±62.5 mV, ADCxMDE = 0x41**
3.53	On/Sinc3	0x8E7C	1.1	0.5	0.27	0.17	0.088
30	Off/Sinc3	0x007E	3	1.4	0.85	0.44	0.27
50	Off/Sinc3	0x007D	3.9	2.2	0.92	0.46	0.3
100	Off/Sinc3	0x004D	5.2	2.8	1.25	0.63	0.38
488	Off/Sinc4	0x100F	9.3	5.0	2.5	1.2	0.75
976	Off/Sinc4	0x1007	12.5	7	3.5	1.75	1.2
1953	Off/Sinc4	0x1003	20.0	10	5.7	2.6	1.71
3906	Off/Sinc4	0x1001	140.0	70.0	35.0	17.2	8.9

Table 7. RMS Noise vs. Gain and Output Update Rate, External Reference (2.5 V), Gain = 32, 64, and 128

			RMS Noise (µV)					
Update Rate (Hz)	**Chop/Sinc**	**ADCFLT Register Value**	**Gain = 32,[1] ±62.5 mV, ADCxMDE = 0x49**	**Gain = 32,[1, 2] ±22.18 mV, ADCxMDE = 0x51**	**Gain = 64,[3] ±22.18 mV, ADCxMDE = 0x59**	**Gain = 64,[3, 4] ±10.3125 mV, ADCxMDE = 0x61**	**Gain = 128,[5] ±10.3125 mV, ADCxMDE = 0x69**	**Gain = 128,[5, 6] ±3.98 mV, ADCxMDE = 0x71**
3.53	On/Sinc3	0x8E7C	0.076	0.07	0.088	0.06	0.068	0.058
30	Off/Sinc3	0x007E	0.21	0.22	0.21	0.19	0.175	0.17
50	Off/Sinc3	0x007D	0.265	0.21	0.27	0.2	0.225	0.19
100	Off/Sinc3	0x004D	0.37	0.32	0.366	0.28	0.32	0.26
488	Off/Sinc4	0x100F	0.73	0.7	0.73	0.57	0.64	0.5
976	Off/Sinc4	0x1007	1.1	0.83	1.01	0.77	0.89	0.75
1953	Off/Sinc4	0x1003	2.05	1.3	1.6	1.24	1.3	1.1
3906	Off/Sinc4	0x1001	9.4	4.8	5.1	2.65	3.2	1.88

[1] ADCxMDE = 0x49 sets the PGA for a gain of 16 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x51 sets the PGA for a gain of 32 with the modulator gain off. ADCxMDE = 0x49 has slightly higher noise but supports a wider input range.
[2] If AVDD < 2.0 V and ADCxMDE = 0x51, the input range is ±17.5 mV.
[3] ADCxMDE = 0x59 sets the PGA for a gain of 32 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x61 sets the PGA for a gain of 64 with the modulator gain off. ADCxMDE = 0x59 has slightly higher noise but supports a wider input range.
[4] If AVDD < 2.0 V and ADCxMDE = 0x61, the input range is ±8.715 mV.
[5] ADCxMDE = 0x69 sets the PGA for a gain of 64 with a modulator gain of 2. The modulator gain of 2 is implemented by adjusting the sampling capacitors into the modulator. ADCxMDE = 0x71 sets the PGA for a gain of 128 with the modulator gain off. ADCxMDE = 0x69 has slightly higher noise but supports a wider input range.
[6] If AVDD < 2.0 V and ADCxMDE = 0x71, the input range is ±3.828 mV.

Table 8. Typical Output RMS Noise Effective Number of Bits in Normal Mode, External Reference (2.5 V), Gain = 1, 2, 4, 8, and 16

		Effective Number of Bits (ENOB) by Input Voltage Range and Gain[1]				
Update Rate (Hz)	**Chop/Sinc**	**Gain = 1, ±V_{REF}, ADCxMDE = 0x01**	**Gain = 2, ±500 mV, ADCxMDE = 0x11**	**Gain = 4, ±250 mV, ADCxMDE = 0x21**	**Gain = 8, ±125 mV, ADCxMDE = 0x31**	**Gain = 16, ±62.5 mV, ADCxMDE = 0x41**
3.53	On/Sinc3	22.1 (19.4 p-p)	20.9 (18.2 p-p)	20.8 (18.1 p-p)	20.5 (17.7 p-p)	20.43 (17.7 p-p)
30	Off/Sinc3	20.7 (18.0 p-p)	19.4 (16.7 p-p)	19.2 (16.4 p-p)	19.1 (16.4 p-p)	18.82 (16.1 p-p)
50	Off/Sinc3	20.3 (17.6 p-p)	18.8 (16.1 p-p)	19.05 (16.3 p-p)	19.05 (16.3 p-p)	18.66 (15.9 p-p)
100	Off/Sinc3	19.9 (17.2 p-p)	18.4 (15.7 p-p)	18.6 (15.9 p-p)	18.6 (15.9 p-p)	18.32 (15.6 p-p)
488	Off/Sinc4	19.0 (16.3 p-p)	17.6 (14.9 p-p)	17.6 (14.9 p-p)	17.7 (14.9 p-p)	17.34 (14.6 p-p)
976	Off/Sinc4	18.6 (15.9 p-p)	17.1 (14.4 p-p)	17.1 (14.4 p-p)	17.1 (14.4 p-p)	16.66 (13.9 p-p)
1953	Off/Sinc4	17.9 (15.2 p-p)	16.6 (13.9 p-p)	16.4 (13.7 p-p)	16.55 (13.8 p-p)	16.15 (13.4 p-p)
3906	Off/Sinc4	15.1 (12.4 p-p)	13.8 (11.1 p-p)	13.8 (11.1 p-p)	13.8 (11.1 p-p)	13.77 (11.05 p-p)

[1] RMS bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/\textit{RMS Noise})$; peak-to-peak (p-p) bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/(6.6 \times \textit{RMS Noise}))$.

Table 9. Typical Output RMS Noise Effective Number of Bits in Normal Mode, External Reference (2.5 V), Gain = 32, 64, and 128

		Effective Number of Bits (ENOB) by Input Voltage Range and Gain[1]					
Update Rate (Hz)	**Chop/Sinc**	**Gain = 32, ±62.5 mV, ADCxMDE = 0x49**	**Gain = 32, ±22.18 mV, ADCxMDE = 0x51**	**Gain = 64, ±22.18 mV, ADCxMDE = 0x59**	**Gain = 64, ±10.3125 mV, ADCxMDE = 0x61**	**Gain = 128, ±10.3125 mV, ADCxMDE = 0x69**	**Gain = 128, ±3.98 mV, ADCxMDE = 0x71**
3.53	On/Sinc3	19.6 (16.9 p-p)	19.3 (16.55 p-p)	18.4 (15.7 p-p)	18.4 (15.7 p-p)	17.8 (15.1 p-p)	17.1 (14.3 p-p)
30	Off/Sinc3	18.2 (15.5 p-p)	17.6 (14.9 p-p)	17.2 (14.5 p-p)	16.7 (14.0 p-p)	16.4 (13.7 p-p)	15.5 (12.8 p-p)
50	Off/Sinc3	17.8 (15.1 p-p)	17.7 (15.0 p-p)	16.8 (14.1 p-p)	16.65 (13.9 p-p)	16.1 (13.4 p-p)	15.35 (12.6 p-p)
100	Off/Sinc3	17.4 (14.6 p-p)	17.1 (14.35 p-p)	16.4 (13.7 p-p)	16.2 (13.4 p-p)	15.6 (12.85 p-p)	14.9 (12.2 p-p)
488	Off/Sinc4	16.4 (13.7 p-p)	16.0 (13.2 p-p)	15.4 (12.7 p-p)	15.1 (12.4 p-p)	14.6 (11.85 p-p)	14.0 (11.2 p-p)
976	Off/Sinc4	15.8 (13.1 p-p)	15.7 (13.0 p-p)	14.9 (12.2 p-p)	14.7 (12.0 p-p)	14.1 (11.4 p-p)	13.4 (10.6 p-p)
1953	Off/Sinc4	14.9 (12.1 p-p)	15.1 (12.3 p-p)	14.25 (11.5 p-p)	14.0 (11.3 p-p)	13.55 (10.8 p-p)	12.8 (10.1 p-p)
3906	Off/Sinc4	12.7 (10.0 p-p)	13.2 (10.4 p-p)	12.6 (9.9 p-p)	12.9 (10.2 p-p)	12.25 (9.5 p-p)	12.0 (9.3 p-p)

[1] RMS bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/\textit{RMS Noise})$; peak-to-peak (p-p) bits are calculated as follows: $\log_2((2 \times \textit{Input Range})/(6.6 \times \textit{RMS Noise}))$.

I²C TIMING SPECIFICATIONS

The capacitive load for each I²C bus line (C_B) is 400 pF maximum as per the I²C bus specifications. I²C timing is guaranteed by design, but is not production tested.

Table 10. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Min	Max	Unit
t_L	Serial clock (SCL) low pulse width	1300		ns
t_H	SCL high pulse width	600		ns
t_{SHD}	Start condition hold time	600		ns
t_{DSU}	Data setup time	100		ns
t_{DHD}	Data hold time	0		ns
t_{RSU}	Setup time for repeated start	600		ns
t_{PSU}	Stop condition setup time	600		ns
t_{BUF}	Bus free time between a stop condition and a start condition	1.3		µs
t_R	Rise time for both SCL and serial data (SDA)	20 + 0.1 C_B	300	ns
t_F	Fall time for both SCL and SDA	20 + 0.1 C_B	300	ns
t_{SUP}	Pulse width of suppressed spike	0	50	ns

Table 11. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.7		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0		µs
t_{RSU}	Setup time for repeated start	4.0		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

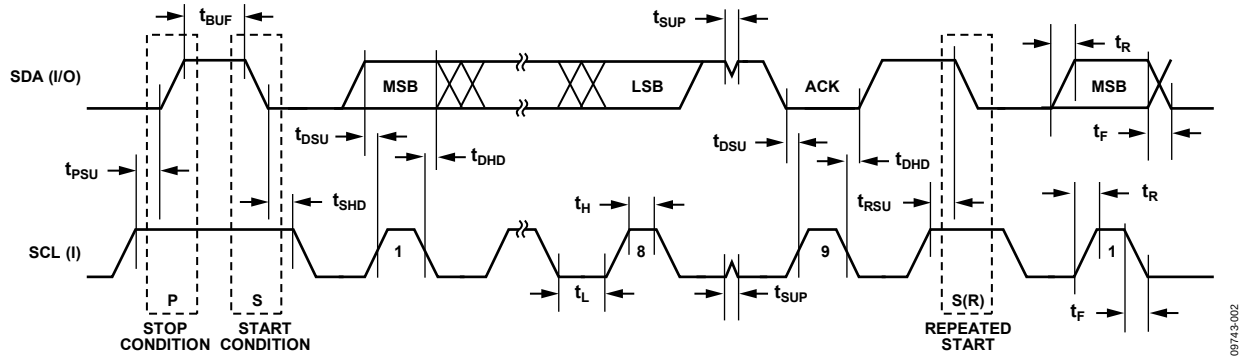


Figure 3. I²C-Compatible Interface Timing

SPI TIMING SPECIFICATIONS

Table 12. SPI Master Mode Timing

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge		0	35.5	ns
t_{DOSU}	Data output setup time before SCLK edge[1]	(SPIDIV + 1) × t_{UCLK}			ns
t_{DSU}	Data input setup time before SCLK edge	58.7			ns
t_{DHD}	Data input hold time after SCLK edge	16			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the internal 16 MHz clock before the clock divider.

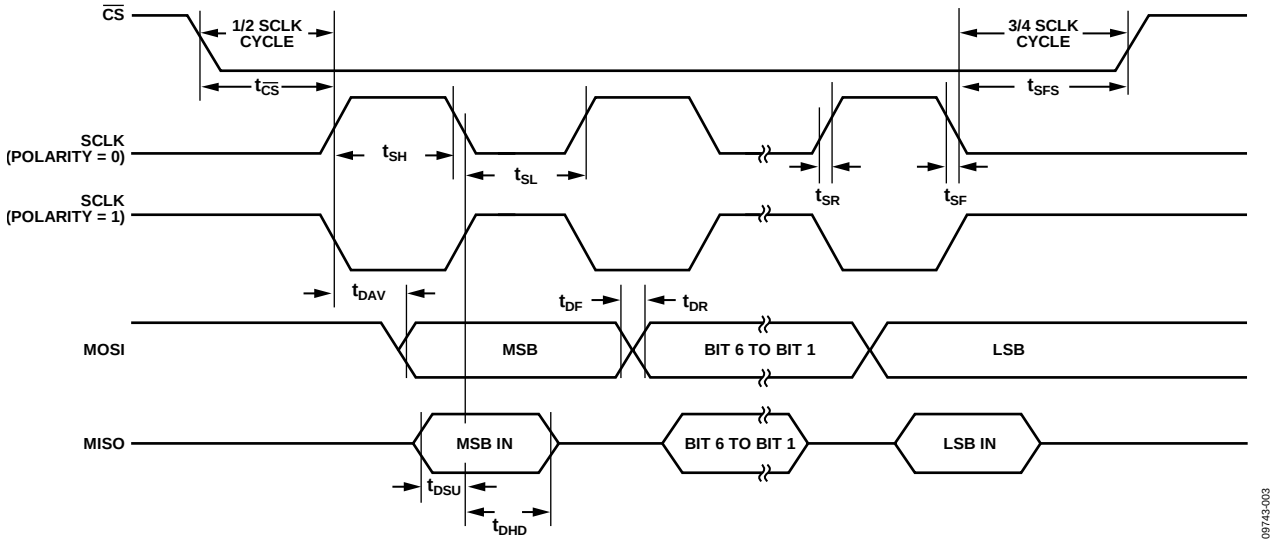


Figure 4. SPI Master Mode Timing (Phase Mode = 1)

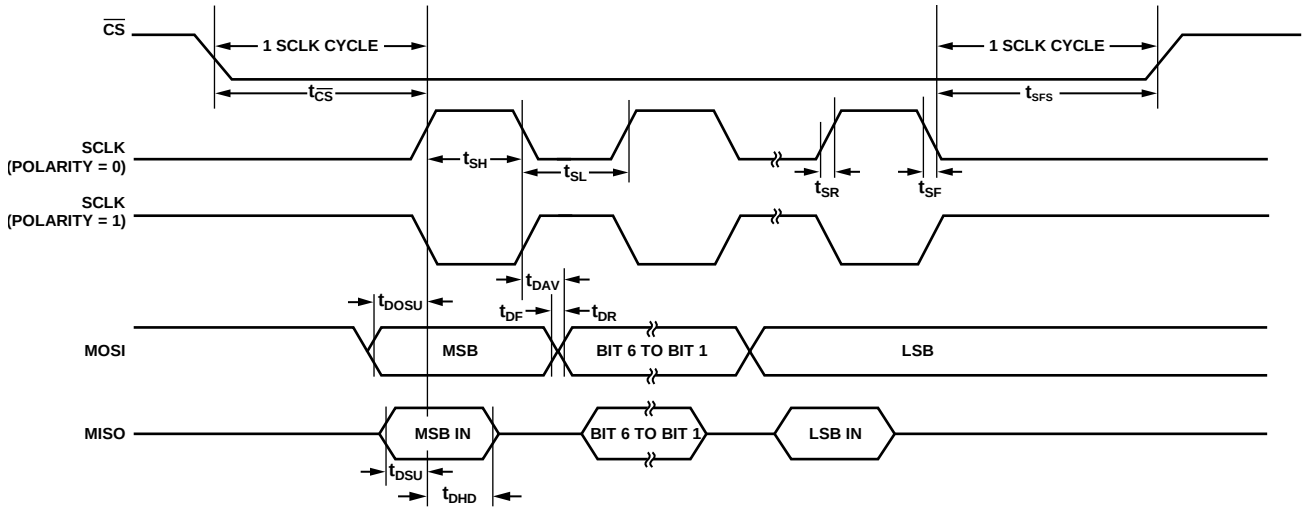


Figure 5. SPI Master Mode Timing (Phase Mode = 0)

Table 13. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	62.5			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]	62.5	(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			49.1	ns
t_{DSU}	Data input setup time before SCLK edge	20.2			ns
t_{DHD}	Data input hold time after SCLK edge	10.1			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the internal 16 MHz clock before the clock divider.

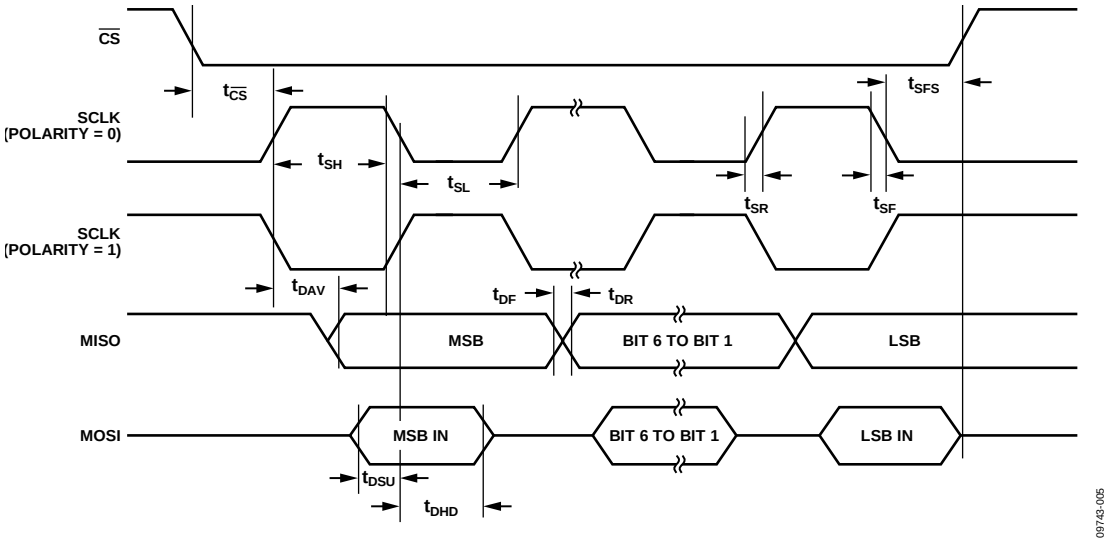


Figure 6. SPI Slave Mode Timing (Phase Mode = 1)

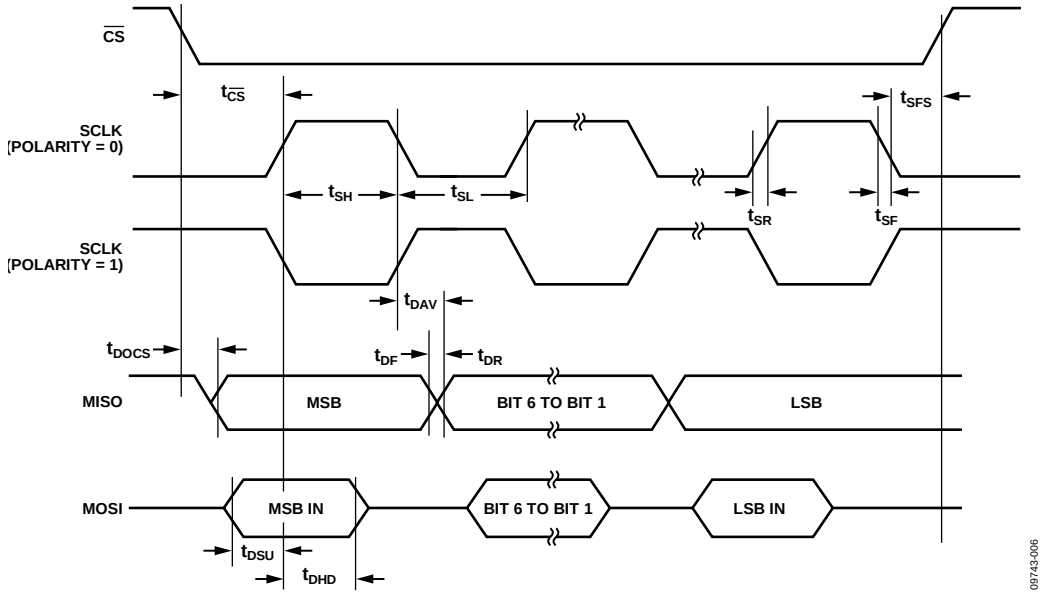


Figure 7. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

Table 14.

Parameter	Rating
AVDD to AGND	−0.3 V to +3.96 V
IOVDD to DGND	−0.3 V to +3.96 V
AGND to DGND	−0.3 V to +0.3 V
AVDD to DVDD	−0.3 V to +0.3 V
Digital Input Voltage to DGND	−0.3 V to +3.96 V
Digital Output Voltage to DGND	−0.3 V to +3.96 V
Analog Inputs to AGND	−0.3 V to +3.96 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Rating, All Pins	
Human Body Model (HBM)	±2 kV
Field-Induced Charged Device Model (FICDM)	±1 kV
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
Pb-Free Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 15. Thermal Resistance

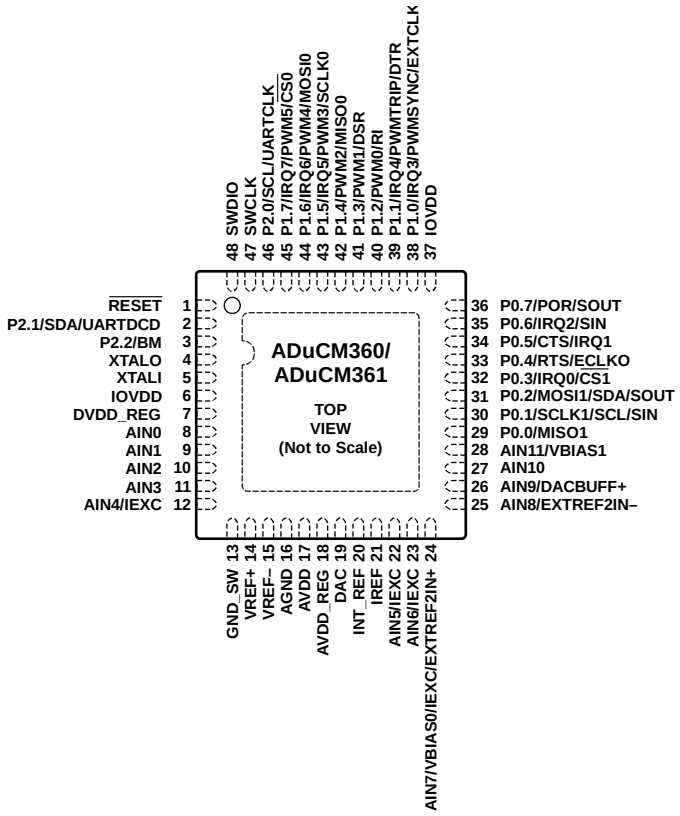
Package Type	θ_{JA}	Unit
48-Lead LFCSP_WQ	27	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS AND TO DGND.

Figure 8. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset Pin, Active Low Input. An internal pull-up is provided.
2	P2.1/SDA/UARTDCD	General-Purpose Input/Output P2.1/I²C Serial Data Pin/UART Data Carrier Detect Pin.
3	P2.2/BM	General-Purpose Input/Output P2.2/Boot Mode Input Select Pin. When this pin is held low during and for a short time after any reset sequence, the part enters UART download mode.
4	XTALO	External Crystal Oscillator Output Pin. Optional 32.768 kHz source for real-time clock.
5	XTALI	External Crystal Oscillator Input Pin. Optional 32.768 kHz source for real-time clock.
6	IOVDD	Digital System Supply Pin. This pin must be connected to DGND via a 0.1 µF capacitor.
7	DVDD_REG	This pin must be connected to DGND via a 470 nF capacitor and to Pin 18, AVDD_REG.
8	AIN0	ADC Analog Input 0. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode.
9	AIN1	ADC Analog Input 1. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode.
10	AIN2	ADC Analog Input 2. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode.
11	AIN3	ADC Analog Input 3. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode.
12	AIN4/IEXC	ADC Analog Input 4/Excitation Current Source. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN4). This pin can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1 (IEXC).
13	GND_SW	Sensor Power Switch to Analog Ground Reference.

Pin No.	Mnemonic	Description
14	VREF+	External Reference Positive Input. An external reference can be applied between the VREF+ and VREF− pins.
15	VREF−	External Reference Negative Input. An external reference can be applied between the VREF+ and VREF− pins.
16	AGND	Analog System Ground Reference Pin.
17	AVDD	Analog System Supply Pin. This pin must be connected to AGND via a 0.1 µF capacitor.
18	AVDD_REG	Internal Analog Regulator Supply Output. This pin must be connected to AGND via a 470 nF capacitor and to Pin 7, DVDD_REG.
19	DAC	DAC Voltage Output.
20	INT_REF	Internal Reference. This pin must be connected to ground via a 470 nF decoupling capacitor.
21	IREF	Optional Reference Current Resistor Connection for the Excitation Current Sources. The reference current used for the excitation current sources is set by a low drift (5 ppm/°C) external resistor connected to this pin.
22	AIN5/IEXC	ADC Analog Input 5/Excitation Current Source. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN5). This pin can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1 (IEXC).
23	AIN6/IEXC	ADC Analog Input 6/Excitation Current Source. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN6). This pin can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1 (IEXC).
24	AIN7/VBIAS0/IEXC/EXTREF2IN+	ADC Analog Input 7/Bias Voltage Output/Excitation Current Source/External Reference 2 Positive Input. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN7). This pin can also be configured as an analog output pin to generate a bias voltage, VBIAS0 of AVDD_REG/2 (VBIAS0); as the output pin for Excitation Current Source 0 or Excitation Current Source 1 (IEXC); or as the positive input for External Reference 2 (EXTREF2IN+).
25	AIN8/EXTREF2IN−	ADC Analog Input 8/External Reference 2 Negative Input. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN8). This pin can also be configured as the negative input for External Reference 2 (EXTREF2IN−).
26	AIN9/DACBUFF+	ADC Analog Input 9/Noninverting Input to the DAC Output Buffer. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN9). This pin can also be configured as the noninverting input to the DAC output buffer when the DAC is configured for NPN mode (DACBUFF+).
27	AIN10	ADC Analog Input 10. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode.
28	AIN11/VBIAS1	ADC Analog Input 11/Bias Voltage Output. This pin can be configured as a positive or negative input to either ADC in differential or single-ended mode (AIN11). This pin can also be configured as an analog output pin to generate a bias voltage, VBIAS1 of AVDD_REG/2 (VBIAS1).
29	P0.0/MISO1	General-Purpose Input/Output P0.0/SPI1 Master Input, Slave Output Pin.
30	P0.1/SCLK1/SCL/SIN	General-Purpose Input/Output P0.1/SPI1 Serial Clock Pin/I²C Serial Clock Pin/UART Serial Input (Data Input for the UART Downloader).
31	P0.2/MOSI1/SDA/SOUT	General-Purpose Input/Output P0.2/SPI1 Master Output, Slave Input Pin/I²C Serial Data Pin/ UART Serial Output (Data Output for the UART Downloader).
32	P0.3/IRQ0/$\overline{CS1}$	General-Purpose Input/Output P0.3/External Interrupt Request 0/SPI1 Chip Select Pin (Active Low).
33	P0.4/RTS/ECLKO	General-Purpose Input/Output P0.4/UART Request-to-Send Signal/External Clock Output Pin for Test Purposes.
34	P0.5/CTS/IRQ1	General-Purpose Input/Output P0.5/UART Clear-to-Send Signal/External Interrupt Request 1.
35	P0.6/IRQ2/SIN	General-Purpose Input/Output P0.6/External Interrupt Request 2/UART Serial Input. Not used by UART downloader.
36	P0.7/POR/SOUT	General-Purpose Input/Output P0.7/Power-On Reset Pin (Active High)/UART Serial Output. Not used by UART downloader.
37	IOVDD	Digital System Supply Pin. This pin must be connected to DGND via a 0.1 µF capacitor.
38	P1.0/IRQ3/PWMSYNC/EXTCLK	General-Purpose Input/Output P1.0/External Interrupt Request 3/PWM External Synchronization Input/External Clock Input Pin.
39	P1.1/IRQ4/PWMTRIP/DTR	General-Purpose Input/Output P1.1/External Interrupt Request 4/PWM External Trip Input/ UART Data Terminal Ready Pin.
40	P1.2/PWM0/RI	General-Purpose Input/Output P1.2/PWM0 Output/UART Ring Indicator Pin.
41	P1.3/PWM1/DSR	General-Purpose Input/Output P1.3/PWM1 Output/UART Data Set Ready Pin.
42	P1.4/PWM2/MISO0	General-Purpose Input/Output P1.4/PWM2 Output/SPI0 Master Input, Slave Output Pin.

Pin No.	Mnemonic	Description
43	P1.5/IRQ5/PWM3/SCLK0	General-Purpose Input/Output P1.5/External Interrupt Request 5/PWM3 Output/SPI0 Serial Clock Pin.
44	P1.6/IRQ6/PWM4/MOSI0	General-Purpose Input/Output P1.6/External Interrupt Request 6/PWM4 Output/SPI0 Master Output, Slave Input Pin.
45	P1.7/IRQ7/PWM5/$\overline{CS0}$	General-Purpose Input/Output P1.7/External Interrupt Request 7/PWM5 Output/SPI0 Chip Select Pin (Active Low).
46	P2.0/SCL/UARTCLK	General-Purpose Input/Output P2.0/I^2C Serial Clock Pin/Input Clock Pin for UART Block Only.
47	SWCLK	Serial Wire Debug Clock Input Pin.
48	SWDIO	Serial Wire Debug Data Input/Output Pin.
	EP	Exposed Pad. The LFCSP has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

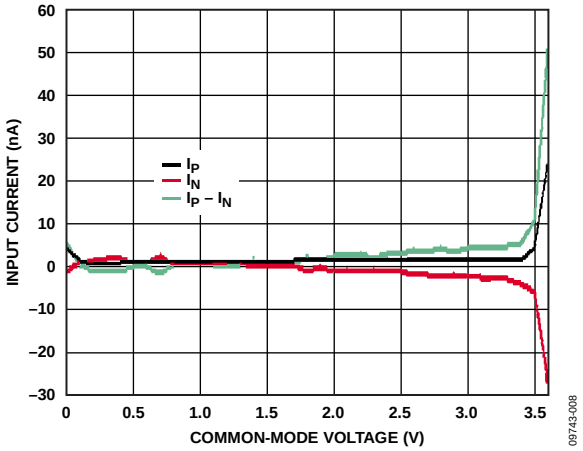


Figure 9. Input Current vs. Common-Mode Voltage (V_{CM}), Gain = 4, ADC Input = 250 mV, AVDD = 3.6 V, T_A = 25°C, V_{CM} = ((AIN+) + (AIN−))/2

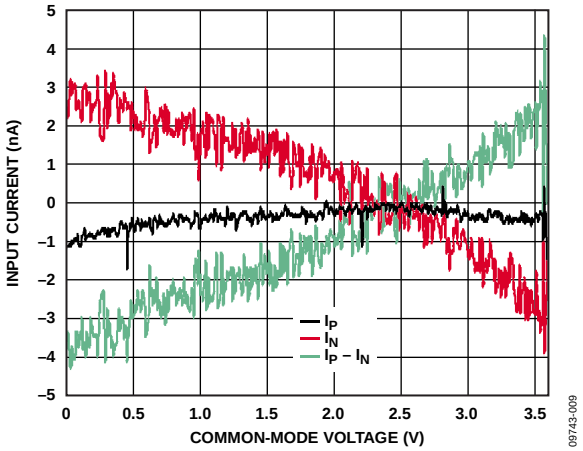


Figure 10. Input Current vs. Common-Mode Voltage (V_{CM}), Gain = 128, ADC Input = 7.8125 mV, AVDD = 3.6 V, T_A = 25°C, V_{CM} = ((AIN+) + (AIN−))/2

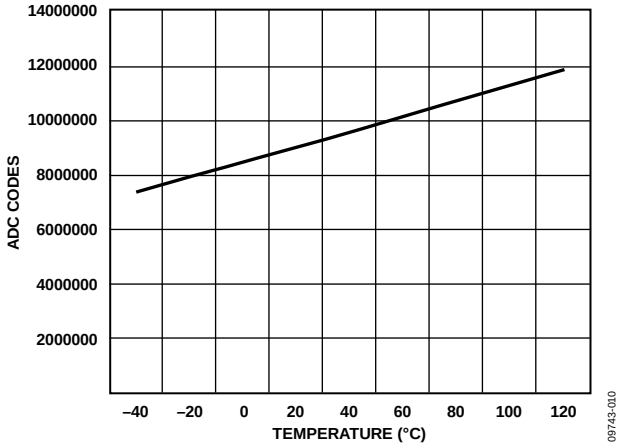


Figure 11. ADC Codes (Decimal Values) vs. Die Temperature Measurements are for the Temperature Sensor Only

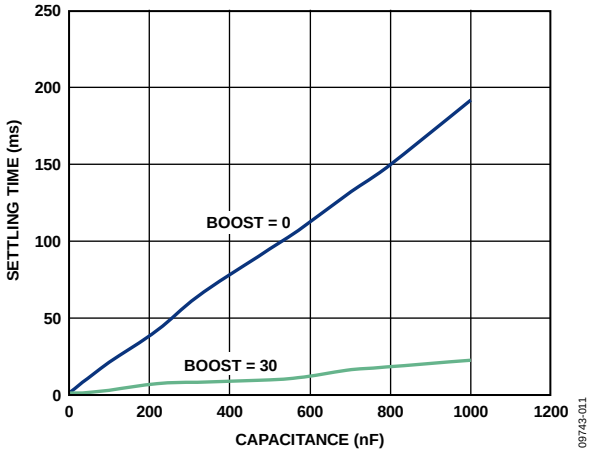


Figure 12. VBIAS Output Settling Time vs. Load Capacitance, T_A = 25°C, IOVDD and AVDD = 3.3 V

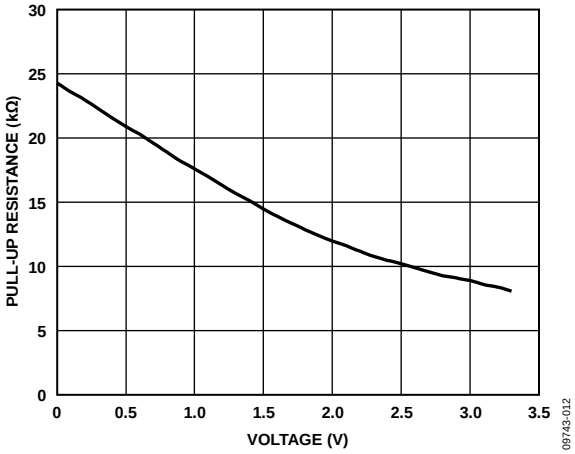


Figure 13. Digital Input Pin Pull-Up Resistance Value vs. Voltage Applied to Digital Pin, T_A = 25°C, IOVDD = 3.4 V

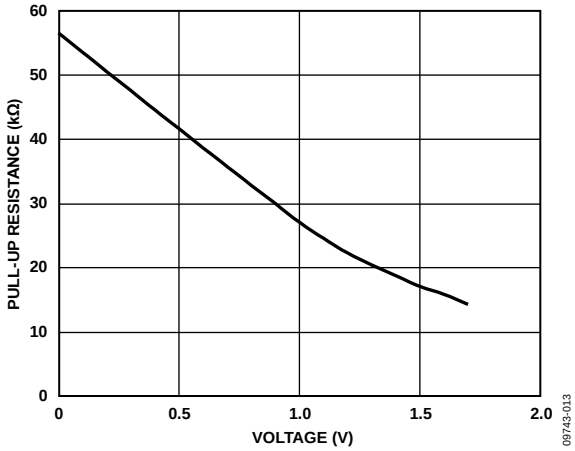


Figure 14. Digital Input Pin Pull-Up Resistance Value vs. Voltage Applied to Digital Pin, T_A = 25°C, IOVDD = 1.8 V

TYPICAL SYSTEM CONFIGURATION

Figure 15 shows a typical ADuCM360/ADuCM361 configuration. This figure illustrates some of the hardware considerations. The bottom of the LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to DGND. The metal plate of the PCB can be connected to ground. The 0.47 µF capacitor on the AVDD_REG and DVDD_REG pins should be placed as close to the pins as possible. In noisy environments, an additional 1 nF capacitor can be added to IOVDD and AVDD.

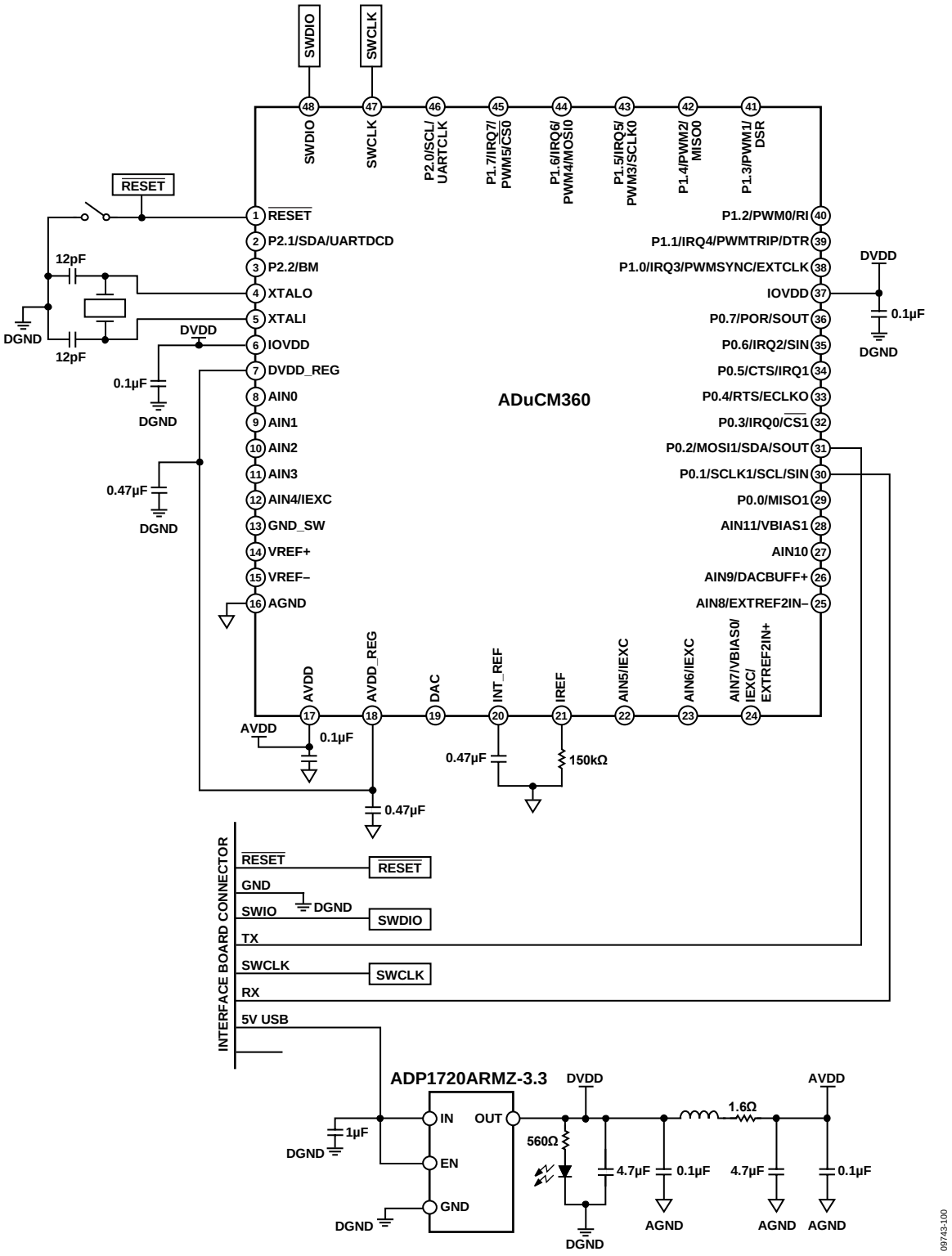


Figure 15. Typical System Configuration

OUTLINE DIMENSIONS

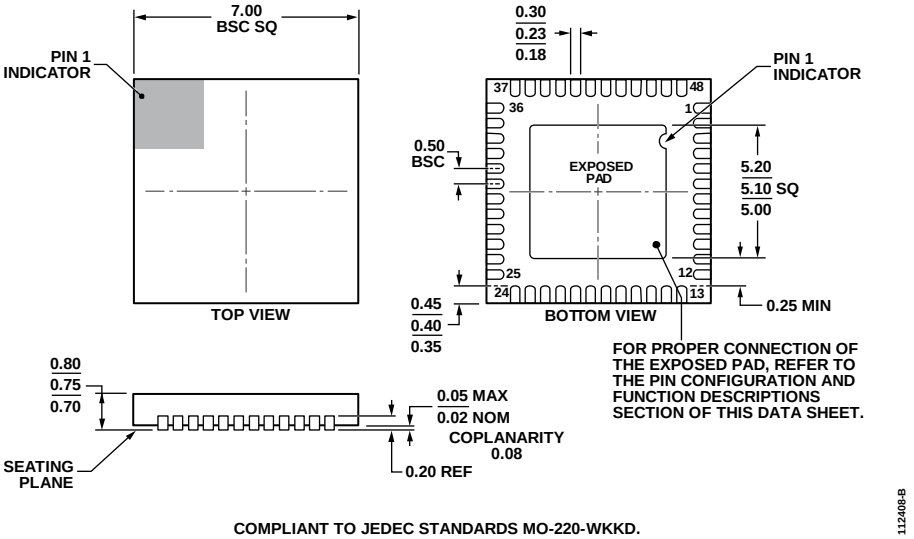


Figure 16. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	ADCs	Flash/SRAM	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuCM360BCPZ128	Dual 24-Bit	128 kB/8 kB	−40°C to +125°C	48-Lead LFCSP_WQ	CP-48-4	
ADuCM360BCPZ128-R7	Dual 24-Bit	128 kB/8 kB	−40°C to +125°C	48-Lead LFCSP_WQ	CP-48-4	750
ADuCM361BCPZ128	Single 24-Bit	128 kB/8 kB	−40°C to +125°C	48-Lead LFCSP_WQ	CP-48-4	
ADuCM361BCPZ128-R7	Single 24-Bit	128 kB/8 kB	−40°C to +125°C	48-Lead LFCSP_WQ	CP-48-4	750
EVAL-ADuCM360QSPZ				ADuCM360 QuickStart Plus Development System		

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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