Dual-Channel Digital Isolator

Data Sheet

ADuM1200-EP

FEATURES

- Narrow body, 8-lead SOIC package
- Low power operation
  - 5 V operation
    - 1.1 mA per channel maximum at 0 Mbps to 2 Mbps
    - 3.7 mA per channel maximum at 10 Mbps
    - 8.2 mA per channel maximum at 25 Mbps
  - 3 V operation
    - 0.8 mA per channel maximum at 0 Mbps to 2 Mbps
    - 2.2 mA per channel maximum at 10 Mbps
    - 4.8 mA per channel maximum at 25 Mbps
- Precise timing characteristics
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
    - V_{IORM} = 560 V peak

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Size-critical multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceiver isolation
- Digital field bus isolation

GENERAL DESCRIPTION

The ADuM1200-EP[1] is a dual-channel, digital isolator based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technologies, this isolation component provides outstanding performance characteristics superior to alternatives, such as optocouplers.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM1200-EP isolator provides two independent isolation channels with a supply voltage on either side ranging from 3.0 V to 5.5 V. In addition, the ADuM1200-EP provides low pulse width distortion and tight channel-to-channel matching. Unlike other optocoupler alternatives, the ADuM1200-EP isolator has a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/ power-down conditions.

Full details about this enhanced product are available in the ADuM1200/ADuM1201 data sheet, which should be consulted in conjunction with this data sheet.

FUNCTIONAL BLOCK DIAGRAM

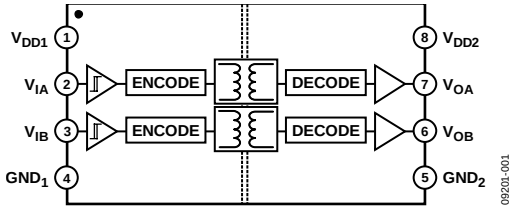


Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. B
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TABLE OF CONTENTS

Features ... 1
Enhanced Product Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Electrical Characteristics—5 V operation ... 3
Electrical Characteristics—3 V operation ... 5
Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation ... 6
Package Characteristics ... 8
Regulatory Information ... 8
Insulation and Safety-Related Specifications ... 8
DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 Insulation Characteristics ... 9
Recommended Operating Conditions ... 9
Absolute Maximum Ratings ... 10
ESD Caution ... 10
Pin Configuration and Function Descriptions ... 11
Typical Performance Characteristics ... 12
Outline Dimensions ... 13
Ordering Guide ... 13

REVISION HISTORY

2/14—Rev. A to Rev. B

Changed +105°C to +125°C in Operating Temperature Range ... Throughout
Changed Minimum V_{DDx} from 2.7 V to 3.0 V ... Throughout
Changes to Table 6 ... 8
Changes to Table 7 ... 9
Changes to Table 10 ... 10

5/12—Rev. 0 to Rev. A

Removed RoHS-Compliant from Features Section ... 1
Changed ADuM1200WSRZ55 to ADuM1200UR-EP, Table 5 ... 8
Changes to Ordering Guide ... 13

7/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground; 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.60	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.30	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		4.3	5.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.3	2.0	mA	5 MHz logic signal frequency
25 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		10	13	mA	12.5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		2.8	3.4	mA	12.5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	μA	
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		45	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			3	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DD1}, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.19		mA/ Mbps	
Output	$I_{DDO (D)}$		0.05		mA/ Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.20	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	3.4	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.1	mA	5 MHz logic signal frequency
25 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		5.2	7.7	mA	12.5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.5	2.0	mA	12.5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	μA	
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		55	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Propagation Delay Skew[5]	t_{PSK}			16	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			3	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DD1}, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.10		mA/ Mbps	
Output	$I_{DDO (D)}$		0.03		mA/ Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground; 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = 3.0 V, V_{DD2} = 5.0 V; or V_{DD1} = 5.0 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.6	mA	
3 V/5 V Operation			0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.11	0.20	mA	
3 V/5 V Operation			0.19	0.25	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.1	1.4	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			0.6	1.0	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.2	0.6	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			0.5	0.8	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			4.3	5.5	mA	5 MHz logic signal frequency
3 V/5 V Operation			2.2	3.4	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.7	1.1	mA	5 MHz logic signal frequency
3 V/5 V Operation			1.3	2.0	mA	5 MHz logic signal frequency
25 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			10	13	mA	12.5 MHz logic signal frequency
3 V/5 V Operation			5.2	7.7	mA	12.5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			1.5	2.0	mA	12.5 MHz logic signal frequency
3 V/5 V Operation			2.8	3.4	mA	12.5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	μA	
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD			3	ns	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			3	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/ Mbps	
3 V/5 V Operation			0.10		mA/ Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO(D)}$					
5 V/3 V Operation			0.03		mA/ Mbps	
3 V/5 V Operation			0.05		mA/ Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1, Pin, 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM1200-EP is approved by the organizations listed in Table 5. See Table 10 for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

UL	CSA	VDE
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM1200UR-EP is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1200UR-EP is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Clearance in the Plane of the PCB	CL_{PCB}	4.5	mm min	Measured from input terminals to output terminals, shortest line of sight distance through air in the plane of the PCB
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. Note that the * marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 second, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 seconds, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 seconds, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

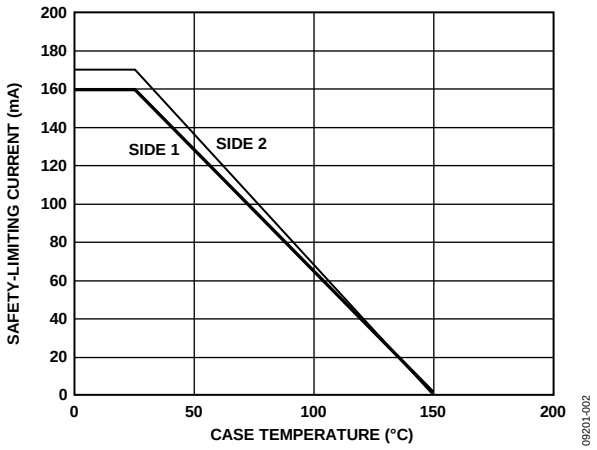


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Rating
Operating Temperature (T_A)	−55°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−55°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin (I_O)[3]	−11 mA to +11 mA
Common-Mode Transients (CM_L, CM_H)[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 2 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage,			
Bipolar Waveform	565	V_{PEAK}	50-year minimum lifetime
Unipolar Waveform	1131	V_{PEAK}	50-year minimum lifetime
DC Voltage	1131	V_{PEAK}	50-year minimum lifetime

[1]Refers to continuous voltage magnitude imposed across the isolation barrier.

Table 11. Truth Table (Positive Logic)

V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DD2} State	V_{OA} Output[1]	V_{OB} Output[1]	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

[1] H = high, L = low, X = undetermined/not relevant.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

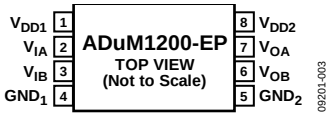


Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

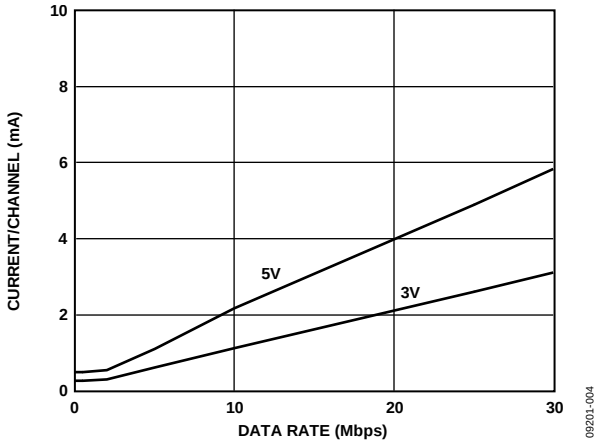


Figure 4. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

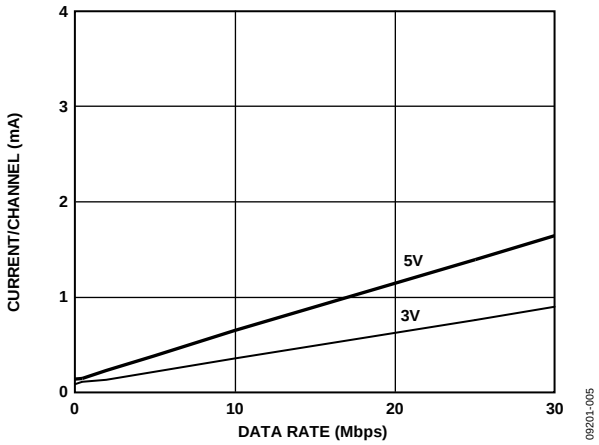


Figure 5. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

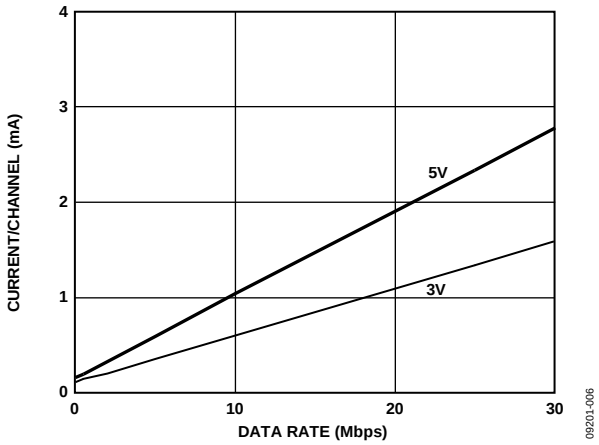


Figure 6. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

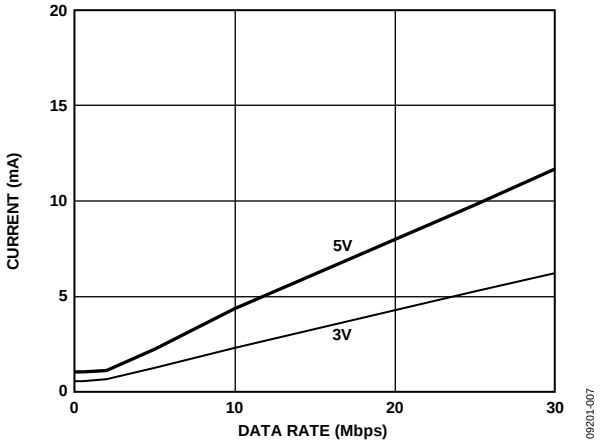


Figure 7. Typical V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

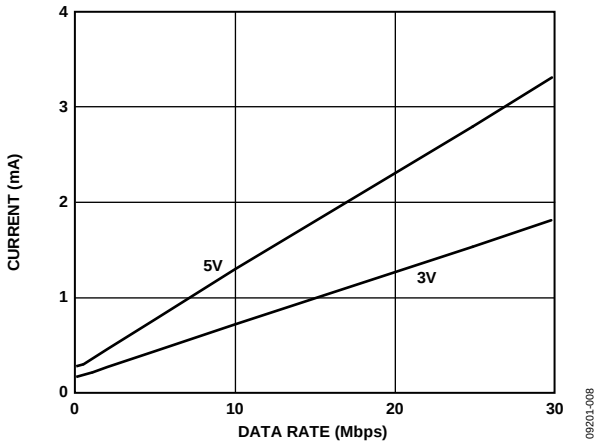


Figure 8. Typical V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

OUTLINE DIMENSIONS

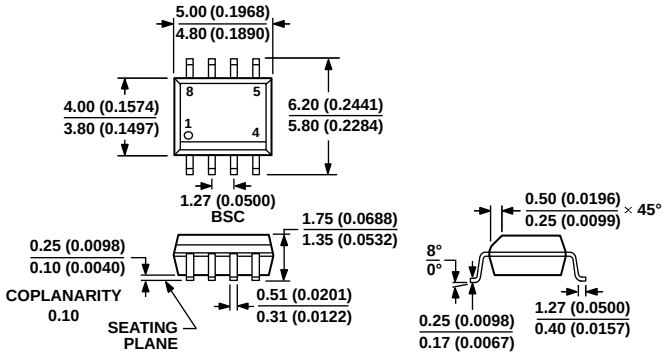


Figure 9. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM1200UR-EP	2	0	25	45	3	−55°C to +125°C	8-Lead SOIC_N	R-8
ADuM1200UR-EP-RL7	2	0	25	45	3	−55°C to +125°C	8-Lead SOIC_N	R-8

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