Data Sheet

ADuM1400/ADuM1401/ADuM1402

Quad-Channel Digital Isolators

FEATURES

- Qualified for automotive applications
- Low power operation
  - 5 V operation
    - 1.0 mA per channel maximum at 0 Mbps to 2 Mbps
    - 3.5 mA per channel maximum at 10 Mbps
    - 31 mA per channel maximum at 90 Mbps
  - 3 V operation
    - 0.7 mA per channel maximum at 0 Mbps to 2 Mbps
    - 2.1 mA per channel maximum at 10 Mbps
    - 20 mA per channel maximum at 90 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High temperature operation: 125°C
- High data rate: dc to 90 Mbps (NRZ)
- Precise timing characteristics
  - 2 ns maximum pulse width distortion
  - 2 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/µs
- Output enable function
- 16-lead SOIC wide body package
- RoHS-compliant models available
- Safety and regulatory approvals
  - UL 1577:
    - V_{ISO}= 2500 V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - EN 60950-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 560 V peak

APPLICATIONS

- General-purpose multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation
- Automotive systems

GENERAL DESCRIPTION

The ADuM1400/ADuM1401/ADuM1402[1] are quad-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one tenth to one sixth of the power of optocouplers at comparable signal data rates.

The ADuM1400/ADuM1401/ADuM1402 isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM1400/ADuM1401/ADuM1402 provide low pulse width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM1400/ADuM1401/ADuM1402 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and when power is not applied to one of the supplies.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

Rev. M

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 3
Specifications ... 4
  Electrical Characteristics—5 V, 105°C Operation ... 4
  Electrical Characteristics—3 V, 105°C Operation ... 6
  Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V, 105°C Operation ... 8
  Electrical Characteristics—5 V, 125°C Operation ... 12
  Electrical Characteristics—3 V, 125°C Operation ... 14
  Electrical Characteristics—Mixed 5 V/3 V, 125°C Operation ... 16
  Electrical Characteristics—Mixed 3 V/5 V, 125°C Operation ... 18
  Package Characteristics ... 20
  Regulatory Information ... 20
  Insulation and Safety Related Specifications ... 21
  DIN EN IEC 60747-17 (VDE V 0884-17) Insulation Characteristics ... 21
  Recommended Operating Conditions ... 22
Absolute Maximum Ratings ... 23
  ESD Caution ... 23
  Maximum Continuous Working Voltage ... 23
  Truth Table (Positive Logic) ... 23
Pin Configurations and Function Descriptions ... 24
Typical Performance Characteristics ... 26
Applications Information ... 28
  PC Board Layout ... 28
  Propagation Delay-Related Parameters ... 28
  DC Correctness and Magnetic Field Immunity ... 28
  Power Consumption ... 29
  Insulation Lifetime ... 29
Outline Dimensions ... 31
  Ordering Guide ... 31
  Number of Inputs, V_{DD1} Side and V_{DD2} Side Options ... 31
  Maximum Data Rate, Maximum Propagation Delay, and Maximum Pulse Width Distortion Options ... 32
  Evaluation Boards ... 33
  Automotive Products ... 33

REVISION HISTORY

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Changes to Features Section ... 1
Moved Figure 1 to Figure 3 ... 3
Changes to Regulatory Information Section and Table 9 ... 20
Changes to Table 10 ... 21
Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE V 0884-10) Insulation Characteristics Section ... 21
Changes to DIN EN IEC 60747-17 (VDE V 0884-10) Insulation Characteristics Section, Table 11, and Figure 4 Caption ... 21
Changes to Table 14 ... 23
Changes to Insulation Lifetime Section ... 29
Deleted Figure 21 to Figure 23; Renumbered Sequentially ... 29
Added Number of Inputs, V_{DD1} Side and V_{DD2} Side Options ... 31
Added Maximum Data Rate, Maximum Propagation Delay, and Maximum Pulse Width Distortion Options ... 32

FUNCTIONAL BLOCK DIAGRAMS

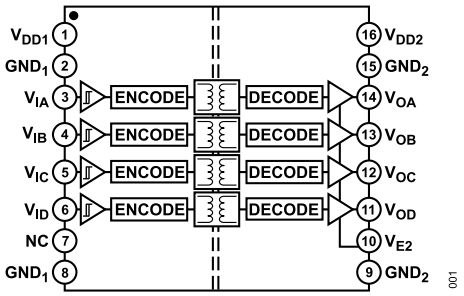


Figure 1. ADuM1400

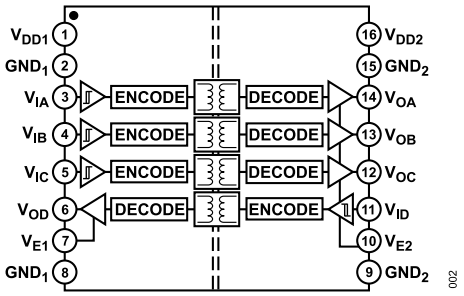


Figure 2. ADuM1401

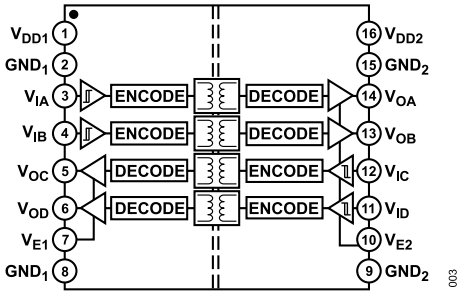


Figure 3. ADuM1402

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		8.6	10.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		70	100	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		7.1	9.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		57	82	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		31	43	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (90)}$, $I_{DD2 (90)}$		44	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	4.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400ARW/ADuM1401ARW/ADuM1402ARW						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400BRW/ADuM1401BRW/ADuM1402BRW						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	32	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM1400CRW/ADuM1401CRW/ADuM1402CRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	18	27	32	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			10	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

SPECIFICATIONS

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION

2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM1400 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	2.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		37	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		11	15	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.2	3.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		30	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		18	27	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{DD1} or V_{DD2} Supply Current	$I_{DD1\ (10)}$, $I_{DD2\ (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1\ (90)}$, $I_{DD2\ (90)}$		24	39	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC},I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH},	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
	V_{OBH},V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.4	2.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL},		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
	V_{OCL}, V_{ODL}		0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400ARW/ADuM1401ARW/ADuM1402ARW						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	75	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400BRW/ADuM1401BRW/ADuM1402BRW						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	38	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM1400CRW/ADuM1401CRW/ADuM1402CRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			16	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1} or V_{DD2}, V_{CM} = 1000 V,transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.10		mA/ Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.03		mA/ Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V, 105°C OPERATION

5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.0 V. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			70	100	mA	45 MHz logic signal freq.
3 V/5 V Operation			37	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation			18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			57	82	mA	45 MHz logic signal freq.
3 V/5 V Operation			30	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			18	27	mA	45 MHz logic signal freq.
3 V/5 V Operation			31	43	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			44	62	mA	45 MHz logic signal freq.
3 V/5 V Operation			24	39	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			24	39	mA	45 MHz logic signal freq.
3 V/5 V Operation			44	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	(V_{DD1} or V_{DD2})		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	(V_{DD1} or V_{DD2}) − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400ARW/ADuM1401ARW/ADuM1402ARW						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	70	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/ t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400BRW/ADuM1401BRW/ADuM1402BRW						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	15	35	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM1400CRW/ADuM1401CRW/ADuM1402CRW						
Minimum Pulse Width[2]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	30	40	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			14	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					C_L = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[7]	$\lvert CM_H \rvert$	25	35		kV/µs	V_{Ix} = V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\lvert CM_L \rvert$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

SPECIFICATIONS

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		8.6	10.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		7.1	9.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	4.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400WSRWZ/ADuM1401WSRWZ/ ADuM1402WSRWZ						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 4. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400WTRWZ/ADuM1401WTRWZ/ ADuM1402WTRWZ						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	18	27	34	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION

3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM1400W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	2.0	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.2	3.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH},	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
	V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.4	2.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400WSRWZ/ADuM1401WSRWZ/ ADuM1402WSRWZ						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	75	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400WTRWZ/ADuM1401WTRWZ/ ADuM1402WTRWZ						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\lvert CM_H \rvert$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V,transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\lvert CM_L \rvert$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 125°C OPERATION

4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 5 V, V_{DD2} = 3.0 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM1400W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		8.6	10.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	2.0	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		7.1	9.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.2	3.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		5.6	7.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	V_{DD1}, V_{DD2} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400WSRWZ/ADuM1401WSRWZ/ ADuM1402WSRWZ						

SPECIFICATIONS

Table 6. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	70	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400WTRWZ/ADuM1401WTRWZ/ ADuM1402WTRWZ						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	30	40	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

SPECIFICATIONS

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 125°C OPERATION

3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions. All voltages are relative to their respective ground.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	V_{DD1}, V_{DD2}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.4	V_{DD1}, V_{DD2} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1400WSRWZ/ADuM1401WSRWZ/ ADuM1402WSRWZ						
Minimum Pulse Width[2]	PW			1000	ns	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Data Rate[3]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	50	70	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM1400WTRWZ/ADuM1401WTRWZ/ ADuM1402WTRWZ						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20	30	40	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

SPECIFICATIONS

[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Case Thermal Resistance, Side 1	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
IC Junction to Case Thermal Resistance, Side 2	θ_{JCO}		28		°C/W	

[1] Device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM1400/ADuM1401/ADuM1402 approvals are listed in Table 9. Refer to Table 14 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 9.

UL	CSA	VDE	CQC	TÜV
UL 1577[1] Single Protection, 2500 V rms	IEC/EN/CSA 62368-1 Basic insulation, 600 V rms Reinforced insulation, 150 V rms IEC/CSA 61010-1 Basic insulation (1 MOPP), 490 V rms Reinforced insulation (2 MOPP), 150 V rms IEC/CSA 61010-1 Reinforced insulation, 150 V rms	DIN EN IEC 60747-17 (VDE 0884-17)[2] Reinforced insulation, 560 V peak	CQC GB4943.1 Basic insulation, 415 V rms	EN 60950-1 Basic insulation, 770 V rms Reinforced insulation, 385 V rms
File E214100	File No. 205078	Certificate No. 40011599	Certificate No. CQC14001114900	Certificate No. U8V 17 04 56232 019

[1] In accordance with UL 1577, each ADuM1400/ADuM1401/ADuM1402 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 µA).

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM1400/ADuM1401/ADuM1402 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17).

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 10.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L(I01)	7.8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)[1]	L(I02)	7.8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, and line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		18	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)[3]	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

[1] In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

[3] CTI rating for the ADuM1400/ADuM1401/ADuM1402 is >400 V and a Material Group II isolation group.

DIN EN IEC 60747-17 (VDE V 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on packages denotes DIN EN IEC 60747-17 (VDE V 0884-10) approval.

Table 11.

Description	Conditions	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
≤ 150 V rms			I to IV	
≤ 300 V rms			I to III	
≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	560	V peak
Maximum Working Insulation Voltage		V_{IOWM}	396	V rms
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$	896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Maximum Transient Isolation Voltage	$V_{TEST} = 1.2 \times V_{IOTM}$, t =1s (100% production)	V_{IOTM}	4000	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	4000	V peak
Maximum Surge Isolation Voltage	$V_{TEST} \geq 1.3 \times V_{IMP}$ (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

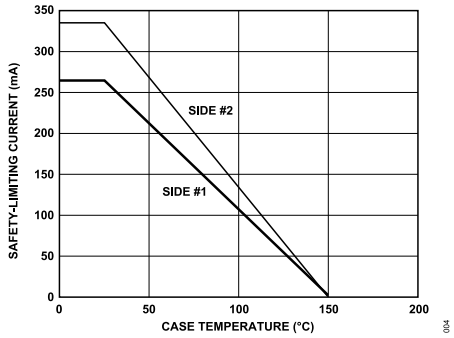


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE V 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Rating
Operating Temperature (T_A)[1]	−40°C to +105°C
Operating Temperature (T_A)[2]	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1, 3]	2.7 V to 5.5 V
Supply Voltages (V_{DD1}, V_{DD2})[2, 3]	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

[1] Does not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

[2] Applies to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

[3] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 13.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)[1]	−40°C to +105°C
Ambient Operating Temperature (T_A)[2]	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[3]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})[3, 4]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[3, 4]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[5]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2 (I_{O2})	−22 mA to +22 mA
Common-Mode Transients[6]	−100 kV/µs to +100 kV/µs

1 Does not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

2 Applies to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

3 All voltages are relative to their respective ground.

4 V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.

5 See Figure 4 for maximum rated current values for various temperatures.

6 This refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 14. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	560	V peak	Reinforced insulation rating as per IEC 60747-17 (VDE 0884-17)

1 Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

TRUTH TABLE (POSITIVE LOGIC)

Table 15. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{Ex} Input[1, 2]	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration if the V_{Ex} state is H or NC. Outputs return to a high impedance state within 8 ns of V_{DDO} power restoration if the V_{Ex} state is L.

1 V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

2 In noisy environments, connecting V_{Ex} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

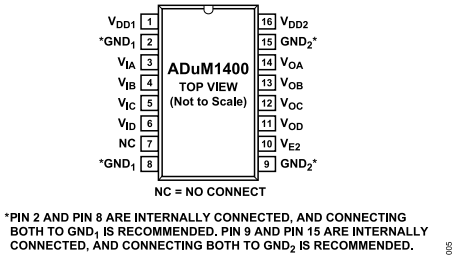


Figure 5. ADuM1400 Pin Configuration

Table 16. ADuM1400 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NC	No Connect.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

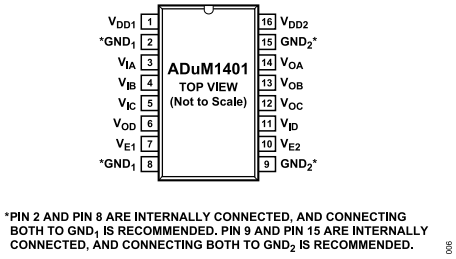


Figure 6. ADuM1401 Pin Configuration

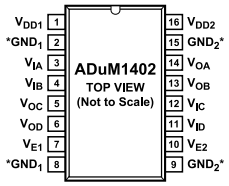
Table 17. ADuM1401 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OD} output is enabled when V_{E1} is high or disconnected. V_{OD} is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 17. ADuM1401 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2.



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 7. ADuM1402 Pin Configuration

Table 18. ADuM1402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OC} and V_{OD} outputs are enabled when V_{E1} is high or disconnected. V_{OC} and V_{OD} outputs are disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

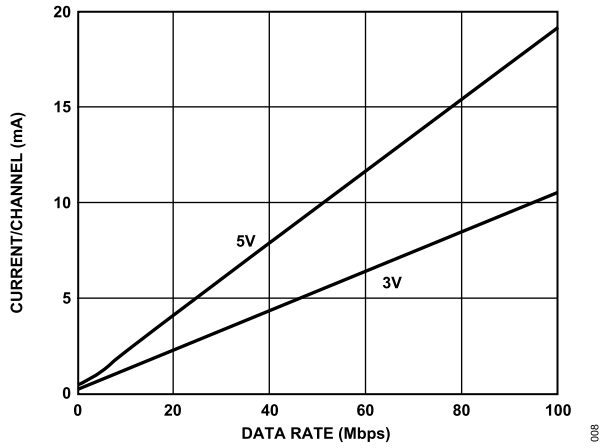


Figure 8. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

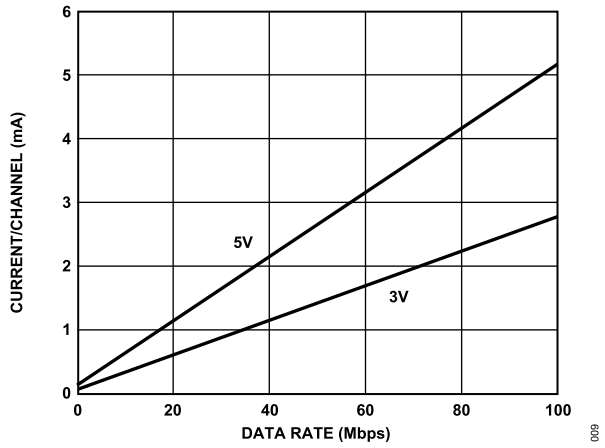


Figure 9. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

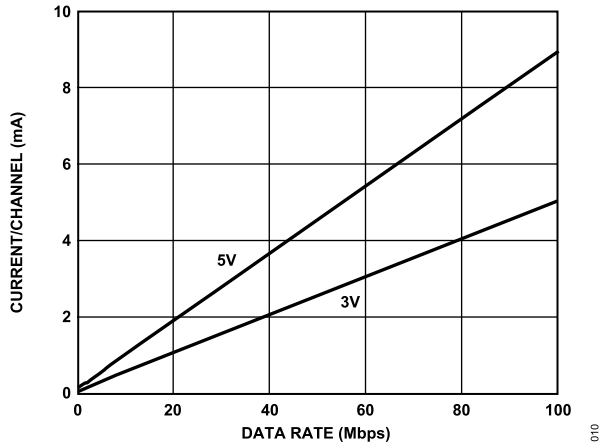


Figure 10. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

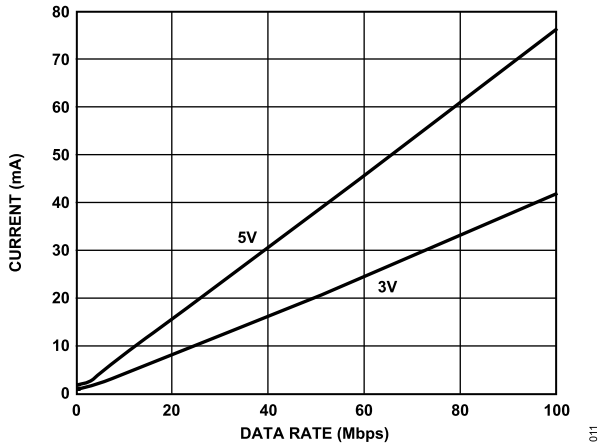


Figure 11. Typical ADuM1400 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

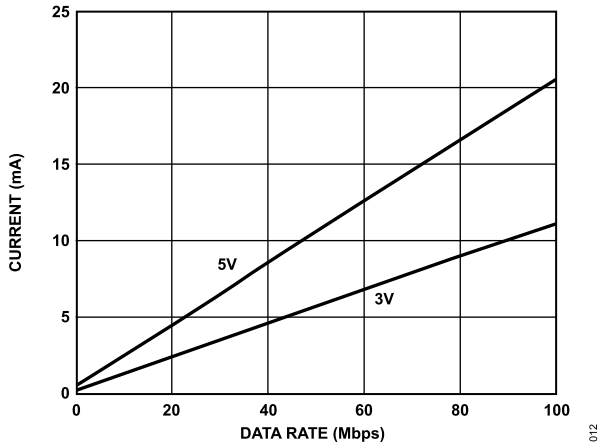


Figure 12. Typical ADuM1400 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

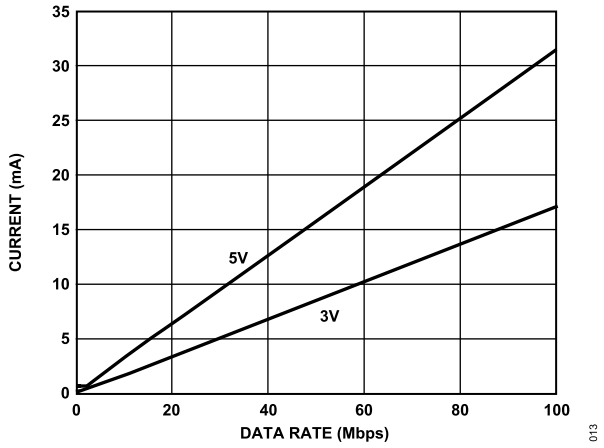


Figure 13. Typical ADuM1401 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

TYPICAL PERFORMANCE CHARACTERISTICS

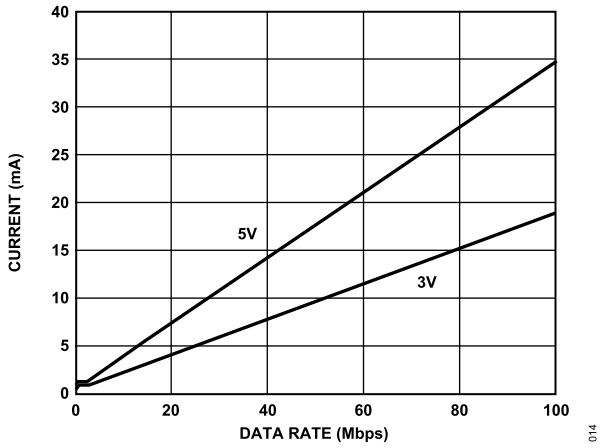


Figure 14. Typical ADuM1401 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

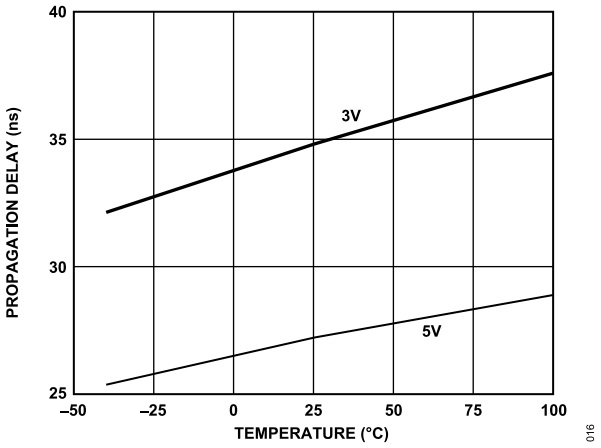


Figure 16. Propagation Delay vs. Temperature, C Grade

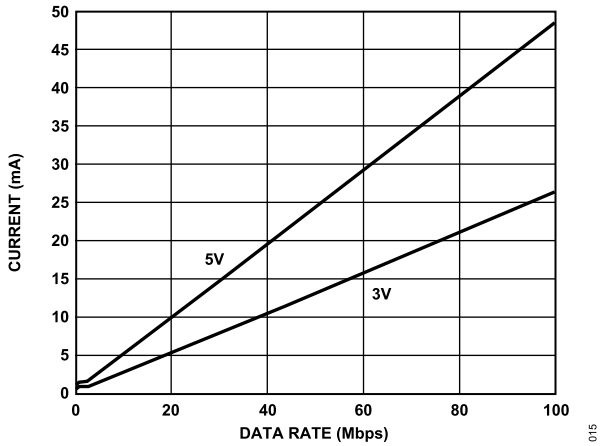


Figure 15. Typical ADuM1402 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM1400/ADuM1401/ADuM1402 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered, unless the ground pair on each package side is connected close to the package.

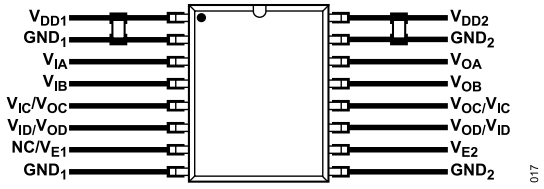


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

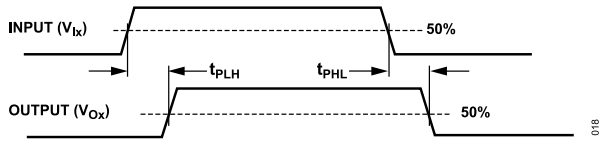


Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM1400/ADuM1401/ADuM1402 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM1400/ADuM1401/ADuM1402 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 15) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM1400/ADuM1401/ADuM1402 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM1400/ADuM1401/ADuM1402 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\prod r_n^2;\ n = 1, 2, \ldots, N \quad (1)$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1400/ADuM1401/ADuM1402 and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

APPLICATIONS INFORMATION

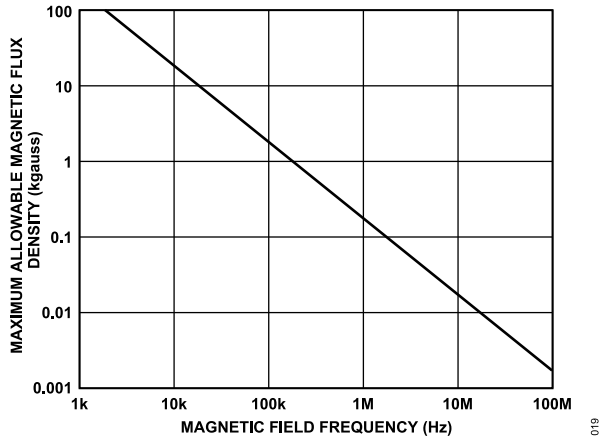


Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM1400/ADuM1401/ADuM1402 transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM1400/ADuM1401/ADuM1402 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM1400/ADuM1401/ADuM1402 to affect the operation of the component.

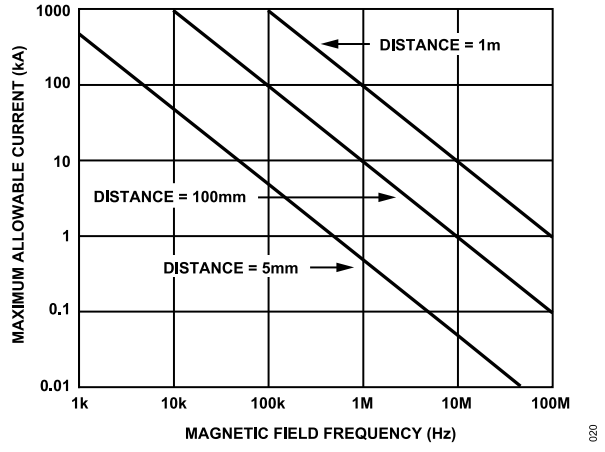


Figure 20. Maximum Allowable Current for Various Current-to-ADuM1400/ADuM1401/ADuM1402 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1400/ADuM1401/ADuM1402 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \quad f \leq 0.5\ f_r \tag{2}$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \quad f > 0.5\ f_r \tag{3}$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \quad f \leq 0.5\ f_r \tag{4}$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \quad f > 0.5\ f_r \tag{5}$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1400/ADuM1401/ADuM1402.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 14 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at

APPLICATIONS INFORMATION

working voltages higher than the service life voltage listed leads to premature insulation failure.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RW-16	SOIC_W	16-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2, 3, 4]	Temperature Range	Package Description	Package Option
ADuM1400ARW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400BRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400CRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400ARWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400BRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400CRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400WSRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1400WTRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1401ARW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401BRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401CRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401ARWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401BRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401CRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401WSRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1401WTRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1402ARW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402BRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402CRW	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402ARWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402BRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402CRWZ	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402WSRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1402WTRWZ	−40°C to +125°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

[3] Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

[4] No tape and reel option is available for the ADuM1400CRW or ADuM1402BRW models.

NUMBER OF INPUTS, V_{DD1} SIDE AND V_{DD2} SIDE OPTIONS

Model[1, 2, 3, 4]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side
ADuM1400ARW	4	0
ADuM1400BRW	4	0
ADuM1400CRW	4	0
ADuM1400ARWZ	4	0
ADuM1400BRWZ	4	0
ADuM1400CRWZ	4	0
ADuM1400WSRWZ	4	0
ADuM1400WTRWZ	4	0
ADuM1401ARW	3	1

OUTLINE DIMENSIONS

Model[1, 2, 3, 4]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side
ADuM1401BRW	3	1
ADuM1401CRW	3	1
ADuM1401ARWZ	3	1
ADuM1401BRWZ	3	1
ADuM1401CRWZ	3	1
ADuM1401WSRWZ	3	1
ADuM1401WTRWZ	3	1
ADuM1402ARW	2	2
ADuM1402BRW	2	2
ADuM1402CRW	2	2
ADuM1402ARWZ	2	2
ADuM1402BRWZ	2	2
ADuM1402CRWZ	2	2
ADuM1402WSRWZ	2	2
ADuM1402WTRWZ	2	2

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

[3] Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

[4] No tape and reel option is available for the ADuM1400CRW or ADuM1402BRW models.

MAXIMUM DATA RATE, MAXIMUM PROPAGATION DELAY, AND MAXIMUM PULSE WIDTH DISTORTION OPTIONS

Model[1, 2, 3, 4]	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)
ADuM1400ARW	1	100	40
ADuM1400BRW	10	50	3
ADuM1400CRW	90	32	2
ADuM1400ARWZ	1	100	40
ADuM1400BRWZ	10	50	3
ADuM1400CRWZ	90	32	2
ADuM1400WSRWZ	1	100	40
ADuM1400WTRWZ	10	34	3
ADuM1401ARW	1	100	40
ADuM1401BRW	10	50	3
ADuM1401CRW	90	32	2
ADuM1401ARWZ	1	100	40
ADuM1401BRWZ	10	50	3
ADuM1401CRWZ	90	32	2
ADuM1401WSRWZ	1	100	40
ADuM1401WTRWZ	10	34	3
ADuM1402ARW	1	100	40
ADuM1402BRW	10	50	3
ADuM1402CRW	90	32	2
ADuM1402ARWZ	1	100	40
ADuM1402BRWZ	10	50	3
ADuM1402CRWZ	90	32	2
ADuM1402WSRWZ	1	100	40
ADuM1402WTRWZ	10	34	3

OUTLINE DIMENSIONS

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

[3] Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

[4] No tape and reel option is available for the ADuM1400CRW or ADuM1402BRW models.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuMQSEBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM1400W/ADuM1401W/ADuM1402W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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