Dual-Channel, 2.5 kV Isolators with Integrated DC-to-DC Converter

Data Sheet

ADuM5200/ADuM5201/ADuM5202

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- Regulated 3.3 V or 5 V output
- Up to 500 mW output power
- Dual, dc-to-25 Mbps (NRZ) signal isolation channels
- 16-lead SOIC package with 7.6 mm creepage
- High temperature operation: 105°C maximum
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A)
  - VDE certificate of conformity (pending)
    - IEC 60747-5-2 (VDE 0884, Part 2):2003-01
    - V_{IORM} = 560 V_{PEAK}

APPLICATIONS

- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation
- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Industrial PLCs

GENERAL DESCRIPTION

The ADuM5200/ADuM5201/ADuM5202[1] are dual-channel digital isolators with isoPower®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides up to 500 mW of regulated, isolated power at either 5.0 V or 3.3 V from a 5.0 V input supply, or 3.3 V from a 3.3 V supply at the power levels shown in Table 1. These devices eliminate the need for a separate, isolated dc-to-dc converter in low power isolated designs. The *i*Coupler chip scale transformer technology is used to isolate the logic signals and for the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

The ADuM5200/ADuM5201/ADuM5202 isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide for more information).

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

FUNCTIONAL BLOCK DIAGRAMS

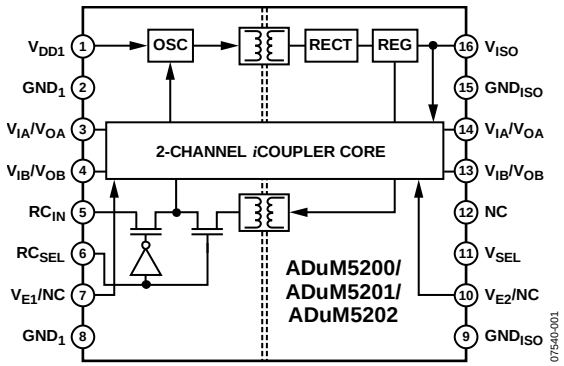


Figure 1.

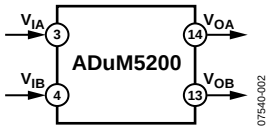


Figure 2. ADuM5200

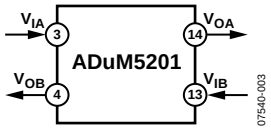


Figure 3. ADuM5201

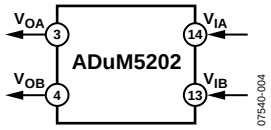


Figure 4. ADuM5202

Table 1. Power Levels

Input Voltage (V)	Output Voltage (V)	Output Power (mW)
5.0	5.0	500
5.0	3.3	330
3.3	3.3	200

Rev. B

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REVISION HISTORY

5/12—Rev. A to Rev. B

Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section ... 1
Updated Outline Dimensions ... 25

9/11—Rev. 0 to Rev. A

Changes to Product Title, Features Section, and General Description Section ... 1
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10/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{SEL} = V_{ISO}$ = 5 V. Minimum/maximum specifications apply over the entire recommended operation range which is 4.5 V ≤ V_{DD1}, V_{SEL}, V_{ISO} ≤ 5.5 V; and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 2. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	4.7	5.0	5.4	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1		mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
PW Modulation Frequency	f_{PWM}		625		kHz	
Output Supply	$I_{ISO (MAX)}$	100			mA	V_{ISO} > 4.5 V
Efficiency at $I_{ISO (MAX)}$			34		%	I_{ISO} = 100 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1 (Q)}$		8	22	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		290		mA	

Table 3. DC-to-DC Converter Dynamic Specifications

		1 Mbps—A Grade or C Grade			25 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
Input									No V_{ISO} load
ADuM5200	I_{DD1}		6			34		mA	
ADuM5201	I_{DD1}		7			38		mA	
ADuM5202	I_{DD1}		7			41		mA	
Available to Load									
ADuM5200	$I_{ISO (LOAD)}$		100			94		mA	
ADuM5201	$I_{ISO (LOAD)}$		100			92		mA	
ADuM5202	$I_{ISO (LOAD)}$		100			90		mA	

Table 4. Switching Specifications

		A Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	100		45	60	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			6	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature						5		ps/°C	
Pulse Width	PW	1000			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			15	ns	Between any two units
Channel Matching									
Codirectional[1]	t_{PSKCD}			50			6	ns	
Opposing Directional[2]	t_{PSKOD}			50			15	ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

[2] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 5. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO} or 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO} or 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.3 or V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout						V_{DD1}, V_{DDL}, V_{ISO} supplies
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	
Input Currents per Channel	I_I	−20	+0.01	+20	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.7 \times V_{DD1}$ or $0.7 \times V_{ISO}$ for a high output or $V_O < 0.3 \times V_{DD1}$ or $0.3 \times V_{ISO}$ for a low output. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{ISO} = 3.3 V, V_{SEL} = GND_{ISO}. Minimum/maximum specifications apply over the entire recommended operation range which is 3.0 V ≤ V_{DD1}, V_{SEL}, V_{ISO} ≤ 3.6 V; and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 6. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1		mV/V	I_{ISO} = 30 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 6 mA to 54 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 54 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 54 mA
Switching Frequency	f_{OSC}		180		MHz	
PW Modulation Frequency	f_{PWM}		625		kHz	
Output Supply	$I_{ISO (MAX)}$	60			mA	V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			34		%	I_{ISO} = 60 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1 (Q)}$		6	15	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		175		mA	

Table 7. DC-to-DC Converter Dynamic Specifications

		1 Mbps—A Grade or C Grade			25 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
Input									No V_{ISO} load
ADuM5200	I_{DD1}		4			23		mA	
ADuM5201	I_{DD1}		4			25		mA	
ADuM5202	I_{DD1}		5			27		mA	
Available to Load									
ADuM5200	$I_{ISO (LOAD)}$		60			56		mA	
ADuM5201	$I_{ISO (LOAD)}$		60			55		mA	
ADuM5202	$I_{ISO (LOAD)}$		60			54		mA	

Table 8. Switching Specifications

		A Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		60	100		45	60	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			6	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature						5		ps/°C	
Pulse Width	PW	1000			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			45	ns	Between any two units
Channel Matching									
Codirectional[1]	t_{PSKCD}			50			6	ns	
Opposing Directional[2]	t_{PSKOD}			50			15	ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

[2] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 9. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO} or 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO} or 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.3 or V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{ISO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout						V_{DD1}, V_{DDL}, V_{ISO} supplies
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	
Input Currents per Channel	I_I	−20	+0.01	+20	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.7 \times V_{DD1}$ or $0.7 \times V_{ISO}$ for a high output or $V_O < 0.3 \times V_{DD1}$ or $0.3 \times V_{ISO}$ for a low output. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = 5.0 V, V_{ISO} = 3.3 V, V_{SEL} = GND_{ISO}. Minimum/maximum specifications apply over the entire recommended operation range which is 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{ISO} ≤ 3.6 V; and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1		mV/V	I_{ISO} = 50 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 6 mA to 54 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
PW Modulation Frequency	f_{PWM}		625		kHz	
Output Supply	$I_{ISO (MAX)}$	100			mA	V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			30		%	I_{ISO} = 90 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1 (Q)}$		5	15	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		230		mA	

Table 11. DC-to-DC Converter Dynamic Specifications

		1 Mbps—A Grade or C Grade			25 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
Input									No V_{ISO} load
ADuM5200	I_{DD1}		5			22		mA	
ADuM5201	I_{DD1}		5			23		mA	
ADuM5202	I_{DD1}		5			24		mA	
Available to Load									
ADuM5200	$I_{ISO (LOAD)}$		100			96		mA	
ADuM5201	$I_{ISO (LOAD)}$		100			95		mA	
ADuM5202	$I_{ISO (LOAD)}$		100			94		mA	

Table 12. Switching Specifications

		A Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		60	100		45	60	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			6	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature						5		ps/°C	
Pulse Width	PW	1000			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			15	ns	Between any two units
Channel Matching									
Codirectional[1]	t_{PSKCD}			50			6	ns	
Opposing Directional[2]	t_{PSKOD}			50			15	ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[2] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 13. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO} or 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO} or 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.2, V_{ISO} − 0.2	V_{DD1} or V_{ISO}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5 or V_{ISO} − 0.5	V_{DD1} − 0.2 or V_{ISO} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout						V_{DD1}, V_{DDL}, V_{ISO} supplies
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	
Input Currents per Channel	I_I	−20	+0.01	+20	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.7 \times V_{DD1}$ or $0.7 \times V_{ISO}$ for a high output or $V_O < 0.3 \times V_{DD1}$ or $0.3 \times V_{ISO}$ for a low output. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 14. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
RESISTANCE AND CAPACITANCE						
Resistance (Input-to-Output)[1]	R_{I-O}		10^2		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at the center of the package underside; test conducted on a 4-layer board with thin traces[3]
THERMAL SHUTDOWN						
Threshold	TS_{SD}		150		°C	T_J rising
Hysteresis	TS_{SD-HYS}		20		°C	

[1] This device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] Refer to the Power Considerations section for thermal model definitions.

REGULATORY INFORMATION

The ADuM5200/ADuM5201/ADuM5202 are approved by the organizations listed in Table 15. Refer to Table 20 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-insulation waveforms and insulation levels.

Table 15.

UL[1]	CSA	VDE (Pending)[2]
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to IEC 60747-5-2 (VDE 0884, Part 2):2003-01[2]
Single protection, 2500 V rms isolation voltage	Testing was conducted per CSA 60950-1-07 and IEC 60950-1 2nd Ed. at 2.5 kV rated voltage Basic insulation at 600 V rms (848 V_{PEAK}) working voltage Reinforced insulation at 250 V rms (353 V_{PEAK}) working voltage	Basic insulation, 560 V_{PEAK}
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM5200/ADuM5201/ADuM5202 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with IEC 60747-5-2 (VDE 0884 Part 2):2003-01, each ADuM520x is proof tested by applying an insulation test voltage ≥ 1590 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates IEC 60747-5-2 (VDE 0884, Part 2):2003-01 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 16. Critical Safety-Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap	L(I01)	8.0	mm	Distance measured from input terminals to output terminals; shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Distance (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		IIIa		Material group (DIN VDE 0110, 1/89, Table 1)

IEC 60747-5-2 (VDE 0884, PART 2):2003-01 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking branded on the components designates IEC 60747-5-2 (VDE 0884, Part 2):2003-1 approval.

Table 17. VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m =$ 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4000	V_{PEAK}
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	2500	V_{RMS}
Surge Isolation Voltage	V_{PEAK} = 6 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Case Temperature		T_S	150	°C
Side 1 I_{DD1} Current		I_{S1}	555	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

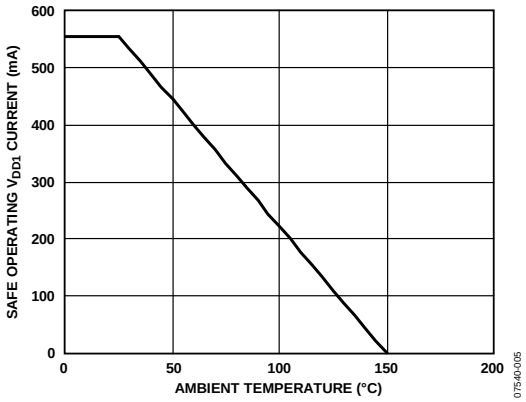


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 18.

Parameter	Symbol	Min	Max	Unit
Operating Temperature[1]	T_A	−40	+105	°C
Supply Voltages[2]				
V_{DD1} @ V_{SEL} = 0 V	V_{DD1}	3.0	5.5	V
V_{DD1} @ $V_{SEL} = V_{ISO}$	V_{DD1}	4.5	5.5	V

[1] Operation at 105°C requires reduction of the maximum load current as specified in Table 19.
[2] Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 19.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{ISO})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, RC_{IN}, RC_{SEL}, V_{SEL})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	−10 mA to +10 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] Each voltage is relative to its respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.
[3] See Figure 5 for maximum rated current values for various temperatures.
[4] Common-mode transients exceeding the absolute maximum slew rate may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 20. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	424	V_{PEAK}	All certifications, 50-year operation
AC Voltage, Unipolar Waveform			
Basic Insulation	600	V_{PEAK}	Working voltage, 50-year operation
Reinforced Insulation	353	V_{PEAK}	Working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	600	V_{PEAK}	Working voltage, 50-year operation
Reinforced Insulation	353	V_{PEAK}	Working voltage per IEC 60950-1

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

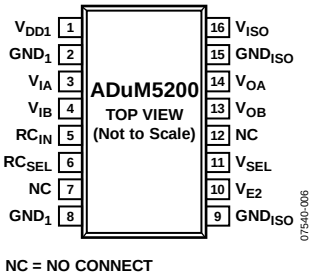


Figure 6. ADuM5200 Pin Configuration

Table 21. ADuM5200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for the isolator primary side. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	RC_{IN}	Regulation Control Input. This pin must be connected to the RC_{OUT} pin of a master *iso*Power device or tied low. Note that this pin must not be tied high if RC_{SEL} is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5200 and possibly the devices that it powers.
6	RC_{SEL}	Control Input. Determines self-regulation mode (RC_{SEL} high) or slave mode (RC_{SEL} low), allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie this pin either high or low.
7, 12	NC	No Internal Connection.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Data Enable Input. When this pin is high or not connected, the secondary outputs are active; when this pin is low, the outputs are in a high-Z state.
11	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V. In slave regulation mode, this pin has no function.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.

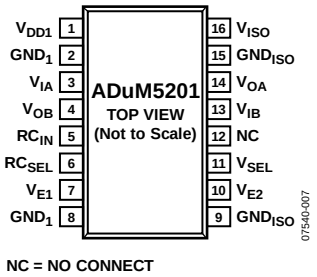


Figure 7. ADuM5201 Pin Configuration

Table 22. ADuM5201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary side. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{OB}	Logic Output B.
5	RC_{IN}	Regulation Control Input. This pin must be connected to the RC_{OUT} pin of a master *iso*Power device or tied low. Note that this pin must not be tied high if RC_{SEL} is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5201 and possibly the devices that it powers.
6	RC_{SEL}	Control Input. Determines self-regulation mode (RC_{SEL} high) or slave mode (RC_{SEL} low), allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie this pin either high or low.
7	V_{E1}	Data Enable Input. When this pin is high or not connected, the primary output is active; when this pin is low, the output is in a high-Z state.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Data Enable Input. When this pin is high or not connected, the secondary output is active; when this pin is low, the output is in a high-Z state.
11	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V. In slave regulation mode, this pin has no function.
12	NC	No Internal Connection.
13	V_{IB}	Logic Input B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.

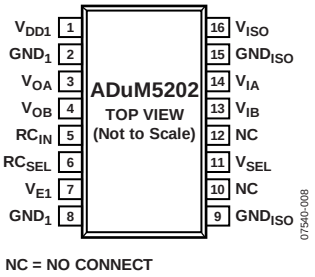


Figure 8. ADuM5202 Pin Configuration

Table 23. ADuM5202 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for the isolator primary side. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{OA}	Logic Output A.
4	V_{OB}	Logic Output B.
5	RC_{IN}	Regulation Control Input. This pin must be connected to the RC_{OUT} pin of a master *iso*Power device or tied low. Note that this pin must not be tied high if RC_{SEL} is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5202 and possibly the devices that it powers.
6	RC_{SEL}	Control Input. Determines self-regulation mode (RC_{SEL} high) or slave mode (RC_{SEL} low), allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie this pin either high or low.
7	V_{E1}	Data Enable Input. When this pin is high or not connected, the primary output is active; when this pin is low, the output is in a high-Z state.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10, 12	NC	No Internal Connection.
11	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V. In slave regulation mode, this pin has no function.
13	V_{IB}	Logic Input B.
14	V_{IA}	Logic Input A.
16	V_{ISO}	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.

TRUTH TABLE

Table 24. Power Section Truth Table (Positive Logic)[1]

RC_{SEL} Input	RC_{IN} Input	V_{SEL} Input	V_{DD1} Input (V)[2]	V_{ISO} (V)	Operation
H	X	H	5.0	5.0	Self regulation mode, normal operation.
H	X	L	5.0	3.3	Self regulation mode, normal operation.
H	X	L	3.3	3.3	Self regulation mode, normal operation.
H	X	H	3.3	5.0	This supply configuration is not recommended due to extremely poor efficiency.
L	H	X	X	X	Part runs at maximum open-loop voltage; therefore, damage can occur.
L	L	X	X	0	Power supply is disabled.
L	$RC_{OUT(EXT)}$	X	X	X	Slave mode, $RC_{OUT(EXT)}$ supplied by a master *iso*Power device.

[1] H refers to a high logic, L refers to a low logic, and X is don't care or unknown.
[2] V_{DD1} must be common between all *iso*Power devices being regulated by a master *iso*Power part.

TYPICAL PERFORMANCE CHARACTERISTICS

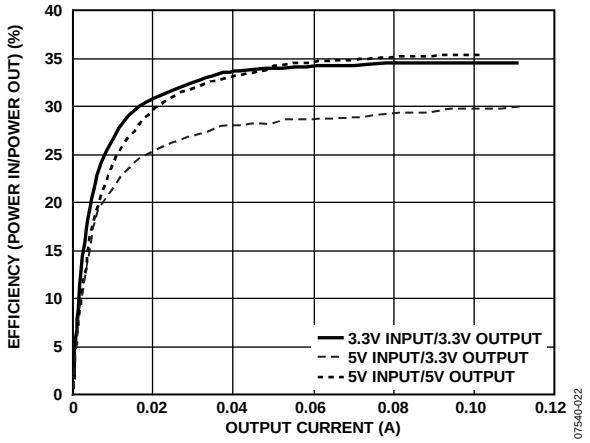


Figure 9. Typical Power Supply Efficiency in All Supported Power Configurations

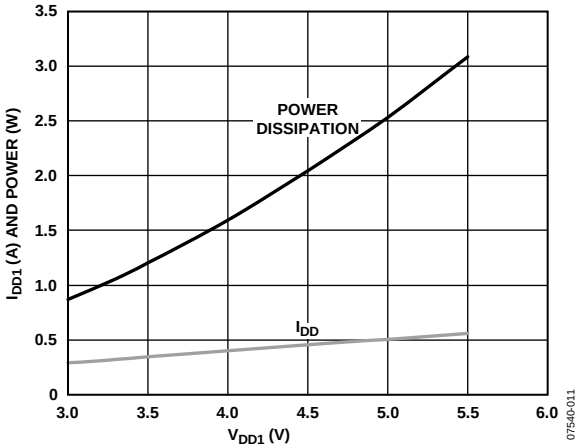


Figure 12. Typical Short-Circuit Input Current and Power vs. V_{DD1} Supply Voltage

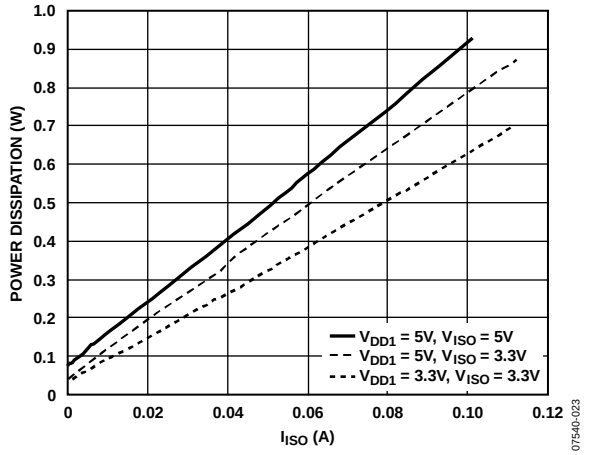


Figure 10. Typical Total Power Dissipation vs. Isolated Output Supply Current in All Supported Power Configurations

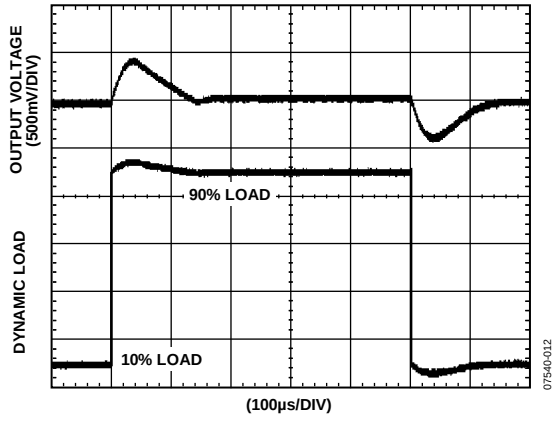


Figure 13. Typical V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

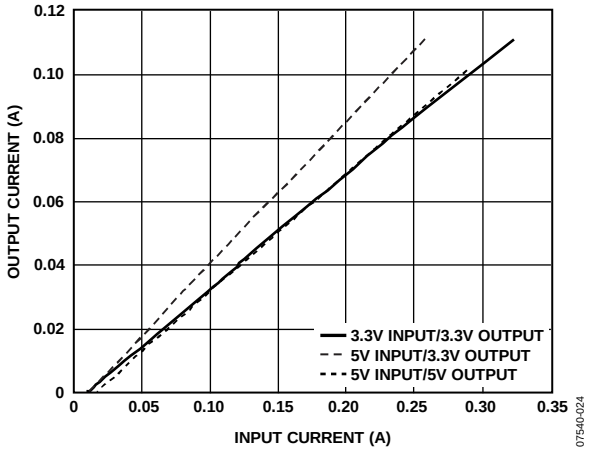


Figure 11. Typical Isolated Output Supply Current vs. Input Current in All Supported Power Configurations

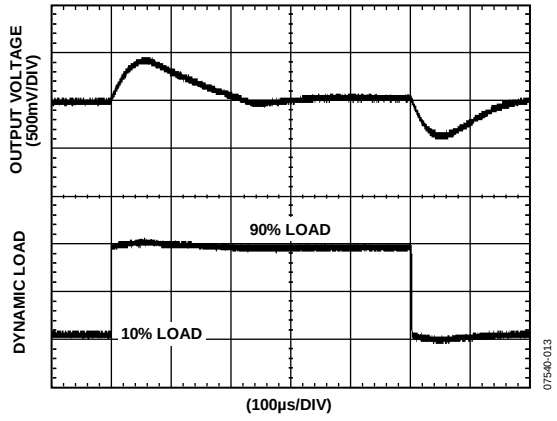


Figure 14. Typical V_{ISO} Transient Load Response, 3 V Output, 10% to 90% Load Step

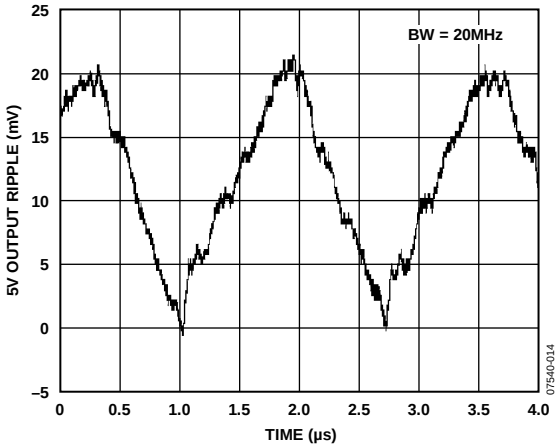


Figure 15. Typical Output Voltage Ripple at 90% Load, V_{ISO} = 5 V

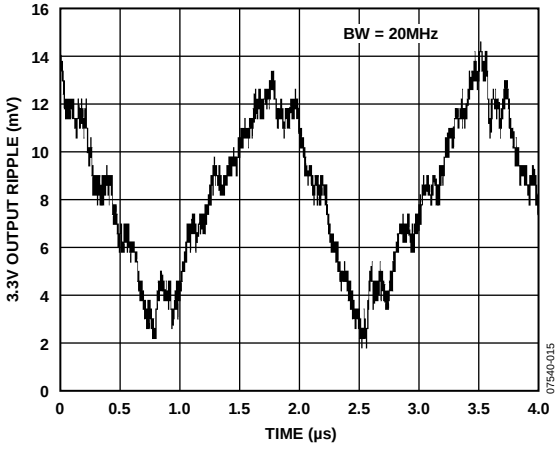


Figure 16. Typical Output Voltage Ripple at 90% Load, V_{ISO} = 3.3 V

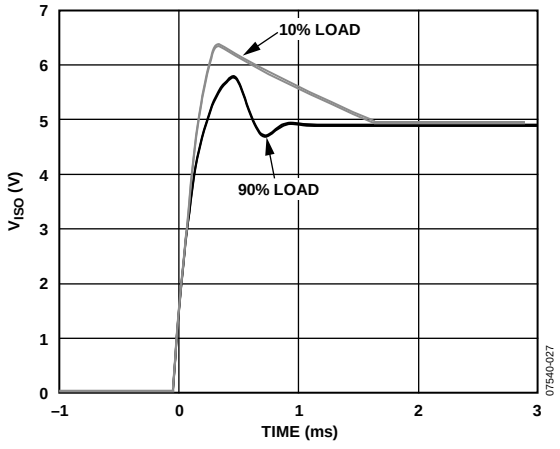


Figure 17. Typical Output Voltage Start-Up Transient at 10% and 90% Load, V_{ISO} = 5 V

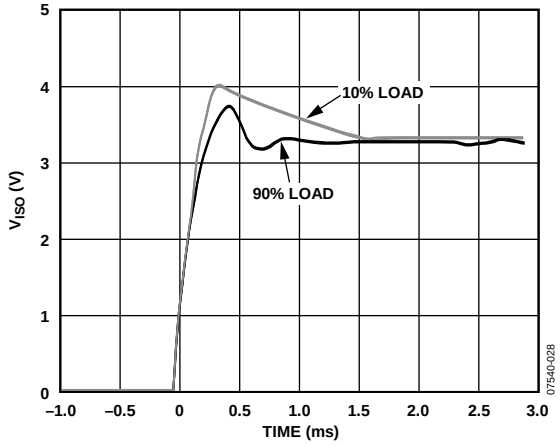


Figure 18. Typical Output Voltage Start-Up Transient at 10% and 90% Load, V_{ISO} = 3.3 V

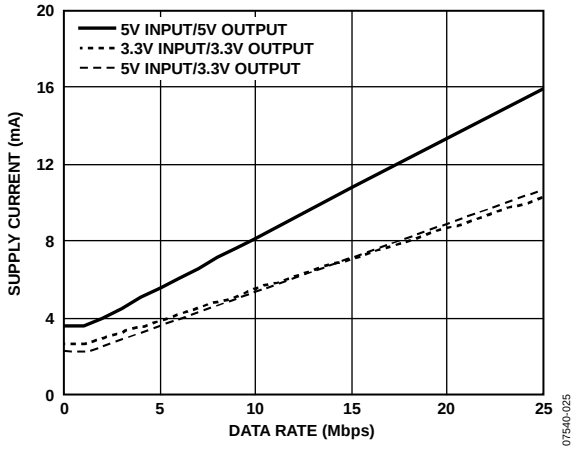


Figure 19. Typical I_{CHn} Supply Current per Forward Data Channel (15 pF Output Load)

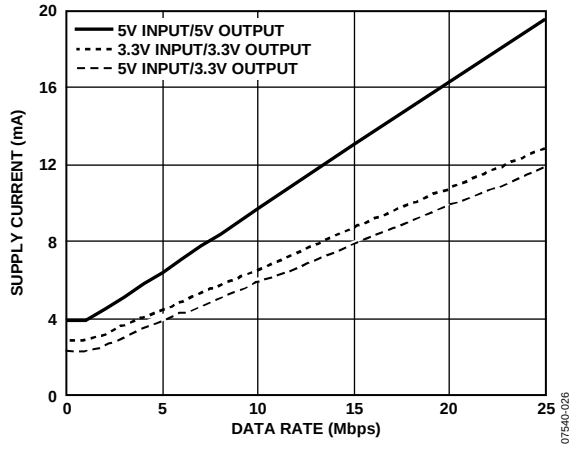


Figure 20. Typical I_{CHn} Supply Current per Reverse Data Channel (15 pF Output Load)

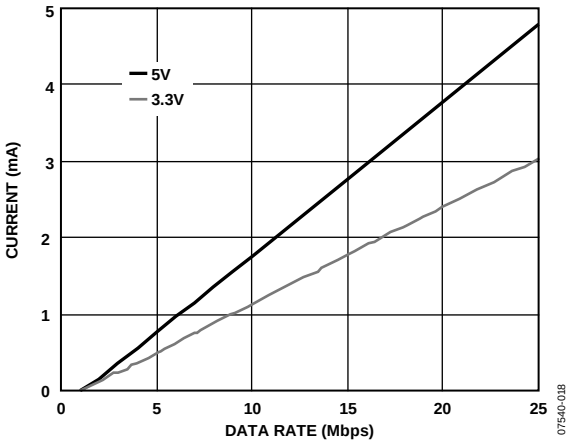


Figure 21. Typical $I_{ISO(D)}$ Dynamic Supply Current per Input

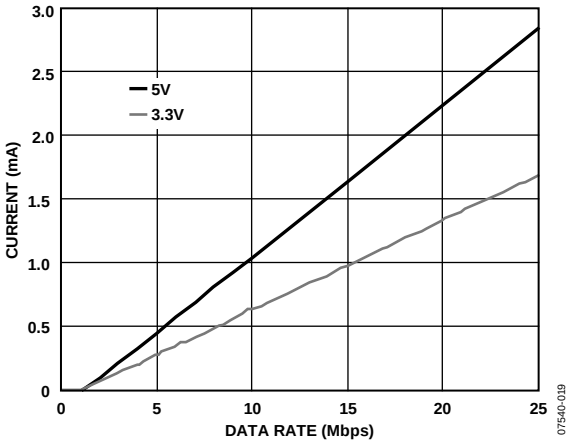


Figure 22. Typical $I_{ISO(D)}$ Dynamic Supply Current per Output (15 pF Output Load)

TERMINOLOGY

$I_{DD1 (Q)}$
$I_{DD1 (Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current. $I_{DD1 (Q)}$ reflects the minimum current operating condition.

$I_{DD1 (D)}$
$I_{DD1 (D)}$ is the typical input supply current with all channels simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.

$I_{DD1 (MAX)}$
$I_{DD1 (MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

$I_{SO (LOAD)}$
$I_{SO (LOAD)}$ is the current available to the load.

t_{PHL} Propagation Delay
t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

t_{PLH} Propagation Delay
t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew, t_{PSK}
t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel-to-Channel Matching, t_{PSKCD}/t_{PSKOD}
Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate
The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM5200/ADuM5201/ADuM5202 works on principles that are common to most switching power supplies. It has a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DD1} power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power transferred to the secondary side is rectified and regulated to either 3.3 V or 5 V. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DD1}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM5200/ADuM5201/ADuM5202 implements under-voltage lockout (UVLO) with hysteresis on the V_{DD1} power input. This feature ensures that the converter does not enter oscillation due to noisy input power or slow power-on ramp rates.

The ADuM5200/ADuM5201/ADuM5202 can accept an external regulation control signal (RC_{IN}) that can be connected to other *iso*Power devices. This allows a single regulator to control multiple power modules without contention. When accepting control from a master power module, the V_{ISO} pins can be connected together, adding their power. Because there is only one feedback control path, the supplies work together seamlessly. The ADuM5200/ADuM5201/ADuM5202 can only regulate themselves or accept regulation (as slave devices) from another device in this product line; they cannot provide a regulation signal to other devices.

PCB LAYOUT

The ADuM5200/ADuM5201/ADuM5202 digital isolators with 0.5 W *iso*Power, integrated dc-to-dc converter require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 23). Note that low ESR bypass capacitors are required between Pin 1 and Pin 2 and between Pin 15 and Pin 16, as close to the chip pads as possible.

The power supply section of the ADuM5200/ADuM5201/ADuM5202 uses a 180 MHz oscillator frequency to pass power efficiently through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor, whereas ripple suppression and proper regulation require a large value capacitor. These capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{ISO}.

To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR; for example, use of a ceramic capacitor is advised.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. Consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 unless both common ground pins are connected together close to the package.

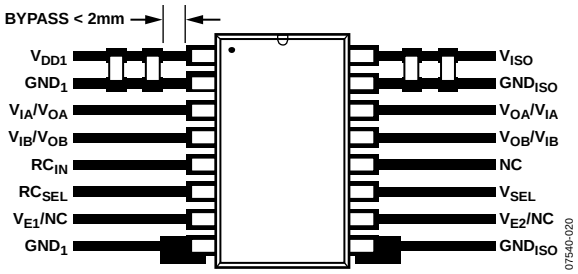


Figure 23. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur affects all pins equally on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings for the device (specified in Table 19), thereby leading to latch-up and/or permanent damage.

The ADuM5200/ADuM5201/ADuM5202 is a power device that dissipates approximately 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device is used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 23 shows enlarged pads for Pin 2, Pin 8, Pin 9, and Pin 15. Multiple vias should be implemented from the pad to the ground plane to significantly reduce the temperature inside the chip. The dimensions of the expanded pads are at the discretion of the designer and depend on the available board space.

START-UP BEHAVIOR

The ADuM5200/ADuM5201/ADuM5202 do not contain a soft start circuit. Take the start-up current and voltage behavior into account when designing with this device.

When power is applied to V_{DD1}, the input switching circuit begins to operate and draw current when the UVLO minimum voltage is reached. The switching circuit drives the maximum available power to the output until it reaches the regulation voltage where PWM control begins. The amount of current and time this takes depends on the load and the V_{DD1} slew rate.

With a fast V_{DD1} slew rate (200 µs or less), the peak current draws up to 100 mA/V of V_{DD1}. The input voltage goes high faster than the output can turn on; therefore, the peak current is proportional to the maximum input voltage.

With a slow V_{DD1} slew rate (in the millisecond range), the input voltage is not changing quickly when V_{DD1} reaches the UVLO minimum voltage. The current surge is approximately 300 mA because V_{DD1} is nearly constant at the 2.7 V UVLO voltage. The behavior during startup is similar to when the device load is a short circuit; these values are consistent with the short-circuit current shown in Figure 12.

When starting the device for V_{ISO} = 5 V operation, do not limit the current available to the V_{DD1} power pin to less than 300 mA. The ADuM5200/ADuM5201/ADuM5202 devices may not be able to drive the output to the regulation point if a current-limiting device clamps the V_{DD1} voltage during startup. As a result, the ADuM5200/ADuM5201/ADuM5202 devices can draw large amounts of current at low voltage for extended periods of time.

The output voltage of the ADuM5200/ADuM5201/ADuM5202 exhibits V_{ISO} overshoot during startup. If this could potentially damage components attached to V_{ISO}, then a voltage-limiting device, such as a Zener diode, can be used to clamp the voltage. Typical behavior is shown in Figure 17 and Figure 18.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM5200/ADuM5201/ADuM5202 devices must operate at 180 MHz to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge emissions and dipole radiation between the primary and secondary ground planes. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note for board layout recommendations.

PROPAGATION DELAY PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

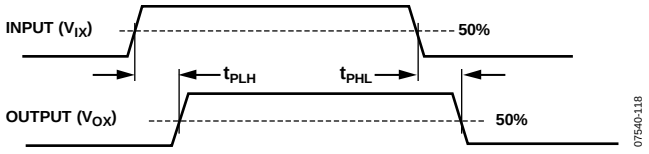


Figure 24. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM5200/ADuM5201/ADuM5202 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM5200/ADuM5201/ADuM5202 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 24) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM5200/ADuM5201/ADuM5202 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM5200/ADuM5201/ADuM5202 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM5200/ADuM5201/ADuM5202 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 25.

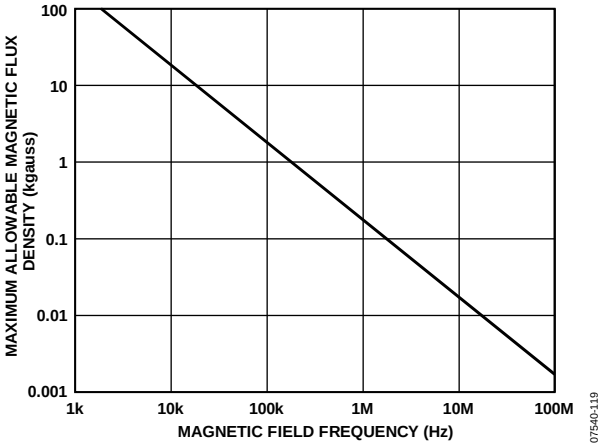


Figure 25. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM5200/ADuM5201/ADuM5202 transformers. Figure 26 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM5200/ADuM5201/ADuM5202 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current placed 5 mm away from the ADuM5200/ADuM5201/ADuM5202 is required to affect the operation of the component.

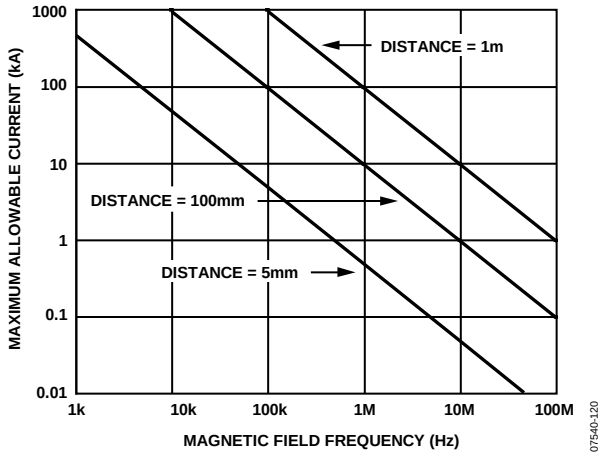


Figure 26. Maximum Allowable Current for Various Current-to-ADuM5200/ADuM5201/ADuM5202 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The V_{DD1} power supply input provides power to the *i*Coupler data channels as well as to the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary input/output channels cannot be determined separately. All of these quiescent power demands have been combined into the $I_{DD1\,(Q)}$ current shown in Figure 27. The total I_{DD1} supply current is the sum of the quiescent operating current, dynamic current $I_{DD1\,(D)}$ demanded by the I/O channels, and any external I_{ISO} load.

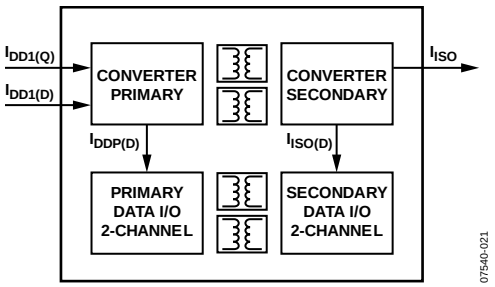


Figure 27. Power Consumption Within the ADuM5200/ADuM5201/ADuM5202

Both dynamic input and output current is consumed only when operating at channel speeds higher than the rate of f_r. Because each channel has a dynamic current determined by its data rate, Figure 19 shows the current for a channel in the forward direction, which means that the input is on the primary side of the part. Figure 20 shows the current for a channel in the reverse direction, which means that the input is on the secondary side of the part. Both figures assume a typical 15 pF load. The following relationship allows the total I_{DD1} current to be calculated:

$$I_{DD1} = (I_{ISO} \times V_{ISO})/(E \times V_{DD1}) + \sum I_{CHn};\ n = 1 \text{ to } 4 \quad (1)$$

where:
I_{DD1} is the total supply input current.
I_{CHn} is the current drawn by a single channel determined from Figure 19 or Figure 20, depending on channel direction.
I_{ISO} is the current drawn by the secondary side external loads.
E is the power supply efficiency at 100 mA load from Figure 9 at the V_{ISO} and V_{DD1} condition of interest.

Calculate the maximum external load by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO\,(LOAD)} = I_{ISO\,(MAX)} - \sum I_{ISO\,(D)n};\ n = 1 \text{ to } 4 \quad (2)$$

where:
$I_{ISO\,(LOAD)}$ is the current available to supply an external secondary side load.
$I_{ISO\,(MAX)}$ is the maximum external secondary side load current available at V_{ISO}.
$I_{ISO\,(D)n}$ is the dynamic load current drawn from V_{ISO} by an input or output channel, as shown in Figure 19 and Figure 20. Data is presented assuming a typical 15 pF load.

The preceding analysis assumes a 15 pF capacitive load on each data output. If the capacitive load is larger than 15 pF, the additional current must be included in the analysis of I_{DD1} and $I_{ISO\,(LOAD)}$.

To determine I_{DD1} in Equation 1, additional primary side dynamic output current (I_{AOD}) is added directly to I_{DD1}. Additional secondary side dynamic output current (I_{AOD}) is added to I_{ISO} on a per-channel basis.

To determine $I_{ISO\,(LOAD)}$ in Equation 2, additional secondary side output current (I_{AOD}) is subtracted from $I_{ISO\,(MAX)}$ on a per-channel basis.

For each output channel with C_L greater than 15 pF, the additional capacitive supply current is given by

$$I_{AOD} = 0.5 \times 10^{-3} \times ((C_L - 15) \times V_{ISO}) \times (2f - f_r); f > 0.5\, f_r \quad (3)$$

where:
C_L is the output load capacitance (pF).
V_{ISO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.
f_r is the input channel refresh rate (Mbps).

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADuM5200/ADuM5201/ADuM5202 are protected against damage due to excessive power dissipation by thermal overload protection circuits. Thermal overload protection limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the PWM is turned off, reducing the output current to zero. When the junction temperature drops below 130°C (typical), the PWM turns on again, restoring the output current to its nominal value.

Consider the case where a hard short from V_{ISO} to ground occurs. At first, the ADuM5200/ADuM5201/ADuM5202 reach their maximum current, which is proportional to the voltage applied at V_{DD1}. Power dissipates on the primary side of the converter (see Figure 12). If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the PWM, and reducing the output current to zero. As the junction temperature cools and drops below 130°C, the PWM turns on, and power dissipates again on the primary side of the converter, causing the junction temperature to rise to 150°C again. This thermal oscillation between 130°C and 150°C causes the part to cycle on and off as long as the short remains at the output.

Thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, externally limit device power dissipation to prevent junction temperatures from exceeding 130°C.

POWER CONSIDERATIONS

The ADuM5200/ADuM5201/ADuM5202 power input, data input channels on the primary side and data input channels on the secondary side are all protected from premature operation by UVLO circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive and all input channel drivers and refresh circuits are idle. Outputs remain in a high impedance state to prevent transmission of undefined states during power-up and power-down operations.

During application of power to V_{DD1}, the primary side circuitry is held idle until the UVLO preset voltage is reached. At that time, the data channels initialize to their default low output state until they receive data pulses from the secondary side.

When the primary side is above the UVLO threshold, the data input channels sample their inputs and begin sending encoded pulses to the inactive secondary output channels. The outputs on the primary side remain in their default low state because no data comes from the secondary side inputs until secondary power is established. The primary side oscillator also begins to operate, transferring power to the secondary power circuits.

The secondary V_{ISO} voltage is below its UVLO limit at this point; the regulation control signal from the secondary is not being generated. The primary side power oscillator is allowed to free run in this circumstance, supplying the maximum amount of power to the secondary, until the secondary voltage rises to its regulation setpoint. This creates a large inrush current transient at V_{DD1}.

When the regulation point is reached, the regulation control circuit produces the regulation control signal that modulates the oscillator on the primary side. The V_{DD1} current is reduced and is then proportional to the load current. The inrush current is less than the short-circuit current shown in Figure 12. The duration of the inrush current depends on the V_{ISO} loading conditions and the current available at the V_{DD1} pin.

As the secondary side converter begins to accept power from the primary, the V_{ISO} voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data is received from the corresponding primary side input. It can take up to 1 µs after the secondary side is initialized for the state of the output to correlate with the primary side input.

Secondary side inputs sample their state and transmit it to the primary side. Outputs are valid about 1 µs after the secondary side becomes active.

Because the rate of charge of the secondary side power supply is dependent on loading conditions and the input voltage level and the output voltage level selected, take care with the design to allow the converter sufficient time to stabilize before valid data is required.

When power is removed from V_{DD1}, the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side hold the last state that they received from the primary side. Either the UVLO level is reached and the outputs are placed in their high impedance state, or the outputs detect a lack of activity from the primary side inputs and the outputs are set to their default low value before the secondary power reaches UVLO.

THERMAL ANALYSIS

The ADuM5200/ADuM5201/ADuM5202 consist of four internal die, attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} value in Table 14. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5200/ADuM5201/ADuM5202 operate at full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

INCREASING AVAILABLE POWER

The ADuM5200/ADuM5201/ADuM5202 are designed with the capability of running in combination with other compatible *iso*Power devices. The RC_{IN} and RC_{SEL} pins allow the ADuM5200/ADuM5201/ADuM5202 to receive a PWM signal from another device through the RC_{IN} pin and act as a slave to that control signal. The RC_{SEL} pin chooses whether the part acts as a stand-alone self-regulated device or a slave device. When the ADuM5200/ADuM5201/ADuM5202 act as a slave, their power is regulated by a PWM signal coming from a master device. This allows multiple *iso*Power parts to be combined in parallel while sharing the load equally. When the ADuM5200/ADuM5201/ADuM5202 are configured as standalone units, they generate their own PWM feedback signal to regulate themselves.

The ADuM5000 can act as a master or a slave device, the ADuM5401, ADuM5402, ADuM5403, and ADuM5404 can only be master/standalone, and the ADuM520x can only be a slave/standalone device. This means that the ADuM5000, ADuM520x, and ADuM5401 to ADuM5404 can only be used in certain master/slave combinations as listed in Table 25.

Table 25. Allowed Combinations of *iso*Power Parts

	Slave		
Master	**ADuM5000**	**ADuM520x**	**ADuM5401 to ADuM5404**
ADuM5000	Yes	Yes	No
ADuM520x	No	No	No
ADuM5401 to ADuM5404	Yes	Yes	No

The allowed combinations of master and slave configured parts listed in Table 25 is sufficient to make any combination of power and channel count.

Table 26 illustrates how *iso*Power devices can provide many combinations of data channel count and multiples of the single unit power.

Table 26. Configurations for Power and Data Channels

	Number of Data Channels			
Power Units	**0 Channels**	**2 Channels**	**4 Channels**	**6 Channels**
1-Unit Power	ADuM5000 master	ADuM520x master	ADuM5401 to ADuM5404 master	ADuM5401 to ADuM5404 master ADuM121x
2-Unit Power	ADuM5000 master ADuM5000 slave	ADuM5000 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave
3-Unit Power	ADuM5000 master ADuM5000 slave ADuM5000 slave	ADuM5000 master ADuM5000 slave ADuM520x slave	ADuM5401 to ADuM5404 master ADuM5000 slave ADuM5000 slave	ADuM5401 to ADuM5404 master ADuM520x slave ADuM5000 slave

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5200/ADuM5201/ADuM5202.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 20 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than a 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM5200/ADuM5201/ADuM5202 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 28, Figure 29, and Figure 30 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 20 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 29 or Figure 30 should be treated as a bipolar ac waveform and its peak voltage limited to the 50-year lifetime voltage value listed in Table 20. The voltage presented in Figure 29 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

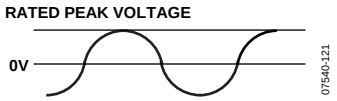


Figure 28. Bipolar AC Waveform

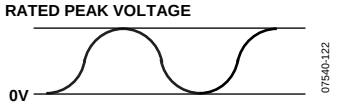


Figure 29. Unipolar AC Waveform

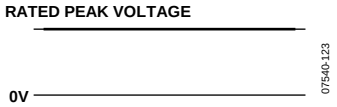
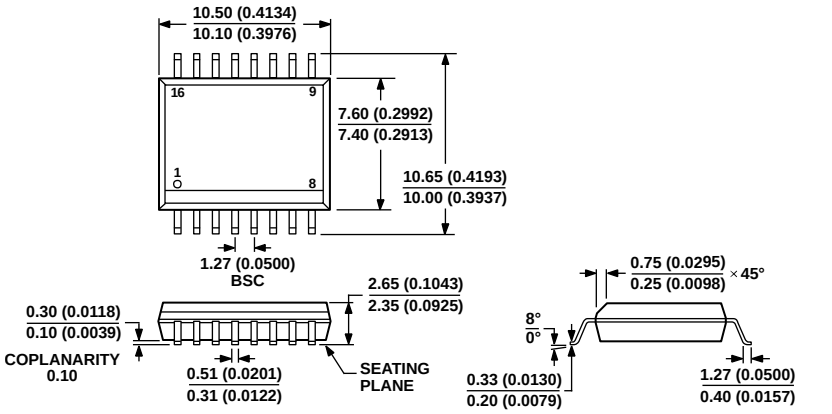


Figure 30. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 31. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM5200ARWZ	2	0	1	100	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5200CRWZ	2	0	25	70	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5201ARWZ	1	1	1	100	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5201CRWZ	1	1	25	70	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5202ARWZ	0	2	1	100	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5202CRWZ	0	2	25	70	3	−40°C to +105°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.
[2] Tape and reel are available. The additional -RL suffix designates a 13-inch (1,000 units) tape and reel option.

NOTES

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