BROADCOM®

Data Sheet

AEAT-8811-Q24



Magnetic Encoder IC: 10-Bit to 16-Bit Programmable Angular Magnetic Encoder with No Offset Calibration

Overview

The Broadcom AEAT-8811-Q24 is an angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation.

It is a sophisticated system that uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A simple two-pole magnet generates the necessary magnetic field by rotating it in perpendicular, placed in alignment to the center of the device.

The Broadcom AEAT-8811-Q24 is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and one-time programmable resolution of 10, 12, 14, or 16 bits. When selected, its positioning data is then represented in its digital form to be assessed through a standard SSI 3-wire communication protocol. Where desired, users may also choose to receive its absolute angle position in PWM-encoded output signals.

The incremental positions are indicated on ABI and UVW signals with user-configurable CPR 32, 64, 128, 256, 512, 1024, 2048, 4096 and 50, 100, 200, 400, 800, 1000, 2000, and 4000 of ABI signals and pole pairs from 1 to 8 (2 to 16 poles) for UVW commutation signals. AEAT-8811-Q24 requires no offset calibration programming and operates at 5V supply.

Key Features

- 5V operation
- Selectable 10, 12, 14, or 16 bits of absolute resolution
- Incremental output of ABI UVW (32, 64, 128, 256, 512, 1024, 2048, 4096, 50, 100, 200, 400, 800, 1000, 2000, 4000 CPR)
- PWM output modes
- User-programmable zero position, direction, and index width
- Selectable zero latency mode option
- Programmable hysteresis
- Available in 2-wire or 3-wire SSI options. Selectable 3-wire SSI option with initial data output at tri-state mode
- Compact QFN-24 leads (5 mm × 5 mm) package
- RoHS compliant
- No programming required for offset calibration

Specifications

- Absolute 10-bit to 16-bit resolution
- Incremental output resolutions of 32 to 4096 CPR
- UVW output of 1 to 8 pole pairs
- Wide operating temperature: –40°C to 125°C

Applications

- Brushless DC motor and stepper motor
- Resolver and potentiometer replacement
- Industrial automation and robotics
- Industrial sewing machine and textile equipment

NOTE: This product is not specifically designed or manufactured for use in any specific device. Customers are solely responsible for determining the suitability of this product for its intended application and are solely liable for all loss, damage, expense, or liability in connection with such use.

Definition

Electrical Degree (°e): CPR × 360 electrical degrees = 360 mechanical degrees.

Cycle (C): One cycle of the incremental signal is 360 mechanical degrees/resolution and is equal to 360 electrical degrees (°e).

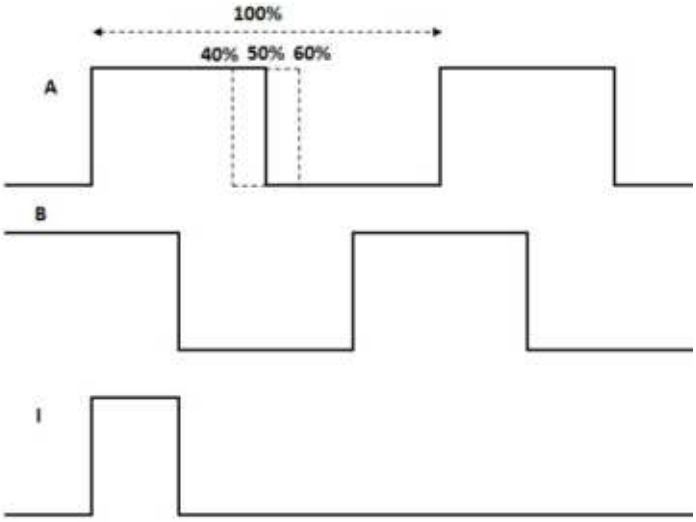
Pulse Width (P): The number of electrical degrees that an output is high during one cycle, nominally 180°e or one-half of a cycle.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are four states per cycle, each nominally 90°e.

Phase (Φ): The number of electrical degrees between the center of the high state on channel A and the center of the high state on channel B.

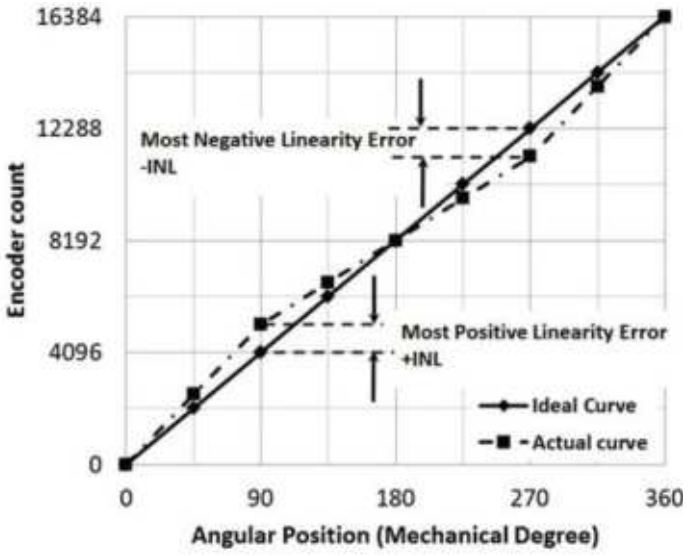
Relative angular accuracy: With reference to the output period at A and B. The relative accuracy of the edges to each other at a CPR setting of 256 is within ± 10% for 5V operation in a typical condition. Therefore, based on a period at A or B, the edge occurs in a window between 40% and 60% as shown in the following figure.

Figure 1: ABI Signals of AEAT-8811-Q24



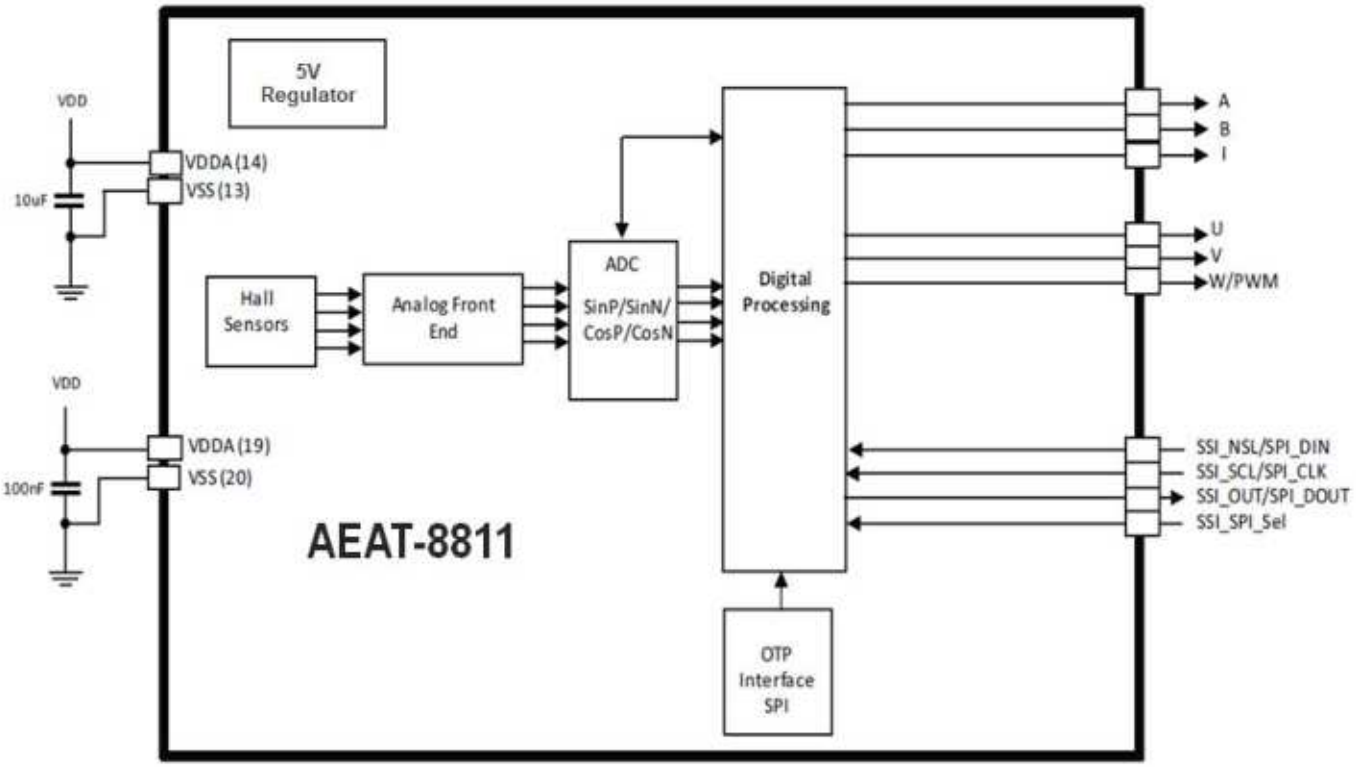
Integral non-linearity (INL): The maximum deviation between the actual angular position and the position indicated by the encoder's output count, over one revolution. It is defined as the most positive linearity error +INL or the most negative linearity error –INL from the best fit line, whichever is larger.

Figure 2: Integral Non-Linearity Example



Functional Description

Figure 3: AEAT-8811-Q24 Block Diagram



Pin Assignment

Figure 4: Pin Configurations for AEAT-8811-Q24

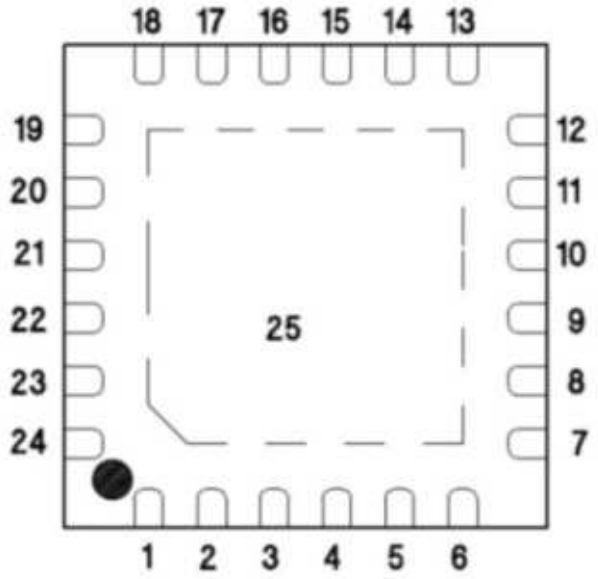


Table 1: Pinout Description

Pin	Symbol	Description
1–6	No Connection	N/A
7	I	Index output (ABI mode)
8	B	Incremental B output (ABI mode)
9	A	Incremental A output (ABI mode)
10	SSI_SCL_SPI_CLK	SSI/SPI clock input
11	SSI_SCL_SPI_DI	SSI/SPI data input
12	SSI_SCL_SPI_D0	SSI/SPI data out
13	VSS	Supply ground
14	VDDA	5V supply input
15	No Connection	No connection
16	No Connection	No connection
17	No Connection	No connection
18	No Connection	No connection
19	VDDA	5V supply input
20	VSS	Supply ground
21	SSI_SCL_SPI_SEL	SSI/SPI select pin
22	U	U commutation output (UVW mode)
23	V	V commutation output (UVW mode)
24	W or PWM	W commutation (UVW mode)/PWM output
25	VSS	Supply ground

The AEAT-8811-Q24 is manufactured with a CMOS standard process. It is capable of accurately measuring a magnet's rotational angle when it is placed in alignment and perpendicular to the device by using its integrated Hall sensors to detect its magnetic field. The detected magnetic signals are then taken as input signals to be properly conditioned to negate its non-idealities before inputting them into the analog amplifiers for strength amplification and filtering. After which, the amplified analog signals are fed into the internal analog-to-digital converter (ADC) to be converted into digital signals for the final stage of digital processing.

The digital processing provides a digitized output of the absolute and incremental signals. For optimal performance, the used magnet's center axis should be aligned with the center of the device with a tolerable displacement radius of 0.5 mm from the defined Hall sensor center as described in Magnet and IC Package Placement. Moreover, the used magnet should have sufficient magnetic field strength (mT) to generate the magnetic field for the signal generation as highlighted in Recommended Magnetic Input Specifications. The device provides digital information of magnetic field strength high (MHi) and magnetic field strength low (MLo) from the SSI read to indicate whether the magnets are too close or too far away from the device's surface.

Users can assess the device's digitized absolute data using standard Synchronous Serial Interface (SSI) protocols. In addition, an absolute angular representation can also be selected using a pulse-width modulated (PWM) signal.

The incremental outputs are available from the digital outputs of their respective A, B, and I pins. This is the same for the U, V, and W pins.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	–40	125	°C	—
DC Supply Voltage VDDA Pin	VDD	–0.3	5.5	Volts	—
Input Voltage Range	V_{in}	–0.3	5.5	Volts	—
Electrostatic Discharge	—	–2.0	+2.0	kVolts	—
Moisture Sensitivity Level	—	—	3	—	Maximum floor life = 168 hours

CAUTION! Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices. These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

Electrical Characteristics

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Ambient Temperature	T_A	–40	—	125	°C	—
DC Supply Voltage to VDD Pin 5V Operation	VDD	4.5	5.0	5.5	Volts	—
OTP Programming Voltage at VDDA Pin	—	5.5	5.6	5.7	Volts	—

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Incremental Output Frequency	f_{MAX}	—	—	1.0	MHz	Frequency = Velocity(rpm) x CPR/60
Load Capacitance	C_L	—	—	15	pF	—

System Parameters

Condition: Electrical characteristics are over the recommended operating conditions. Typical values are specified at VDD = 5.0V and 25°C, optimum placement of magnet.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Current Consumption						
Supply Current Normal Operation Mode	I_{DD}	—	24	28	mA	—
Digital Outputs (DO)						
High Level Output Voltage	V_{OH}	VDD – 0.5	—	—	Volts	Normal operation
Low Level Output Voltage	V_{OL}	—	—	GND + 0.4	Volts	—
Power-Up Time Absolute Output Incremental Output PWM Output	t_{PwrUp}	—	4		ms	—
Digital Inputs (DI)						
Input High Level	V_{IH}	0.7 x VDD	—	—	Volts	—
Input Low Level	V_{IL}	—	—	0.3 x VDD	Volts	—
Pull-Up Low Level Input Current	I_{IL}	—	—	120	µA	—
Pull-Down High Level Input Current	I_{IH}	—	—	120	µA	—

Encoding Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Absolute Output						
Resolution	RES	10	—	16	Bit	10, 12, 14, or 16 bits
Integral Non-Linearity (Optimum)	INL_{nom}	—	—	±0.35	Deg	Best fit line, centered magnet. Tamb = 25°C at 5V
Integral Non-Linearity	INL	—	—	±1.0	Deg	Best fit line, over displacement of magnet. Tamb = –40 to +125°C Voltage = 5V
Output Sampling Rate	f_S	—	10	—	MHz	Based on the SSI protocol
Code Monotony 10, 12, 14 bit	—	—	1	—	Step	Tamb = –40 to 125ºC @5V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Incremental Output (Channel ABI)						
Resolution	R_{INC}	32	—	4096	CPR	Programmable options 32, 64, 128, 256, 512, 1024, 4096, 50, 100, 200, 400, 800, 1000, 2000, and 4000 CPR
Index Pulse Width	P_O	90	—	360	°e	Programmable options: 90, 180, 270, or 360 °e
Relative Angular Accuracy	%	—	±10%	—	%	Reference to an output period at output A and B, at 256 CPR, 5V, and 10,000 RPM
Commutation Characteristic (Channel U,V,W)						
Commutation Format	Programmable pole pairs from 1 to 8 (2 to 16 poles)					
Commutation Accuracy	ΔUVW	—	±2	—	°mechanical	—
PWM Output						
PWM Frequency	f_{PWM}	122	—	976	Hz	Adjustable based on the PWM settings
Minimum Pulse Width	PW_{MIN}	—	1	—	µs	—
Maximum Pulse Width	PW_{MAX}	—	8192	—	µs	—

NOTE: Encoding characteristics are over the recommended operating range unless otherwise specified.

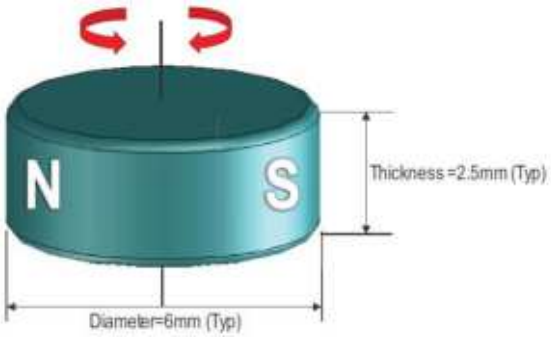
Encoding Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Incremental Output (ABI & UVW)						
System Reaction Time	t_{delay}	—	4	—	ms	First ABI pulse detection upon power-up.

Recommended Magnetic Input Specifications

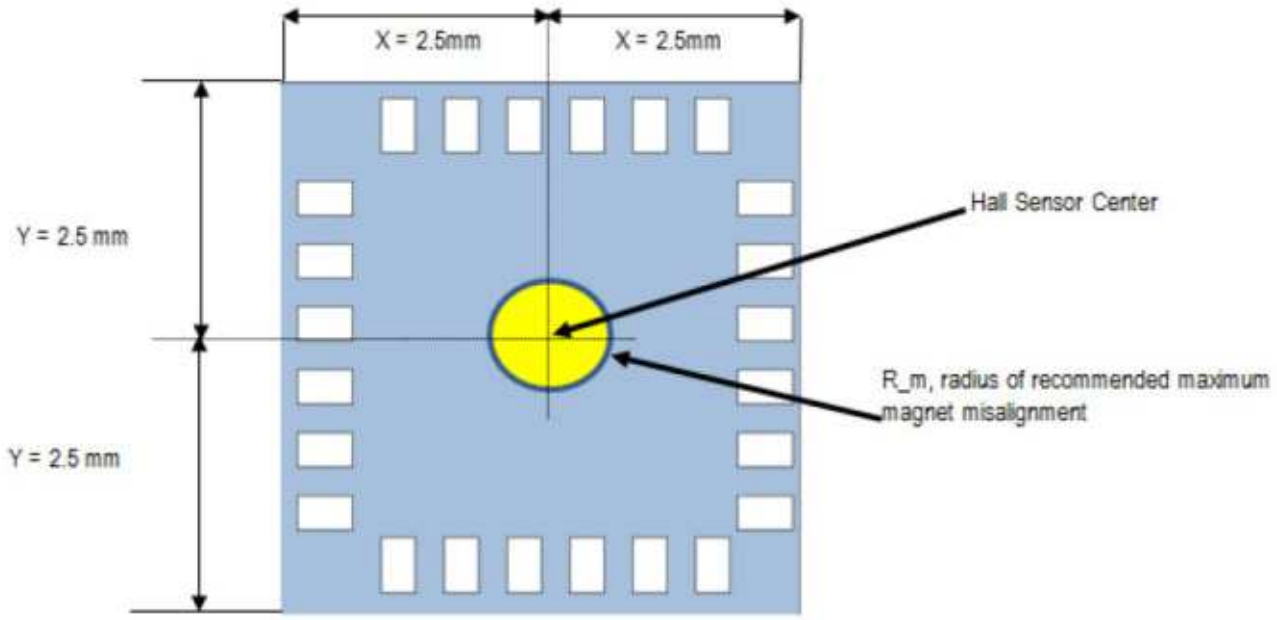
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter	d	—	6	—	mm	Recommended magnet: Cylindrical magnet, diametrically magnetized and 1 pole pair.
Thickness	t	—	2.5	—	mm	
Magnetic Input Field Magnitude	Bpk	45	—	75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet Displacement Radius	R_m	—	—	0.25	mm	Displacement between the magnet axis and the device center.
Recommended Magnet Material and Temperature Drift	—	—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Diametrically Magnetized Magnet



Magnet and IC Package Placement

Figure 5: Defined Chip Sensor Center and Magnet Displacement Radius

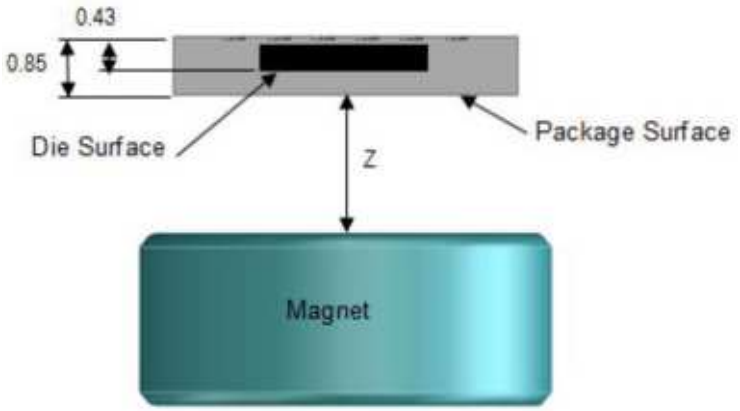


Align the magnet's center axis within a displacement radius of 0.25 mm from the defined Hall sensor center.

Place the magnet so that it faces the sensor. The magnet must be mounted on a nonmagnetic part. The Z gap varies depending on the magnetic strength on the die surface, with the recommended magnet material and dimensions.

The typical distance Z is 0.75 mm to 1.25 mm (1 mm ± 0.25 mm). It is important not to put magnetic material close to the magnet because it will affect the magnetic field and increase the INL.

Figure 6: Vertical Placement of the Magnet



Timing Characteristic

Symbol	Min.	Typ.	Max.	Unit	Notes
Fclk	—	—	10,000	kHz	SCL clock frequency for the SSI protocol
tREQ	300	—		ns	Minimum time required for the encoder to prepare SSI output
tNSLH	200	—	—	ns	Minimum wait time between SSI requests

NOTE: SSI timing characteristics are over the recommended operating range unless otherwise specified. See SSI 3 Wires for more information on the table.

Memory Map

The Broadcom AEAT-8811-Q24 uses nonvolatile one-time programmable (OTP) as shown in the following tables.

The memory is separated into 8 bits per address.

Nonvolatile Register (OTP)

1. OTP is one-time programmable only. Any OTP bit with value 0 can be written to 1, but *not* vice versa. Do *not* program 1 to the same address bit twice.
2. OTP shadow registers are volatile registers that are loaded with corresponding OTP values after power-on.
3. All bits (except addresses 0x00–0x03, 0x10–0x12, and 0x1B) are in a LOCK mode by default after power-on. To enter UNLOCK mode (to be able to write to the OTP shadow registers or registers), write 0xAB to address 0x10.
4. In UNLOCK mode, write to *any* OTP shadow registers or registers. Values written remain until power-off.
5. The UNLOCK state is maintained until the power supply is turned OFF or any value (except 0xAB) is written to address 0x10.
6. All OTP memory is programmable only by writing appropriate commands to addresses 0x11–0x14 and 0x1B.

OTP Shadow Registers

1. OTP shadow registers are volatile (upon power-up, reload values from OTP) and are not written to OTP automatically.
2. To write OTP shadow register values to OTP (nonvolatile) memory, see Programming OTP via SPI.
3. The OTP shadow registers are from addresses 0x00 to 0x0D. The following tables show the registers.

Customer Reserve and Zero Offset Registers

Table 2: Customer Reserve and Zero Reset Registers

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h0
0x01	[7:0]	Customer Reserve 1	User programmable	8'h0
0x02	[7:0]	Zero Reset0	Zero Reset Position [7:0]	8'h0
0x03	[7:0]	Zero Reset1	Zero Reset Position [15:8]	8'h0

Customer Configuration Registers

These registers are required to unlock and can be done by writing 8'hAB to address 0x10 and then writing to the OTP shadow register.

Customer Configuration 0

Table 3: Customer Configuration 0 Registers

Address	Bit(s)	Name	Description	Default
0x04	[7]	UVW Select	■ 1: select UVW mode ■ 0: select PWM mode	0
	[4:3]	I-width Setting	■ 11: (ABI) I-width = 360 electrical deg (edeg) ■ 10: (ABI) I-width = 270 electrical deg (edeg) ■ 01: (ABI) I-width = 180 electrical deg (edeg) ■ 00: (ABI) I-width = 90 electrical deg (edeg)	00
	[2:0]	UVW Setting/PWM Setting	■ 111: UVW = 2 pole pairs ■ 110: UVW = 1 pole pair ■ 101: UVW = 8 pole pairs ■ 100: UVW = 7 pole pairs ■ 011: UVW = 6 pole pairs ■ 010: UVW = 5 pole pairs ■ 001: UVW = 4 pole pairs ■ 000: UVW = 3 pole pairs	000

Customer Configuration 1

Table 4: Customer Configuration 1 Registers

Address	Bit(s)	Name	Description	Default
0x05	[6:3]	CPR Setting 1	■ 1111: (ABI) 512 CPR ■ 1110: (ABI) 256 CPR ■ 1101: (ABI) 128 CPR ■ 1100: (ABI) 64 CPR ■ 1011: (AB I) 32 CPR ■ 1010: (ABI) 4000 CPR ■ 1001: (ABI) 2000 CPR ■ 1000: (ABI) 1000 CPR ■ 0111: (ABI) 800 CPR ■ 0110: (ABI) 400 CPR ■ 0101: (ABI) 200 CPR ■ 0100: (ABI) 100 CPR ■ 0011: (ABI) 50 CPR ■ 0010: (ABI) 4096 CPR ■ 0001: (ABI) 2048 CPR ■ 0000: (ABI) 1024 CPR	0000
	[2:0]	Hysteresis Setting	■ 111: 0.18 mechanical degree (mdeg) ■ 110: 0.09 mechanical degree (mdeg) ■ 101: 0.04 mechanical degree (mdeg) ■ 100: 0.02 mechanical degree (mdeg) ■ 011: 0.01 mechanical degree (mdeg) ■ 010: 0.00 mechanical degree (mdeg) ■ 001: 0.07 mechanical degree (mdeg) ■ 000: 0.35 mechanical degree (mdeg)	000

Customer Configuration 2

Table 5: Customer Configuration 2 Registers

Address	Bit(s)	Name	Description	Default
0x06	[7]	Dir[a]	■ 1: Count up in a counter-clockwise rotation ■ 0: Count up in a clockwise rotation	0
	[6]	Zero Latency Mode[b]	■ 1: Zero Latency is ON ■ 0: Zero Latency is OFF	0
	[5:4]	Absolute Resolution	■ 11: 14-b absolute resolution (SSI) ■ 10: 16-b absolute resolution (SSI) ■ 01: 10-b absolute resolution (SSI) ■ 00: 12-b absolute resolution (SSI)	00
	[3]	SSI_Select	■ 1: Data 1st clock edge[c] ■ 0: Default	00
	[2:0]	CPR Setting 2[d]	■ 111: (ABI) 32, 64, 128, 256, 50, 100, 200, 400 CPR ■ 011: (ABI) 2048, 4096, 2000, 4000 CPR ■ 001: (ABI) 512, 1024, 800, 1000 CPR[e] ■ 000: (ABI) 512, 1024, 800, 1000 CPR	000

a. See Figure 7 for the direction definition.

b. When Zero Latency Mode is On, the user must set CPR setting 2 in 0x06 to 010 for all the applicable CPR (32–4096).

c. Initial Data Output tri-state (high impedance).

d. Incremental: CPR setting 1 in address 0x05 must match CPR setting 2 in 0x06.
Absolute: For absolute only application, set CPR setting 2 in 0x06 to 010.

e. For better dynamic performance, a higher latency setting is required.

Feature Settings

Zero Reset

The AEAT-8811-Q24 allows the user to configure a Zero Reset position. This value is stored at OTP 0x02 (lower 8-b) and 0x03 (upper 8-b). To set the Zero Reset position, for example, to position X, perform the following steps.

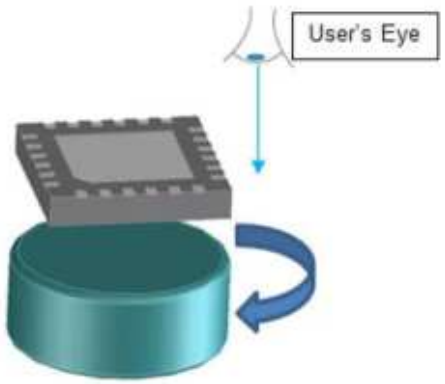
NOTE: The user should decide the desired direction or orientation (as detailed in Direction) before setting the Zero Reset position.

1. Stop the motor at position X.
2. Read the 16-b value of position X using the SSI protocol (for example, read 16'hABCD).
3. Write lower 8-b (from the preceding example, 8'hCD) to OTP shadow registers 0x02 using SPI.
4. Write upper 8-b (from the preceding example, 8'hAB) to OTP shadow registers 0x03 using SPI.
5. Confirm that the correct Zero Reset value is written to OTP shadow registers by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding step jumps incurred by noise).
6. To permanently save this Zero Reset value, write 8'hA2 to internal registers 0x12.
7. Power-cycle (power off and power on) the chip, and confirm that the correct Zero Reset value is written to OTP by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding step jumps incurred by noise).

Direction

The direction must be defined as to whether to count up clockwise or counterclockwise per rotation. Per the default setting, if the magnet is spinning clockwise based on the user's line of sight per the following figure, then the AEAT-8811-Q24 will count up.

Figure 7: Direction Definition When the Magnet Rotates



Absolute Output Format

The AEAT-8811-Q24 provides SSI 3 wires and PWM outputs to indicate the absolute position of the motor.

SSI 3 Wires

The SSI protocol uses three pins that are shared between the SSI and SPI protocols. Use SSI_SPI_sel (the input pin) to select either protocol at a time. Assert 1 on SSI_SPI_sel to select the SSI protocol, which supports up to 10-MHz clock rates.

- SSI_NSL_SPI_DIN → NSL (enable) signal for the SSI protocol, input to the AEAT-8811-Q24
- SSI_SCL_SPI_CLK → SCL (clock) signal for the SSI protocol, input to the AEAT-8811-Q24
- SSI_DO_SPI_DO → DO (data out) signal for the SSI protocol, output from the AEAT-8811-Q24

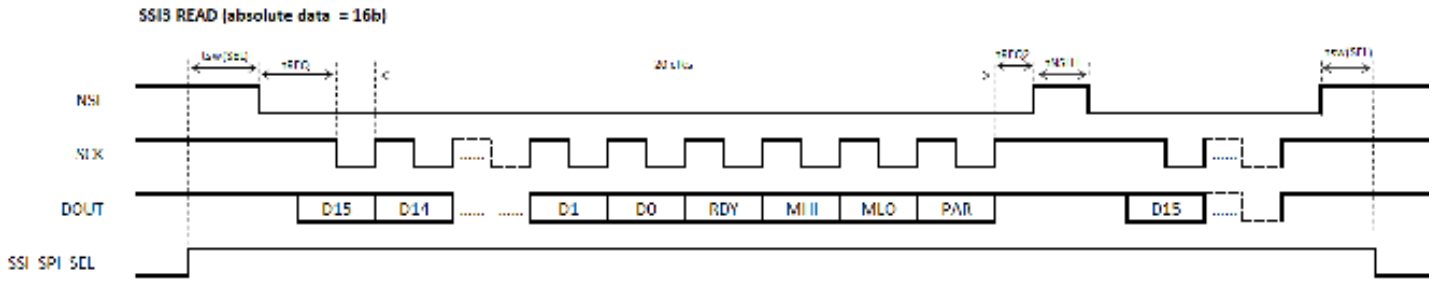
NOTE Notes for timing diagram in the following figure:

- NSL must be held high for at least 3 ms after power-up.
- NSL = 1 means it is in load mode and is used to obtain the position of the magnet.
- NSL = 0 is shift mode of the registers, and with the SCL (clock) pin, the register will be clocked.
- tREQ ≥ 300 ns.
- tNSLH ≥ 200 ns.

The user is advised to read from the SSI falling edge.

Figure 8: SSI Protocol Timing Diagram

Default: Data Output with 3-Wire SSI (SSI3 Mode), up to 10-MHz Clock Rates



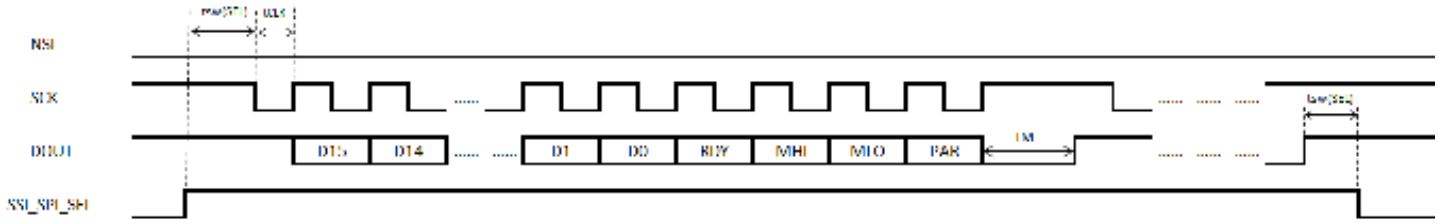
Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tREQ	SCL high time between the NLS falling edge and first SCL falling edge	300	—	—	ns
tREQ2	NSL low time after the rising edge of the last clock period for an SSI read	200	—	—	ns
tNSLH	NSL high time between two successive SSI reads	200	—	—	ns

NOTE:

- CLK = 1 when inactive; DIN = 1 when inactive.
- Important: Make sure that CLK is high when switching between SSI and SPI modes.
- The SSI data format may vary depending on the different settings on absolute resolution (16 bits, 14 bits, 12 bits, or 10 bits).
- The total data length is shown in the following figure.
- The three-bit status is for Ready, MHI, and MLO.

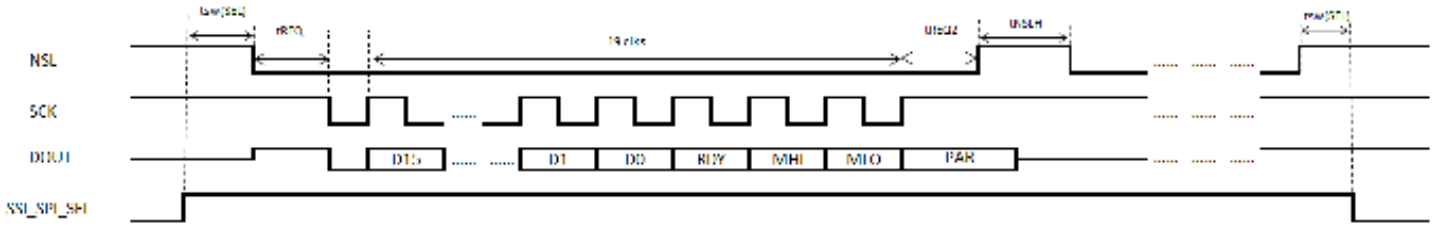
Configurable—Data readout with 2-wire SSI mode below:

NSL must be held *low* upon power cycle (NSL high will turn the IC into the default SSI3 mode), up to 2-MHz clock rates.



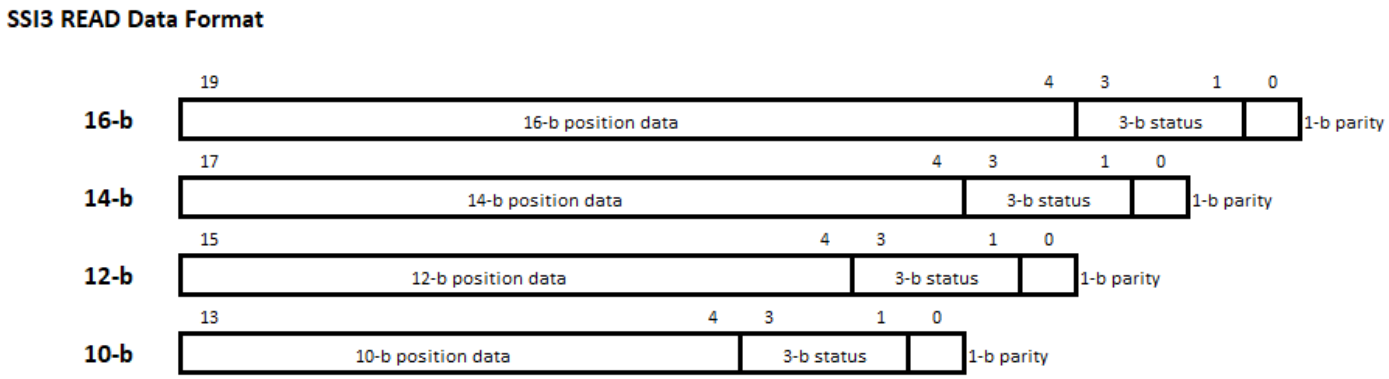
Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tClk	NSL low time after the rising edge of the last clock period for an SSI read	250	—	tM/2	ns
tM	NSL high time between two successive SSI reads	—	16.5	18.0	µs

User-programmable register option 3-wire SSI with initial data output tri-state (high impedance) to logic high to initiate the read-out, up to 10-MHz clock rates



Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tREQ	SCL high time between the NLS falling edge and the first SCL falling edge	300	—	—	ns
tREQ2	NSL low time after the rising edge of the last clock period for an SSI read	200	—	—	ns
tNSLH	NSL high time between two successive SSI reads	200	—	—	ns

Figure 9: SSI Output Format for Different Absolute Resolution Settings



NOTE:

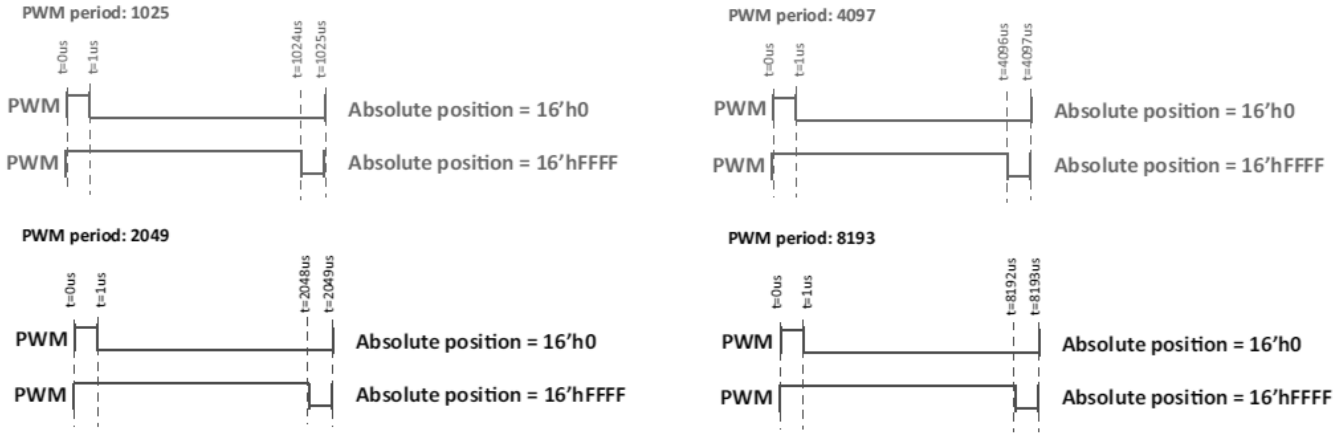
- Total data length: 16-b pos → 20-b, 14-b pos → 18-b, 12-b pos → 16-b, 10-b pos → 14-b
- 3-b status: {Ready, MHI, MLO}

- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready:** The chip is ready, and the ready value is 1.
  1-b parity is even parity.

PWM

The PWM protocol uses one output pin (W_PWM) from the AEAT-8811-Q24. Note that the W_PWM pin is shared between the UVW and PWM protocols. The PWM signals are configurable to have a period of 1025, 2049, 4097, or 8193 µs. During power-up, the PWM signal is 0 before the chip is ready.

Figure 10: PWM Signals (Period = 1025/2049/4097/8193 µs)



Incremental Output Format

The AEAT-8811-Q24 provides ABI and UVW signals to indicate the incremental position of the motor.

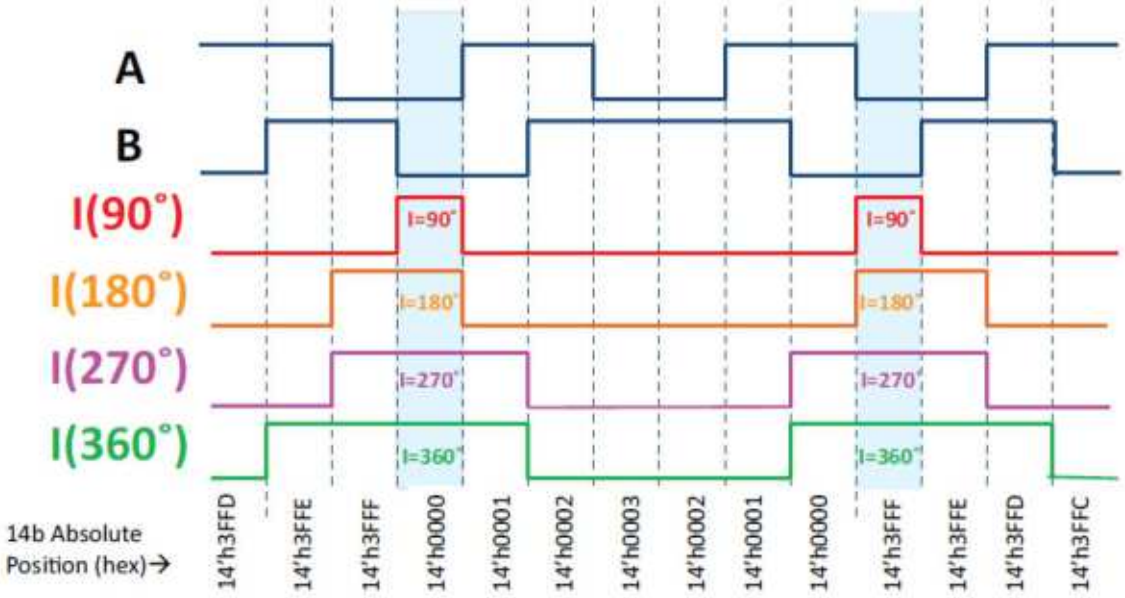
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

- Programmable CPR: 32, 64, 128, 256, 512, 1024, 2048, or 4096
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)

Figure 11: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming User Sets Hysteresis at 0.02 Mechanical Degrees

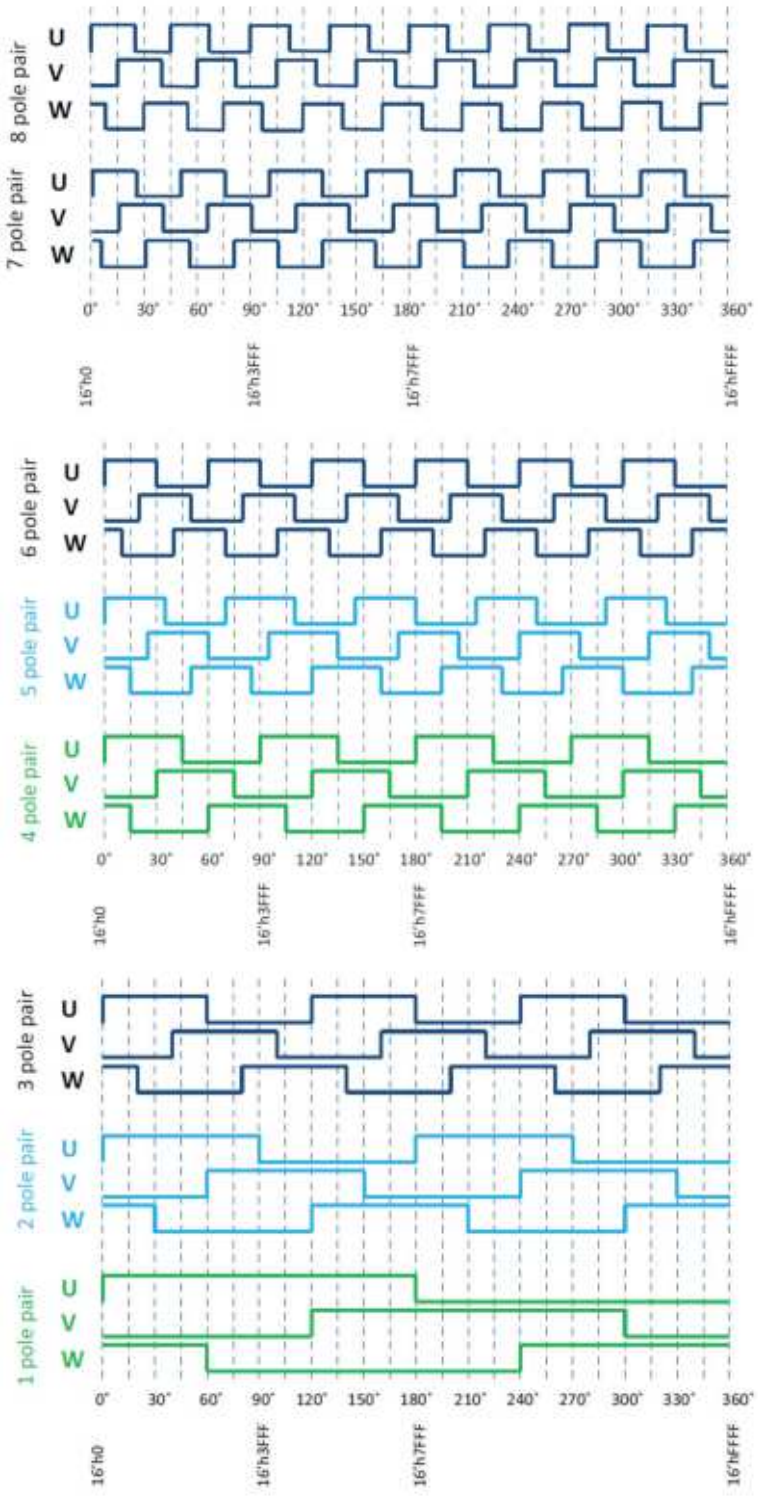


UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that the W_PWM pin is shared between the UVW and PWM protocols.

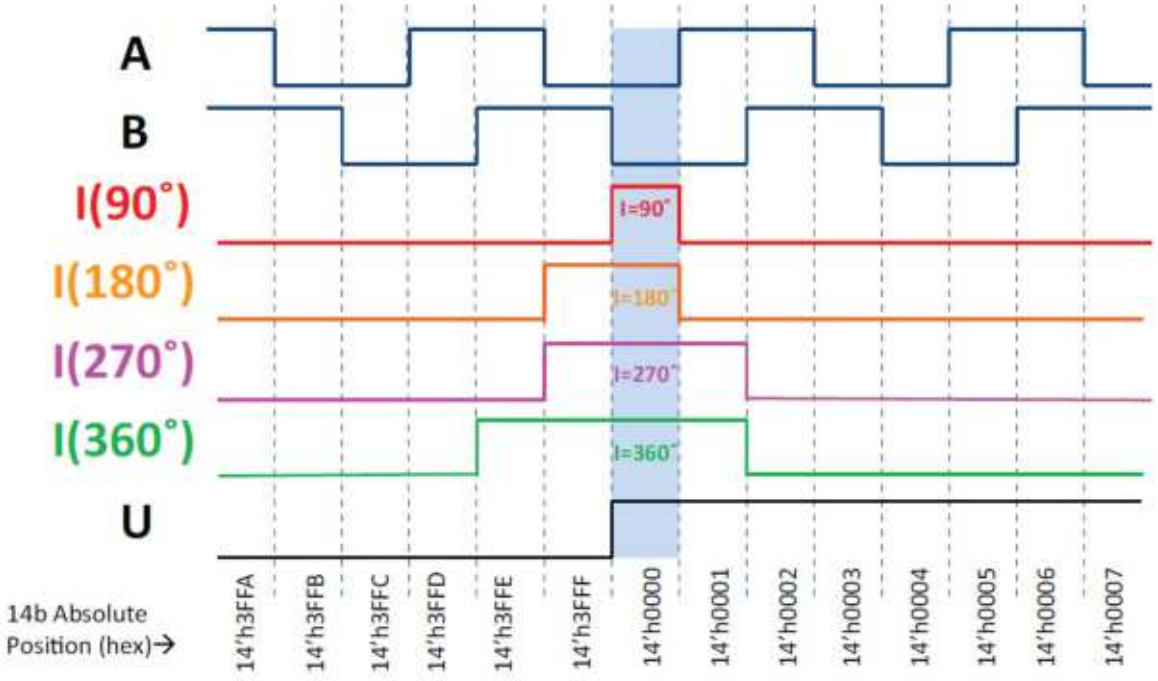
The AEAT-8811-Q24 can configure pole pairs from 1 to 8 (equivalent to 2 to 16 poles).

Figure 12: UVW Signals (1 to 8 Pole Pairs)



Note that signal U from the UVW protocol is tagged to signal I from the ABI protocol, as shown in the following figure.

Figure 13: U-to-I Tagging



Programming the AEAT-8811-Q24

The OTP shadow registers and internal registers are programmable using the SPI protocol. Writing specific commands to specific addresses of internal registers will program values of OTP shadow registers to OTP permanently.

SPI Protocol

The SPI protocol uses three pins from the AEAT-8811-Q24. These three pins are shared between the SSI and SPI protocols. SSI_SPI_sel (input pin) selects either protocol at a time. Assert 0 on SSI_SPI_sel to select the SPI protocol. The AEAT-8811-Q24 supports the SPI protocol from 10 kHz to 1 MHz.

- SSI_NSL_SPI_DIN → DIN (data in) signal for the SPI protocol, input to the AEAT-8811-Q24
- SSI_SCL_SPI_CLK → CLK (clock) signal for the SPI protocol, input to the AEAT-8811-Q24
- SSI_DO_SPI_DO → DO (data out) signal for the SPI protocol, output from the AEAT-8811-Q24

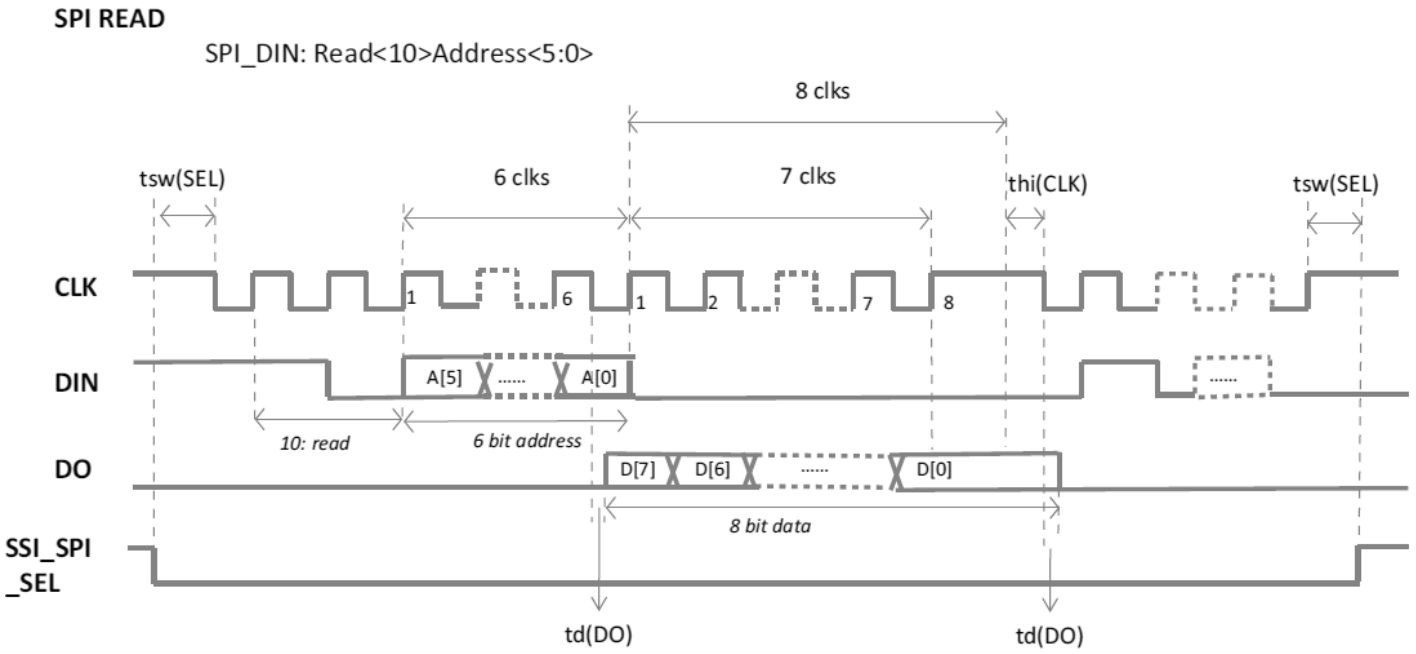
To read an address using SPI:

DIN: Read<2'b10>Address<5:0>; from 8 bits DIN

Read 8-bit data on DO by clocking 8 SPI_CLK clock.

NOTE: The user should read output data at the rising edge of SPI_CLK.

Figure 14: SPI Read Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time.	1	—	—	µs
td(DO)	DO data valid after the falling edge of CLK. The user should read output data at the rising edge of SPI_CLK.	—	—	200	ns
thi(CLK)	CLK high time after the end of the last clock period for an SPI read/write command.	300	—	—	ns

NOTE:

- CLK = 1 when inactive; DIN = 1 when inactive.
- Important: Make sure that CLK is high when switching between SSI and SPI modes.

To write to an address using SPI:

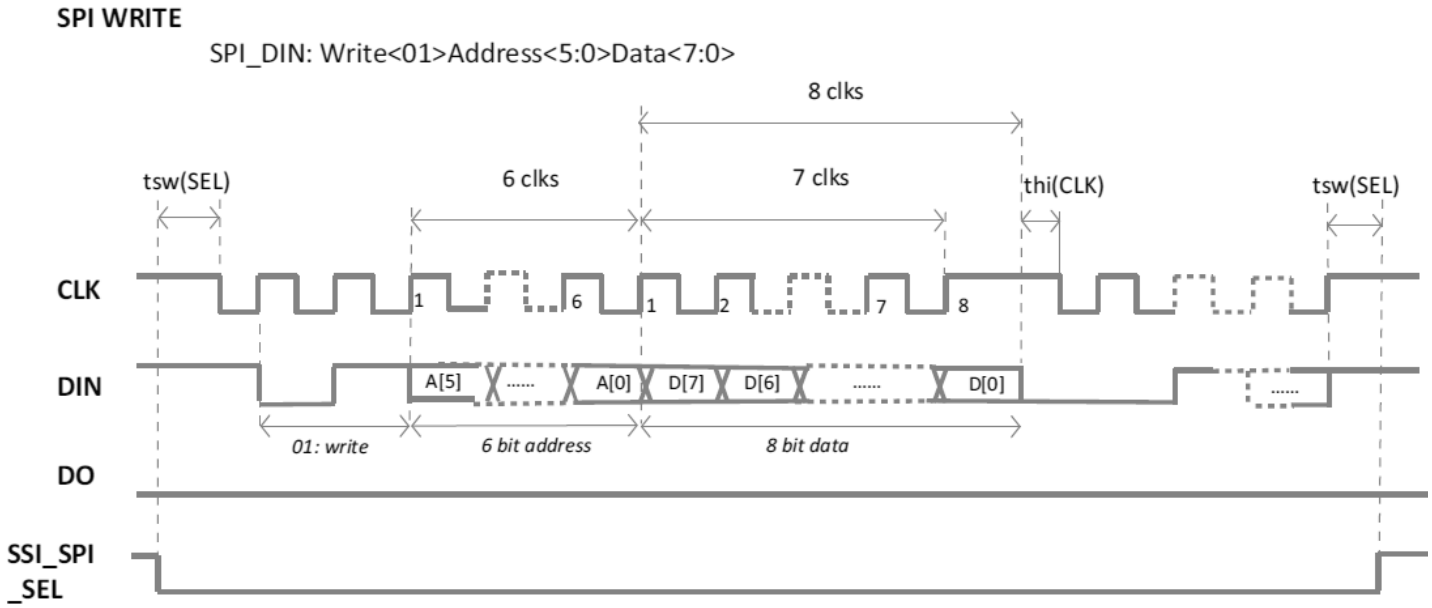
Write <2'b01>Address<5:0>; from 8 bits DIN

SPI_DIN: Write<01>Address<5:0>Data<7:0>

Write is specified as 2 bits (01) in the MSB of the address bus, followed by the 6-bit address, and lastly by the 8-bit data.

NOTE: The user should read back the data to confirm that the data was written successfully.

Figure 15: SPI Write Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time.	1	—	—	µs
thi(CLK)	CLK high time after the end of the last clock period for an SPI read/write command.	300	—	—	ns

NOTE:

- CLK = 1 when inactive; DIN = 1 when inactive.
- Important: Make sure that CLK is high when switching between SSI and SPI modes.

Programming OTP via SPI

Here are steps for permanently programming the OTP nonvolatile memory.

Change the voltage at the VDDA pin to 5.6V ± 0.1V for OTP programming.

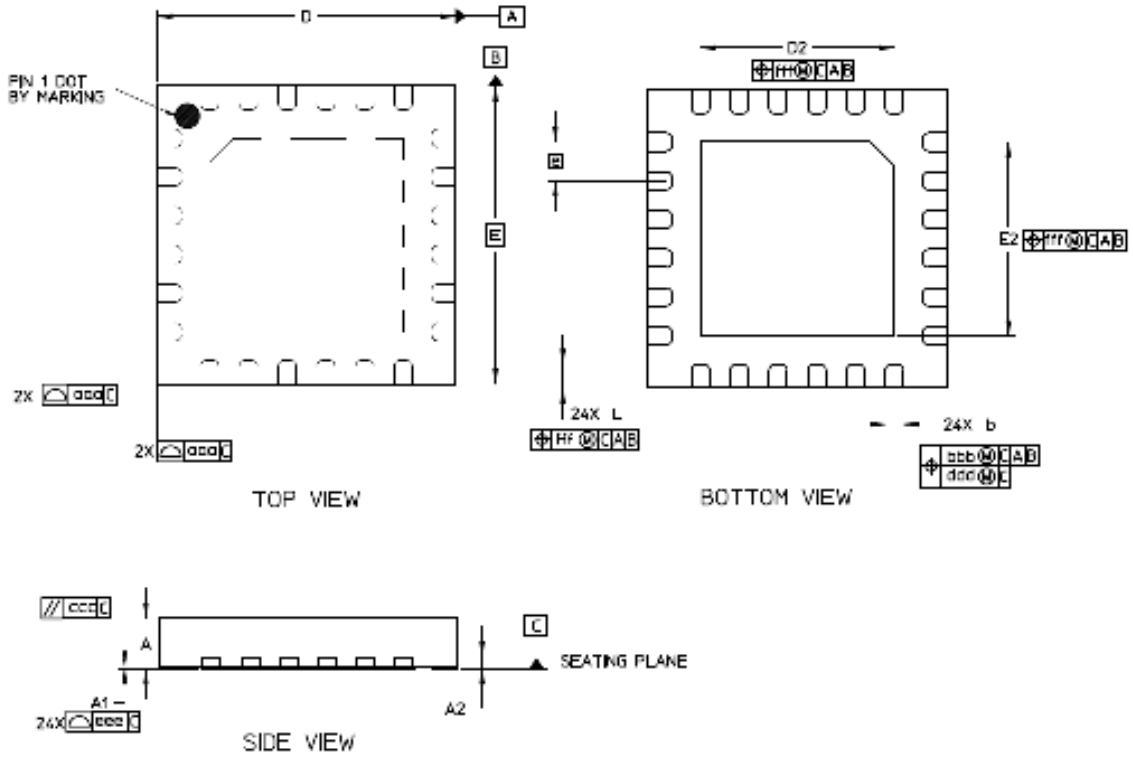
See the memory map address as described in Memory Map.

The following are details on register 0x10 to 0x13.

Address	Bit(s)	Name	Description	Default
0x10	[7:0]	Unlock Registers	Write 0xAB to this address to unlock all OTP shadow registers and internal registers (except 0x00–0x03, 0x10, 0x11, 0x12, and 0x1B, which are not locked).	8'h0
0x11	[7:0]	Program Customer Reserved OTP (0x00, 0x01)	Write 0xA1 to this address to program Customer Reserved OTP (0x00, 0x01) to OTP.	8'h0
0x12	[7:0]	Program ST Zero Reset OTP (0x02, 0x03)	Write 0xA2 to this address to program ST Zero Reset OTP (0x02, 0x03) to OTP.	8'h0
0x13	[7:0]	Program Customer Configuration OTP (0x04, 0x05, 0x06)	Write 0xA3 to this address to program Customer Configuration OTP (0x04, 0x05, 0x06) to OTP.	8'h0

Package Drawings (in mm)

Figure 16: AEAT-8811, 24 QFN Dimensions



Dimension Reference			
REF	**Min.**	**Nom.**	**Max.**
A	0.8	0.85	0.9
A1	0	—	0.05
A2	0.203	REF	—
D	5	BSC	—
E	5	BSC	—
D2	3.2	3.25	3.3
E2	3.2	3.25	3.3
b	0.25	0.3	0.35
e	0.65	BSC	—
L	0.35	0.4	0.45
Dimension Tolerance			
aaa	0.1		
bbb	0.1		
ccc	0.05		
ddd	0.05		
eee	0.08		
fff	0.05		

Recommended PCB Land Pattern (in mm)

Figure 17: Land Pattern Dimension

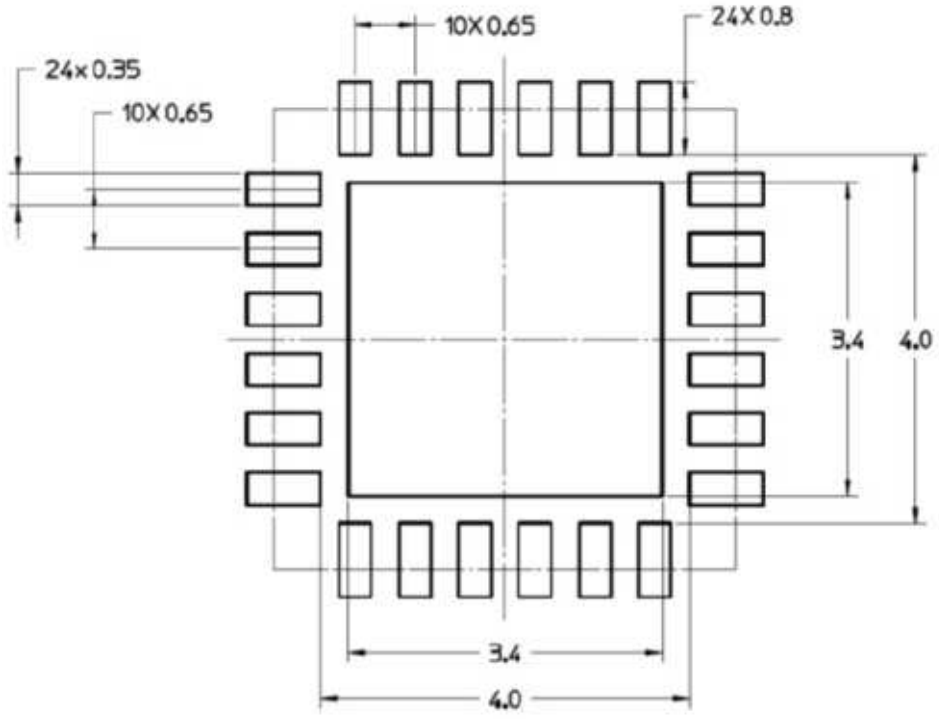
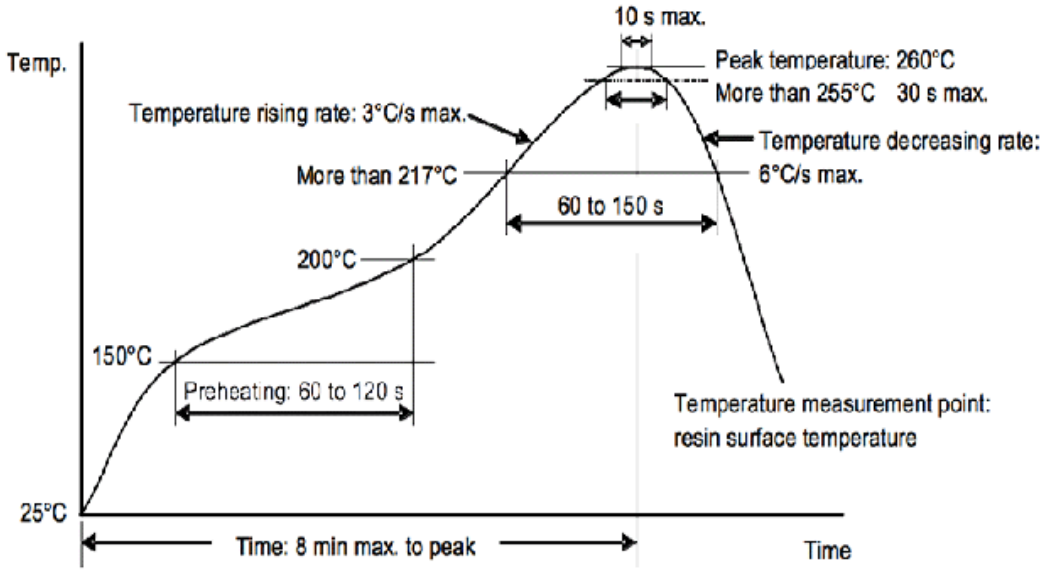


Figure 18: Recommended Lead-Free Solder Reflow Soldering Temperature Profile



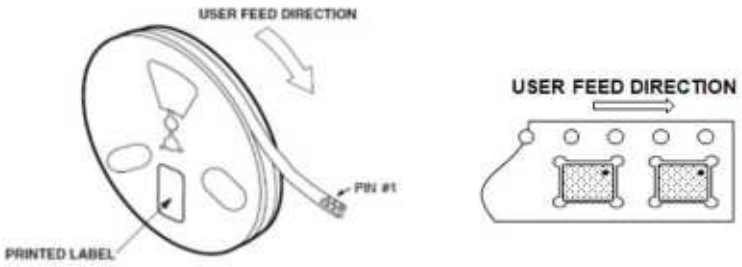
Product Ordering Information

Ordering Part Number	Product Description	Package	Delivery Form
AEAT-8811-Q24	Programmable 16-bit rotary magnetic encoder	QFN 24 leads, 5 mm × 5 mm	Tube
AEAT-8811-Q24TR	Programmable 16-bit rotary magnetic encoder	QFN 24 leads, 5 mm × 5 mm	Tape and Reel

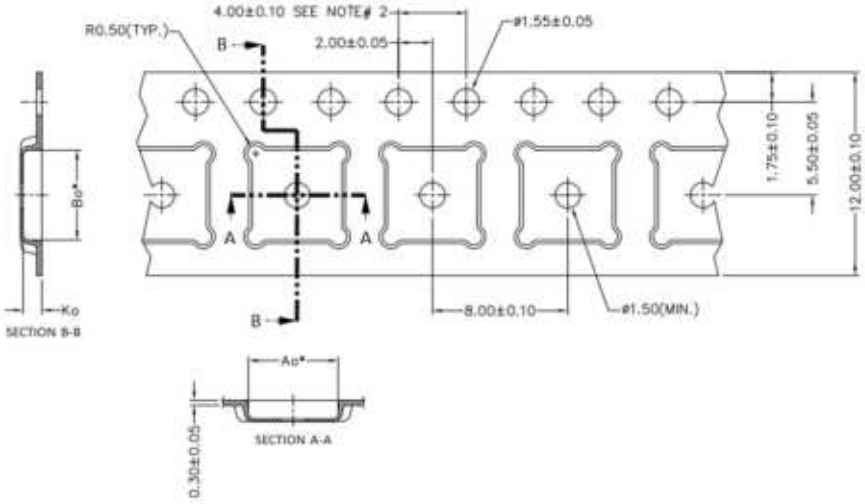
OTP Programming Kit Ordering Information (Optional)

Ordering Part Number	Product Description
HEDS-8999	AEAT-8811-Q24 Magnetic Encoder Programming Kit

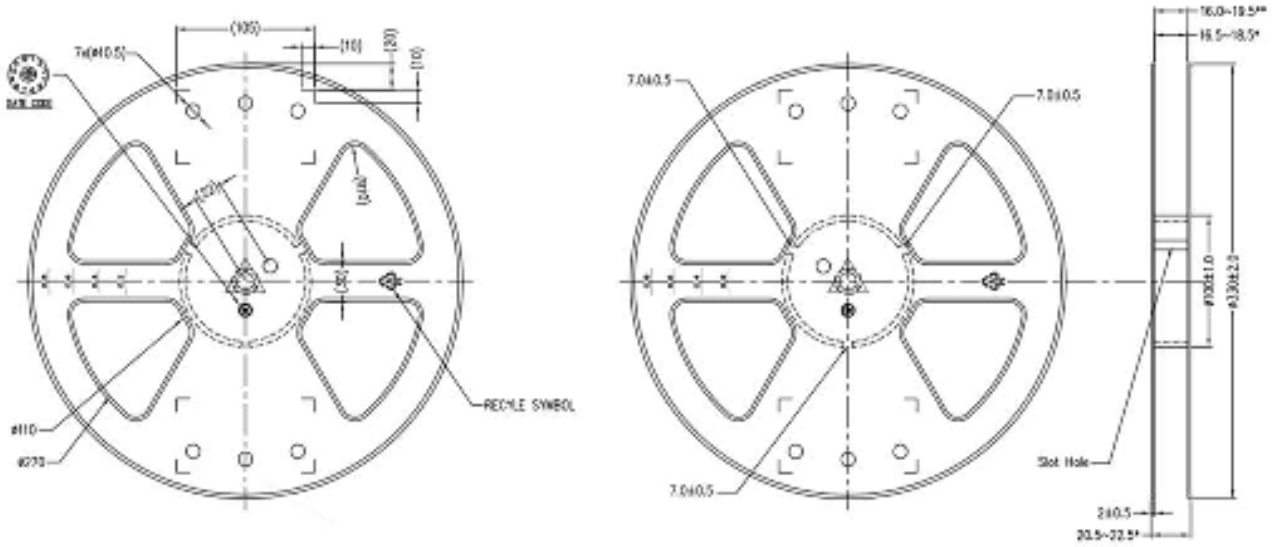
Packaging Information



Tape cavity dimension



Reel dimension



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