BURR - BROWN®



AFE1205

2Mbps, Single Pair HDSL ANALOG FRONT END

FEATURES

- E1/T1 SINGLE PAIR 2B1Q OPERATION
- COMPLETE ANALOG INTERFACE
- 385mW POWER DISSIPATION
- PROGRAMMABLE POWER
- 48-LEAD SSOP PACKAGE
- SCALEABLE DATA RATE
- OPERATION FROM 2.3Mbps TO 160kbps
- +5V ONLY (5V OR 3.3V DIGITAL)
- –40°C TO +85°C OPERATION

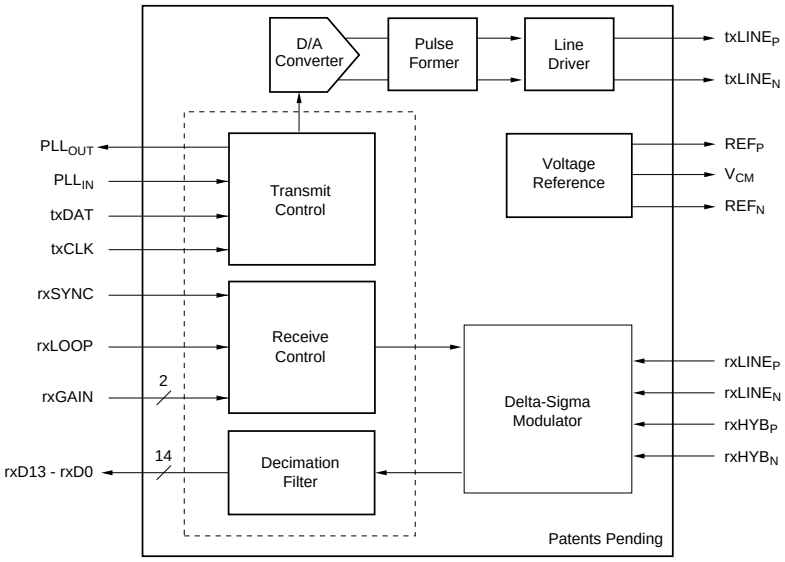
DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of a single pair HDSL (High bit rate Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect an HDSL digital signal processor to an external compromise hybrid and an HDSL line transformer. The transmit and receive filter responses automatically change with clock frequency, allowing the AFE1205 to operate over a wide range of data rates. The power dissipation of the device can be reduced under digital control for operation at lower speeds. The AFE1205 will operate at bit rates from 160kbps to 2.3Mbps. It meets ETSI PSD specifications for single pair E1, as well as ETSI and ANSI PSD specifications for two pair E1 and T1.

Functionally, this unit consists of a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. The chip uses only 385mW for full-speed operation. It is housed in a small 48-lead SSOP package.

The receive channel is designed around a fourth-order delta-sigma analog-to-digital converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first-order analog echo cancellation. A programmable gain amplifier with gains 0dB to +9dB is also included. The delta-sigma modulator, operating at a 24X oversampling ratio, produces a 14-bit output at symbol rates up to 1168kHz (for 2.3Mbps operation).

The transmit channel consists of a digital-to-analog converter and switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data and generates a standard 2B1Q output waveform. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).



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SPECIFICATIONS

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{tx} = 1168kHz (E1 single pair rate) and Normal Power mode, unless otherwise specified.

PARAMETER	COMMENTS	AFE1205E MIN	AFE1205E TYP	AFE1205E MAX	UNITS
RECEIVE CHANNEL					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential(1)		±3.0		V
Common-Mode Voltage	1.5V CMV Recommended		+1.5		V
Input Impedance	All Inputs		See Typical Performance Curves		
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Resolution		14			Bits
Programmable Gain	Four Gains: 0dB, 3.25dB, 6dB, and 9dB				
Settling Time	Gain, rxSYNC, or Power Mode Change(8)		6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR(2)
Output Data Coding			Binary Two's Complement		
Data Rate	Normal Power	384		2320	kbps
	Medium Power	192		1168	kbps
	Low Power	160		320	kbps
Output Word Rate	Normal Power, rxSYNC(3)	196		1168	kHz
TRANSMIT CHANNEL					
Transmit Clock Rate, f_{TX}	Symbol Rate, Normal Power	196		1168	kHz
	Symbol Rate, Medium Power	96		584	kHz
	Symbol Rate, Low Power	80		160	kHz
Transmit –3dB Point	2320kbps		485		kHz
	1168kbps		292		kHz
	784kbps		196		kHz
Transmit Power(5)		13	13.5	14	dBm
Pulse Output			See Typical Performance Curves		
Common-Mode Voltage, V_{CM}			$AV_{DD}/2$		V
Output Resistance(5)	DC to 1MHz		1		Ω
TRANSCEIVER PERFORMANCE					
Uncancelled Echo(6)	rxGAIN = 0dB, Loopback Enabled			–67	dB
	rxGAIN = 0dB, Loopback Disabled			–67	dB
	rxGAIN = 3.25dB, Loopback Disabled			–69	dB
	rxGAIN = 6dB, Loopback Disabled			–71	dB
	rxGAIN = 9dB, Loopback Disabled			–73	dB
DIGITAL INTERFACE(5)					
Logic Levels					
V_{IH}	$\|I_{IH}\| < 10\mu A$	$DV_{DD} - 1$		$DV_{DD} + 0.3$	V
V_{IL}	$\|I_{IL}\| < 10\mu A$	–0.3		+0.8	V
V_{OH}	$I_{OH} = -20\mu A$	$DV_{DD} - 0.5$			V
V_{OL}	$I_{OL} = 20\mu A$			+0.4	V
POWER					
Analog Power Supply Voltage	Specification		5		V
	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
	Operating Range	3.15		5.25	V
Power Dissipation(4, 7)	Normal Power, 1:2 Line Transformer		385		mW
	Medium Power, 1:2 Line Transformer		300		mW
	Low Power, 1:2 Line Transformer		240		mW
Power Dissipation(7)	Normal Power, DV_{DD} = 5V, 1:2 Line Transformer		415		mW
PSRR			55		dB
TEMPERATURE RANGE					
Operating(5)		–40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from $txLINE_P$ and $txLINE_N$). (5) Guaranteed by design and characterization. (6) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (7) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. The AFE1205 is tested with a 1:2 line transformer. (8) This is the settling time required for any gain change, change of rxSYNC or any change of power mode.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	AGND	Analog Ground for PLL
2	Power	AV_{DD}	Analog Supply (+5V) for PLL
3	Input	txCLK	Symbol Clock
4	Ground	DGND	Digital Ground
5	Input	txDAT	XMTDA from MtH1210B
6	Output	rxD0	ADC Output Bit 0
7	Output	rxD1	ADC Output Bit 1
8	Output	rxD2	ADC Output Bit 2
9	Output	rxD3	ADC Output Bit 3
10	Output	rxD4	ADC Output Bit 4
11	Output	rxD5	ADC Output Bit 5
12	Ground	DGND	Digital Ground
13	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
14	Output	rxD6	ADC Output Bit 6
15	Output	rxD7	ADC Output Bit 7
16	Output	rxD8	ADC Output Bit 8
17	Output	rxD9	ADC Output Bit 9
18	Output	rxD10	ADC Output Bit 10
19	Output	rxD11	ADC Output Bit 11
20	Output	rxD12	ADC Output Bit 12
21	Output	rxD13	ADC Output Bit 13
22	Input	PWSEL	Power Control
23	Input	rxSYNC	ADC Sync Signal
24	Input	rxGAIN0	Receive Gain Control Bit 0
25	Input	rxGAIN1	Receive Gain Control Bit 1
26	Input	rxLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	AV_{DD}	Analog Supply (+5V)
28	Input	$rxHYB_N$	Negative Input from Hybrid Network
29	Input	$rxHYB_P$	Positive Input from Hybrid Network
30	Input	$rxLINE_N$	Negative Line Input
31	Input	$rxLINE_P$	Positive Line Input
32	Ground	AGND	Analog Ground
33	Ground	AGND	Analog Ground
34	Output	REF_P	Positive Reference Output, Nominally 3.5V
35	Output	V_{CM}	Common-Mode Voltage (buffered), Nominally 2.5V
36	Output	REF_N	Negative Reference Output, Nominally 1.5V
37	Power	AV_{DD}	Analog Supply (+5V)
38	Ground	AGND	Analog Ground
39	Output	$txLINE_N$	Transmit Line Output Negative
40	Power	AV_{DD}	Analog Supply (+5V)
41	Output	$txLINE_P$	Transmit Line Output Positive
42	Ground	AGND	Analog Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL_{OUT}	PLL Filter Output
48	Input	PLL_{IN}	PLL Filter Input

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ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} + 0.3V
Analog Outputs Short Circuit to Ground (+25°C)	Continuous
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
PLL_{IN} or PLL_{OUT} to AGND	–0.3V to AV_{DD} + 0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} + 0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} + 0.3V
AGND, DGND Differential Voltage	0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	700mW

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
AFE1205E	48-Lead SSOP	333	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



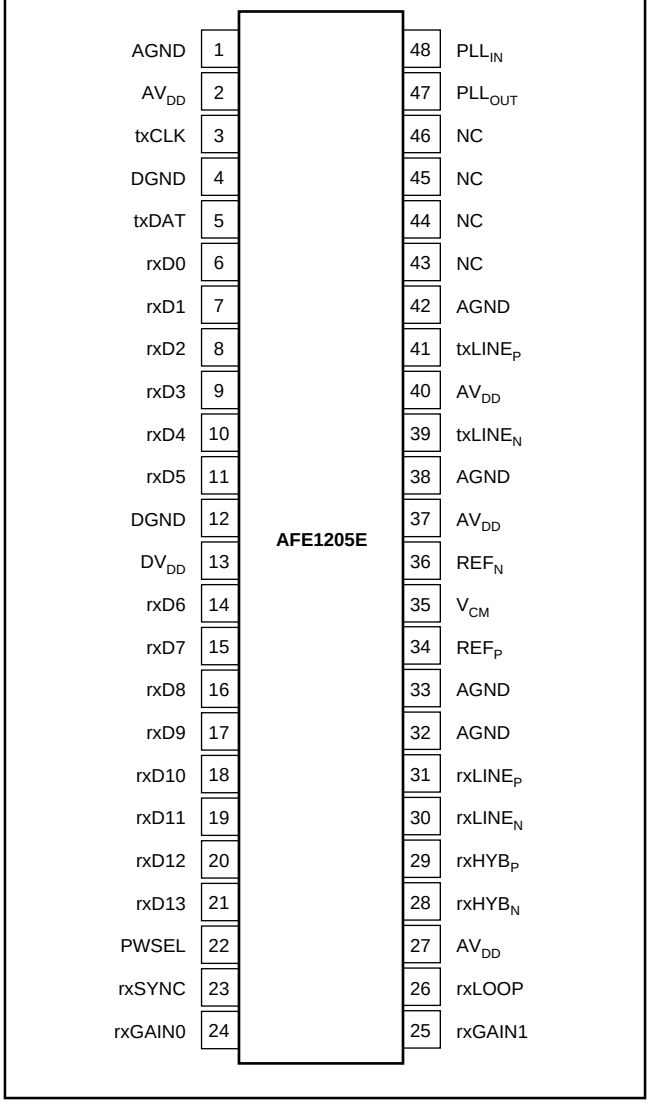
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

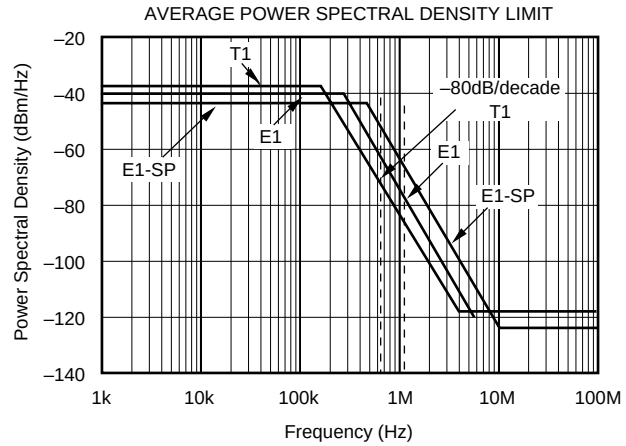
Top View **SSOP**



TYPICAL PERFORMANCE CURVES

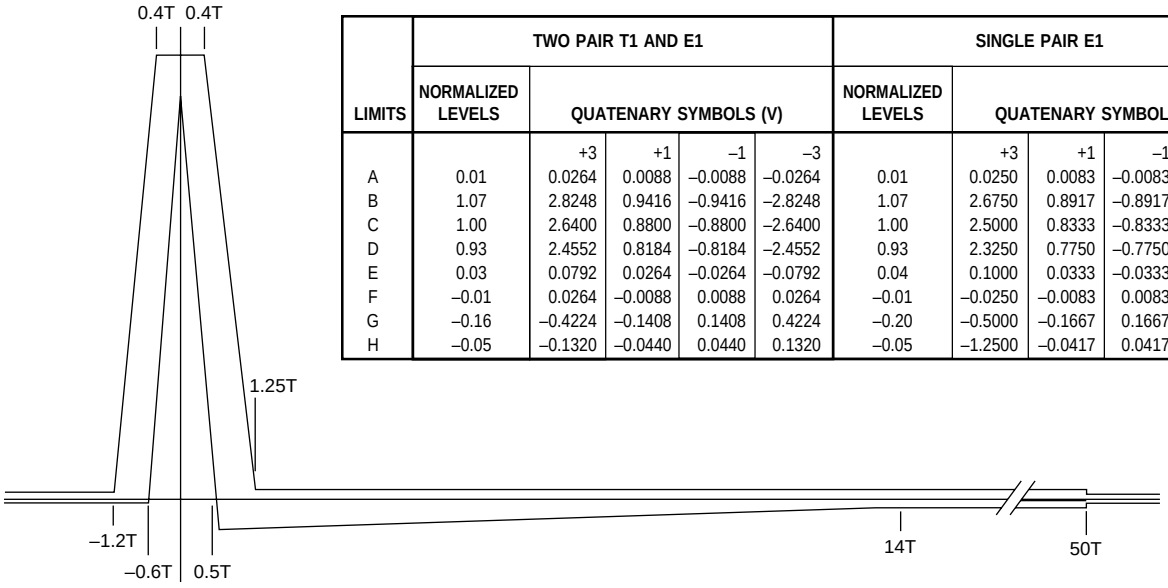
At Output of Pulse Transformer

Typical at 25°C, AV_{DD} = +5V, and DV_{DD} = +3.3V, unless otherwise specified.



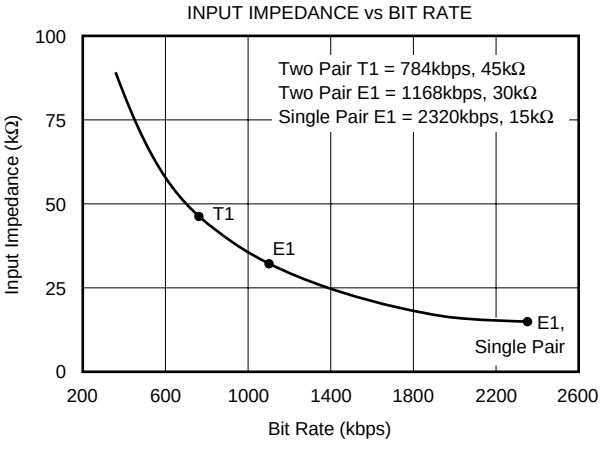
SPEED	LOWER LIMIT	BREAK FREQUENCY	SLOPE	UPPER LIMIT
T1, Two Pair	–38dBm/Hz	196kHz	–80dB/decade	–118dBm/Hz
E1, Two Pair	–40dBm/Hz	292kHz	–80dB/decade	–120dBm/Hz
E1, Single Pair (E1-SP)	–42.5dBm/Hz	485kHz	–80dB/decade	–122dBm/Hz

CURVE 1. Upper Bound of Power Spectral Density Measured at the Transformer Output.



LIMITS	TWO PAIR T1 AND E1					SINGLE PAIR E1				
	NORMALIZED LEVELS	QUATENARY SYMBOLS (V)				NORMALIZED LEVELS	QUATENARY SYMBOLS (V)			
		+3	+1	–1	–3		+3	+1	–1	–3
A	0.01	0.0264	0.0088	–0.0088	–0.0264	0.01	0.0250	0.0083	–0.0083	0.0250
B	1.07	2.8248	0.9416	–0.9416	–2.8248	1.07	2.6750	0.8917	–0.8917	–2.6750
C	1.00	2.6400	0.8800	–0.8800	–2.6400	1.00	2.5000	0.8333	–0.8333	–2.5000
D	0.93	2.4552	0.8184	–0.8184	–2.4552	0.93	2.3250	0.7750	–0.7750	–2.3250
E	0.03	0.0792	0.0264	–0.0264	–0.0792	0.04	0.1000	0.0333	–0.0333	–0.1000
F	–0.01	0.0264	–0.0088	0.0088	0.0264	–0.01	–0.0250	–0.0083	0.0083	0.0250
G	–0.16	–0.4224	–0.1408	0.1408	0.4224	–0.20	–0.5000	–0.1667	0.1667	0.5000
H	–0.05	–0.1320	–0.0440	0.0440	0.1320	–0.05	–1.2500	–0.0417	0.0417	0.1250

CURVE 2. Transmitted Pulse Template and Actual Performance as Measured at the Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

THEORY OF OPERATION

The transmit channel consists of a D/A converter and a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from the DSP and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first-order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces 14 bits of resolution at output rates up to 584kHz. The basic functionality of the AFE1205 is illustrated in Figure 1.

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, rxD13-rxD0.

SCALEABLE TIMING

The AFE1205 scales operation with the clock frequency. All internal filters, the A/D converter, the D/A converter, and the pulse former change frequency with the clock speed so that the unit can be used at different frequencies by changing the clock speed.

rxLOOP INPUT

rxLOOP is the loopback control signal. When enabled, the $rxLINE_P$ and $rxLINE_N$ inputs are disconnected from the AFE. The $rxHYB_P$ and $rxHYB_N$ inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to rxLOOP.

ECHO CANCELLATION IN THE AFE

The rxHYB input is designed to be subtracted from the rxLINE input for first-order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the rxHYB input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in Binary Two's Complement code.

ANALOG INPUT	OUTPUT CODE (rxD13 - rxD0)
Positive Full Scale	01111111111111
Mid Scale	00000000000000
Negative Full Scale	10000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, rxGAIN1 and rxGAIN0. The resulting gain between 0dB and +9dB is shown below.

rxGAIN1	rxGAIN0	GAIN
0	0	0dB
0	1	3.25dB
1	0	6dB
1	1	9dB

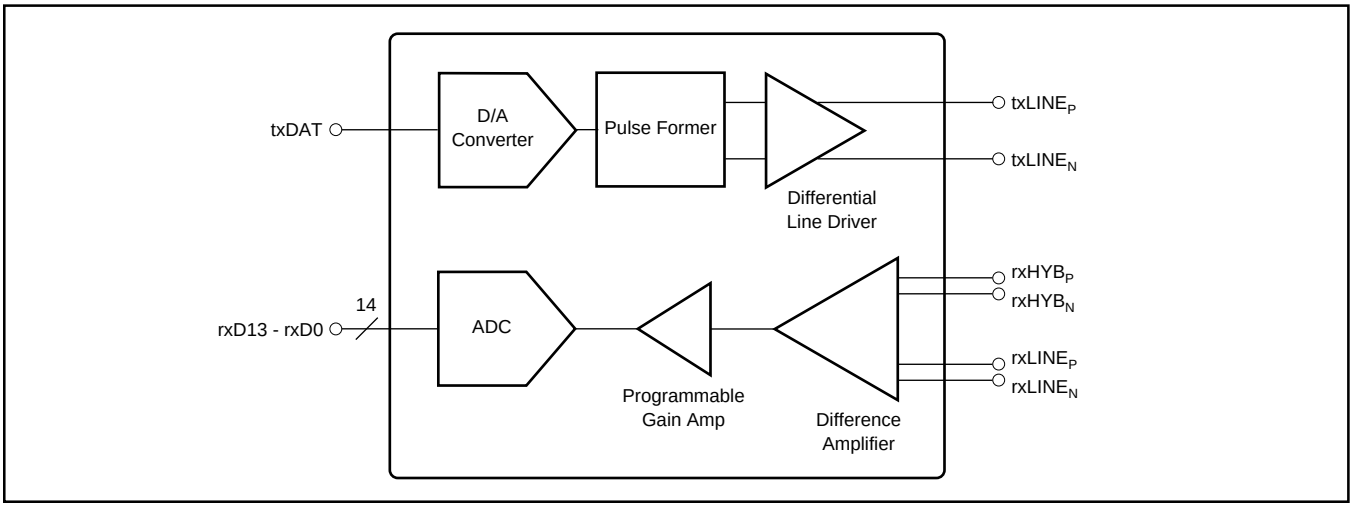


FIGURE 1. Functional Block Diagram of AFE1205.

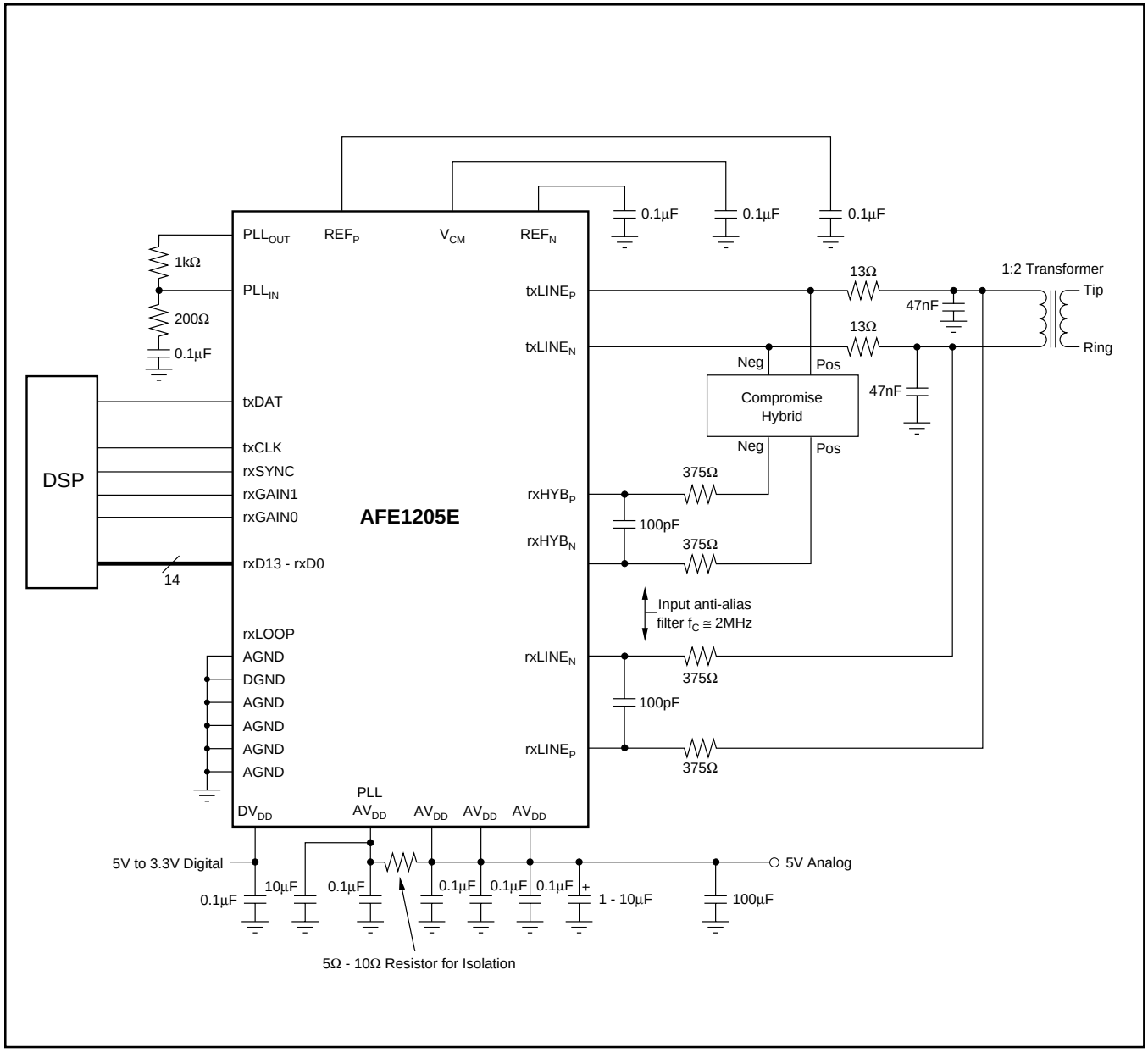


FIGURE 2. Basic Connection Diagram.

rxHYB AND rxLINE INPUT ANTI-ALIASING FILTERS

The –3dB frequency of the input anti-aliasing filter for the rxLINE and rxHYB differential inputs should be approximately 2MHz for operation at 2.3Mbps. Suggested values for the filter are 375Ω for each of the two input resistors and 100pF for the capacitor. Together the two 375Ω resistors and the 100pF capacitor result in –3dB frequency of just over 2MHz. The 375Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1205.

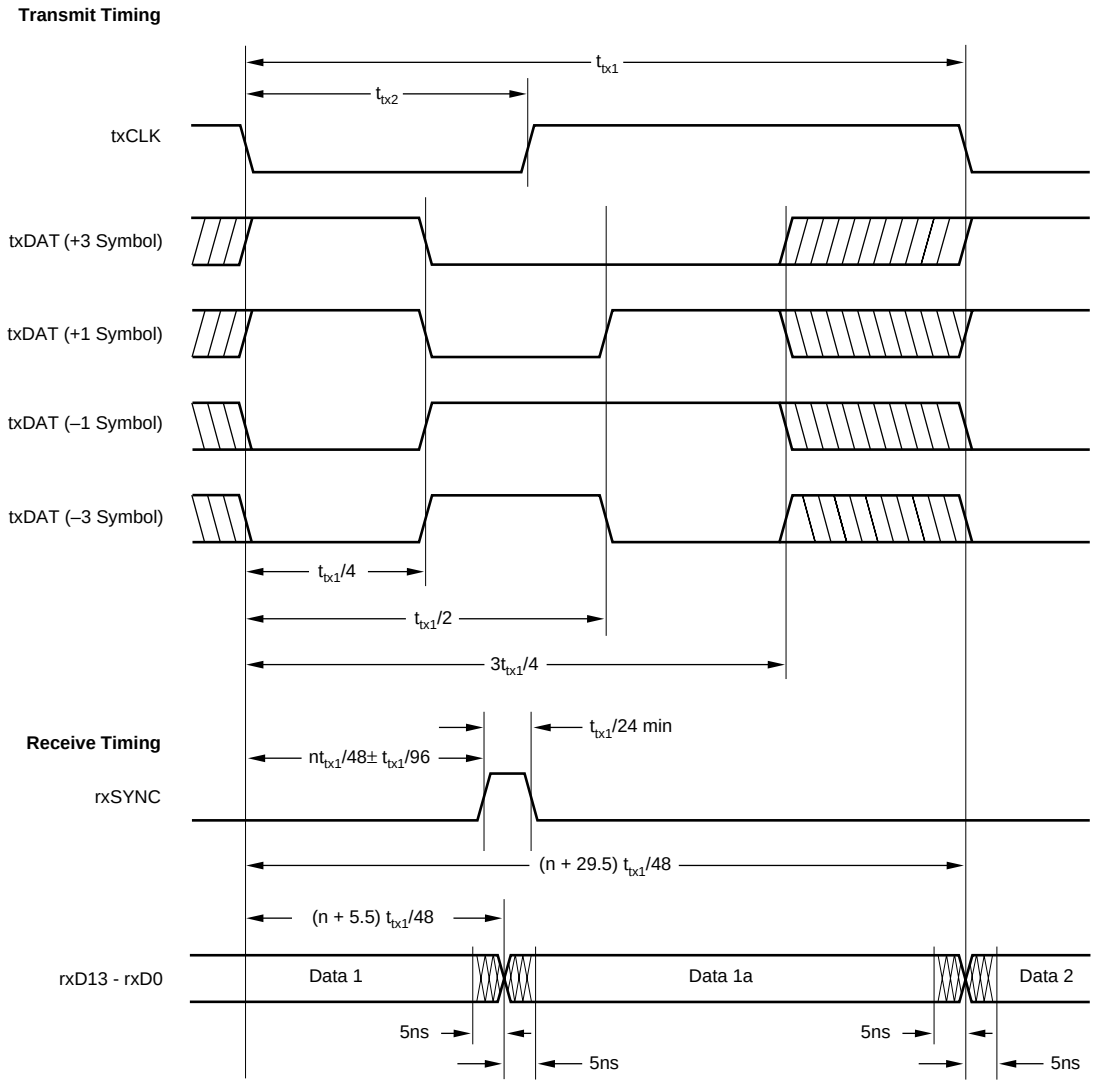
This circuit applies at rates of 1Mbps to 2Mbps. For slower rates, the anti-aliasing filters will give best performance with their –3dB frequency approximately equal to the bit rate. For example, a –3dB frequency of 500kHz should be used for a single pair bit rate of 500kbps.

rxHYB AND rxLINE INPUT BIAS VOLTAGE

The transmitter output on the txLINE pins and the rxLINE inputs are centered at midscale, 2.5V.

Inside the AFE1205, the rxHYB and rxLINE signals are subtracted as described in the paragraph on echo cancellation above. This means that the rxHYB inputs need to be centered at 2.5V just as the rxLINE signal is centered at 2.5V. The external compromise hybrid must be designed so that the signal into the rxHYB inputs remains centered at 2.5V.

TIMING DIAGRAM



NOTES: (1) An output symbol must be sent to the AFE1205 through the txDAT pin during each baud period. (2) Any transmit sequence not shown above will result in a zero symbol. (3) All transitions are specified relative to the falling edge of txCLK. (4) For each new symbol period, the initial txDAT transition occurs on the falling edge of txCLK. (5) The maximum allowable timing error for the initial txDAT transition is $\pm t_{tx1}/10$ (±86ns for single pair E1 rates). The maximum allowable timing error for the two subsequent txDAT transitions is $\pm t_{tx1}/12$ (±72ns for single pair E1 rates). (6) The txDAT input is read by the AFE1205 at 1/8, 3/8, and 5/8 of a symbol period from the falling edge of txCLK. (7) rxSYNC can shift to one of 48 discrete delay times from the falling edge of txCLK. (8) It is recommended that rxD13 - rxD0 be read on the rising edge of rxSYNC.

FIGURE 3. Timing Diagram.

RECEIVE TIMING

The rxSYNC signal controls portions of the A/D converter's decimation filter and the data output timing of the A/D converter. It is generated at the symbol rate by the user and must be synchronized with txCLK. The rising edge of rxSYNC can occur at the falling edge of txCLK or it can be shifted by the user in increments of 1/48 of a symbol period to one of 47 discrete delay times after the falling edge of txCLK.

RECEIVE OUTPUT DATA RATE

The receive channel delta-sigma A/D converter of the AFE1205 uses a modulator which operates at an oversampling rate of 24X the symbol rate. The A/D converter's decimation filter downsamples the modulator output by a factor of 12. The bandwidth of the decimation filter is equal to one-half the symbol rate. This yields two output words per symbol period. These two output words are shown as Data 1 and Data 1a in Figure 3. The specifications of the AFE1205 assume that one A/D converter output is used per symbol period and the other output is ignored. The Receive Timing diagram above suggests using the rising edge of the rxSYNC pulse to read the first data output in a symbol period. Either data output may be used. Both data outputs may be used for more flexible post-processing.

DISCUSSION OF SPECIFICATIONS

UNCANCELLED ECHO

The key measure of transceiver performance is uncancelled echo. This measurement is made as shown in the diagram of Figure 4. The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncancelled echo signal. Once the filter taps have converged, the rms value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncancelled echo contains only noise and linearity errors generated in the transmitter and receiver.

The data sheet value for uncancelled echo is the ratio of the rms uncancelled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted (S_1 closed in Figure 4).

PROGRAMMABLE POWER DISSIPATION

The power dissipation of the AFE1205 is digitally programmable by the user to three levels: Normal, Medium, and Low. The maximum bit rate of the AFE1205 is 2.3Mbps with Normal power dissipation. At lower power dissipation levels, the maximum bit rate is lower and in addition, the minimum bit rate is lower. The power control pin (pin 22) has three input levels: Logic 1, Logic 0, and high impedance. In the high impedance state, up to 20µA leakage current can be tolerated out of the power control pin. The AFE1205 requires six baud periods to settle after a change in the power control pin status.

Typical power dissipation specifications, shown in Table I, assume a 5V analog supply, a 3.3V digital supply, standard 13.5dBm delivered to the line, a pseudo random equiprobable sequence of HDSL output pulses, and a 1:2 turns ratio line transformer. The power dissipation specifications includes all power dissipated in the AFE1205—it does not include power dissipated in the external load. The external power is 16.5dBm, 13.5dBm to the line and 13.5dBm to the impedance matching resistors. The external power of 16.5dBm is 45mW. If a 5V digital supply is used rather than a 3.3V supply, the power dissipation increases by approximately 3mW.

POWER LEVEL	MAXIMUM SPEED (Mbps)	MINIMUM SPEED (kbps)	TYPICAL POWER DISSIPATION (mW)	PIN 22 INPUT
Normal	2.320	384	385	Logic 1
Medium	1.168	192	300	Logic 0
Low	0.320	160	240	High Impedance

TABLE I. Power Control Operation.

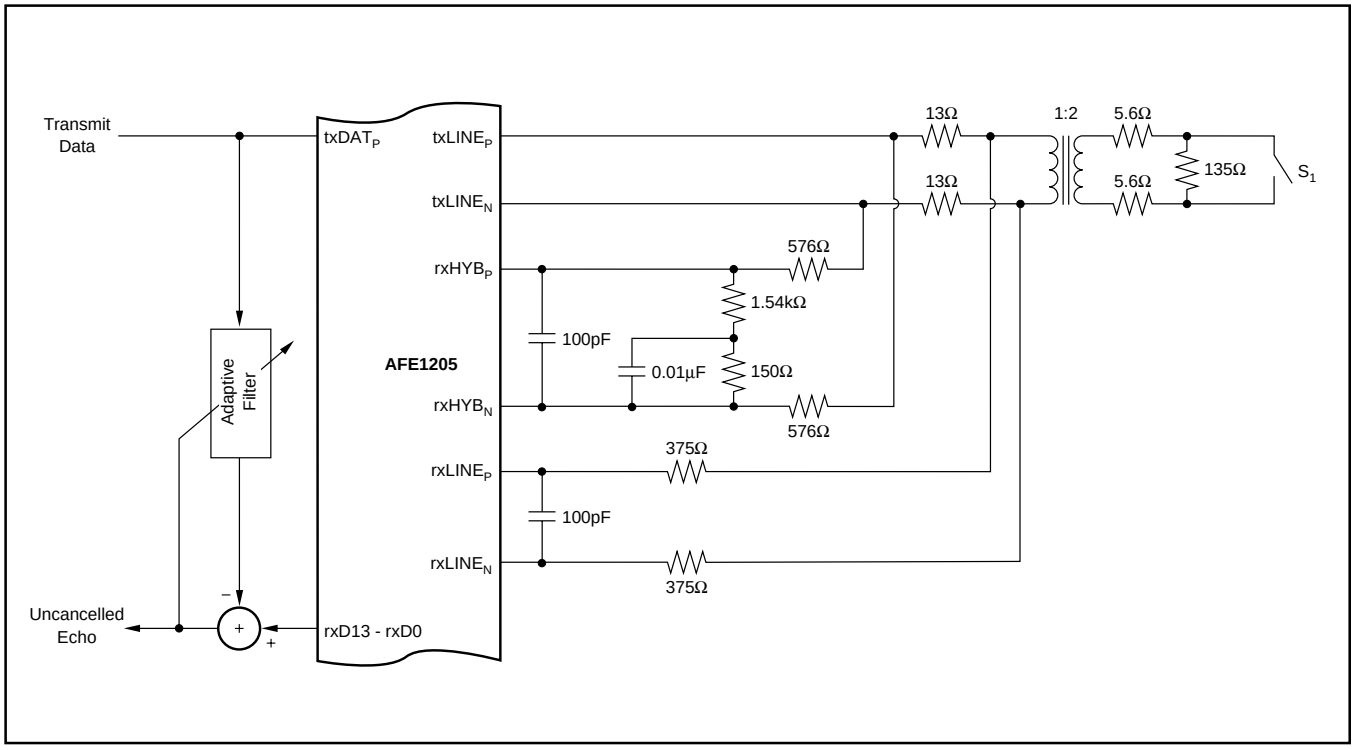


FIGURE 4. Uncancelled Echo Test Diagram.

LAYOUT

The analog front end of an HDSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, phase-lock to a high-speed digital clock, and convert the line input to a high-precision (14-bit) digital output. Thus, there are really three sections of the AFE1205: the digital section, the phase-locked loop, and the analog section. A combined analog and digital ground plane is recommended. The ground plane should pass under all of the AFE1205 and its pins.

The power supply for the digital section of the AFE1205 can range from 3.3V to 5V. This supply should be decoupled to digital ground with a ceramic 0.1µF capacitor placed as close to DGND (pin 12) and DV_{DD} (pin 13) as possible. Ideally, both a digital power supply plane and a ground plane should run up to and underneath the digital pins of the AFE1205 (pins 3 through 26). However, DV_{DD} may be supplied by a wide printed circuit board (PCB) trace. A ground plane underneath all digital pins is strongly recommended.

The Phase Locked Loop (PLL) analog supply, pin 2, must be derived from AV_{DD}, the general analog supply. The power supply to the PLL must be in the range of 4.75V to 5.25V.

The PLL section of the AFE1205 should be decoupled with both a 10µF tantalum capacitor and a 0.1µF ceramic capacitor. Both capacitors should be placed between pins 1 and 2. The ceramic capacitor should be placed as close to the AFE1205 as possible. The placement of the tantalum capacitor is not as critical, but should be close. A 5Ω to 10Ω resistor should be used to connect the PLL supply (pin 2) to the analog supply. This resistor, in combination with the 10µF tantalum capacitor, form a low pass filter to keep glitches that occur on the general analog supply, AV_{DD}, from affecting the PLL supply. The PLL ground (pin 1) should connect directly to the grond plane.

The remaining portion of the AFE1205 should be considered analog. All AGND pins should be connected directly to a common analog ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE1205 by a small trace.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
AFE1205E	ACTIVE	SSOP	DL	48	30
AFE1205E/1K	ACTIVE	SSOP	DL	48	1000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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