AK4348

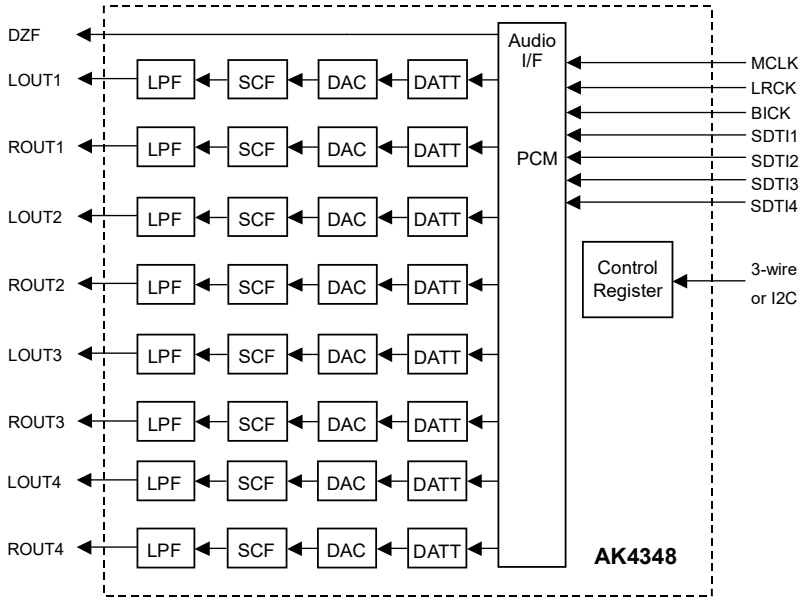
3.3V 192kHz 24-Bit 8-Channel DAC

GENERAL DESCRIPTION

The AK4348 is an 8-channel 24bit DAC operating off of a single +3.3V power supply. The outputs are single-ended, and it samples at rates from 8kHz to 192kHz. It uses AKM's advanced multi-bit architecture for the modulator to achieve a wide dynamic range while preserving linearity for improved THD+N performance. The output circuit includes a switched-cap filter and a second-order analog low pass filter, minimizing the need for external filtering.

FEATURES

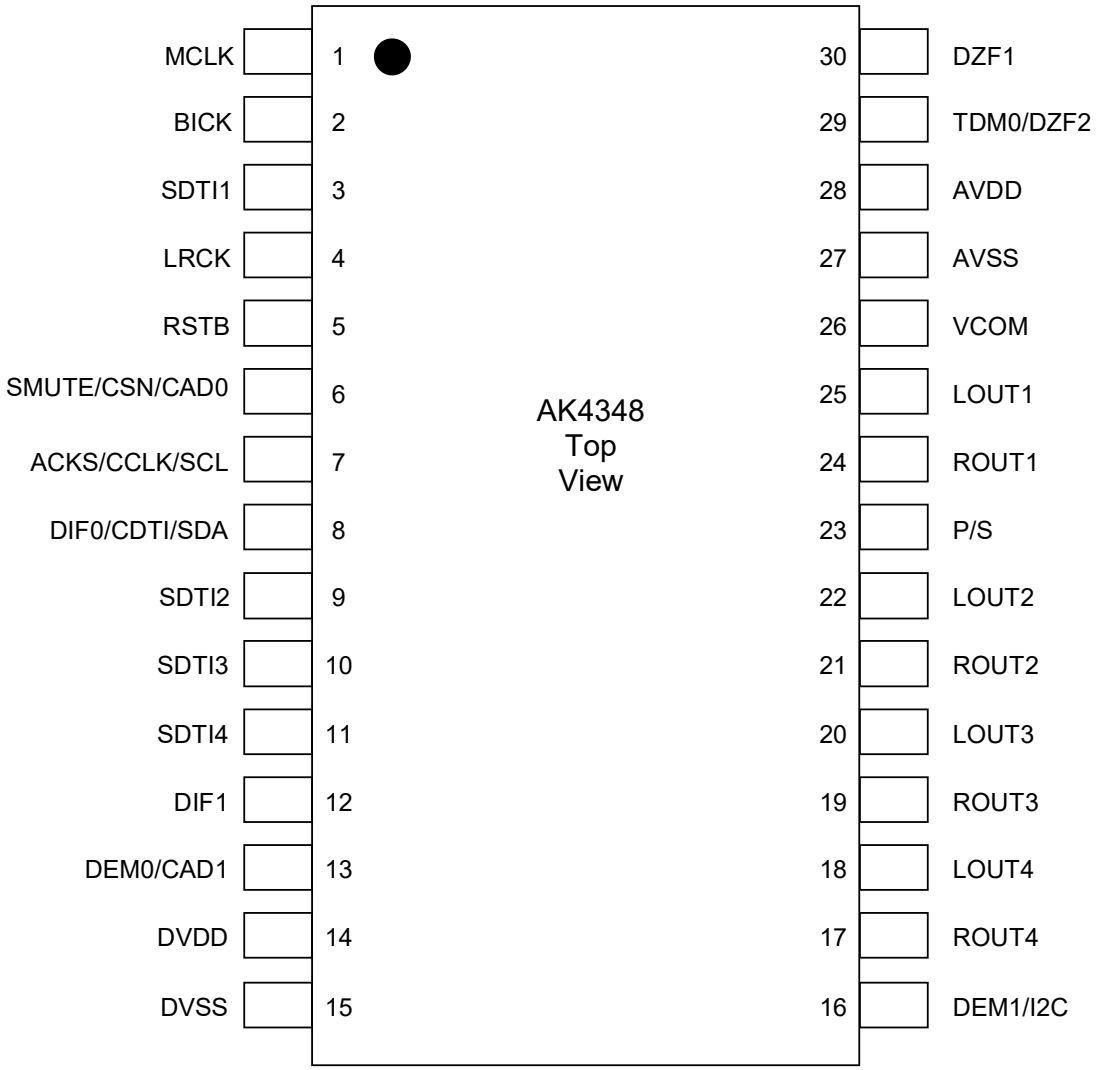
- ☐ **Sampling Rate: 8kHz to 192kHz**
- ☐ **24-Bit 8 times Digital Filter with Slow Roll-Off Option**
- ☐ **DR, S/N: 104dB**
- ☐ **THD+N: -90dB**
- ☐ **High Tolerance to Clock Jitter**
- ☐ **Single Ended Output Buffer with Second Order Analog LPF**
- ☐ **Digital De-emphasis for 32, 44.1 & 48kHz sampling**
- ☐ **Zero Detect Function**
- ☐ **Channel Independent Digital Attenuator (Linear 256 steps)**
- ☐ **3-wire Serial or I^2C Control**
- ☐ **I/F format: MSB justified, LSB justified (16-, 20-, 24-bit), I^2S, TDM**
- ☐ **Master clock: 256fs, 384fs, 512fs or 768fs or 1152fs (Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs or 192fs (Quad Speed Mode)
- ☐ **Power Supply: 2.7V to 3.6V**
- ☐ **Ta = –20 ~ 85°C (EF), –40 ~ 85°C (VF)**
- ☐ **Package: 30-pin VSOP**
- ☐ **AK4359 Pin Compatible**



■ Ordering Guide

AK4348EF	-20 ~ +85°C	30pin VSOP
AK4348VF	-40 ~ +85°C	30pin VSOP
AKD4348	Evaluation Board for AK4348	

■ Pin Layout



■ Compatibility with AK4359

Function	AK4359	AK4348
Power supply voltage	4.5 to 5.5V	2.7 to 3.6V
#29 pin function in parallel control mode	"L" output	TDM0 pin (pull-down pin)
Chip address for 3-wire uP I/F	N/A	CAD1 (CAD0 is fixed.)
Chip address for I2C uP I/F	CAD0	CAD0, CAD1

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock
3	SDTI1	I	DAC1 Audio Serial Data Input
4	LRCK	I	L/R Clock
5	RSTB	I	Reset Mode When at "L", the AK4348 is in reset mode. The AK4348 must be reset once upon power-up.
6	SMUTE	I	Soft Mute in parallel control mode "H": Enable, "L": Disable
	CSN	I	Chip Select in serial 3-wire mode
	CAD0	I	Chip Address in serial I2C mode
7	ACKS	I	Auto Setting Mode in parallel control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock in serial 3-wire control mode
	SCL		Control Data Clock in serial I2C control mode
8	DIF0	I	Audio Data Interface Format in parallel control mode
	CDTI	I	Control Data Input in serial 3-wire control mode
	SDA	I/O	Control Data in serial I2C control mode
9	SDTI2	I	DAC2 Audio Serial Data Input
10	SDTI3	I	DAC3 Audio Serial Data Input
11	SDTI4	I	DAC4 Audio Serial Data Input
12	DIF1	I	Audio Data Interface Format
13	CAD1	I	Chip Address in serial control mode
	DEM0	I	De-emphasis Filter Enable
14	DVDD		Digital Power Supply, +2.7~+3.6V
15	DVSS		Digital Ground
16	I2C	I	μP I/F Mode Select in serial control mode "L": 3-wire Serial, "H": I^2C Bus
	DEM1	I	De-emphasis Filter Enable in parallel control mode
17	ROUT4	O	DAC4 Right Channel Analog Output
18	LOUT4	O	DAC4 Left Channel Analog Output
19	ROUT3	O	DAC3 Right Channel Analog Output
20	LOUT3	O	DAC3 Left Channel Analog Output
21	ROUT2	O	DAC2 Right Channel Analog Output
22	LOUT2	O	DAC2 Left Channel Analog Output
23	P/S	I	Parallel/Serial Control Mode Select (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
24	ROUT1	O	DAC1 Right Channel Analog Output
25	LOUT1	O	DAC1 Left Channel Analog Output
26	VCOM	O	Common Voltage, AVDD/2 Normally connected to AVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
27	AVSS	-	Analog Ground
28	AVDD	-	Analog Power Supply, +2.7~+3.6V
29	TDM0	I	TDM I/F Format Mode in parallel control mode (Internal pull-down pin) "L": Normal mode, "H": TDM 256 mode
	DZF2	O	Data Zero Input Detect in serial control mode
30	DZF1	O	Data Zero Input Detect

Note: All input pins except P/S and TDM0 pins should not be left floating.

■ Handling of Unused Pins

Unused I/O pins should be resolved as shown in this table.

Classification	Pin Name	Setting
Analog	LOUT4-1, ROUT4-1	Leave open.
Digital	DZF2-1	Leave open.
	SDTI4-1 SMUTE (Parallel control mode)	Connect to DVSS.
	DEM0, DIF1 (Serial control mode)	Connect to DVDD or DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter			Symbol	Min	Max	Units
Power Supplies	Analog		AVDD	-0.3	4.6	V
	Digital		DVDD	-0.3	4.6	V
	|AVSS-DVSS|	(Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)			IIN	-	±10	mA
Analog Input Voltage			VINA	-0.3	AVDD+0.3	V
Digital Input Voltage			VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature		AK4348EF	Ta	-20	85	°C
		AK4348VF	Ta	-40	85	°C
Storage Temperature			Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies (Note 1)	Analog	AVDD	2.7	3.3	3.6	V
	Digital	DVDD	2.7	3.3	3.6	V

Note 3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3.3V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; R_L ≥5kΩ; unless otherwise specified)

Parameter			Min	Typ	Max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 4)						
THD+N	Fs=44.1kHz	0dBFS		-90	-80	dB
	BW=20kHz	-60dBFS		-40	-	dB
	fs=96kHz	0dBFS		-86	-	dB
	BW=40kHz	-60dBFS		-37	-	dB
	fs=192kHz	0dBFS		-86	-	dB
	BW=40kHz	-60dBFS		-37	-	dB
Dynamic Range (-60dBFS with A-weighted) (Note 5)			96	104		dB
S/N (A-weighted) (Note 6)			96	104		dB
Interchannel Isolation (1kHz)			80	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage (Note 7)			2.09	2.24	2.39	Vpp
Load Resistance (Note 8)			5			kΩ
Load Capacitance					25	pF
Power Supplies						
Power Supply Current (AVDD+DVDD)						
Normal Operation (RSTB pin = "H", fs≤96kHz)				45	72	mA
Normal Operation (RSTB pin = "H", fs=192kHz)				52	78	mA
Reset Mode (RSTB pin = "L") (Note 9)				33	133	μA

Note 4. Measured by Audio Precision System Two. Refer to the evaluation board manual.
Note 5. 100dB when using 16bit data.
Note 6. S/N does not depend on input data resolution.
Note 7. Full scale voltage (0dB). Output voltage scales with the voltage of AVDD pin. AOUT (typ. @0dB) = 2.24Vpp×AVDD/3.3
Note 8. For AC-load.
Note 9. P/S pin is tied to DVDD and the other all digital input pins including clock pins (MCLK, BICK, LRCK) are tied to DVSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.7 ~ 3.6V; fs = 44.1kHz; DEM = OFF; SLOW = "0")

Parameter			Symbol	Min	Typ	Max	Units
Digital filter							
Passband	±0.05dB (Note 10)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband	(Note 10)		SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay	(Note 11)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	Fs=44.1kHz	FR	-	+ 0.06/-0.10	-	dB
	40.0kHz	Fs=96kHz	FR	-	+ 0.06/-0.13	-	dB
	80.0kHz	Fs=192kHz	FR	-	+ 0.06/-0.51	-	dB

Note 10. The passband and stopband frequencies scale with fs(system sampling rate). For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 11. Calculated delay time caused by the digital filter. This time is measured from when the serial data of both channels is in the input register to the output of the analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.7~3.6V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter			Symbol	Min	Typ	Max	Units
Digital Filter							
Passband	±0.04dB (Note 12)		PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband	(Note 12)		SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay	(Note 11)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0.1/-4.3	-	dB
	40.0kHz	fs=96kHz	FR	-	+0.1/-3.3	-	dB
	80.0kHz	fs=192kHz	FR	-	+0.1/-3.7	-	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.7 ~ 3.6V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL		-	30%DVDD	V
High-Level Output Voltage	(Iout = -80μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current	(Note 13)	Iin	-	-	± 10	μA

Note 13. P/S pin has an internal pull-up device and TDM0 pin has an internal pull-down device, nominally 100kΩ.

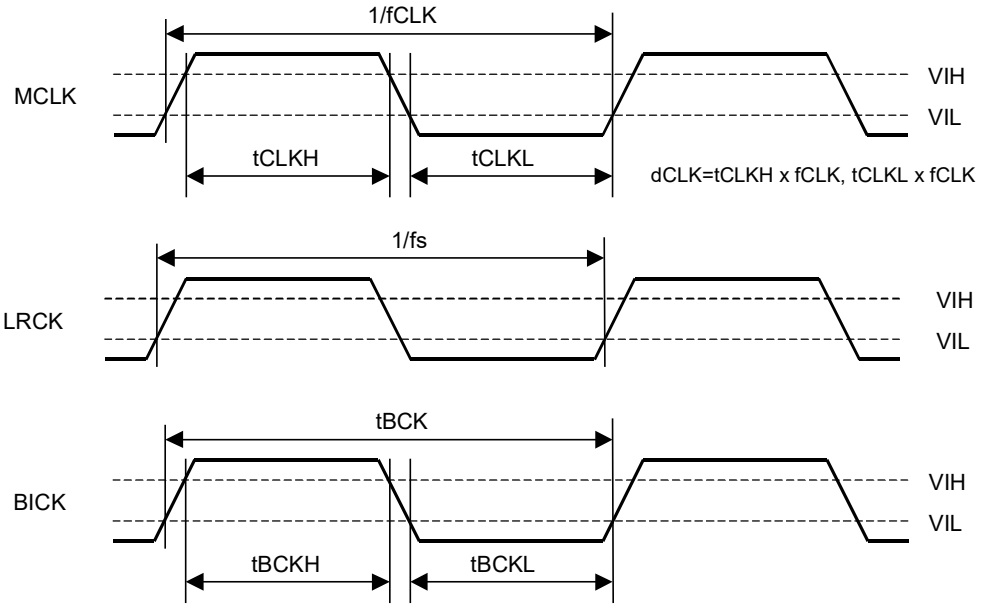
SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 2.7 ~ 3.6V; C_L = 20pF)

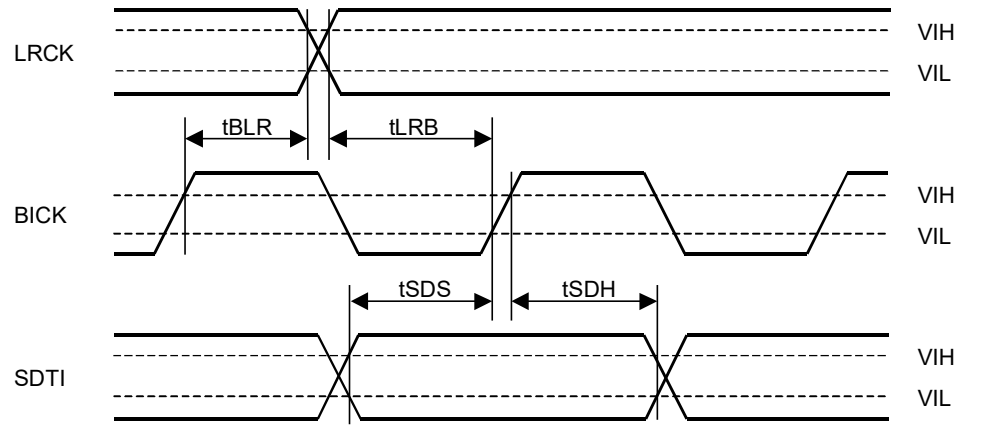
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Mode (TDM0= "0", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "1", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
High time	tLRH	1/256fs			ns
Low time	tLRL	1/256fs			ns
TDM128 mode (TDM0= "1", TDM1= "1")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
High time	tLRH	1/128fs			ns
Low time	tLRL	1/128fs			ns
Audio Interface Timing					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 14)	tLRB	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 15)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
RSTB Pulse Width (Note 16)	tRST	150			ns

Note 14. BICK rising edge must not occur at the same time as LRCK edge.
Note 15. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 16. The AK4348 can be reset by bringing RSTB pin = "L".
Note 17. I^2C is a registered trademark of Philips Semiconductors.

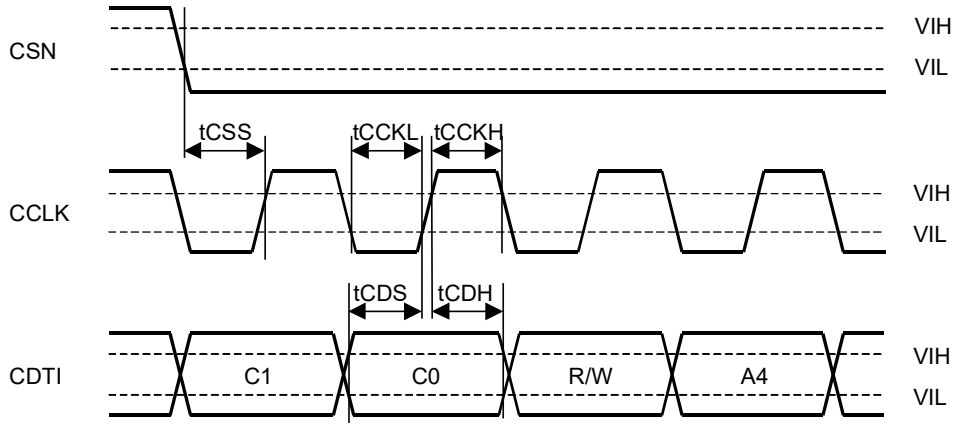
■ Timing Diagram



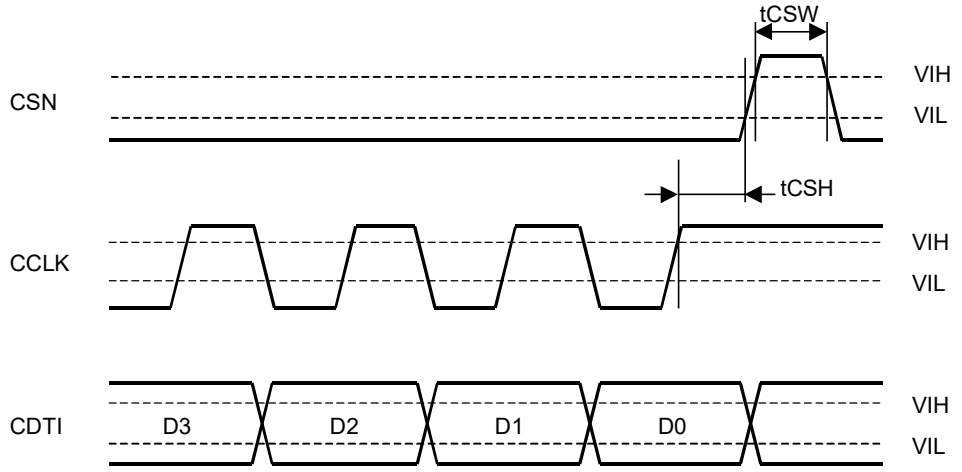
Clock Timing



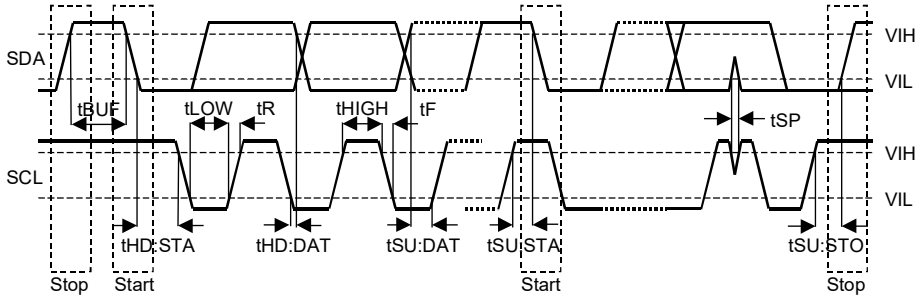
Audio Serial Interface Timing



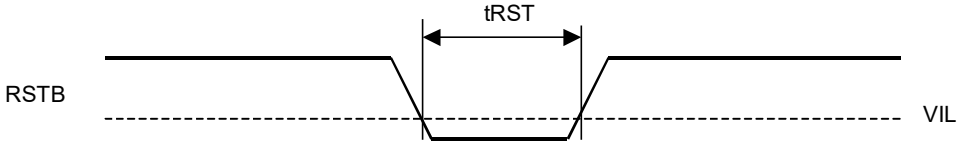
WRITE Command Input Timing



WRITE Data Input Timing



I^2C Bus mode Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4348 are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit = "0": Register 00H), the sampling speed is set by DFS0-1 bits (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2~Table 4) In Auto Setting Mode (ACKS bit = "1": Default), the MCLK frequency is detected automatically (Table 5), and the internal master clock is set to the appropriate frequency (Table 6) and it is not necessary to set DFS0-1.

In parallel control mode, the sampling speed can be set by only the ACKS pin. When ACKS pin = "L", the AK4348 operates by normal speed mode. When ACKS pin = "H", auto setting mode is enabled. The parallel control mode does not support 128fs and 192fs of double speed mode.

All external clocks (MCLK, BICK and LRCK) should be present whenever the AK4348 is in normal operation mode (RSTB pin = "H"). If these clocks are not provided, the AK4348 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. The AK4348 should be reset by setting RSTB pin = "L" after these clocks are provided. If the external clocks are not present, the AK4348 should be in the power-down mode (RSTB pin = "L"). After exiting reset(RSTB = "↑") at power-up, the AK4348 is in the power-down mode until MCLK is input.

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	Default
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK					BICK
fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	36.8640MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	N/A	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	N/A	3.0720MHz

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	106896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	106896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

In parallel control mode, the DIF0-1 and TDM0 pins can select eight serial data modes (Table 7). The register value of DIF0-1 and TDM0bits are ignored. In serial control mode, the DIF0-2 and TDM0-1 bits shown in Table 8 can select 11 serial data modes. The default format is Mode 2 (24-bit MSB justified format in normal mode). The setting of DIF1 pin is ignored. In all modes the audio data is MSB-first, 2's complement format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20-bit MSB justified formats by zeroing the unused LSB's.

In parallel control mode, when the TDM0 pin = "H", the audio interface format is TDM256 mode (Table 7). The audio data of all DACs (eight channels) is input to the SDTI1 pin. The input data to SDTI2-4 pins is ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be at least 1/256fs. The audio data is MSB-first, 2's complement format. The input data to SDTI1 pin is latched on the rising edge of BICK.

In serial control mode, when the TDM0 bit = "1" and the TDM1 bit = "0", the audio interface format is TDM256 mode (Table 8), and the audio data of all DACs (eight channels) is input to the SDTI1 pin. The input data to SDTI2-4 pins is ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be at least 1/256fs. The audio data is MSB-first, 2's complement format. The input data to SDTI1 pin is latched on the rising edge of BICK. In TDM128 mode (TDM0 bit = "1" and TDM1 bit = "1", Table 8), the audio data of DACs (four channels; L1, R1, L2, R2) is input to the SDTI1 pin. The other four data (L3, R3, L4, R4) is input to the SDTI2 pin. The input data to SDTI3-4 pins is ignored. BICK should be fixed to 128fs. The audio data is MSB-first, 2's complement format. The input data to SDTI1-2 pins is latched on the rising edge of BICK.

Mode		TDM0	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure
Normal	0	L	L	L	16-bit LSB Justified	H/L	≥32fs	Figure 1
	1	L	L	H	20-bit LSB Justified	H/L	≥40fs	Figure 2
	2	L	H	L	24-bit MSB Justified	H/L	≥48fs	Figure 3
	3	L	H	H	24-bit I^2S Compatible	L/H	≥48fs	Figure 4
TDM256		H	L	L	N/A			
		H	L	H	N/A			
	5	H	H	L	24-bit MSB Justified	↑	256fs	Figure 5
	6	H	H	H	24-bit I^2S Compatible	↓	256fs	Figure 6

Table 7. Audio Data Formats (Parallel control mode)

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure
Normal	0	0	0	0	0	0	16-bit LSB Justified	H/L	≥32fs	Figure 1
	1	0	0	0	0	1	20-bit LSB Justified	H/L	≥40fs	Figure 2
	2	0	0	0	1	0	24-bit MSB Justified	H/L	≥48fs	Figure 3
	3	0	0	0	1	1	24-bit I^2S Compatible	L/H	≥48fs	Figure 4
	4	0	0	1	0	0	24-bit LSB Justified	H/L	≥48fs	Figure 2
TDM256		0	1	0	0	0	N/A			
		0	1	0	0	1	N/A			
	5	0	1	0	1	0	24-bit MSB Justified	↑	256fs	Figure 5
	6	0	1	0	1	1	24-bit I^2S Compatible	↓	256fs	Figure 6
	7	0	1	1	0	0	24-bit LSB Justified	↑	256fs	Figure 7
TDM128		1	1	0	0	0	N/A			
		1	1	0	0	1	N/A			
	8	1	1	0	1	0	24-bit MSB Justified	↑	128fs	Figure 8
	9	1	1	0	1	1	24-bit I^2S Compatible	↓	128fs	Figure 9
	10	1	1	1	0	0	24-bit LSB Justified	↑	128fs	Figure 10

Table 8. Audio Data Formats (Serial control mode, Default: Mode 2)

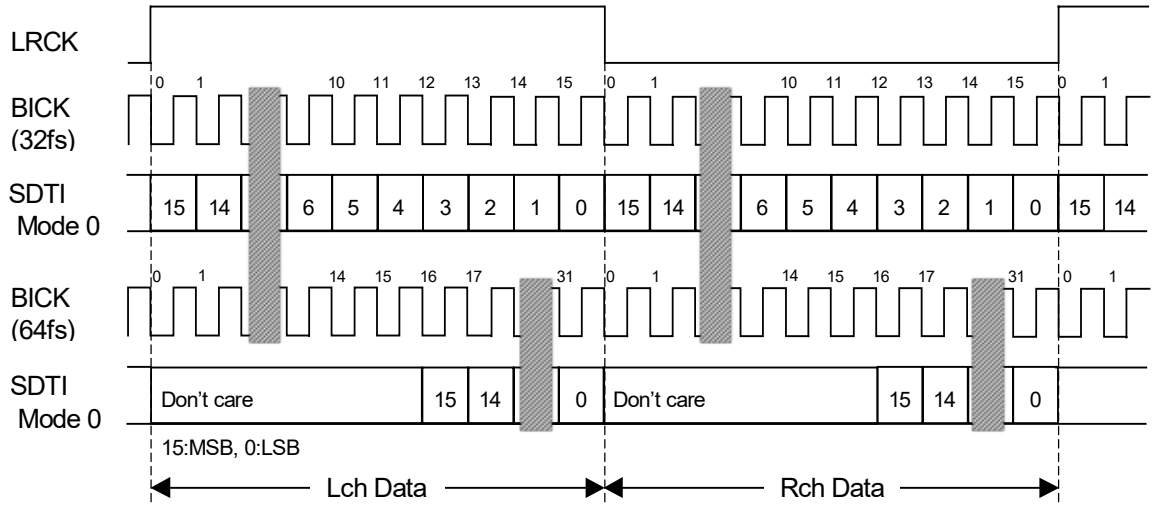


Figure 1. Mode 0 Timing

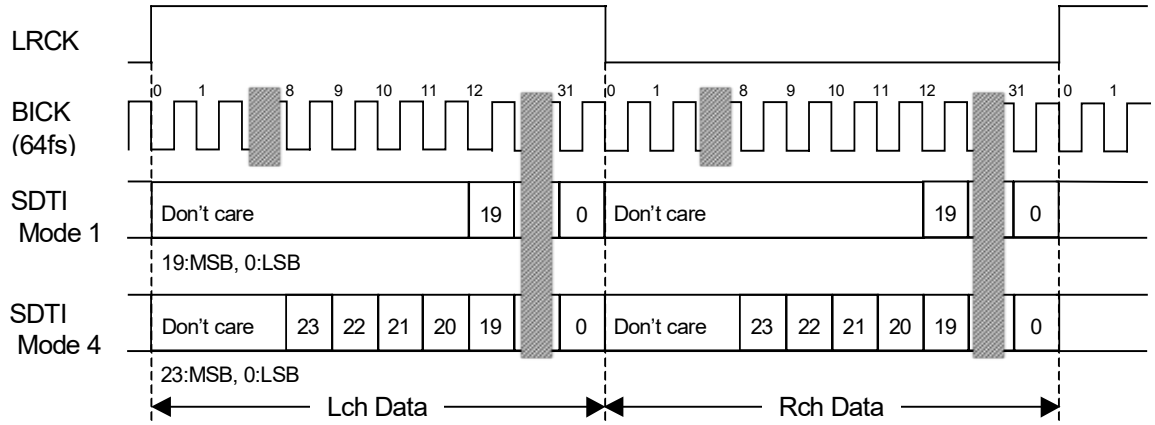


Figure 2. Mode 1,4 Timing

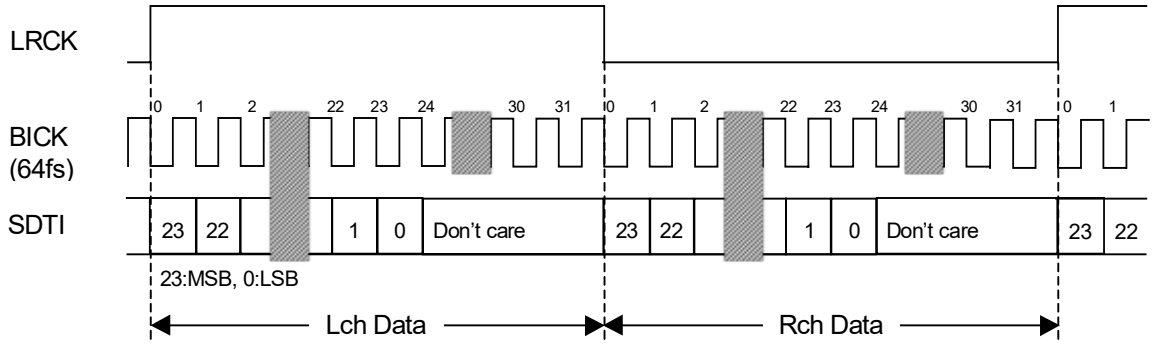


Figure 3. Mode 2 Timing

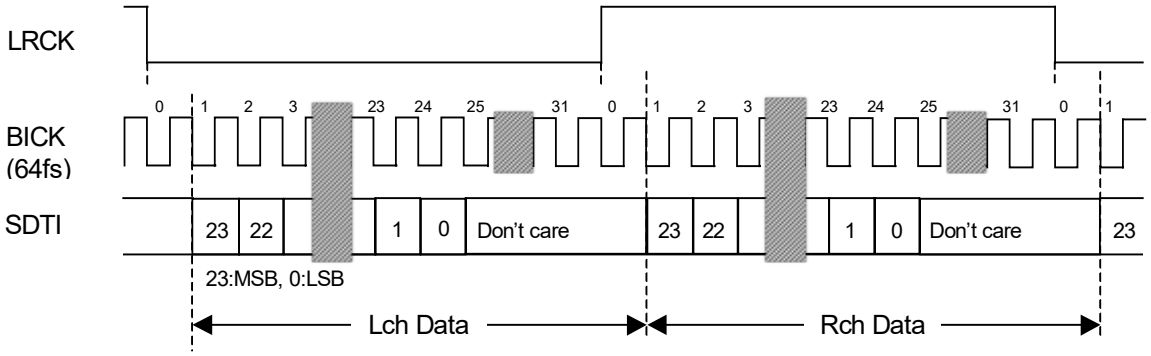


Figure 4. Mode 3 Timing

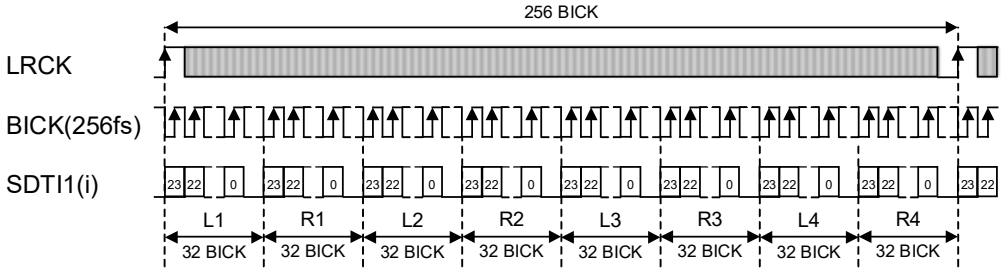


Figure 5. Mode 5 Timing

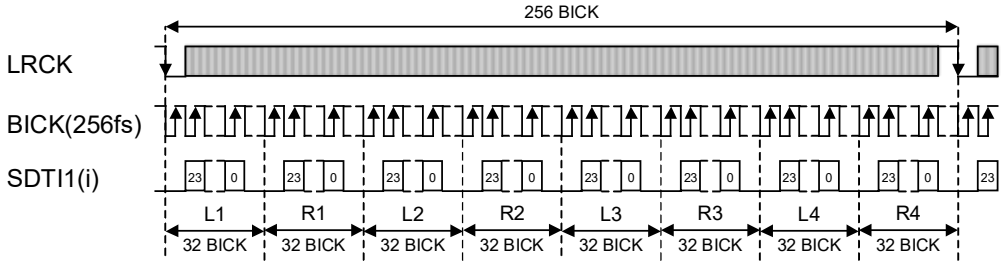


Figure 6. Mode 6 Timing

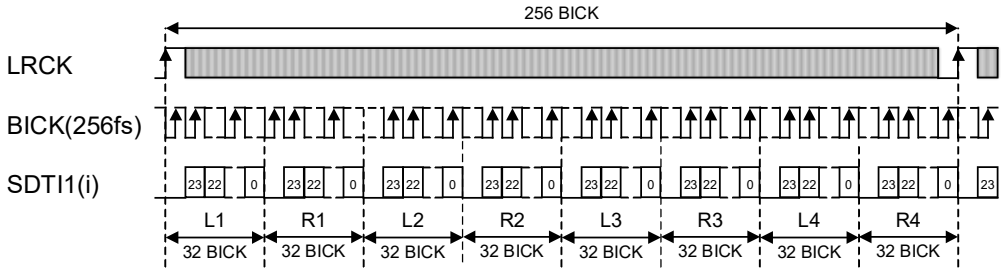


Figure 7. Mode 7 Timing

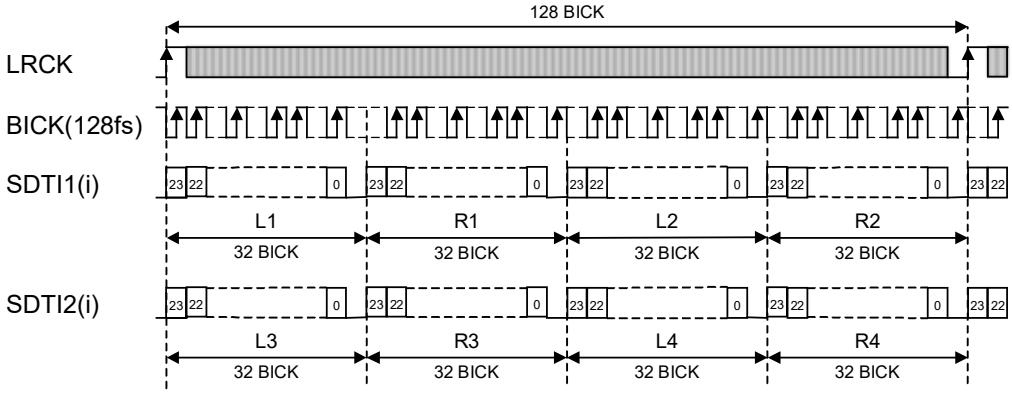


Figure 8. Mode 8 Timing

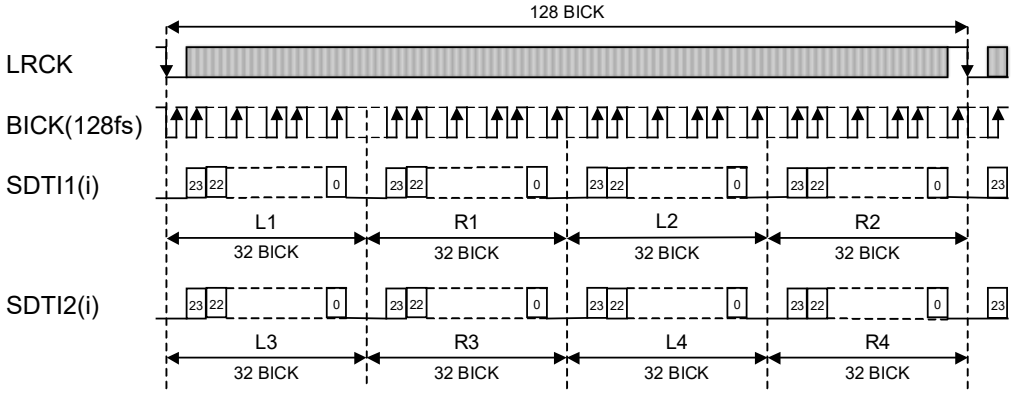


Figure 9. Mode 9 Timing

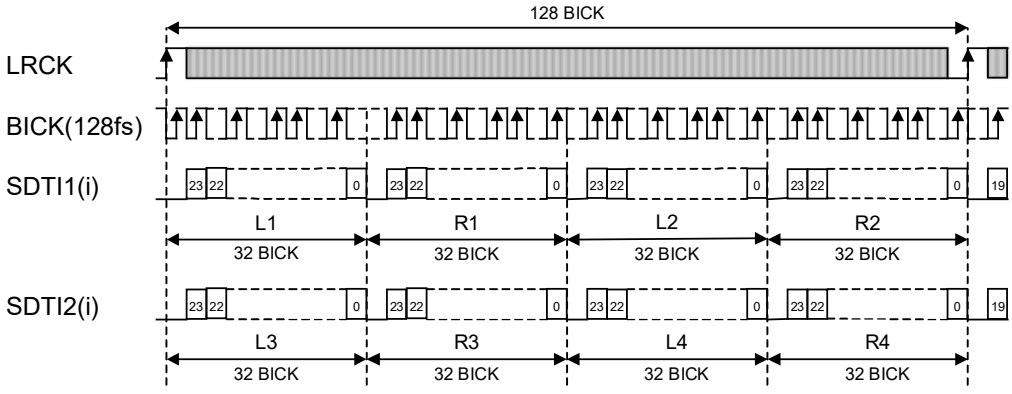


Figure 10. Mode 10 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs). The digital de-emphasis filter is always off when the AK4348 is operated in double or quad speed modes. In serial control mode, the DEM0-1 bits are valid for the DAC enabled by the DEMA-D bits. In parallel control mode, the DEM0-1 pins are valid.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 9. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4348 includes channel independent digital volume controls (ATT) with 256 linear steps, including MUTE. The volume controls are in front of the DAC and can attenuate the input data from 0dB to –48dB, and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 10. The attenuation level is calculated by ATT = 20 $\log_{10}$ (ATT_DATA / 255) [dB] and MUTE at ATT_DATA = "0".

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 10. ATT Transition time

■ Zero Detection

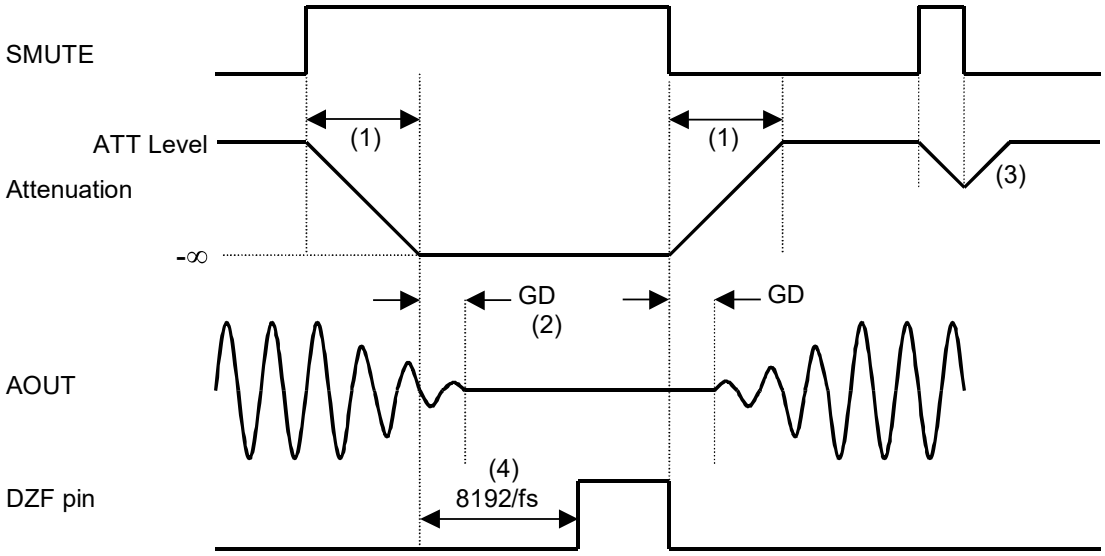
When the input data at all channels are continuously zeros for 8192 LRCK cycles, the AK4348 has a Zero Detect function detailed in Table 11. The DZF pin immediately goes to "L" if the input data for each channel is not zero after the DZF pin is "H". If the RSTN bit is "0", the DZF pin goes to "H". The DZF pin goes to "L" after 4 to 5LRCK cycles if the input data of each channel is not zero after the RSTN bit returns to "1". The Zero Detect function can be disabled by the DZFE bit. In this case, both DZF pins are always "L". When one of the PW1-4 bits is set to "0", the input data of the DAC for which the PW bit is set to "0" should be zero in order to enable zero detection of the other channels. When all PW1-4 bits are set to "0", both DZF pins are fixed to "L". The DZFB bit can invert the polarity of the DZF pin. In parallel control mode, the zero detect function is disabled and the DZF1 pin is fixed to "L".

DZF Pin	Operations
DZF1	AND'ed output of zero detection flag of each channel set to "1" in 0CH register
DZF2	AND'ed output of zero detection flag of each channel set to "1" in 0DH register

Table 11. DZF pins Operation

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by -∞ during the ATT_DATA×ATT transition time (Table 10) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during the ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective when changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 10). For example, in Normal Speed Mode, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at each channel is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin immediately goes to "L" if input data are not zero after going DZF "H". In parallel control mode, the DZF pin is fixed to "L" regardless of the state of SMUTE pin.

Figure 11. Soft Mute and Zero Detection (DZFB bit = "0")

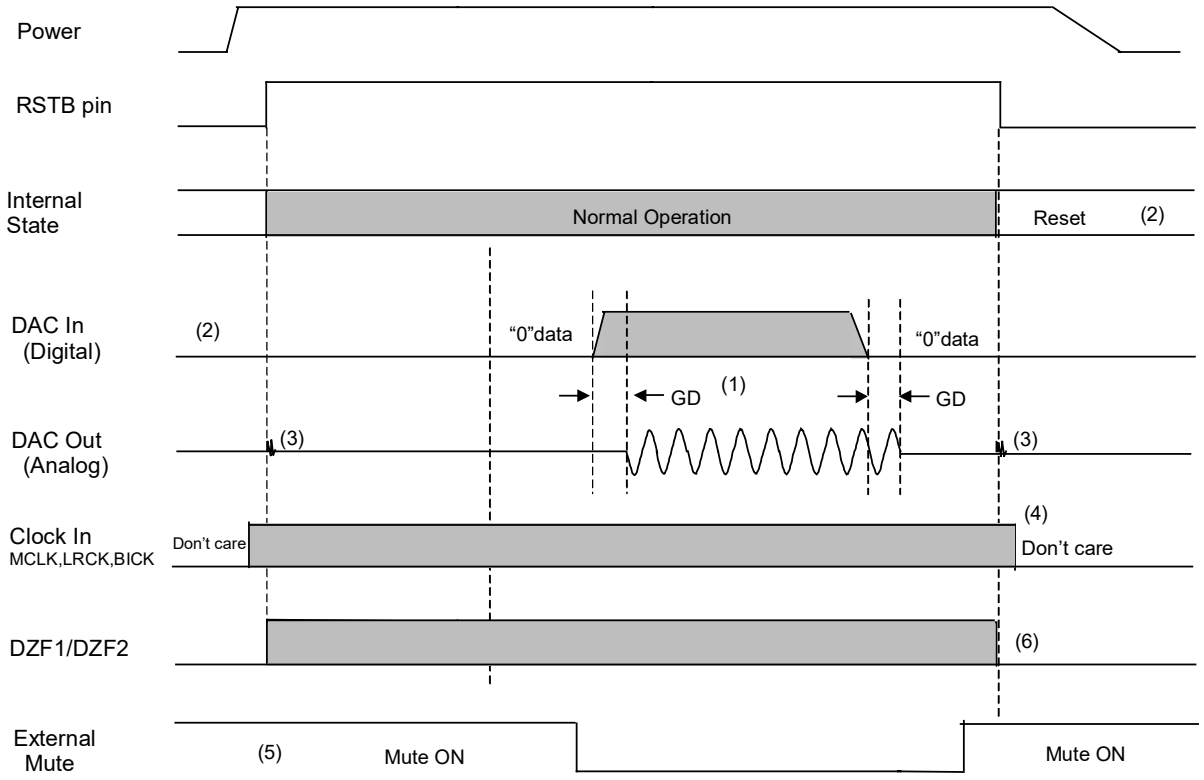
■ System Reset

The AK4348 should be reset once by bringing RSTB pin = "L" upon power-up. The AK4348 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4348 is in the power-down mode until MCLK and LRCK are input.

■ Power ON/OFF timing

All DACs are placed in the power-down mode by bringing RSTB pin "L" and the registers are initialized. The analog outputs go to VCOM. Since some click noise occurs at the edge of the RSTB signal, the analog output should be muted externally if the click noise influences system application.

Each DAC can be powered down by setting each power-down bit (PW1-4 bits) to "0". In this case, the registers are not initialized and the corresponding analog outputs go to VCOM. Since some click noise occurs at the edge of the RSTB signal, the analog output should be muted externally if the click noise influences system application.



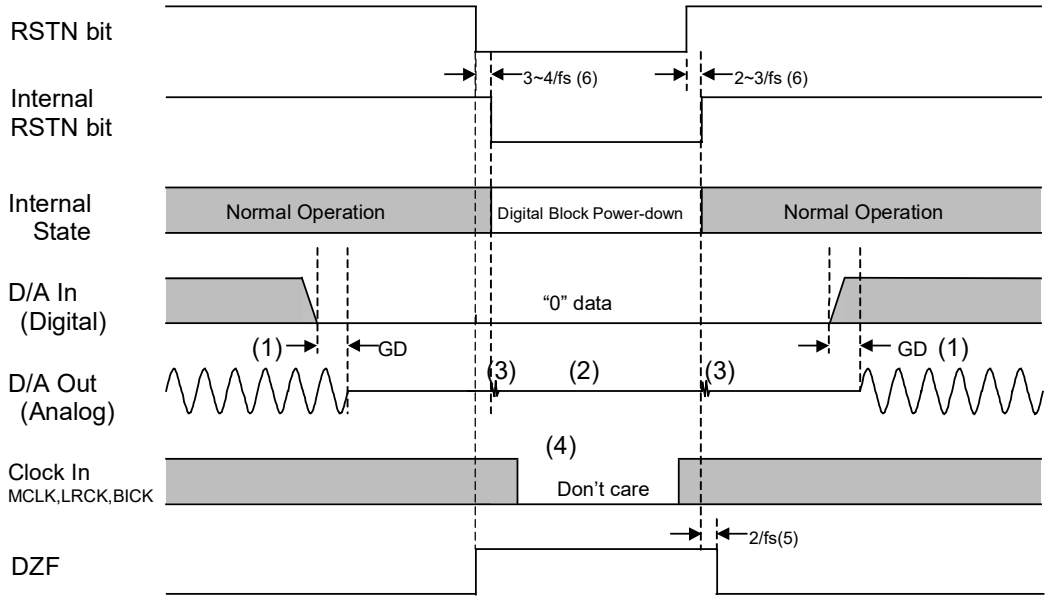
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are VCOM at power-down mode.
(3) Click noise occurs at the edge of RSTB signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (RSTB pin = "L").
(5) Mute the analog output externally if the click noise (3) influences the system application.
The timing example is shown in this figure.
(6) DZF pins are "L" in the power-down mode (RSTB pin = "L"). (DZFB bit = "0")

Figure 12. Power-down/up Sequence Example

■ Reset Function (RSTN bit)

When the RSTN bit = "0", the internal circuit of the DAC is powered down but the registers are not initialized. The analog outputs go to VCOM voltage and the DZF pins go to "H" when the DZFB bit = "0". Figure 13 shows the example of reset by the RSTN bit. When the RSTN bit = "0", click noise is decreased at no clock state.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Small click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN bit = "0").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".

Figure 13. Reset Sequence Example (DZFB bit = "0")

■ Register Control Interface

The AK4348 controls its functions via registers. Two types of control mode can be used to write to the internal registers. In I^2C-bus mode, the chip address is determined by the state of the CAD0-1 pins. In 3-wire mode, the chip address can be selected by the state of the CAD1 pin. RSTB pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit resets the internal timing circuit, but the registers are not initialized.

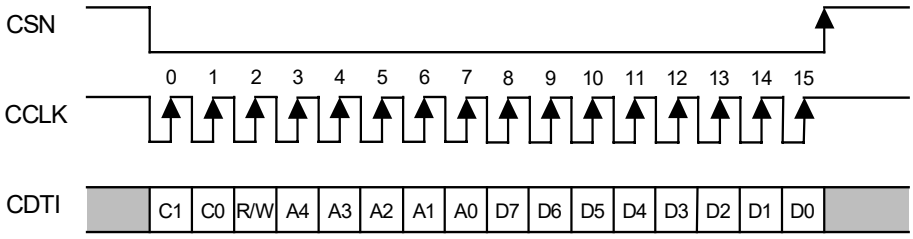
* The AK4348 does not support the read command.
* When the AK4348 is in the power down mode (RSTB bit = "L") or the MCLK is not provided, writing to control registers is prohibited.
* When the state of P/S pin is changed, the AK4348 should be reset by RSTB bit = "L".
* In serial control mode, the setting of parallel pins is invalid.

Function	Parallel control mode	Serial control mode
Double sampling mode at 128/192fs	-	O
De-emphasis	O	O
SMUTE	O	O
Zero Detection	-	O
24bit LSB justified format	-	O
TDM256 mode	O	O
TDM128 mode	-	O

Table 12. Function Table (O: Supported, -: Not supported)

(1) 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written to via the 3-wire μP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Chip Address (2-bits, C1/0; C1=CAD1 and C0 is fixed to "1"), Read/Write (1-bit; fixed to "1", Write only), Register Address (MSB first, 5-bits) and Control Data (MSB first, 8-bits). The AK4348 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by the rising edge of CSN. The clock speed of CCLK is 5MHz (max).



C1-C0: Chip Address (C1=CAD1, C0="1")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 14. Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4348 supports fast-mode I²C-bus system (max: 400kHz).

Figure 15 shows the data transfer sequence at the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 19). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) (Figure 16). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (chip address bits). The bits identify the specific device on the bus. The hard-wired input pins (CAD1 and CAD0 pins) set them. If the slave address match that of the AK4348 and R/W bit is "0", the AK4348 generates the acknowledge and the write operation is executed. If R/W bit is "1", the AK4348 generates the not acknowledge since the AK4348 can be only a slave-receiver. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 20).

The second byte consists of the address for control registers of the AK4348. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 17). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 18). The AK4348 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 19).

The AK4348 is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4348 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the addresses exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 21) except for the START and the STOP condition.

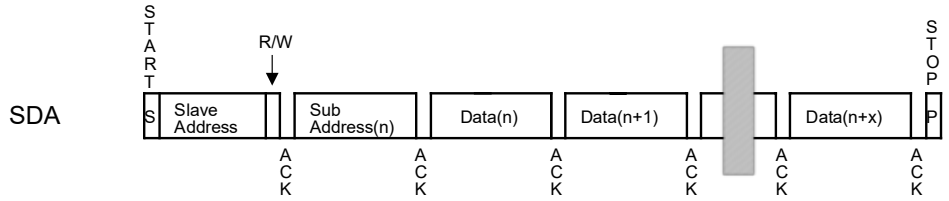


Figure 15. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)

Figure 16. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 17. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 18. Byte structure after the second byte

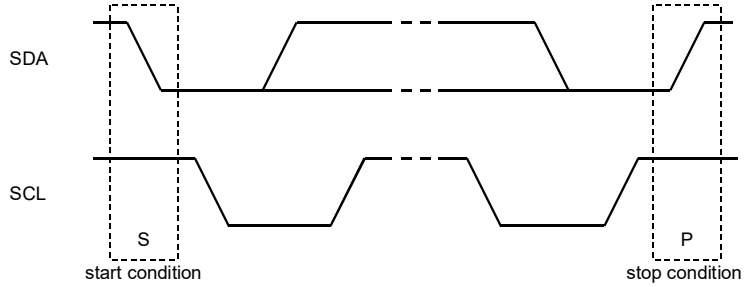


Figure 19. START and STOP conditions

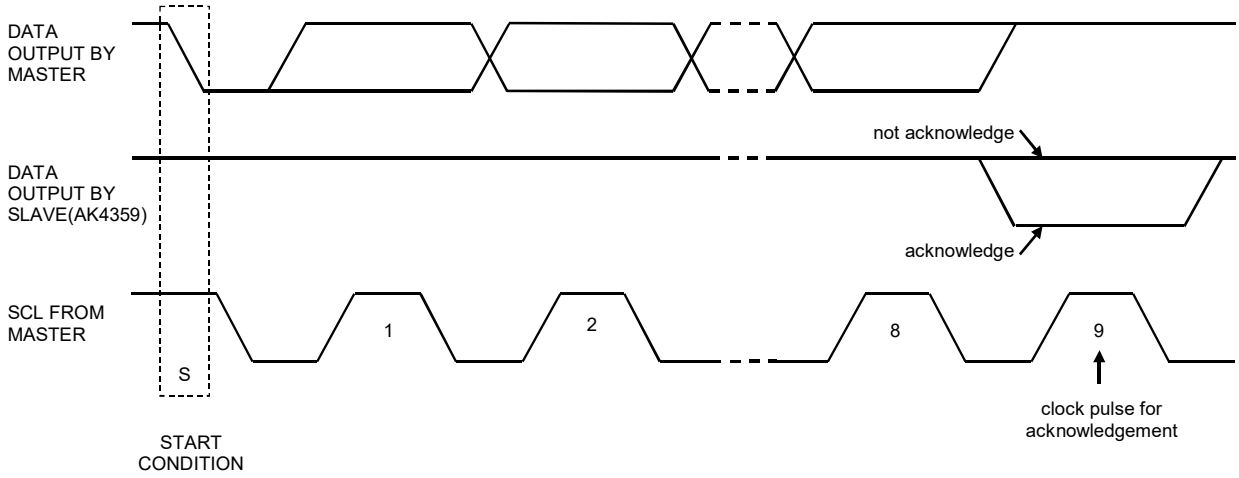


Figure 20. Acknowledge on the I^2C-bus

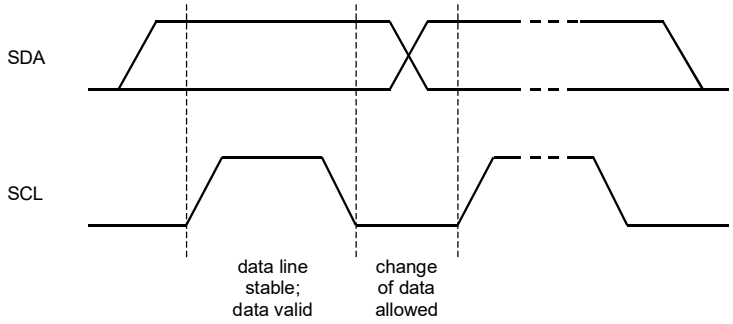


Figure 21. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	TDM1	TDM0	DIF2	DIF1	DIF0	PW1	RSTN
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	PW4	PW3	PW2	0	0	DZFB	PW1	0
03H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	LOUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	ROUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0BH	Invert Output Signal	INVL1	INVR1	INVL2	INVR2	INVL3	INVR3	INVL4	INVR4
0CH	DZF1 Control	L1	R1	L2	R2	L3	R3	L4	R4
0DH	DZF2 Control	L1	R1	L2	R2	L3	R3	L4	R4
0EH	DEM Control	0	0	0	0	DEMA	DEMB	DEMC	DEMD

Note: For addresses from 0FH to 1FH, data must not be written.
When RSTB pin goes to "L", the registers are initialized to their default values.
When RSTN bit goes to "0", the only internal timing is reset, and the registers are not initialized to their default values. All data can be written to the registers even if PW1-4 bits or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	TDM1	TDM0	DIF2	DIF1	DIF0	PW1	RSTN
Default		1	0	0	0	1	0	1	1

RSTN: Internal timing reset
0: Reset. All DZF pins go to "H" and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the click noise can be reduced by RSTN bit.

PW1: Power-down control (0: Power-down, 1: Power-up)
PW1: Power down control of DAC1
This bit is duplicated into D1 of 02H.

DIF2-0: Audio data interface modes (See Table 7, Table 8)
Initial: "010", Mode 2

TDM0-1: TDM Mode Select

Mode	TDM1	TDM0	BICK	SDTI	Sampling Speed
Normal	0	0	32fs~	1-4	Normal, Double, Quad Speed
TDM256	0	1	256fs fixed	1	Normal Speed
TDM128	1	1	128fs fixed	1-2	Normal, Double Speed

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically when the ACKS bit = "1". In this case, the setting of DFS1-0 bits is ignored. When this bit is "0", DFS1-0 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
Default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (See Table 9)
Initial: "01", OFF

DFS1-0: Sampling speed control (See Table 1)
00: Normal speed
01: Double speed
10: Quad speed
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

Adr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Speed & Power Down Control	PW4	PW3	PW2	0	0	DZFB	PW1	0
Default		1	1	1	0	0	0	1	0

PW1: Power-down control (0: Power-down, 1: Power-up)
PW1: Power down control of DAC1
This bit is duplicated into D1 of 00H.

DZFB: Inverting Enable of DZF
0: DZF goes "H" at Zero Detection
1: DZF goes "L" at Zero Detection

PW4-2: Power-down control (0: Power-down, 1: Power-up)
PW2: Power down control of DAC2
PW3: Power down control of DAC3
PW4: Power down control of DAC4
All sections are powered-down by PW1=PW2=PW3=PW4=0.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	LOUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	ROUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT = 20 $\log_{10}$ (ATT_DATA / 255) [dB]

00H: Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Invert Output Signal	INVL1	INVR1	INVL2	INVR2	INVL3	INVR3	INVL4	INVR4
Default		0	0	0	0	0	0	0	0

INVL1-4, INVR1-4: Inverting Output Polarity

0: Normal Output

1: Inverted Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	DZF1 Control	L1	R1	L2	R2	L3	R3	L4	R4
0DH	DZF2 Control	L1	R1	L2	R2	L3	R3	L4	R4
Default		0	0	0	0	0	0	0	0

L1-4, R1-4: Zero Detect Flag Enable for DZF1/2 pins

0: Disable

1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	DEM Control	0	0	0	0	DEMA	DEMB	DEMC	DEMD
Default		0	0	0	0	0	0	0	0

DEMA-D: De-emphasis Enable of DAC1/2/3/4

0: Disable

1: Enable

SYSTEM DESIGN

Figure 22 and 23 shows the system connection diagram. An evaluation board (AKD4348) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

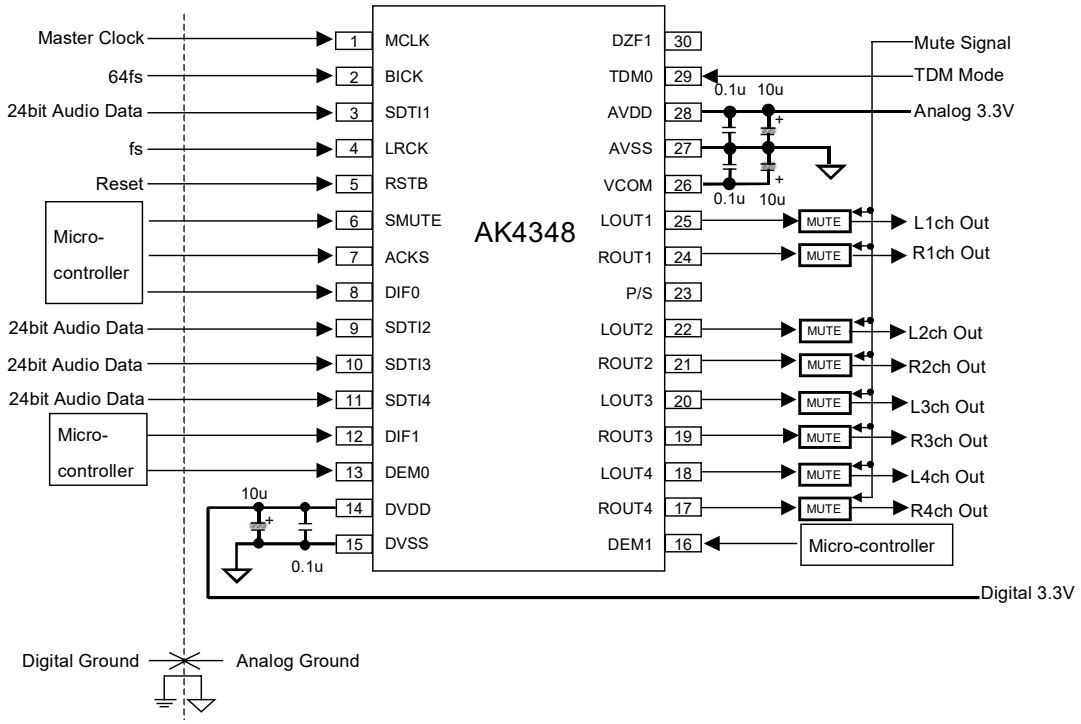


Figure 22. Typical Connection Diagram (Parallel Control Mode)

Notes:

- LRCK = fs, BICK = 64fs.
- When LOUT/ROUT drives some capacitive load, some resistor should be added in series between LOUT/ROUT and capacitive load.
- All input pins except P/S and TDM0 pins should not be left floating.

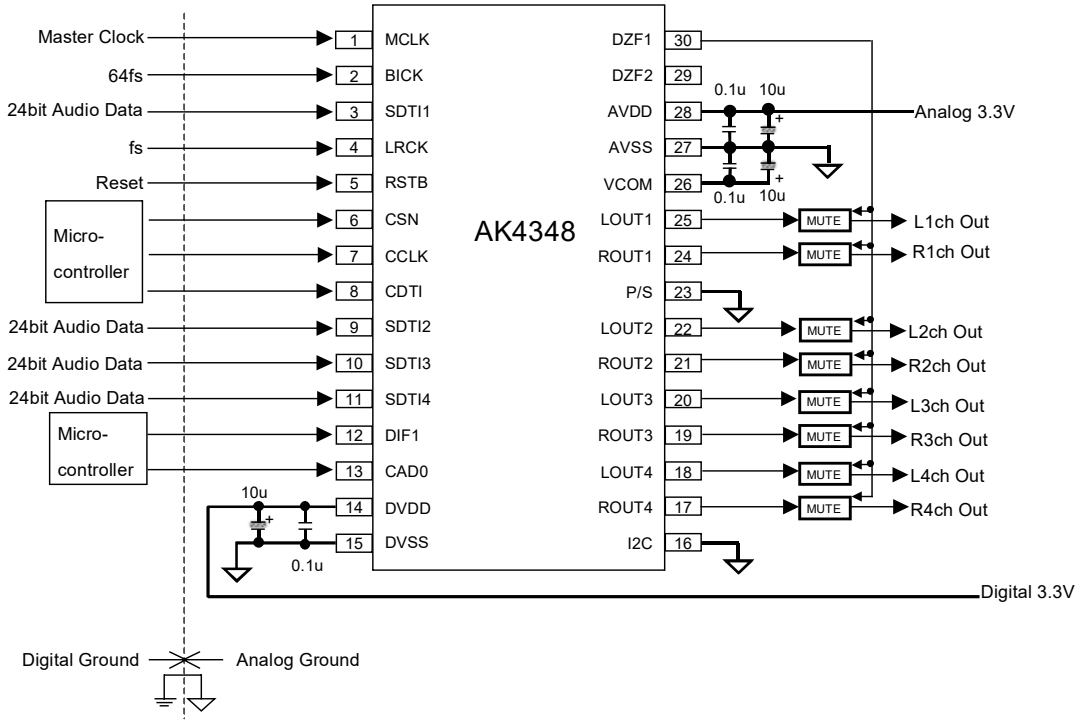


Figure 23. Typical Connection Diagram (3-wire Serial Control Mode)

Notes:

- LRCK = fs, BICK = 64fs.
- When LOUT/ROUT drives some capacitive load, some resistor should be added in series between LOUT/ROUT and capacitive load.
- All input pins except P/S pin should not be left floating.
- DZF1 pin goes to “H” when zero data input is detected or SMUTE bit is set to “1”.

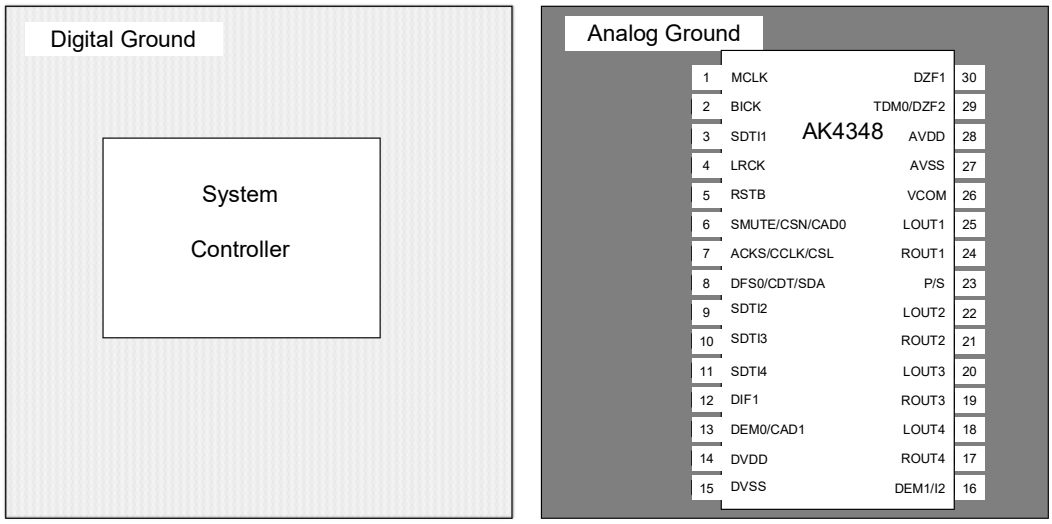


Figure 24. Ground Layout

AVSS and DVSS must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

AVDD and DVDD are usually supplied from the analog supply in the system and it should be separated from system digital supply. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4348 must be connected to the analog ground plane**. System analog ground and digital ground should be connected together close to where the supplies are brought onto the printed circuit board. A decoupling capacitor, typically a 0.1μF ceramic capacitor for high frequency bypass, should be placed as near to AVDD and DVDD as possible.

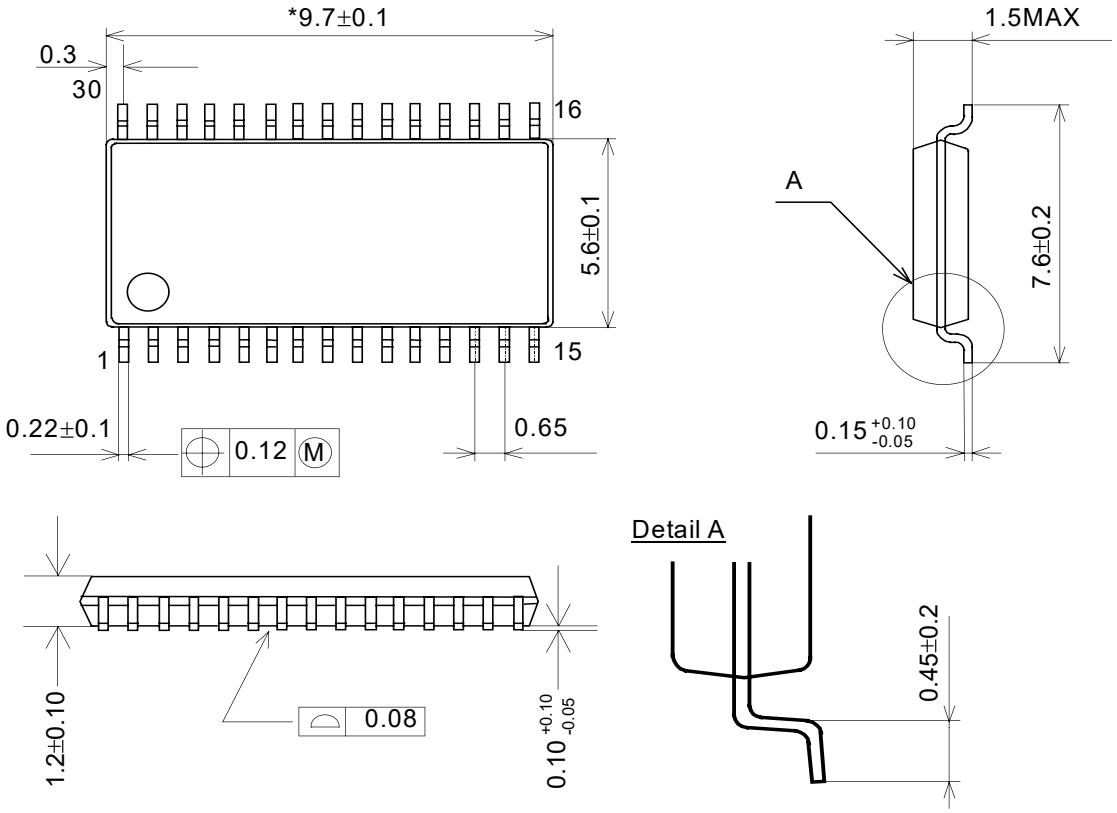
2. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage. The output signal range is typically 2.24Vpp (when AVDD=3.3V). The phase of the analog outputs can be inverted channel independently by the INVL/INVR bits. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24-bit) and a negative full scale for 800000H (@24-bit). The ideal output is VCOM voltage for 000000H (@24-bit).

DC offsets on the analog outputs are eliminated by AC coupling since the analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

30pin VSOP (Unit: mm)

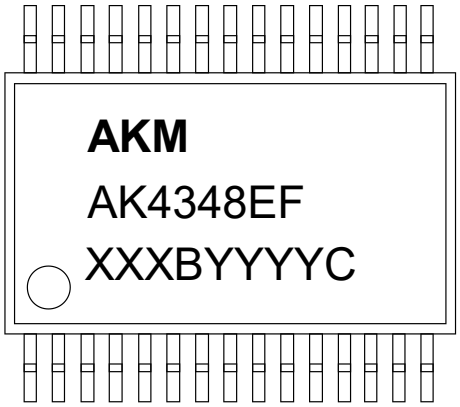


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

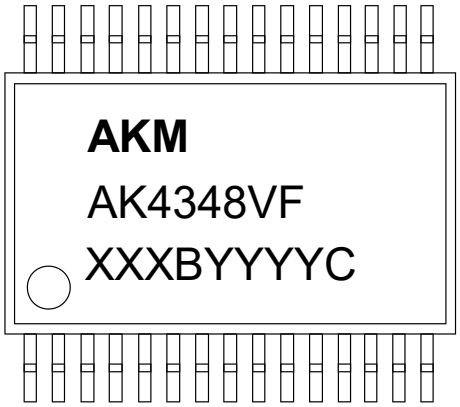
MARKING (AK4348EF)



XXXBYYYYC Date code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

MARKING (AK4348VF)



XXXBYYYYC Date code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/07/28	00	First edition		

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