ATP Electronics, Inc.
2590 North First Street, San Jose, CA 95131, U.S.A.
Tel: 408-732-5000
Fax: 408-732-5055
http://www.atpinc.com

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ATP AL48P72L8BNK0M

16GB DDR3-1600 REGISTERED ECC DIMM

DESCRIPTION

The ATP AL48P72L8BNK0M is a high performance 16GB DDR3-1600 Registered ECC SDRAM memory module. It is organized as 2048M x 72 in a 240-pin Dual-In-Line Memory Module (DIMM) package. The module utilizes eighteen 1024Mx8 DDR3 SDRAMs in FBGA package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 16GB (2048M x 72)
- DIMM Rank: 2 Ranks
- Cycle Time: 1.25ns (800MHz)
- CAS Latency: 11
- Power supply: 1.35V(1.28V~1.45V) Backward compatible to 1.5V ±0.075V
- Internal self calibration through ZQ
- Burst lengths: 8
- On-board I^2C temperature sensor with integrated (SPD) EEPROM
- Auto & Self refresh
- Asynchronous Reset
- Minimum Thickness of Golden Finger: 30 Micro-inch
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Support address and command signals parity function
- Dynamic On Die Termination
- Fly-by topology
- PCB Height: 0.74 inches(Very Low Profile)
- RoHS compliant

Part No.	Max Freq	Interface
AL48P72L8BNK0M	800MHz (1.25ns@CL=11) x2	SSTL_15

PIN DESCRIPTION

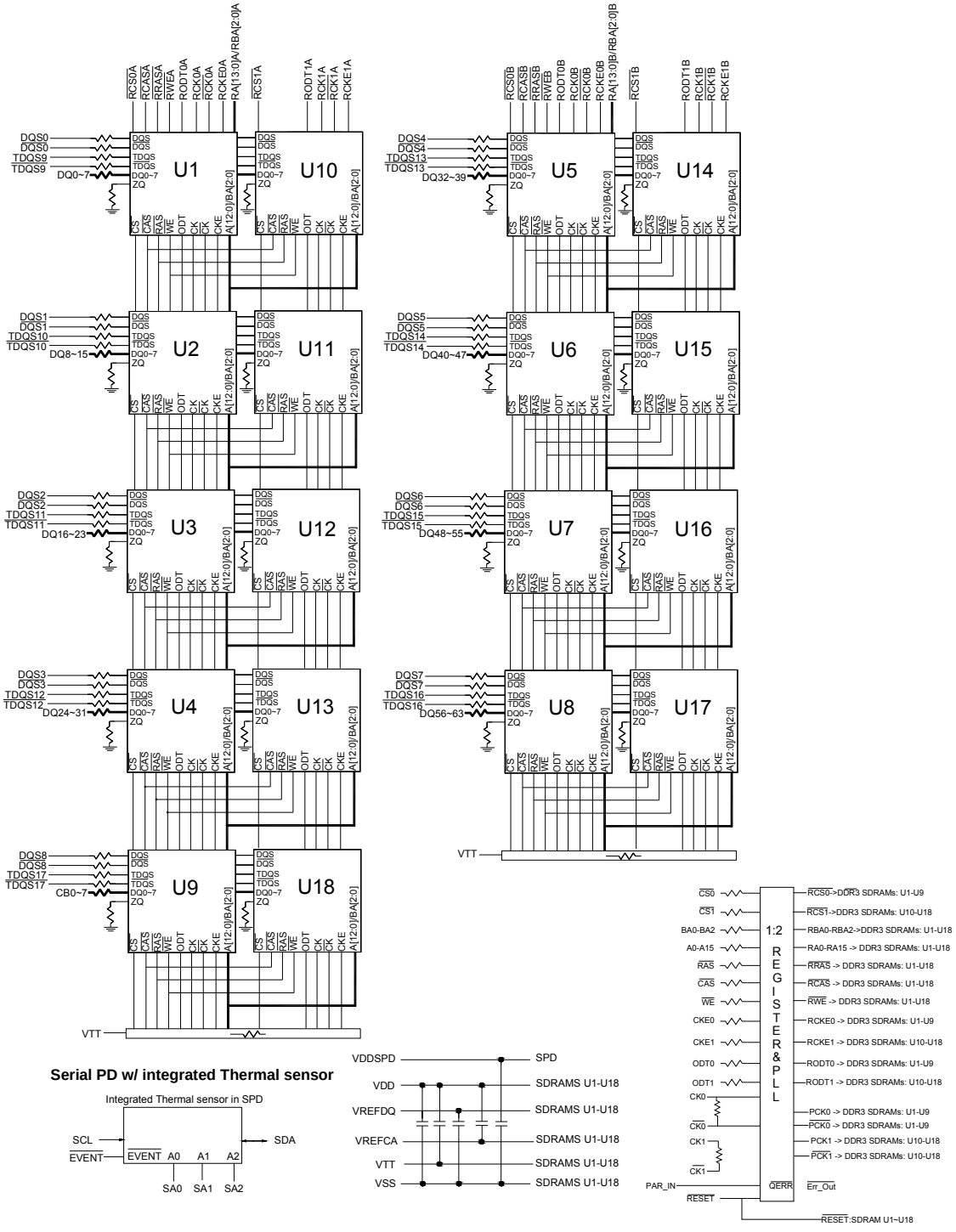
Pin Name	Description	Pin Name	Description
A0~A9, A11~A15	Address Inputs	ODT0, ODT1	On die termination
A10/AP	Address Input/Auto precharge	Par_In	Parity bit for the Address and Control bus
BA0~BA2	SDRAM Bank Address	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{RESET}$	Register and PLL control pin
CB0~CB7	Data check bits Input/Output	$\overline{WE}$	Write Enable
CK0	Clock Inputs, positive line	$\overline{CS0}$, $\overline{CS1}$	Chip Selects
$\overline{CK0}$	Clock Inputs, negative line	SA0~SA2	SPD address
CKE0, CKE1	Clock Enables	SCL	Serial Presence Detect (SPD) Clock Input
DM0~DM8	Data Masks	SDA	SPD Data Input/Output
$\overline{Event}$	Temperature sensor Event output	TEST	Memory bus test tool
DQ0~DQ63	Data Input/Output	VDD	Core Power
DQS0~DQS8	Data strobes	VDDQ ,VDDSPD	I/O Power, SPD Power
$\overline{DQS0}$ ~ $\overline{DQS8}$	Data strobes, negative line	VREFDQ ,VREFCA	Reference Voltage for DQ ,CA
TDQS9~TDQS17	Termination Data Strobe	VSS	Ground
$\overline{TDQS9}$ ~ $\overline{TDQS17}$	Termination Data Strobe, negative line	NC	No Connect
Err_Out	Parity error found in the Address and Control bus	RFU	Reserved for Future Use
		VTT	Termination Voltage

PIN ASSIGNMENT

Your Ultimate Memory Solution!

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	DQ4	62	VDD	182	VDD
3	DQ0	123	DQ5	63	NC	183	VDD
4	DQ1	124	VSS	64	NC	184	CK0
5	VSS	125	TDQS9	65	VDD	185	$\overline{CK0}$
6	$\overline{DQS0}$	126	$\overline{TDQS9}$	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	$\overline{EVENT}$
8	VSS	128	DQ6	68	PAR_IN	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	$\overline{RAS}$
13	DQ9	133	VSS	73	$\overline{WE}$	193	$\overline{CS0}$
14	VSS	134	TDQS10	74	$\overline{CAS}$	194	VDD
15	$\overline{DQS1}$	135	$\overline{TDQS10}$	75	VDD	195	ODT0
16	DQS1	136	VSS	76	$\overline{CS1}$	196	A13
17	VSS	137	DQ14	77	ODT1	197	VDD
18	DQ10	138	DQ15	78	VDD	198	NC
19	DQ11	139	VSS	79	NC	199	VSS
20	VSS	140	DQ20	80	VSS	200	DQ36
21	DQ16	141	DQ21	81	DQ32	201	DQ37
22	DQ17	142	VSS	82	DQ33	202	VSS
23	VSS	143	TDQS11	83	VSS	203	TDQS13
24	$\overline{DQS2}$	144	$\overline{TDQS11}$	84	$\overline{DQS4}$	204	$\overline{TDQS13}$
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	DQ22	86	VSS	206	DQ38
27	DQ18	147	DQ23	87	DQ34	207	DQ39
28	DQ19	148	VSS	88	DQ35	208	VSS
29	VSS	149	DQ28	89	VSS	209	DQ44
30	DQ24	150	DQ29	90	DQ40	210	DQ45
31	DQ25	151	VSS	91	DQ41	211	VSS
32	VSS	152	TDQS12	92	VSS	212	TDQS14
33	$\overline{DQS3}$	153	$\overline{TDQS12}$	93	$\overline{DQS5}$	213	$\overline{TDQS14}$
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	DQ30	95	VSS	215	DQ46
36	DQ26	156	DQ31	96	DQ42	216	DQ47
37	DQ27	157	VSS	97	DQ43	217	VSS
38	VSS	158	CB4	98	VSS	218	DQ52
39	CB0	159	CB5	99	DQ48	219	DQ53
40	CB1	160	VSS	100	DQ49	220	VSS
41	VSS	161	TDQS17	101	VSS	221	TDQS15
42	$\overline{DQS8}$	162	$\overline{TDQS17}$	102	$\overline{DQS6}$	222	$\overline{TDQS15}$
43	DQS8	163	VSS	103	DQS6	223	VSS
44	VSS	164	CB6	104	VSS	224	DQ54
45	CB2	165	CB7	105	DQ50	225	DQ55
46	CB3	166	VSS	106	DQ51	226	VSS
47	VSS	167	NC (TEST)	107	VSS	227	DQ60
48	VTT	168	$\overline{RESET}$	108	DQ56	228	DQ61
KEY				109	DQ57	229	VSS
49	VTT	169	CKE1	110	VSS	230	TDQS16
50	CKE0	170	VDD	111	$\overline{DQS7}$	231	$\overline{TDQS16}$
51	VDD	171	A15	112	DQS7	232	VSS
52	BA2	172	A14	113	VSS	233	DQ62
53	ERR_OUT	173	VDD	114	DQ58	234	DQ63
54	VDD	174	A12/ $\overline{BC}$	115	DQ59	235	VSS
55	A11	175	A9	116	VSS	236	VDDSPD
56	A7	176	VDD	117	SA0	237	SA1
57	VDD	177	A8	118	SCL	238	SDA
58	A5	178	A6	119	SA2	239	VSS
59	A4	179	VDD	120	VTT	240	VTT
60	VDD	180	A3				

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975V	V	1
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1
Storage Temperature	T_{STG}	-55 to +150	°C	1
Operating Temperature	T_{CASE}	0 to +95	°C	1,2,3

Note:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (Refresh interval =3.9 µs) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

AC & DC OPERATING CONDITIONS (SSTL-15)

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage	V_{DD}	1.283	1.35	1.45	V
Supply Voltage for Output [4]	V_{DDQ}	1.283	1.35	1.45	V
V_{REF} CA(DC)	I/O	0.49 * V_{DD}	0.50 * V_{DD}	0.51 * V_{DD}	V
V_{REF} DQ(DC)	I/O	0.49 * V_{DD}	0.50 * V_{DD}	0.51 * V_{DD}	V
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.09	-	V_{DD}	V
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.135	-	-	V
Input Low Voltage (DC)	V_{IL} (DC)	V_{SS}	-	V_{REF} - 0.09	V
Input Low Voltage (AC)	V_{IL} (AC)	-	-	V_{REF} - 0.135	V

Note:
1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed ±2% VREF (DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDL tied together.

RELIABILITY

MTBF @25 °C (Hours) [1]	FIT @ 25 °C [2]	MTBF @40 °C (Hours) [1]	FIT @ 40 °C [2]
5,044,000	198	2,869,000	348

Notes:
1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours

IDD SPECIFICATION PARAMETER & POWER CONSUMPTION

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating one bank active-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Timing table ; BL: 8; AL: 0;/ CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	2,250	mA
IDD1	**Operating one bank active-read-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Timing table ; BL: 8; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	2,500	mA
IDD2P0	**Precharge Power-Down Current Slow Exit** CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	800	mA
IDD2P1	**Precharge Power-Down Current Fast Exit** CKE: Low; External clock: On; tCK, CL: see Timing table; BL: 81); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	860	mA
IDD2N	**Precharge standby current;** CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-gling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	1,450	mA
IDD2NT	**Precharge Standby ODT Current** CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-gling ; Data IO: FLOATING;DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers	1,560	mA
IDD2Q	**Precharge quiet standby current;** CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	1,420	mA
IDD3P	**Active Power-Down Current** CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	1,300	mA
IDD3N	**Active Standby Current** CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-gling ; Data IO: FLOATING; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	1,750	mA
IDD4R	**Operating Burst Read Current** CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: High between RD; Command, Address, Bank Address Inputs: par-tially toggling ; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	3,350	mA
IDD4W	**Operating Burst Write Current** CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: par-tially toggling ; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH;	3,350	mA
IDD5B	**Burst Refresh Current** CKE: High; External clock: On; tCK, CL, nRFC: see Timing table ; BL: 8; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING;DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	5,700	mA
IDD6	**Self Refresh Current: Normal Temperature Range TCASE:** 0 - 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normale); CKE: Low; External clock: Off; CK and CK: LOW; CL: see Timing table ; BL: 8; AL: 0; /CS, Command, Address, Bank Address, Data IO: FLOATING;DM:stable at 0; Bank Activity: Self- Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: FLOATING	480	mA
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Timing table ; BL: 8; AL: CL-1; /CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one ; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	4,900	mA
PDIMM	**Power Consumption per DIMM** System is operating at 800 MHz clock. This parameter is calculated at a common loading.	6,570	mW

TIMING PARAMETER

Parameter	Symbol	DDR3-1600		Units
		min	Max	
Clock cycle time at CL=11, CWL=8	tCK	1.25	<1.5	ns
Internal read command to first data	tAA	13.75(13.125[2])	20	ns
ACT to internal read or write delay time	tRCD	13.75(13.125[2])		ns
PRE command period	tRP	13.75(13.125[2])		ns
ACT to ACT or REF command period	tRC	48.75(48.125[2])		ns
ACTIVE to PRECHARGE command period	tRAS	35	9*tREFI	ns
Average high pulse width	tCH(avg)	0.47	0.53	tCK
Average low pulse width	tCL(avg)	0.47	0.53	tCK
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ		100	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38		tCK
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)		225	ps
Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	tDS(base)	10		ps
Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	tDH(base)	45		ps
DQS, $\overline{DQS}$ READ Preamble	tRPRE	0.9	-	tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3		tCK
DQS, $\overline{DQS}$ output high time	tQSH	0.4	-	tCK
DQS, $\overline{DQS}$ output low time	tQSL	0.4	-	tCK
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE	0.9	-	tCK
DQS, $\overline{DQS}$ WRITE Postamble	tWPST	0.3	-	tCK
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK	-225	225	ps
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.27	0.27	tCK
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.9	-	tCK
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.3	-	tCK
DLL locking time	tDLLK	512		nCK[1]
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)		
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)		
WRITE recovery time	tWR	15		ns
Mode Register Set command cycle time	tMRD	4		nCK[1]
Mode Register Set command update delay	tMOD	max(12nCK,15ns)		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4		nCK[1]
Auto precharge write recovery + precharge time	tDAL	tWR + roundup (tRP / tCK)		nCK[1]
Multi-Purpose Register Recovery Time	tMPRR	1		nCK[1]
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK,6ns)		
Four activate window for 1KB page size	tFAW	30		ns
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	45		ps
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	120		ps
Power-up and RESET calibration time	tZQinitI	512		nCK[1]
Normal operation Full calibration time	tZQoper	256		nCK[1]
Normal operation short calibration time	tZQCS	64		nCK[1]
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC+ 10ns)		
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK,6ns)		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK
RTT dynamic change skew	tADC	0.3	0.7	tCK
8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	350	70,200	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC+10ns)		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)		nCK[1]
Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI	tCK
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

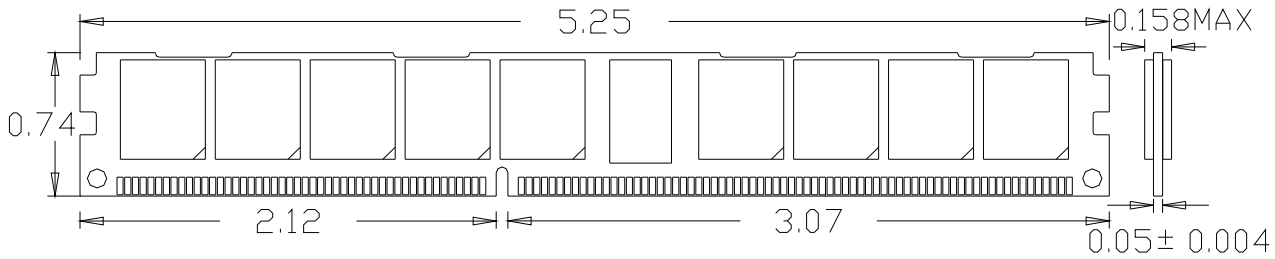
1:Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
2: For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match.

PHYSICAL DIMENSIONS (UNITS IN INCHES)

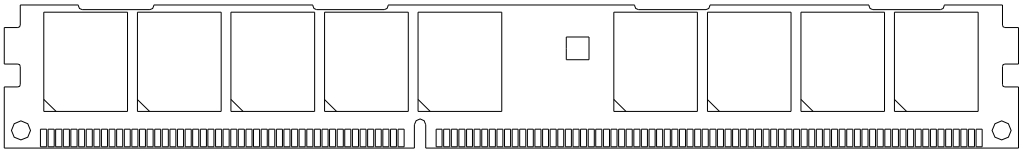
(Drawing not to scale)

240-pin DIMM

Front



Back



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