ALPHA RF TRANSCEIVER

ALPHA-TRX433S
ALPHA-TRX915S



- FM Transceiver Module
- Low cost, high performance
- Fast PLL lock time
- Wakeup timer
- 2.2V - 5.4V power supply
- Low power consumption
- 10MHz crystal for PLL timing
- Clock and reset signal output for external MCU use
- 16 bit RX Data FIFO
- SPI interface
- Internal data filtering and clock recover
- Analog and digital signal strength indicator (ARSSI/DRSSI)
- Programmable TX frequency deviation (from 15 to 240 KHz)
- Programmable receiver bandwidth (from 67 to 400 kHz)
- Standby current less than 0.3us
- Two 8 bit TX data registers
- High data rate (up to 115.2 kbps with internal demodulator, with external RC filter highest data rate is 256 kbps)
- Operates from -45 to +85^{O}C

Applications

- Wireless Security Systems
- Car Alarms
- Remote Gate Controls
- Remote Sensing
- Data Capture
- Sensor Reporting

Introduction

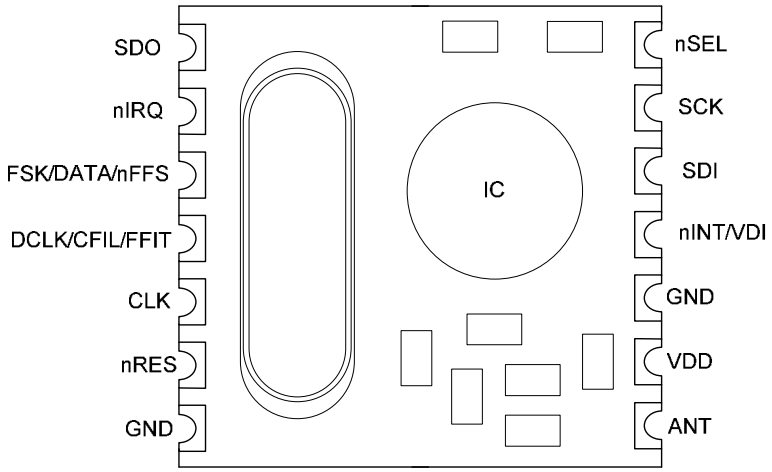
The Alpha Modules are extremely cost effective but high performance radio modules. Supplied in a miniature Surface mount package this Transceiver module can Transmit/Receive at upto 115Kbps at a maximum of 300m.
Operating at 2-5V, the module monitors its battery voltage and can sleep with very low standby current. The module can wake intermittently and provide direct control outputs to a microcontroller making it ideally suited to battery applications.
These Modules will suit one to one multi-node wireless links in applications including car and building security, POS and inventory tracking, remote process monitoring.

Part Numbers

Part Number	Description
ALPHA-TRX433S	FM Transceiver Module, 433MHz
ALPHA-TRX915S	FM Transceiver Module, 915MHz

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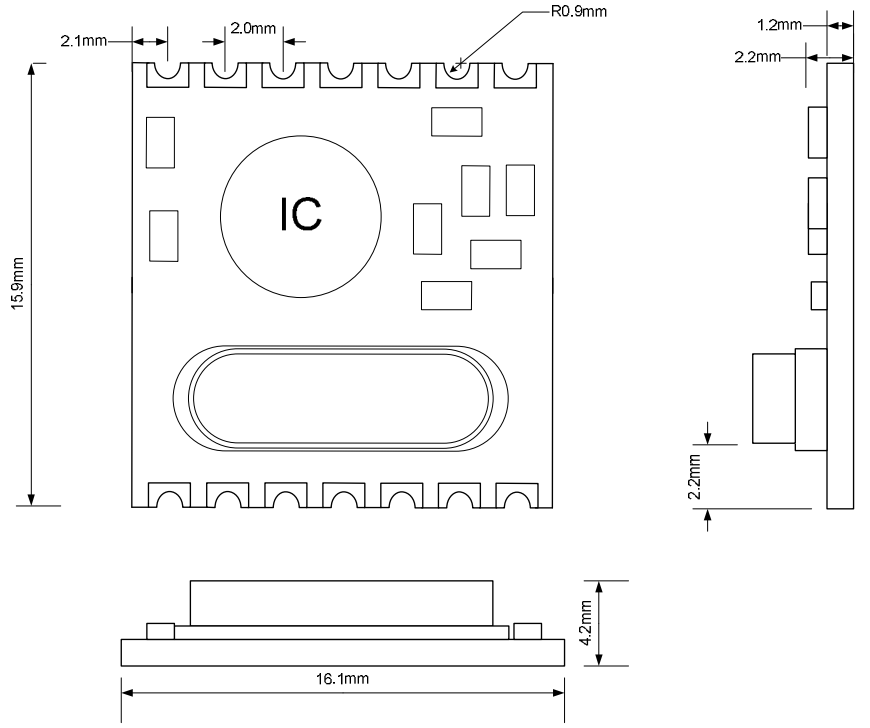
Pin Description



Pin	definition	Type	Function
11	nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
13	VDD	S	Positive power supply
10	SDI	DI	SPI data input
9	SCK	DI	SPI clock input
8	nSEL	DI	Chip select (active low)
1	SDO	DO	Serial data output with bus hold
2	nIRQ	DO	Interrupts request output（active low）
3	FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
4	DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
5	CLK	DO	Clock output for external microcontroller
6	nRES	DIO	Reset output（active low）
7, 12	GND	S	Power ground
14	ANT	IN	Antenna Connection

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Mechanical Dimensions



Electrical Parameters

Maximum (not in working mode)

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
I_{in}	Input current except power	-25	25	mA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	℃
T_{ld}	Soldering temperature(10s)		260	℃

Recommended working range

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	2.2	5.4	V
T_{op}	Working temperature	-40	85	℃

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DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
$I_{dd_TX_0}$	Supply current (TX mode, P_{out} = 0dBm)	433MHz band 915MHz band		13 17		mA
$I_{dd_TX_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	433MHz band 915MHz band		21 25		mA
I_{dd_RX}	Supply current (RX mode)	433MHz band 915MHz band		10 13		mA
I_x	Stand by current	Crystal and base band on		3. 0	3. 5	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
I_{lb}	Low battery detection			0.5		uA
V_{lb}	Low battery step	0.1V per step	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Low level input				$0.3*V_{dd}$	V
V_{ih}	High level input		$0.7*V_{dd}$			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	$V_{ih}=V_{dd}$, V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC characteristic

symbol	parameter	remark	min	typical	max	Unit
f_{ref}	PLL frequency		8	10	12	MHz
f_{LO}	frequency (10MHz crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	430.24 900.72		439.75 929.27	MHz
f_{LO}	frequency (8MHZ crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	344.19 720.57		351.80 743.41	MHz
f_{LO}	frequency (12MHZ crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	3516.28 1080.8		527.71 1115.1	MHz
BW	Receiver bandwidth	1 2 3 4 5 6	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	KHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		us
BR	Data rate	With internal digital demodulator	0.6		115.2	kbps
BR_A	Data rate	With external RC filter			256	kbps
		BW=134KHz,BR=1.2kbps,433MHz band		-106	-100	
		BW=134KHz,BR=1.2kbps,915MHz band		-102	-95	
AFC_{range}	AFC working range	df_{FSK} FSK deviation in the received signal		0.8* df_{FSK}		
RS_A	RSSI accuracy			±5		dB
RS_R	RSSI range			46		dB
C_{ARSSI}	ARSSI filter			1		nF
RS_{STEP}	RSSI programmable step			6		dB

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RS_{RESP}	DRSSI response time	RSSI output high after valid , CARRSI=5nF		500		us

AC characteristic(Transmitter)

symbol	parameter	remark	min	typical	max	Unit
		433MHz band	**3**	**5**		
		915MHz band	**-2**	**0**		
P_{out}	Typical output power	Selectable in 3 dB steps	P_{max}-21		P_{max}	dbm
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In low bands In high bands	2 2.1	2.6 2.7	3.2 3.3	pf
Q_o	Quality factor of the output capacitance	In low bands In high bands	13 8	15 10	17 12	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier			-75 -85	dbc/HZ
BR	FSK bit rate				256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHZ

AC characteristic(Turn-on/Turnaround timings)

symbol	parameter	remark	min	typical	max	Unit
T_{st}	Crystal oscillator startup time	Crystal ESR < 100			5	ms
$T_{tx_rx_XTAL_ON}$	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on		450		us
$T_{rx_tx_XTAL_ON}$	Receiver - Transmitter turnover time	Synthesizer off, crystal oscillator on		350		us
$T_{tx_rx_SYNT_ON}$	Transmitter - Receiver turnover time	Synthesizer on, crystal oscillator on		425		us
$T_{rx_tx_SYNT_ON}$	Receiver - Transmitter turnover time	Synthesizer on, crystal oscillator on		300		us
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
$C_{in,\ D}$	Digital input apacitance				2	pf
$t_{r,\ f}$	Digital output rise/fall time	15pF pure capacitive load			10	ns

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