AMIS-39101

Octal High Side Driver with Protection

General Description

The AMIS−39101 is a robust high side driver IC featuring eight independent high current output drive channels along with a number of integrated fault−protection circuits. This highly integrated product is designed for controlled delivery of power to a large variety of loads in industrial applications including motors, relays and LED arrays, among others. With all driver output channels in the conducting state, each channel can source up to 350 mA of continuous current (resistive load). In cases where all output drivers are not active, higher output current per channel can be achieved provided that the thermal limits of the device are not exceeded. Furthermore, in order to minimize system cost each output driver has built−in fly−back diodes. The device withstands short−circuits to ground and supply, respectively. It is designed with an array of integrated protection features including over−temperature and over−current detection and shut down. The integrated charge pump requires only one external capacitor and provides for operation of the critical fault−protection circuitry even in case of low supply voltages. The device can be interfaced to a variety of microcontrollers via the serial interface link, in turn allowing for monitoring and controlling the state of each of the output drivers individually. In this case, at the onset of a potential hazardous situation the drivers are switched off and the diagnostic state of the drivers can be extracted via the serial interface. The device also features a power down mode for reduced power consumption and has high built−in electrostatic discharge (ESD) protection capability for robust operation.

Key Features

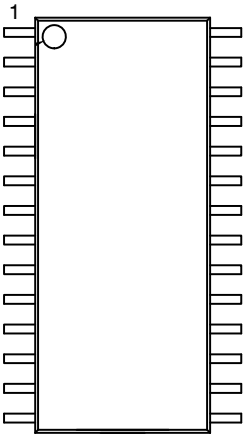
- Eight High Side Output Drivers
- Up to 830 mA Continuous Current per Driver Pair (Resistive Load)
- Charge Pump with One External Capacitor
- Serial Interface
- Short−circuit Protection
- Diagnostic Features
- Power−down Mode
- Internal Thermal Shutdown
- 3.3 V and 5 V Microcontroller Compliant
- Excellent System ESD
- Automotive Compliant
- SO28 Package with Low $R_{\theta JA}$
- This is a Pb−Free Device*

Typical Applications

- Actuator Control
- LED Drivers
- Relays and Solenoids
- Industrial Process Control
- Automotive Load Management

ON Semiconductor®

http://onsemi.com



SOIC 28
PN SUFFIX
CASE 751AR

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

© Semiconductor Components Industries, LLC, 2008

December, 2008 − Rev. 2

Publication Order Number:
AMIS−39101/D

ORDERING INFORMATION

Product Name	Package	Shipping Configuration	Temperature Range
AMIS39101PNPB4G	PSOP 300-28 (JEDEC MS-013)	Tube/Tray	−40°C to 85°C
AMIS39101PNPB4RG	PSOP 300-28 (JEDEC MS-013)	Tape & Reel	−40°C to 85°C

NOTE: For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

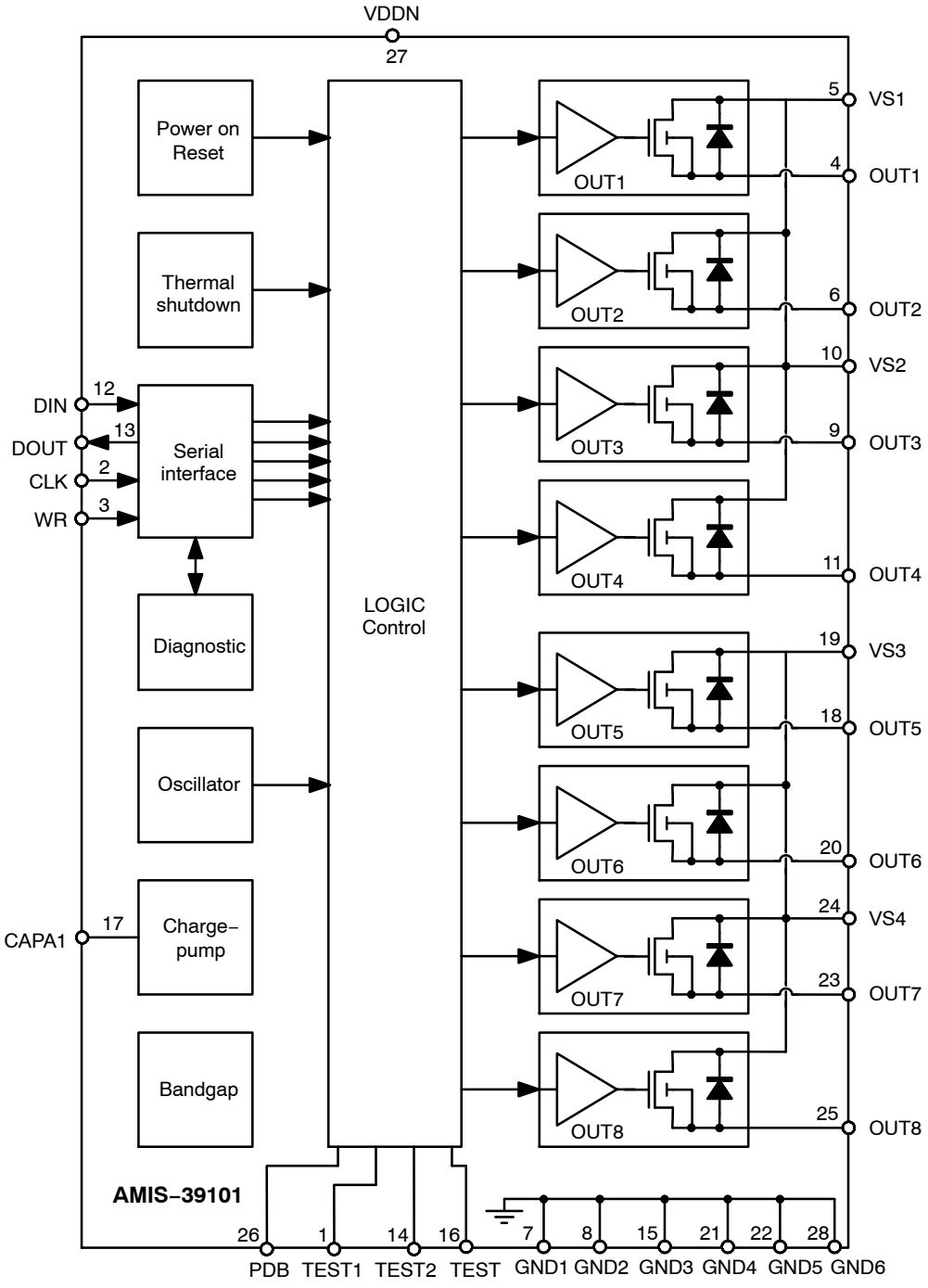


Figure 1. Block Diagram

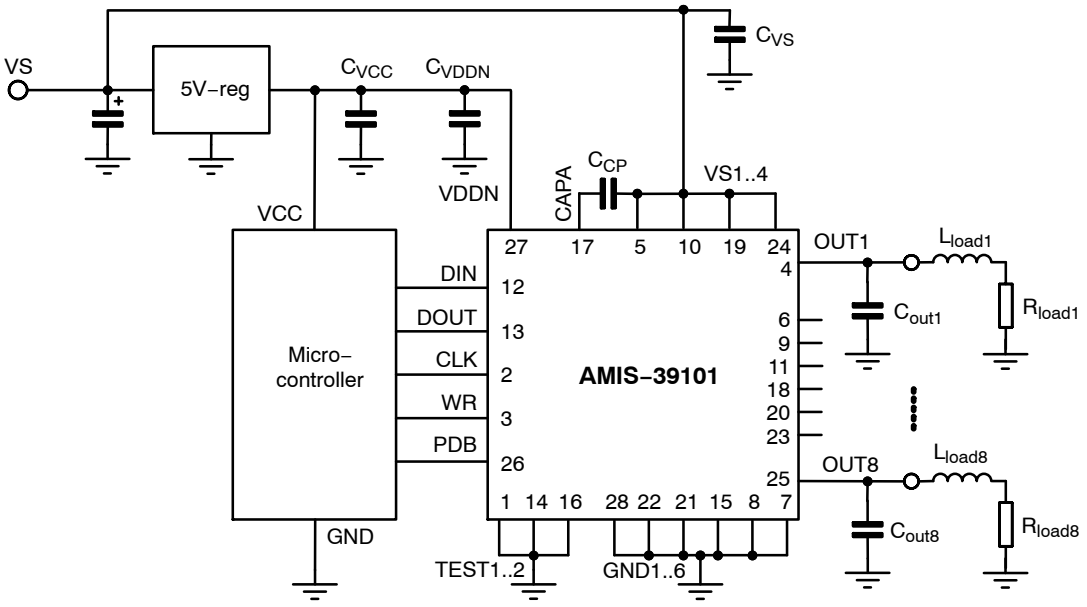


Figure 2. Typical Application Diagram

External Components

It is important to properly decouple the power supplies of the chip with external capacitors that have good high frequency properties.

The VS1, VS2, VS3, and VS4 pins are shorted on the PCB level. Also GND1, GND2, GND3, GND4, GND5, GND6, TEST, TEST1, and TEST2 are shorted on the PCB level.

Table 1. EXTERNAL COMPONENTS

Component	Function	Min.	Value	Max.	Tol. [%]	Units
C_{VS}	Decoupling capacitor; X7R	100			±20	nF
C_{charge_pump}	Charge pump capacitor (Note 1)	0.47		47		nF
C_{out} (Note 2)	EMC connector on connector	1				nF
C_{out} (Note 2)	Decoupling capacitors; 50 V	22			±20	nF
C_{VDD}	Decoupling capacitors; 50 V	22			±20	nF
R_{Load}	Load resistance		65		±10	Ω
L_{Load}	Load inductance at maximum current		300	350		mH

1. The capacitor must be placed close to the AMIS−39101 pins on the PCB.
2. Both capacitors are optional and depend on the final application and board layout.

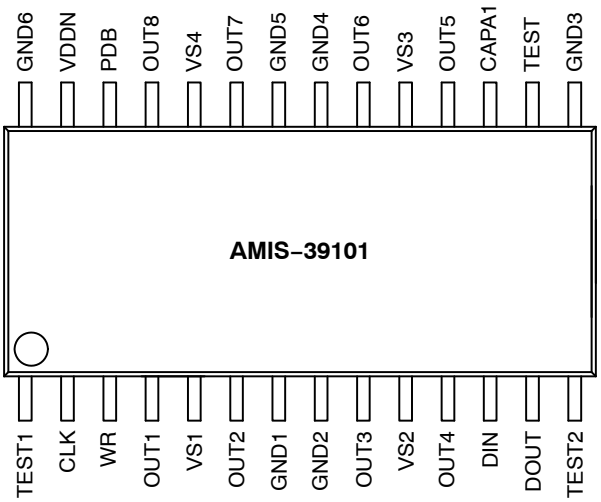


Figure 3. Pin Description of the AMIS−39101

Table 2. PIN OUT

Pin	Name	Description
1	TEST1	Connect to GND
2	CLK	Schmitt trigger serial interface CLK input
3	WR	Schmitt trigger serial interface write enable input
4	OUT1	HS driver output
5	VS1	VS power supply
6	OUT2	HS driver output
7	GND1	Power ground and thermal dissipation path junction−to−PCB
8	GND2	Power ground and thermal dissipation path junction−to−PCB
9	OUT3	S driver output
10	VS2	VS power supply
11	OUT4	HS driver output
12	DIN	Serial interface input pin (Schmitt trigger or CMOS inverter)
13	DOUT	Digital three state output for serial interface
14	TEST2	Connect to GND
15	GND3	Power ground and thermal dissipation path junction−to−PCB
16	TEST	Connect to GND
17	CAPA1	Charge pump capacitor pin
18	OUT5	HS driver output
19	VS3	VS power supply
20	OUT6	HS driver output
21	GND4	Power ground and thermal dissipation path junction−to−PCB
22	GND5	Power ground and thermal dissipation path junction−to−PCB
23	OUT7	HS driver output
24	VS4	VS power supply
25	OUT8	HS driver output
26	PDB	Schmitt trigger power−down input
27	VDDN	Digital supply
28	GND6	Power ground and thermal dissipation path junction−to−PCB

ELECTRICAL AND ENVIRONMENTAL RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Unit
VDDN	Power supply voltage	GND − 0.3	6	V
VS	VS power supply on pins VS1 to VS4, load dump, Pulse 5b 400 ms	GND − 0.3	35	V
Iout_ON	Maximum output current OUTx pins (Note 3) The HS driver is switched on	−3000	350	mA
Iout_OFF	Maximum output current OUTx pins (Note 3) The HS driver is switched off	−350	350	mA
I_OUT_VS	Maximum output current VS1, 2, 3, 4 pins	−700	3750	mA
Vcapa1	DC voltage on pin CAPA1	0	VS+16.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	−0.3	VDDN+0.3	V
V_{ESD}	Pins that connect the application (pins VS1..4 and Out1..8) (Note 4) All other pins (Note 4)	−4 −2	+4 +2	kV kV
V_{ESD}	ESD according charged device model (Note 5)	−750	+750	V
Tj	Junction temperature (T<100 hours)	−40	175	°C
Tmr	Ambient temperature under bias	−40	85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. The power dissipation of the chip must be limited not to exceed the maximum junction temperature Tj.
4. According to HBM standard MIL−STD−883 method 3015.7.
5. According to norm EOS/ESD−STM5.3.1−1999 robotic mode.

Thermal Characteristics

Table 4. THERMAL CHARACTERISTICS OF THE PACKAGE

Symbol	Description	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in power−SO28 package	In free air	145	K/W

Table 5. THERMAL CHARACTERISTICS OF THE AMIS−39101 ON A PCB

PCB Design	Conductivity − Top and Bottom Layer	**Rthja** (Note 6)	Unit
Two layer (35 μm)	Copper planes according to Figure 4 + 25% copper for the remaining areas	24	K/W
Two layer (35 μm)	Copper planes according to Figure 4 + 0% copper for the remaining areas	53	K/W
Four layer JEDEC: EIA/JESD51−7	25% copper coverage	25	K/W
One layer JEDEC: EIA/JESD51−3	25% copper coverage	46	K/W

6. These values are informative only.

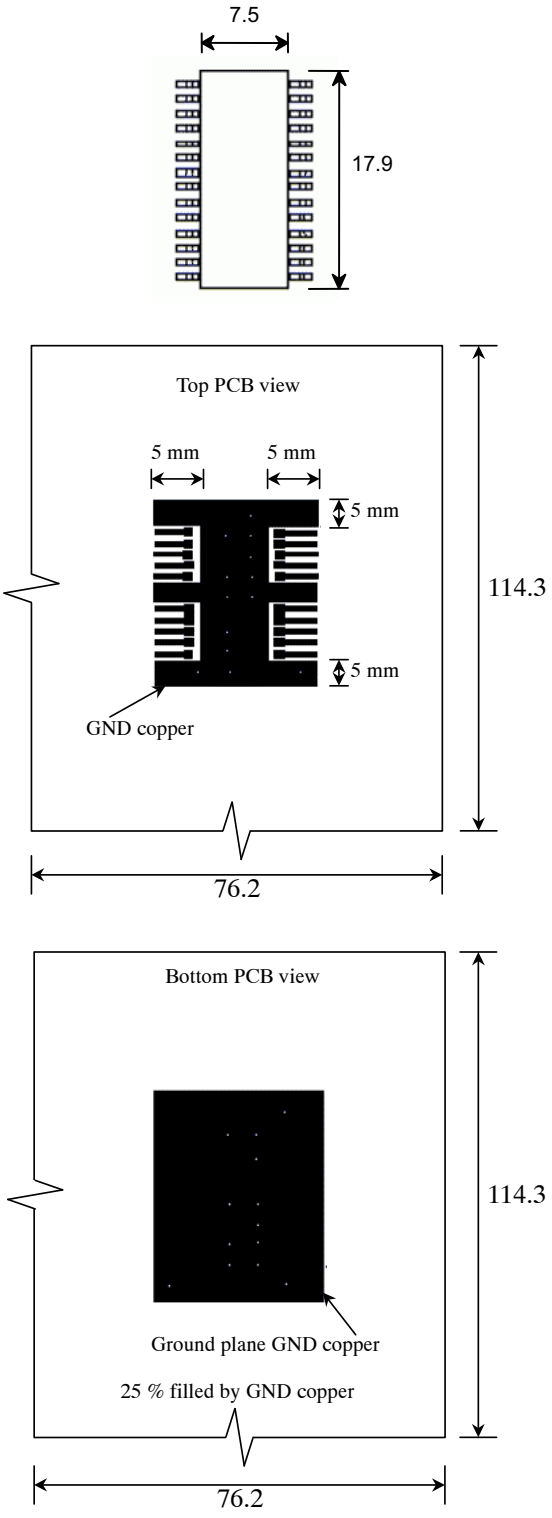


Figure 4. Layout Recommendation for Thermal Characteristics

Electrical Parameters

Operation outside the operating ranges for extended periods may affect device reliability. Total cumulative dwell time above the maximum operating rating for the power supply or temperature must be less than 100 hours.

The parameters below are independent from load type. (see Load Specific Parameters section)

Table 6. OPERATING RANGES

Symbol	Description	Min.	Max.	Unit
VDDN	Digital power supply voltage	3.1	5.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	−0.3	VDDN	V
VS (1)	VS power supply on Pins VS1 to VS4	3.5	28	V
Tamb	Ambient temperature	−40	85	°C

7. The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj of 130°C.

Table 7. ELECTRICAL CHARACTERISTICS

Symbol	Description	Min.	Max.	Unit
I_VS_norm (Note 8)	Consumption on VS without load currents In normal mode of operation PDB = high		3.5	mA
I_PDB_3.3 (Notes 8 and 9)	Sum of VS and VDDN consumption in power−down mode of operation PDB = low, VDDN 3.3 V, VS = 24 V, 23°C ambient CLK and WR are at VDDN voltage		25	μA
I_PDB_5 (Notes 8 and 9)	Sum of VS and VDDN consumption in power−down mode of operation PDB = low, VDDN 5 V, VS = 24 V, 23°C ambient CLK and WR are at VDDN voltage		40	μA
I_PDB_MAX_VS	VS consumption in power−down mode of operation PDB = low, VS = 28 V		10	μA
I_VDDN_norm (Note 8)	Consumption on VDDN, In normal mode of operation PDB = high CLK is 500 kHz, VDDN = 5.5 V, VS = 28 V		1.6	mA
R_on_1..8	On resistance of the output drivers 1 through 8 t VS = 24 V (nominal VS power supply condition) t VS = 4.6 V (worst case VS power supply condition)		 1 3	Ω
I_OUT_lim_x (Note 8)	Internal over−current limitation of HS driver outputs	0.65	2	A
T_shortGND_HSdoff	The time from short of HS driver OUTx pin to GND and the driver deactivation; driver is Off Detection works from VS minimum of 7 V, VDDN minimum is 3 V	5,4		μs
TSD_H (Note 8)	High TSD threshold for junction temperature (temperature rising)	130	170	°C
TSD_HYST	TSD hysteresis for junction temperature	9	18	°C

8. The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj.
9. The cumulative operation time mentioned above may cause permanent device failure.

Load Specific Parameters

High side driver parameters for specific loads are specified in following categories:

1. Parameters for inductive loads up to 350 mH and $T_{ambient}$ up to 85°C
2. Parameters for inductive loads up to 300 mH and $T_{ambient}$ up to 85°C
3. Parameters for resistive loads and $T_{ambient}$ up to 85°C

Table 8. LOAD SPECIFIC CHARACTERISTICS

Symbol	Description	Min.	Max.	Unit
A. Inductive Load up to 350 mH and $T_{ambiant}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		240	mA
B. Inductive Load up to 300 mH and $T_{ambiant}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		275	mA
C. Resistive Load and $T_{ambiant}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		350	mA
	Maximum output per one HS driver, only one can be active		650	mA
	Maximum output per HS driver, only two HS drivers from a different pair can be active simultaneously		500	mA
	Maximum output per one HS driver pair		830	mA

NOTE: The parameters above are not tested in production but are guaranteed by design. The overall current capability limitations need to be respected at all times.

The maximum current specified in Table 8 cannot always be obtained. The practically obtainable maximum drive current heavily depends on the thermal design of the application PCB (see Thermal Characteristics section).

The available power in the package is: (TSD_H − T_ambient) / Rthja

With TSD_H = 130°C and Rthja according to Table 5.

Charge Pump

The high side drivers use floating NDMOS transistors as power devices**.** To provide the gate voltages for the NDMOS of the high side drivers, a charge pump is integrated. The storage capacitor is an external one. The charge pump oscillator has typical frequency of 4 MHz.

DIAGNOSTICS

Short Circuit Diagnostics

The diagnostic circuit in the AMIS−39101 monitors the actual output status at the pins of the device and stores the result in the diagnostic register which is then latched in the output register at the rising edge of the WR−pin. Each driver has its corresponding diagnostic bit DIAG_x. By comparing the actual output status (DIAG_x) with the requested driver status (CMD_x) you can diagnose the correct operation of the application according to Table 9.

Thermal Shutdown (TSD) Diagnostic

In case of TSD activation, all bits DIAG1 to DIAG8 in the serial interface output register are set into the fault state and all drivers will be switched off (see Table 9).

The TSD error condition is active until it is reset by the next correct communication on serial interface (i.e. number of clock pulses during WR = 0 is divisible by 8), provided that the device has cooled down under the TSD trip point.

Table 9. OUT DIAGNOSTICS

Requested Driver Status	CMD_x	Actual Output Status	DIAG_x	Diagnosis
On	1	High	1	Normal state
On	1	Low	0	Short to ground or TSD (Note 11)
Off	0	High	1	Short to VS or missing load (Note 10) or TSD (Note 11)
Off	0	Low	0	Normal state (Note 10)

10. The correct diagnostic information is available after T_diagnostic_OFF time.
11. All 8 diagnostic bits DIAG_x must be in the fault condition to conclude a TSD diagnostic.

Ground Loss

Due to its design, the AMIS−39101 is protected for withstanding module ground loss and driver output shorted to ground at the same time.

Table 10. POWER LOSS

VDDN	VS	Possible Case	Action
0	0	System stopped	Nothing
0	1	Start case or sleeping mode with missing VDDN	Eight switches in the off−state Power down consumption on VS
1	0	Missing VS supply VDDN normally present	Eight switches in the off−state Normal consumption on VDDN
1	1	System functional	Nominal functionality

Serial Interface

The serial interface is used to allow an external microcontroller (MCU) to communicate with the device. The AMIS−39101 always acts as a slave and it can't initiate any transmission.

Serial Interface Transfer Format and Pin Signals

The serial interface block diagram and timing characteristics are shown in Figures 6 and 7.

During a serial interface transfer, data is simultaneously sent to and received from the device. A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DIN and DOUT). DOUT signal is the output from the AMIS−39101 to the external MCU and DIN signal is the input from the MCU to the AMIS−39101. The WR−pin selects the AMIS−39101 for communication and can also be used as a chip select (CS) in a multiple−slave system. The WR−pin is active low. If AMIS−39101 is not selected, DOUT is in high impedance state and it does not interfere with serial interface bus activities. Since AMIS−39101 always shifts data out on the rising edge and samples the input data also on the rising edge of the CLK signal, the MCU serial interface port must be configured to match this operation. Serial interface clock idles high between the transferred bytes.

The diagram in Figure 7 represents the serial interface timing diagram for 8−bit communication.

Communication starts with a falling edge on the WR−pin which latches the status of the diagnostic register into the serial interface output register. Subsequently, the CMD_x bits – representing the newly requested driver status – are shifted into the input register and simultaneously, the DIAG_x bits – representing the actual output status – are shifted out. The bits are shifted with x = 1 first and ending with x = 8. At the rising edge of the WR−pin, the data in the input register is latched into the command register and all drivers are simultaneously switching to the newly requested status. Serial interface communication is ended.

In case the serial interface master does only support 16−bit communication, then the master must first send 8 clock pulses with dummy DIN data and ignoring the DOUT data. For the next 8 clock pulses the above description can be applied.

The required timing for serial to peripheral interface is shown in Table 11.

Table 11. DIGITAL CHARACTERISTICS

Symbol	Description	Min.	Max.	Unit
T_CLK	Maximum applied clock frequency on CLK input		500	kHz
T_DATA_ready	Time between falling edge on WR and first bit of data ready on DOUT output (driver going from HZ state to output of first diagnostic bit)		2	µs
T_CLK_first	First clock edge from falling edge on WR	3		µs
T_setup (Note 12)	Setup time on DIN	20		ns
T_hold (Note 12)	Hold time on DIN	20		ns
T_DATA_next	Time between rising edge on CLK and next bit ready on DOUT (capa on DOUT is 30 pF max.)		100	ns
T_serial interface_END	Time between last CLK edge and WR rising edge	1		µs
T_risefall	Rise and fall time of all applied signals (maximum loading capacitance is 30 pF)	5	20	ns
T_WR	Time between two rising edge on WR (repetition of the same command)	300		µs

12. Guaranteed by design

Normal mode verification:

- The *command* is the set of eight bits loaded via serial interface, which drives the eight HS drivers on or off.
- The *command* is activated with rising edge on WR pin.

Table 12. DIGITAL CHARACTERISTICS

Symbol	Description	Min.	Max.	Unit
T_command_L_max. (Note 13)	Minimum time between two opposite commands for inductive loads and maximum HS driver current of 275 mA	1		s
T_command_R (Note 13)	Minimum time between two opposite commands for resistive loads and maximum HS driver current of 350 mA	2		ms
T_PDB_recov	The time between the rising edge on the PDB input and 90 percent of VS−1V on all HS driver outputs. (all drivers are activated, pure resistive load 35 mA on all outputs)		1	ms

13. Guaranteed by design

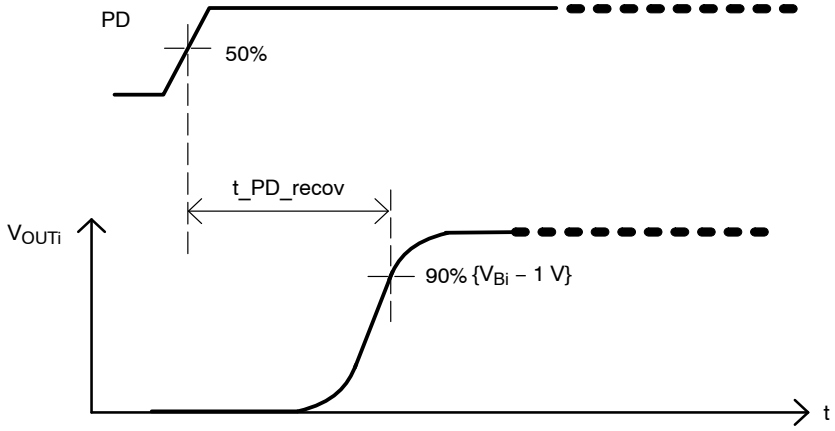


Figure 5. Timing for Power−down Recovery

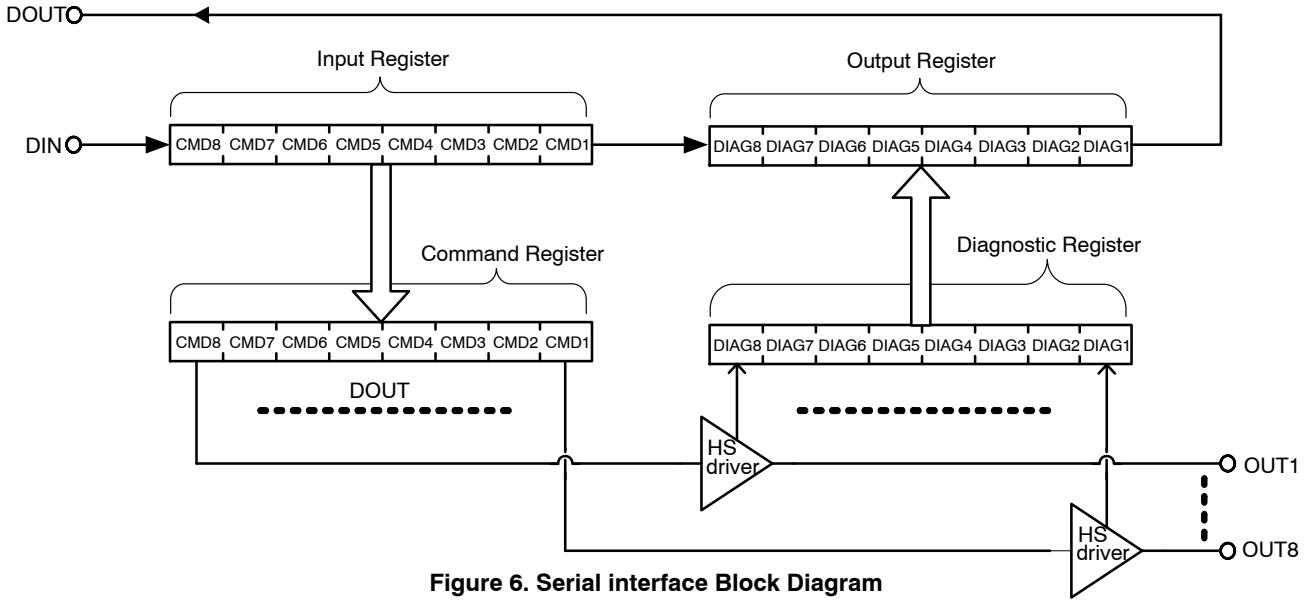


Figure 6. Serial interface Block Diagram

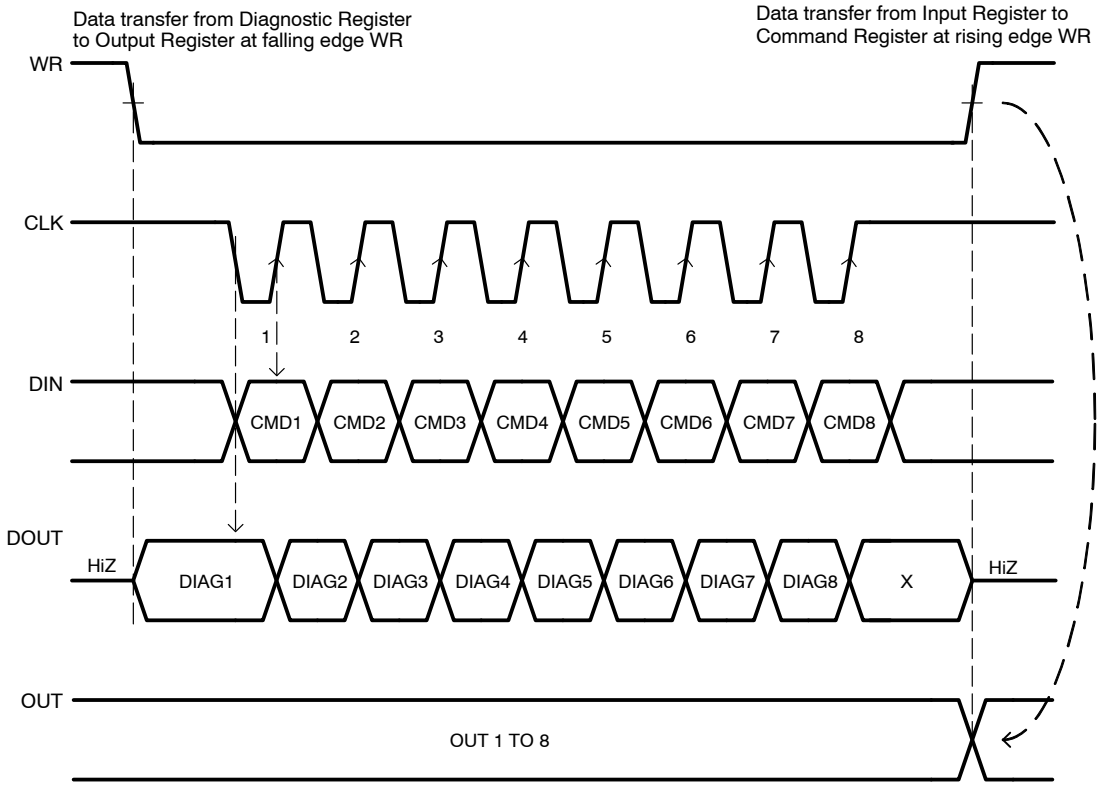


Figure 7. Timing Diagram

Quality and Reliability

A quality system with certification against TS16949 is maintained.

An AEC−Q100 compatible product qualification is performed. Monitoring of production is performed according to the dedicated AMIS specifications for assembly and wafer fabrication.

All products are tested using a production test program. Lot conformance to specification in volume production is guaranteed by means of following quality conformance tests:

Table 13. QUALIFICATION

QC Test	Conditions	AQL Level	Inspection Level
Electrical functional and parametric	To product data sheet	0.04	II
External visual (mechanical)	Physical damage to body or leads (e.g. bent leads) Dimensions affecting PCB manufacturability (e.g. coplanarity)	0.15	II
External visual (cosmetic)	Correctness of marking All other cosmetic defects	0.65	II

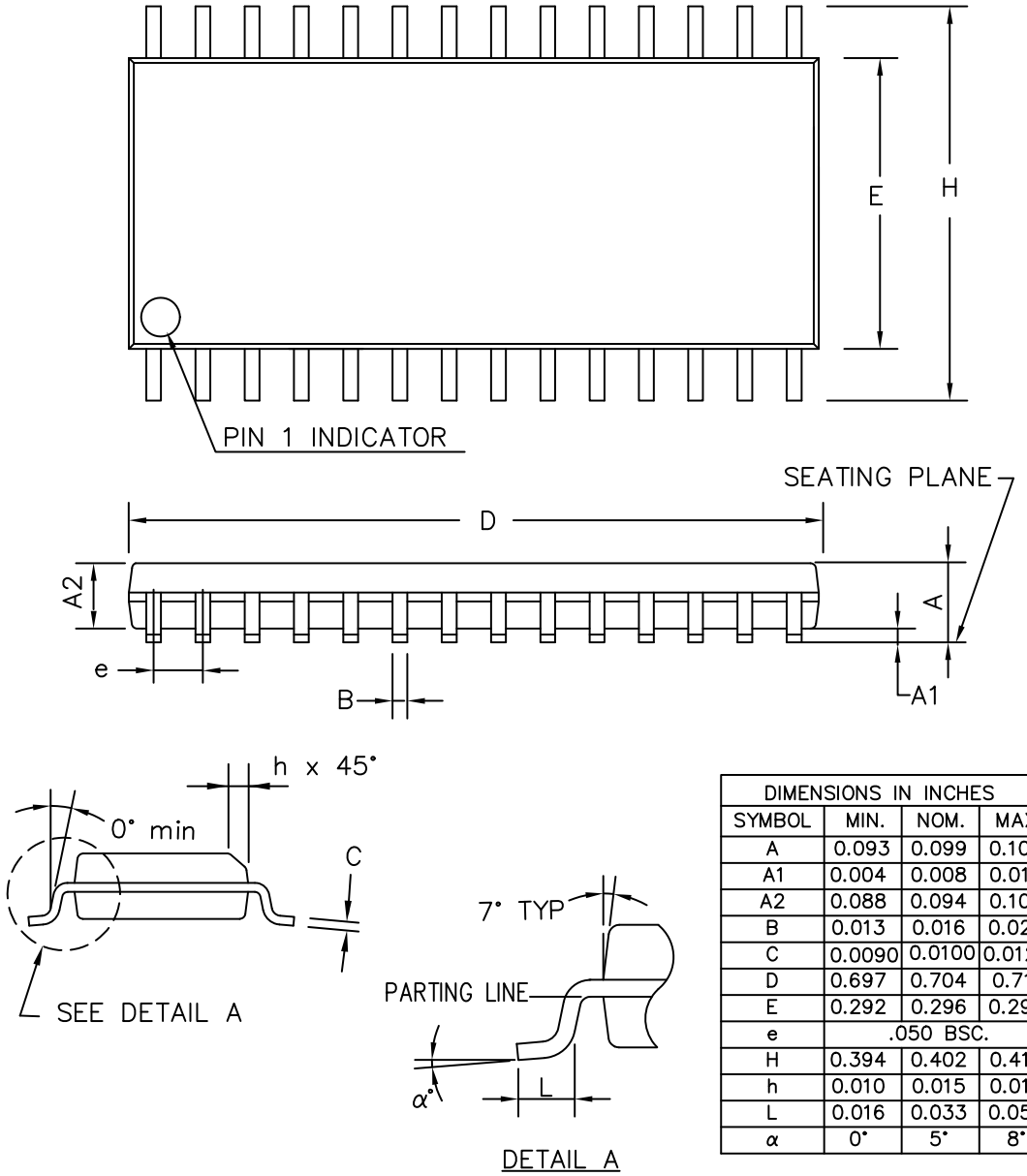
NOTE: Each production lot will be accompanied with a Certificate of Conformance.

Company or Product Inquiries

For more information about ON Semiconductor's products or services visit our Web site at http://www.onsemi.com.

PACKAGE DIMENSIONS

SOIC 28 W
CASE 751AR−01
ISSUE O



DIMENSIONS IN INCHES			
SYMBOL	MIN.	NOM.	MAX.
A	0.093	0.099	0.104
A1	0.004	0.008	0.012
A2	0.088	0.094	0.100
B	0.013	0.016	0.020
C	0.0090	0.0100	0.0125
D	0.697	0.704	0.711
E	0.292	0.296	0.299
e	.050 BSC.		
H	0.394	0.402	0.419
h	0.010	0.015	0.019
L	0.016	0.033	0.050
α	0°	5°	8°

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative